Part Number: ISP1761ET-T
USB On-the-Go Dual Role Controllers

General Description:

The ISP1761 is a single-chip Hi-Speed Universal Serial Bus (USB) On-The-Go (OTG) Controller integrated with our advanced USB slave host controller and our ISP1582 peripheral controller.

The Hi-Speed USB host controller and peripheral controller comply to Ref. 1 "Universal Serial Bus Specification Rev. 2.0" and support data transfer speeds of up to 480 Mbit/s. The Enhanced Host Controller Interface (EHCI) core implemented in the host controller is adapted from Ref. 2 "Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0". The OTG controller adheres to Ref. 3 "On-The-Go Supplement to the USB Specification Rev. 1.3".

The ISP1761 has three USB ports. Port 1 can be configured to function as a downstream port, an upstream port or an OTG port; ports 2 and 3 are always configured as downstream ports. The OTG port can switch its role from host to peripheral, and peripheral to host. The OTG port can become a host through the Host Negotiation Protocol (HNP) as specified in the OTG supplement.

Key Features:

- Compliant with Ref. 1 "Universal Serial Bus Specification Rev. 2.0"; supporting data transfer at high-speed (480 Mbit/s), full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s)
- Integrated Transaction Translator (TT) for Original USB (full-speed and low-speed) peripheral support
- Three USB ports that support three operational modes:
  - Mode 1: Port 1 is an OTG controller port, and ports 2 and 3 are host controller ports
  - Mode 2: Ports 1, 2 and 3 are host controller ports
  - Mode 3: Port 1 is a peripheral controller port, and ports 2 and 3 are host controller ports
- Supports OTG Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- Multitasking support with virtual segmentation feature (up to four banks)

- High-speed memory controller (variable latency and SRAM external interface)
- Directly addressable memory architecture
- Generic processor interface to most CPUs, such as Hitachi SH-3 and SH-4, NXP XA, Intel StrongARM, NEC and Toshiba MIPS, Freescale DragonBall and PowerPC Reduced Instruction Set Computer (RISC) processors
- Configurable 32-bit and 16-bit external memory data bus
- Supports Programmed I/O (PIO) and Direct Memory Access (DMA)
- Slave DMA implementation on CPU interface to reduce the host systems CPU load
- Separate IRQ, DREQ and DACK lines for the host controller and the peripheral controller
- Integrated multi-configuration FIFO
- Double-buffering scheme increases throughput and facilitates real-time data transfer
- Integrated Phase-Locked Loop (PLL) with external 12 MHz crystal for low EMI
- Tolerant I/O for low voltage CPU interface (1.65 V to 3.3 V)
- 3.3 V-to-5.0 V external power supply input
- Integrated 5.0 V-to-1.8 V or 3.3 V-to-1.8 V voltage regulator (internal 1.8 V for low-power core)
- Internal power-on reset or low-voltage reset and block-dedicated software reset
- Supports suspend and remote wake-up
- Built-in overcurrent circuitry (analog overcurrent protection)
- Hybrid-power mode: $V_{CC(5V0)}$ (can be switched off), $V_{CC(I/O)}$ (permanent)
- Target total current consumption:
  - Normal operation; one port in high-speed active: I_{CC} < 100 mA when the internal charge pump is not used
  - Suspend mode: $I_{CC(susp)}$ < 150 µA at ambient temperature of +25 Cel
- Available in LQFP128 and TFBGA128 packages
- Host controller-specific features
  - High performance USB host with integrated Hi-Speed USB transceivers; supports high-speed, full-speed and low-speed
  - EHCI core is adapted from Ref. 2 "Enhanced Host Controller Interface Specification for Universal Serial Bus Rev. 1.0"
  - Configurable power management
  - Integrated TT for Original USB peripheral support on all three ports
  - Integrated 64 kB high-speed memory (internally organized as 8 k x 64 bit)
  - Additional 2.5 kB separate memory for TT
  - Individual or global overcurrent protection with built-in sense circuits
  - Built-in overcurrent circuitry (digital or analog overcurrent protection)
- OTG controller-specific features

- OTG transceiver: fully integrated; adheres to Ref. 3 "On-The-Go Supplement to the USB Specification Rev. 1.3"
- Supports HNP and SRP for OTG dual-role devices
- HNP: status and control registers for software implementation
- SRP: status and control registers for software implementation
- Programmable timers with high resolution (0.01 ms to 80 ms) for HNP and SRP
- Supports external source of V_{BUS}

- Peripheral controller-specific features
- High-performance USB peripheral controller with integrated Serial Interface Engine (SIE), FIFO memory and transceiver
- Complies with Ref. 1 "Universal Serial Bus Specification Rev. 2.0" and most device class specifications
- Supports auto Hi-Speed USB mode discovery and Original USB fallback capabilities
- Supports high-speed and full-speed on the peripheral controller
- Bus-powered or self-powered capability with suspend mode
- Slave DMA, fully autonomous and supports multiple configurations
- Seven IN endpoints, seven OUT endpoints and one fixed control IN and OUT endpoint
- Integrated 8 kB memory
- Software-controllable connection to the USB bus, SoftConnect

Connection Diagram: