SSD1961

Product Preview

675KB Embedded Display SRAM
LCD Display Controller

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FIGURES

1 GENERAL DESCRIPTION

SSD1961 is a display controller of 5,529,600 bit frame buffer to support up to 640 x 480 x 18bit graphics content. It also equips parallel MCU interfaces in different bus width to receive graphics data and command from MCU. Its display interface supports common RAM-less LCD driver of color depth up to 18 bit-per-pixel.

2 FEATURES

- Display feature
  - 675kbyte (5,529,600bit) built-in frame buffer. Support up to 640 x 480 at 18bpp display
  - Support TFT 18 bit generic RGB and TTL interface panel
  - Hardware rotation of 0, 90, 180, 270 degree
  - Hardware display mirroring
  - Hardware windowing
  - Programmable brightness, contrast and saturation control
  - Dynamic Backlight Control (DBC) / Ambient Backlight Control (ABC) via PWM signal
- MCU connectivity
  - 8bit/16bit/18bit MCU interface
  - Support packed 18bit RGB data in 16bit bus
  - Tearing effect signal
- I/O Connectivity
  - 4 GPIO pins
- Built-in clock generator
- Deep sleep mode for power saving
- 64 pin BGA package
- Core supply power (V_{DDPLL} and V_{DDD}): 1.2V±10%
- I/O supply power (V_{DDIO}): 1.8V to 3.3V±10%
- LCD interface supply power (V_{DDLCD}): 1.8V to 3.3V±10%

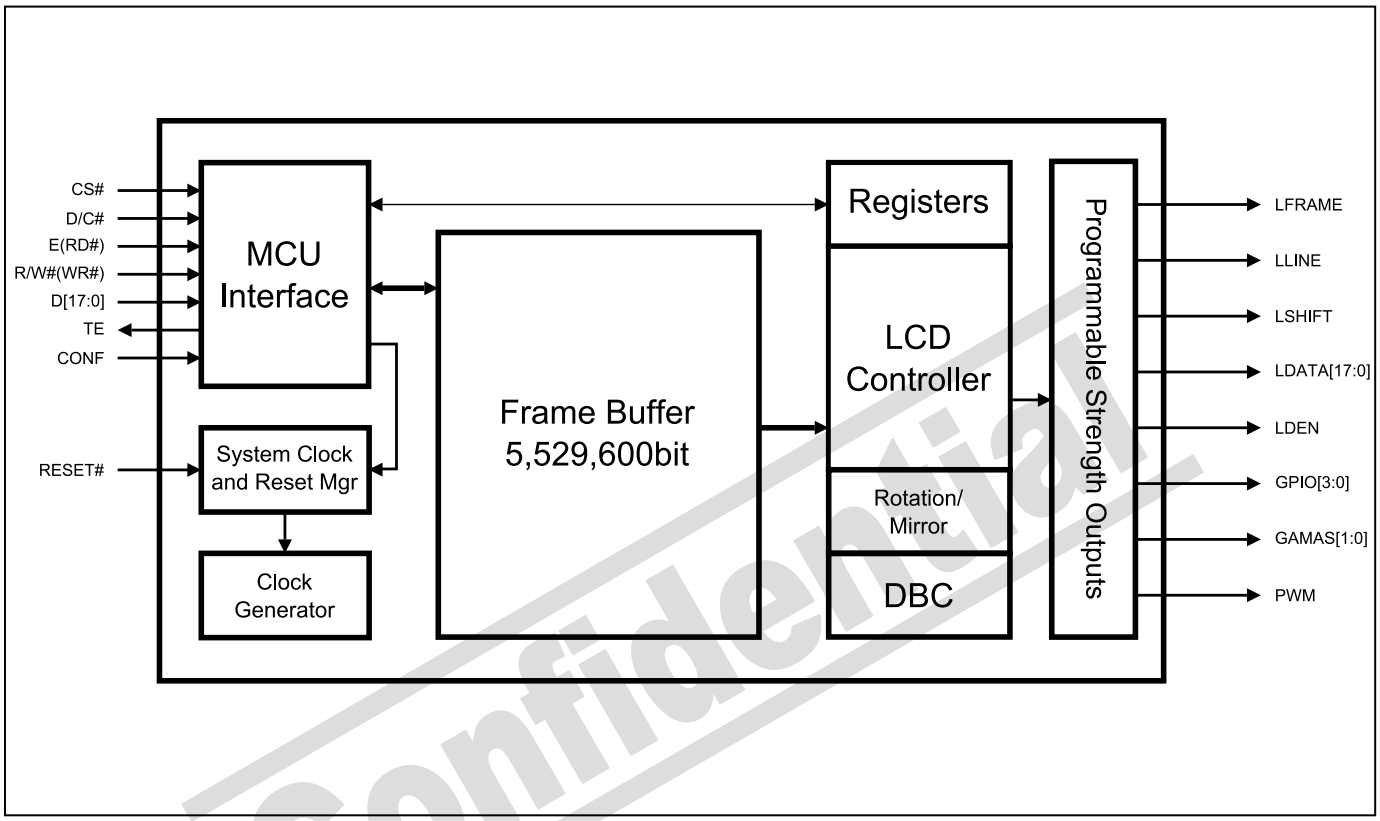
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD1961G40	64 TFBGA

4 BLOCK DIAGRAM

Figure 4-1: SSD1961 Block Diagram



5 PIN ARRANGEMENT

5.1 64 Pin TFBGA

Figure 5-1: Pinout Diagram – 64 pin TFBGA (Top view)

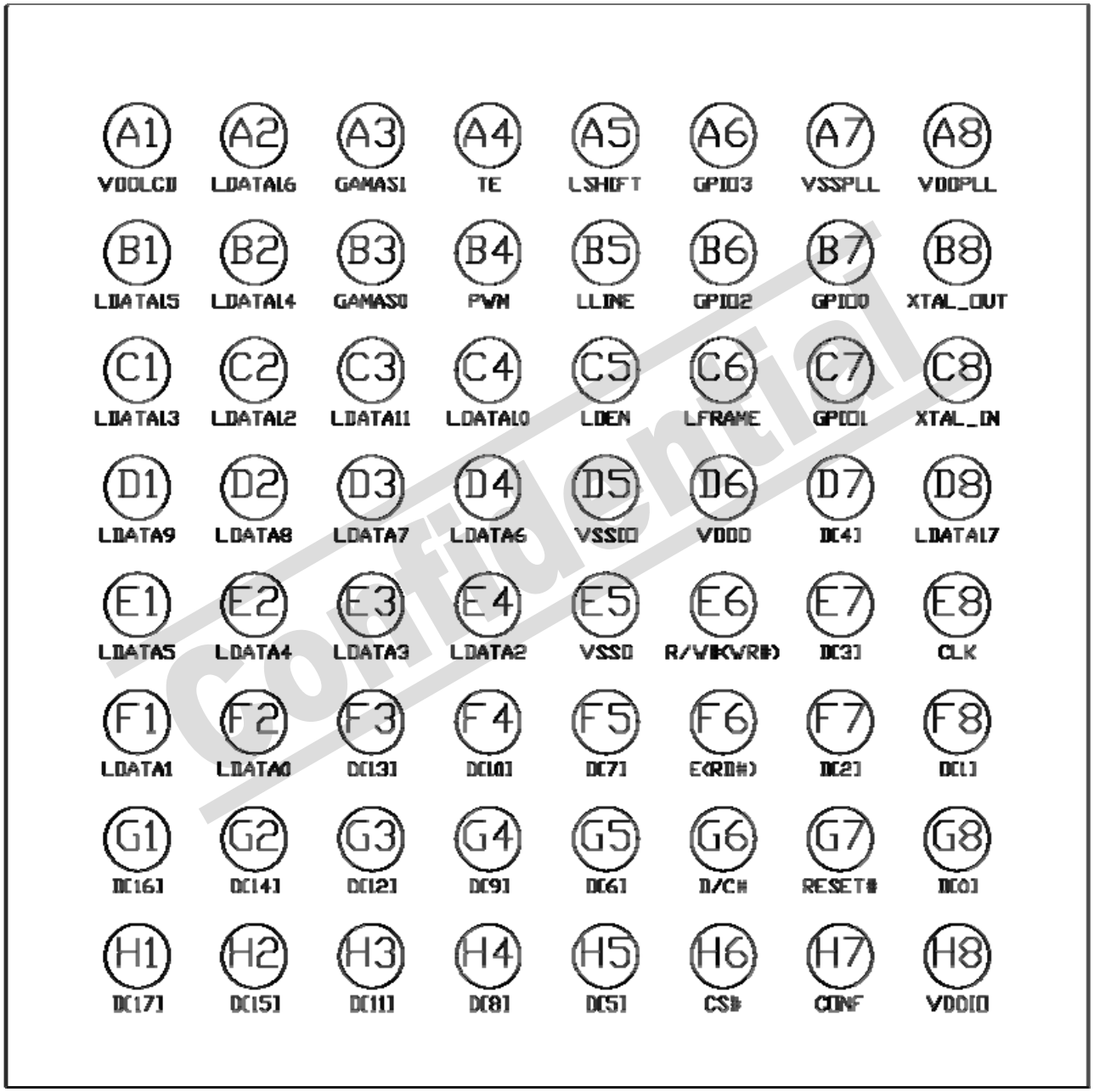


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Table 5-1: TFBGA Pin Assignment Table

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
A1	VDDLCD	C1	LDATA13	E1	LDATA5	G1	D[16]
A2	LDATA16	C2	LDATA12	E2	LDATA4	G2	D[14]
A3	GAMAS1	C3	LDATA11	E3	LDATA3	G3	D[12]
A4	TE	C4	LDATA10	E4	LDATA2	G4	D[9]
A5	LSHIFT	C5	LDEN	E5	VSSD	G5	D[6]
A6	GPIO3	C6	LFRAME	E6	R/W#(WR#)	G6	D/C#
A7	VSSPLL	C7	GPIO1	E7	D[3]	G7	RESET#
A8	VDDPLL	C8	XTAL_IN	E8	CLK	G8	D[0]
B1	LDATA15	D1	LDATA9	F1	LDATA1	H1	D[17]
B2	LDATA14	D2	LDATA8	F2	LDATA0	H2	D[15]
B3	GAMAS0	D3	LDATA7	F3	D[13]	H3	D[11]
B4	PWM	D4	LDATA6	F4	D[10]	H4	D[8]
B5	LLINE	D5	VSSIO	F5	D[7]	H5	D[5]
B6	GPIO2	D6	VDDD	F6	E(RD#)	H6	CS#
B7	GPIO0	D7	D[4]	F7	D[2]	H7	CONF
B8	XTAL_OUT	D8	LDATA17	F8	D[1]	H8	VDDIO

6 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin
Hi-Z = High impedance

Table 6-1: MCU Interface Pin Mapping

Pin Name	Type	Pin #	Description
CLK	I	E8	TTL clock input
XTAL_IN	I	C8	Crystal oscillator input
XTAL_OUT	O	B8	Crystal oscillator output
CS#	I	H6	Chip select
D/C#	I	G6	Data/Command select
E(RD#)	I	F6	6800 mode: E (enable signal) 8080 mode: RD# (read strobe signal)
R/W#(WR#)	I	E6	6800 mode: R/W# 0: Write cycle 1: Read cycle 8080 mode: WR# (write strobe signal)
D[17:0]	IO	D7, E7, F3-F5, F7-F8, G1-G5, G8, H1-H5	Data bus
TE	O	A4	Tear effect

Table 6-2: LCD Interface Pin Mapping

Pin Name	Type	Pin #	Description
LFRAME	O	C6	Vertical sync (Frame pulse)
LLINE	O	B5	Horizontal sync (Line pulse)
LSHIFT	O	A5	Pixel clock (Pixel shift signal)
LDEN	O	C5	Data valid
LDATA[17:0]	O	A2, B1-B2, C1-C4, D1-D4, D8, E1-E4, F1-F2	RGB data
GPIO[3:0]	IO	A6, B6-B7, C7	GPIO[3:0] can be configured for display miscellaneous signals or as general purpose I/O.
GAMAS [1:0]	O	A3, B3	Gamma selection for panel
PWM	O	B4	PWM output for backlight driver

Table 6-3: Control Signal Pin Mapping

Pin Name	Type	Pin #	Description
RESET#	I	G7	Master synchronize reset
CONF	I	H7	MCU interface configuration 0: 6800 Interface 1: 8080 Interface

Table 6-4: Power Pin Mapping

Pin Name	Type	Pin #	Description
VDDD	P	D6	Power supply for internal digital circuit
VDDLCD	P	A1	Power supply for LCD interface related pads
VDDPLL	P	A8	Power supply for internal analog circuit and analog I/O pads
VDDIO	P	H8	Power supply for digital I/O pads
VSSD	P	E5	Ground for internal digital circuit
VSSPLL	P	A7	Ground for internal analog circuit and analog I/O pads
VSSIO	P	D5	Ground for digital I/O pads

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 MCU Interface

The MCU interface connects the MCU and SSD1961 graphics controller. The MCU interface can be configured as 6800 mode and 8080 mode by the CONF pin. By pulling the CONF pin to VSSIO, the MCU interface will be configured as 6800 mode interface. If the CONF pin is connected to VDDIO, the MCU interface will be configure in 8080 mode.

7.1.1 6800 Mode

The 6800 mode MCU interface consist of CS#, D/C#, E, R/W#, D[17:0], and TE signals (Please refer to Table 6-1 for pin multiplexed with 8080 mode). This interface supports both fixed E and clock E scheme to define a read/write cycle. If the E signal is kept high and used as enable signal, the CS# signal acts as a bus clock, the data or command will be latched into the system at the rising edge of CS#. If the user wants to use the E pin as the clock pin, the CS# pin then need to be fixed to logic 0 to select the chip. Then the falling edge of the E signal will latch the data or command. For details, please refer to the timing diagram in chapter 11.1.1.

7.1.2 8080 Mode

The 8080 mode MCU interface consist of CS#, D/C#, RD#, WR#, D[17:0] and TE signals (Please refer to Table 6-1 for pin multiplexed with 6800 mode). This interface use WR# to define a write cycle and RD# for read cycle. If the WR# goes low when the CS# signal is low, the data or command will be latched into the system at the rising edge of WR#. Similarly, the read cycle will start when RD# goes low and end at the rising edge of RD#. The detailed timing will show in the chapter 11.1.2.

7.1.3 Register Pin Mapping

When user access the registers via the parallel MCU interface, only D[7:0] will be used regardless the width of the pixel data is. Therefore, D[17:8] will only be used to address the display data only. This provided the possibility that the pixel data format as shown in Table 7-1 can be configured by register 0xF0.

7.1.4 Pixel Data Format

Both 6800 and 8080 support 8 bit, 16 bit, 18 bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Table 7-1: Pixel Data Format

Interface	Cycle	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
18 bits	1st	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1st			R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1st			R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X
	2nd			B5	B4	B3	B2	B1	B0	X	X	R5	R4	R3	R2	R1	R0	X	X
	3rd			G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X
8 bits	1st											R5	R4	R3	R2	R1	R0	X	X
	2nd											G5	G4	G3	G2	G1	G0	X	X
	3rd											B5	B4	B3	B2	B1	B0	X	X

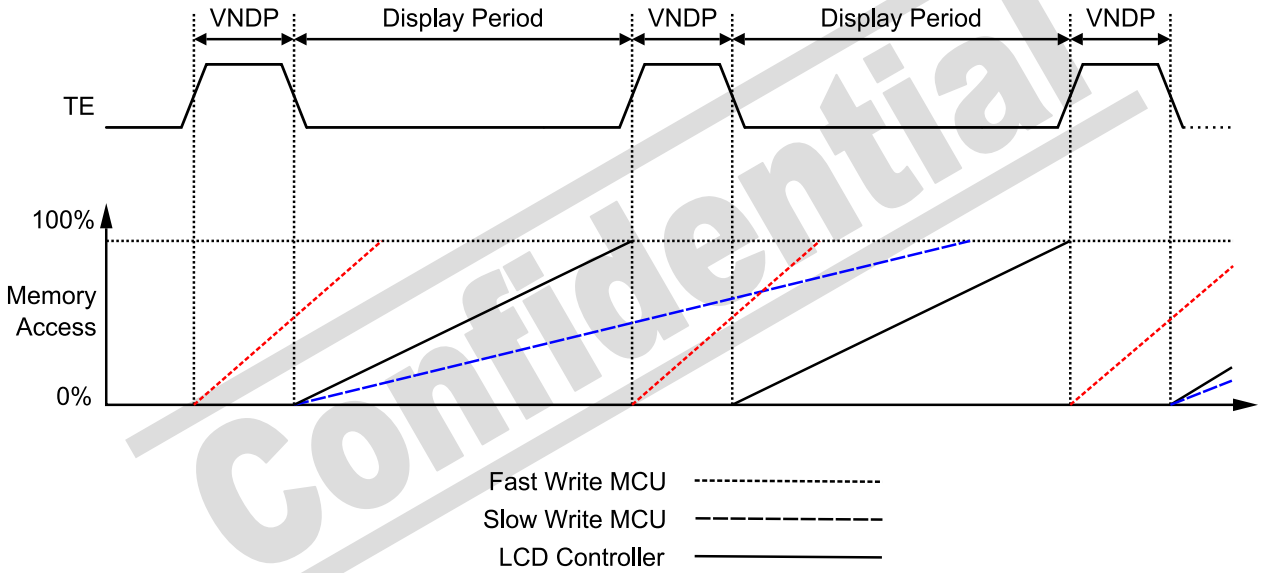
X: Don't Care

7.1.5 Tearing Effect Signal (TE)

The Tearing Effect Signal (TE) is a feedback signal from the LCD Controller to MCU. This signal reveals the display status of LCD controller. In the non-display period, the TE signal will go high. Therefore, this signal enables the MCU to send data by observing the non-display period to avoid tearing.

Figure 7-1 shows how the TE signal helps to avoid tearing. If the MCU writing speed is slower than the display speed, the display data should be updated after the LCD controller start to scan the frame buffer. Then the LCD controller will always display the old memory content until the next frame. However, if the MCU is faster than the LCD controller, it should start updating the display content in the vertical non-display period (VNDP) to enable the LCD controller will always get the newly updated data.

Figure 7-1: Relationship between Tearing Effect Signal and MCU Memory Writing



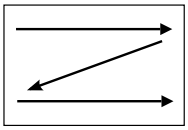
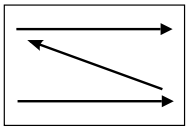
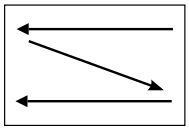
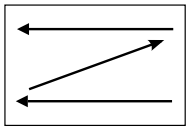
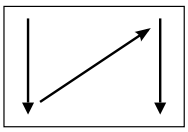
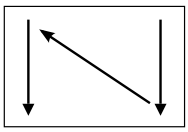
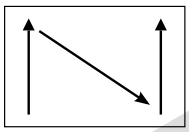
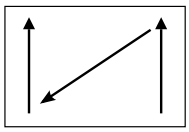
In SSD1961 graphics controller, users can configure the TE signal to reflect the vertical non-display period only or reflect both vertical and horizontal non-display period. With the additional horizontal non-display period information, the MCU can control the refresh action in more accurately by counting the horizontal line scanned by the LCD controller. Usually, a fast MCU will not need horizontal non-display period. But a slow MCU will need it to ensure the frame buffer update process always lags behind the LCD controller.

The TE signal is not generated by the MCU interface but the LCD controller. The MCU interface only route the signal to the external pad.

7.2 Frame Buffer

There are 5,529,600 bit built-in SRAM inside SSD1961 to use as frame buffer. When the frame buffer is written or read, the “address counter” will automatically increase by one or decrease by one depends on the frame buffer settings.

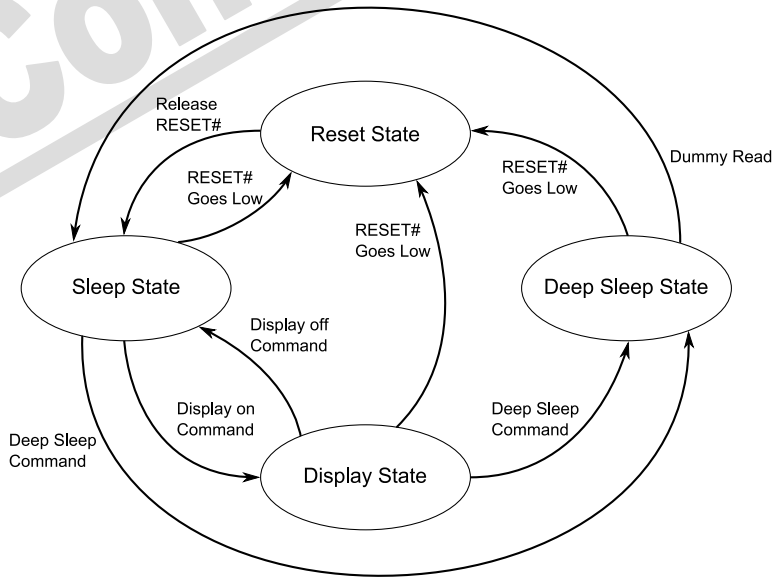
Table 7-2: Frame Buffer Settings Regrading to set_address_mode Command

	Option 1 Horizontal: Increment Vertical: Increment B6 = 0; B7 = 0	Option 2 Horizontal: Increment Vertical: Decrement B6 = 0; B7 = 1	Option 3 Horizontal: Decrement Vertical: Increment B6 = 1; B7 = 0	Option 4 Horizontal: Decrement Vertical: Decrement B6 = 1; B7 = 1
Horizontal Frame Buffer Mode B5 = 0	00000h  4B000h	00000h  4B000h	00000h  4B000h	00000h  4B000h
Vertical Frame Buffer Mode B5 = 1	00000h  4B000h	00000h  4B000h	00000h  4B000h	00000h  4B000h

7.3 System Clock and Reset Manager

The “System Clock and Reset Manager” distributes the reset signal and clock signal to the entire system. It controls the Clock Generator and contains clock gating circuitry to turn on and off the clock of each functional module. Also, it divides the root clock from Clock Generator to operation clocks for different module. The System Clock and Reset Manager also manage the reset signals to ensure all the module are reset to appropriate status when the system are in reset state, deep sleep state, sleep state and display state. Figure 7-2 shows a state diagram of four operation states of SSD1961.

Figure 7-2: State Diagram of SSD1961



Reset State:	Deep Sleep State:	Sleep State:	Display State:
Clock Generator Stop	Clock Generator Stop	Clock Generator On	Clock Generator On
Unable to Receive Command	Unable to Receive Command	Able to Receive Command	Able to Receive Command
Unable to Update Frame Buffer	Unable to Update Frame Buffer	Able to Update Frame Buffer	Able to Update Frame Buffer
Display Off	Display Off	Display Off	Display On
All Settings Reset	All Settings Retain	All Settings Retain	All Settings Retain

7.4 LCD Controller

7.4.1 Display Format

The LCD controller reads the frame buffer and generates display signals according to the selected display panel format. SSD1961 supports common RAM-less TFT driver using generic RGB data format or TTL format.

7.4.2 General Purpose Input/Output (GPIO)

The GPIO pins can operate in 2 modes, GPIO mode and miscellaneous display signal mode. When the pins are configured as GPIOs, these pins can be controlled directly by MCU. Therefore, user can use these pins to emulate other interface such as SPI or I2C. If these pins are configured as display signals, they will toggle with display periodically according to the signal settings. They can be set to toggle once a frame, once a line or in arbitrary period. Therefore they can be configured as some common signal needed for different panels such as STH or LP.

8 COMMAND TABLE

Hex Code	Command	Description
0x 00	nop	No operation
0x 01	soft_reset	Software Reset
0x 0A	get_power_mode	Get the current power mode
0x 0B	get_address_mode	Get the frame memory to the display panel read order
0x 0C	get_pixel_format	Get the current pixel format
0x 0D	get_display_mode	The display module returns the Display Signal Mode.
0x 0E	get_diagnostic_result	The display module returns the self-diagnostic results following a Sleep Out command.
0x 0F	get_signal_mode	Get the current display mode from the peripheral
0x 10	enter_sleep_mode	Turn off the panel. This command will pull low the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x 11	exit_sleep_mode	Turn on the panel. This command will pull high the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x 12	enter_partial_mode	Part of the display area is used for image display.
0x 13	enter_normal_mode	The whole display area is used for image display.
0x 20	exit_invert_mode	Displayed image colors are not inverted.
0x 21	enter_invert_mode	Displayed image colors are inverted.
0x 26	set_gamma_curve	Selects the gamma curve used by the display device.
0x 28	set_display_off	Blanks the display device
0x 29	set_display_on	Show the image on the display device
0x 2A	set_column_address	Set the column extent
0x 2B	set_page_address	Set the page extent
0x 2C	write_memory_start	Transfer image information from the host processor interface to the peripheral starting at the location provided by set_column_address and set_page_address
0x 2E	read_memory_start	Transfer image data from the peripheral to the host processor interface starting at the location provided by set_column_address and set_page_address
0x 30	set_partial_area	Defines the partial display area on the display device
0x 33	set_scroll_area	Defines the vertical scrolling and fixed area on display area
0x 34	set_tear_off	Synchronization information is not sent from the display module to the host processor
0x 35	set_tear_on	Synchronization information is sent from the display module to the host processor at the start of VFP
0x 36	set_address_mode	Set the read order from frame buffer to the display panel
0x 37	set_scroll_start	Defines the vertical scrolling starting point
0x 38	exit_idle_mode	Full color depth is used for the display panel
0x 39	enter_idle_mode	Reduce color depth is used on the display panel.
0x 3A	set_pixel_format	Defines how many bits per pixel are used in the interface
0x 3C	write_memory_continue	Transfer image information from the host processor interface to the peripheral from the last written location
0x 3E	read_memory_continue	Read image data from the peripheral continuing after the last read_memory_continue or read_memory_start

Hex Code	Command	Description
0x 44	set_tear_scanline	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the provided scanline
0x 45	get_scanline	Get the current scan line
0x A1	read_ddb_start	Read the DDB from the provided location
0x A8	read_ddb_continue	Continue reading the DDB from the last read location
0x B0	set_lcd_mode_pad_size	Set the LCD panel mode (RGB TFT or TTL)
0x B1	get_lcd_mode_pad_size	Get the current LCD panel mode, pad strength and resolution
0x B4	set_hori_period	Set front porch
0x B5	get_hori_period	Get current front porch settings
0x B6	set_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0x B7	get_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0x B8	set_gpio_conf	Set the GPIO configuration. If the GPIO is not used for LCD, set the direction. Otherwise, they are toggled with LCD signals.
0x B9	get_gpio_conf	Get the current GPIO configuration
0x BA	set_gpio_value	Set GPIO value for GPIO configured as output
0x BB	get_gpio_status	Read current GPIO status. If the individual GPIO was configured as input, the value is the status of the corresponding pin. Otherwise, it is the programmed value.
0x BC	set_post_proc	Set the image post processor
0x BD	get_post_proc	Set the image post processor
0x BE	set_pwm_conf	Set the image post processor
0x BF	get_pwm_conf	Set the image post processor
0x C0	set_lcd_gen0	Set the rise, fall, period and toggling properties of LCD signal generator 0
0x C1	get_lcd_gen0	Get the current settings of LCD signal generator 0
0x C2	set_lcd_gen1	Set the rise, fall, period and toggling properties of LCD signal generator 1
0x C3	get_lcd_gen1	Get the current settings of LCD signal generator 1
0x C4	set_lcd_gen2	Set the rise, fall, period and toggling properties of LCD signal generator 2
0x C5	get_lcd_gen2	Get the current settings of LCD signal generator 2
0x C6	set_lcd_gen3	Set the rise, fall, period and toggling properties of LCD signal generator 3
0x C7	get_lcd_gen3	Get the current settings of LCD signal generator 3
0x C8	set_gpio0_rop	Set the GPIO0 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO0 is configured as general GPIO.
0x C9	get_gpio0_rop	Get the GPIO0 properties with respect to the LCD signal generators.
0x CA	set_gpio1_rop	Set the GPIO1 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO1 is configured as general GPIO.
0x CB	get_gpio1_rop	Get the GPIO1 properties with respect to the LCD signal generators.
0x CC	set_gpio2_rop	Set the GPIO2 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO2 is configured as general GPIO.

Hex Code	Command	Description
0x CD	get_gpio2_rop	Get the GPIO2 properties with respect to the LCD signal generators.
0x CE	set_gpio3_rop	Set the GPIO3 with respect to the LCD signal generators using ROP3 operation. No effect if the GPIO3 is configured as general GPIO.
0x CF	get_gpio3_rop	Get the GPIO3 properties with respect to the LCD signal generators.
0x D0	set_abc_dbc_conf	Set the ambient back light and dynamic back light configuration
0x D1	get_abc_dbc_conf	Get the ambient back light and current dynamic back light configuration
0x D2	set_dbc_histo_pointer	Set the histogram pointer for DBC
0x D3	get_dbc_histo_pointer	Get the current histogram pointer settings and data
0x D4	set_dbc_th	Set the threshold for each level of power saving
0x D5	get_dbc_th	Get the threshold for each level of power saving
0x D6	set_amb_timer	Set ambient back light timer
0x D7	get_amb_timer	Get ambient back light timer configuration
0x D8	set_amb_lv0	Set ambient back light control level 0 to 3
0x D9	get_amb_lv0	Get current configuration of ambient back light control level 0
0x DA	set_amb_lv1	Set ambient back light control level 1
0x DB	get_amb_lv1	Get current configuration of ambient back light control level 1
0x DC	set_amb_lv2	Set ambient back light control level 0
0x DD	get_amb_lv2	Get current configuration of ambient back light control level 0
0x DE	set_amb_lv3	Set ambient back light control level 1
0x DF	get_amb_lv3	Get current configuration of ambient back light control level 1
0x E0	set_pll_start	Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input
0x E1	set_pll_disable	Disable the PLL. When the PLL is disable, the system will start to operate with crystal oscillator or clock input
0x E2	set_pll_mnk	Set the PLL
0x E3	get_pll_mnk	Get the PLL settings
0x E4	get_pll_status	Get the current PLL status
0x E5	set_deep_sleep	Set deep sleep mode
0x E6	set_lshift_freq	Set the LSHIFT (pixel clock) frequency
0x E7	get_lshift_freq	Get current LSHIFT (pixel clock) frequency setting
0x E8	Reserved	Internal Use Only
0x E9	Reserved	Internal Use Only
0x F0	set_pixel_data_interface	Set the pixel data format to 8 bit/12bit/16bit/16bit(565)/18bit in the parallel host processor interface
0x F1	get_pixel_data_interface	Get the current pixel data format settings
0x FF	Reserved	Internal Use Only

9 MAXIMUM RATINGS

Table 9-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DDD}	Digital Core power supply	-0.3 to 1.5	V
V_{DDPLL}	PLL power supply	-0.3 to 1.5	V
V_{DDLCD}	LCD Interface power supply	-0.3 to 4.0	V
V_{DDIO}	I/O power supply	-0.3 to 4.0	V
V_{IN}	Input Voltage	-0.3 to 4.0	V
V_{OUT}	Output Voltage	-0.3 to 4.0	V
T_A	Solder Temperature / Time	225 for 40 sec max at solder ball	^oC
T_{STG}	Storage temperature	-40 to 100	^oC

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DDIO}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

10 DC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DDD}, V_{DDPLL} = 1.2V ± 10%
V_{DDIO}, V_{DDLCD} = 3.3V ± 10%
T_A = -30 to 85°C

Table 10-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
P_{STY}	Quiescent Power			TBD		uW
I_{IZ}	Input leakage current		TBD		TBD	uA
I_{OZ}	Output leakage current		TBD		TBD	uA
V_{OH}	Output high voltage		TBD			V
V_{OL}	Output low voltage				TBD	V
V_{IH}	Input high voltage		TBD			V
V_{IL}	Input low voltage				TBD	V

11 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}
V_{DDD}, V_{DDPLL} = 1.2V ± 10%
V_{DDIO}, V_{DDLCD} = 3.3V ± 10%
T_A = -30°C to 85°C
C_L = 50pF (Bus/CPU Interface)
C_L = 0pF (LCD Panel Interface)

11.1 MCU Interface Timing

11.1.1 6800 Mode

Table 11-1: 6800 Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{cyc}	Reference Clock Cycle Time	9	-	-	ns
t_{PWCSL}	Pulse width CS# or E low	1	-	-	t_{CYC}
t_{PWCSH}	Pulse width CS# or E high	1	-	-	t_{CYC}
t_{FDRD}	First Data Read Delay	5	-	-	t_{CYC}
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	1	-	-	ns
t_{DSW}	Data Setup Time	4	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{DSR}	Data Access Time	-	-	5	ns
t_{DHR}	Output Hold time	1	-	-	ns

Figure 11-1: 6800 Mode Timing Diagram (Use CS# as Clock)

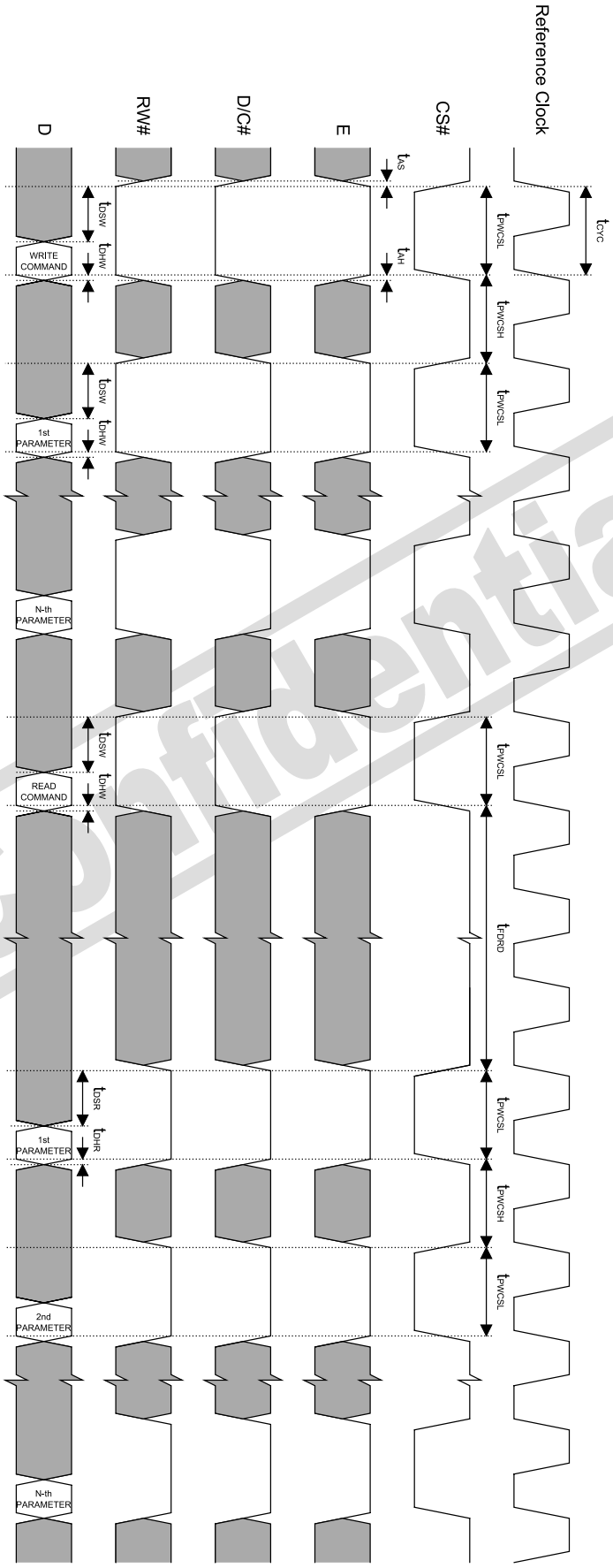
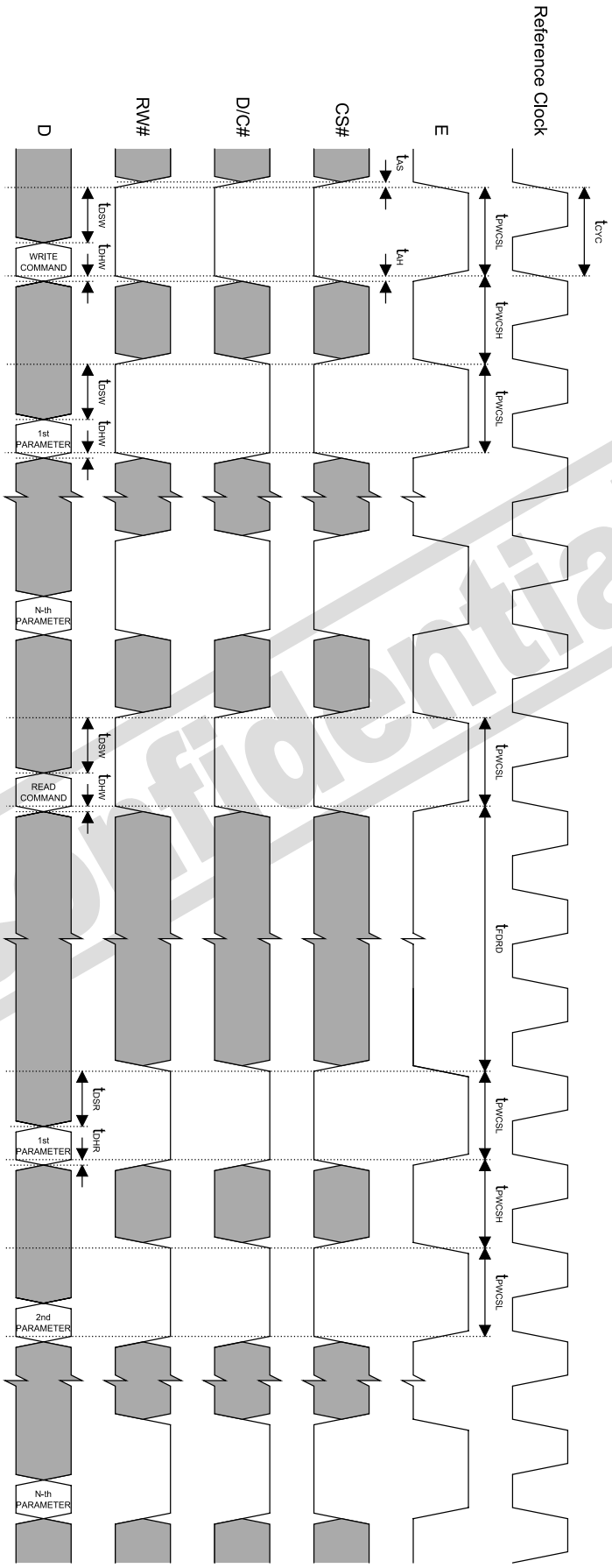


Figure 11-2: 6800 Mode Timing Diagram (Use E as Clock)

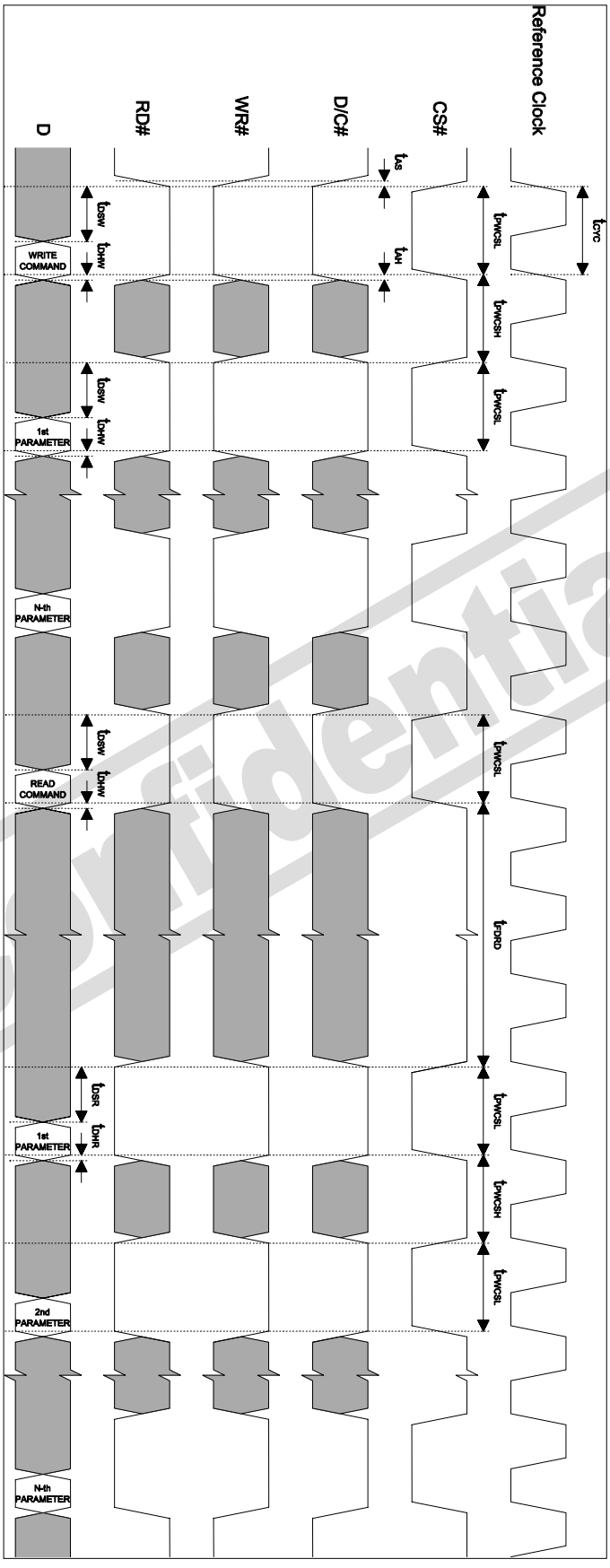


11.1.2 8080 Mode Write Cycle

Table 11-2: 8080 Mode Timing

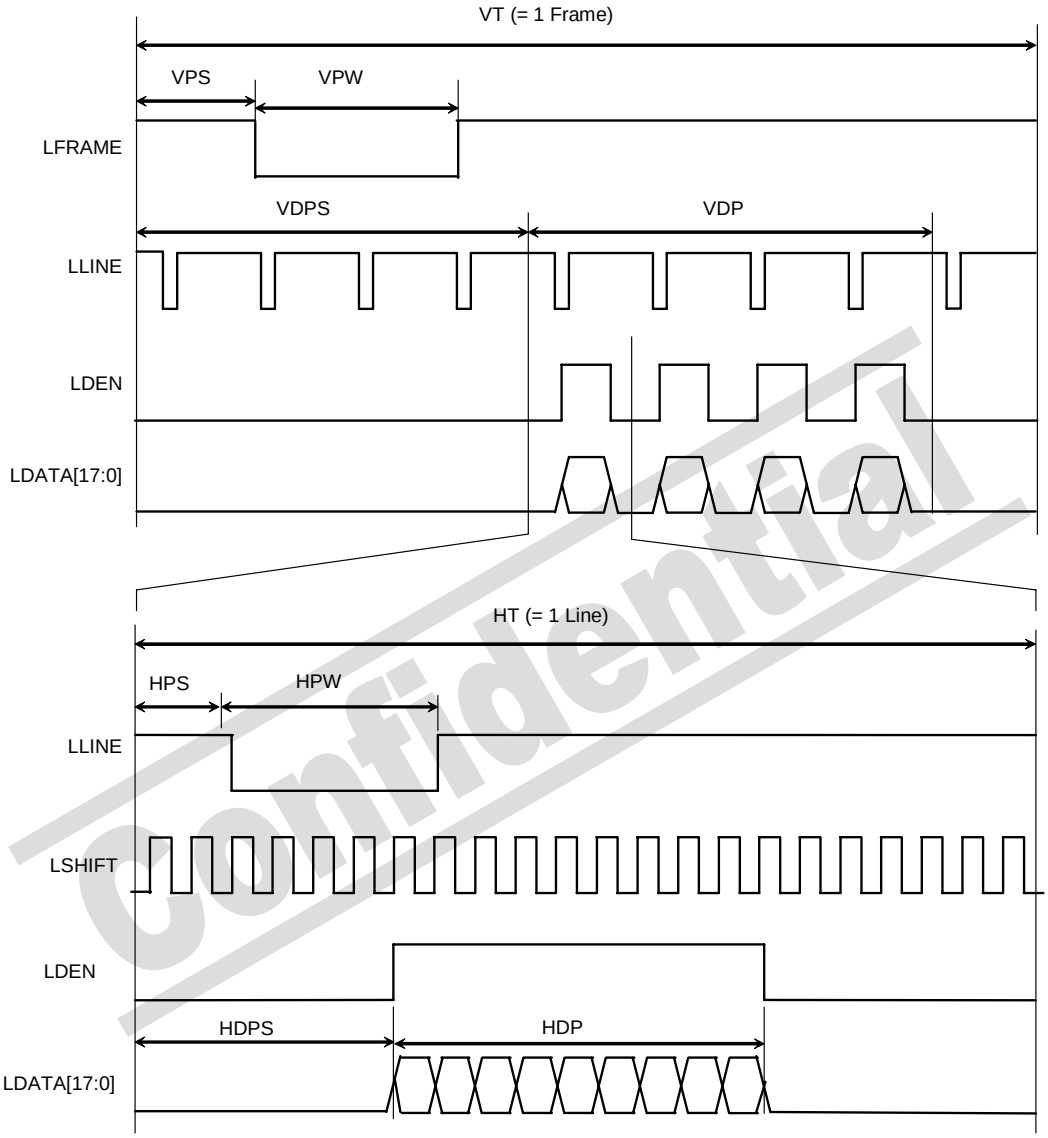
Symbol	Parameter	Min	Typ	Max	Unit
t_{cyc}	Reference Clock Cycle Time	9	-	-	ns
t_{PWCSL}	Pulse width CS# low	1	-	-	t_{CYC}
t_{PWCSH}	Pulse width CS# high	1	-	-	t_{CYC}
t_{FDRD}	First Read Data Delay	5	-	-	t_{CYC}
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	1	-	-	ns
t_{DSW}	Data Setup Time	4	-	-	ns
t_{DHW}	Data Hold Time	1	-	-	ns
t_{DSR}	Data Access Time	-	-	5	ns
t_{DHR}	Output Hold time	1	-	-	ns

Figure 11-3: 8080 Mode Timing Diagram



11.2 LCD Interface Timing

Figure 11-4: Generic TFT Panel Timing



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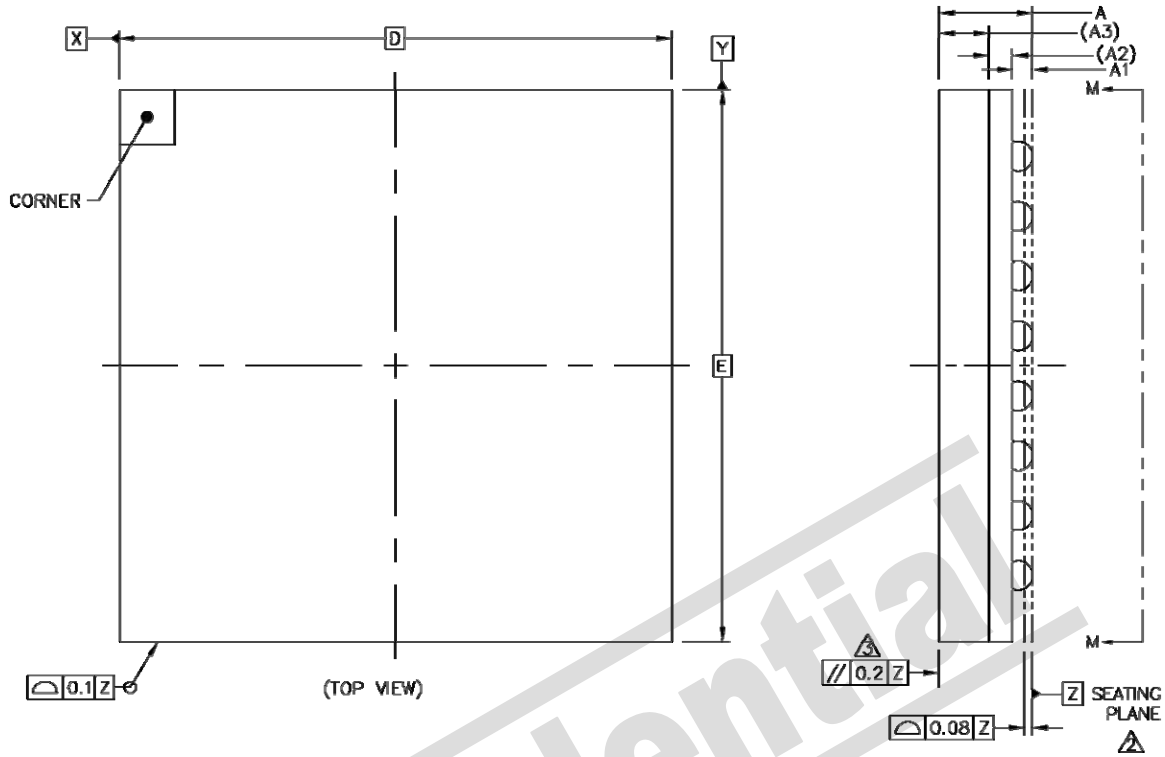

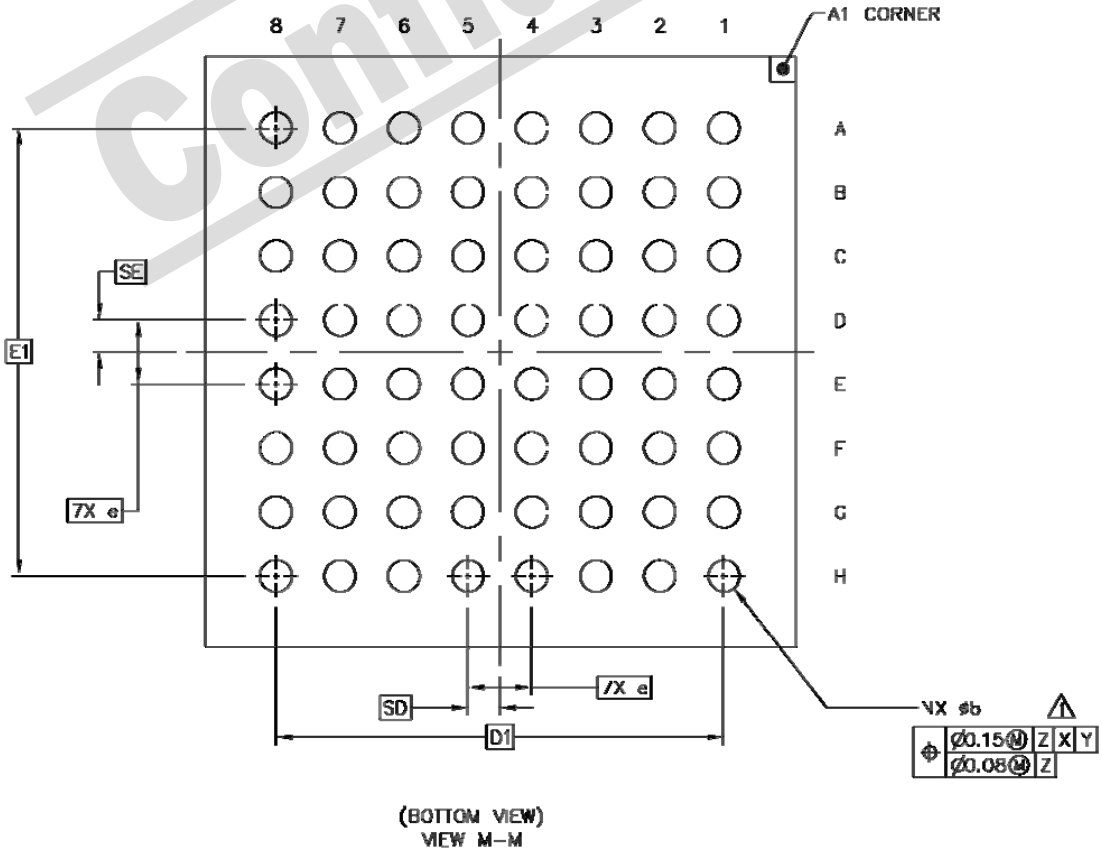

Dimension in mm			
Symbol	**Min**	**Typical**	**Max**
A	--	---	1.1
A1	0.16	---	0.26
A2	---	0.26	---
A3	---	0.54	---
b	0.27	---	0.37
D	---	6.00 BSC	---
E	---	6.00 BSC	---
e	---	0.65	---
D1	---	4.55 BSC	---
E1	---	4.55 BSC	---

All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol . Hazardous Substances test report is available upon requested.

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