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RTL8201E-GR
RTL8201EL-GR
RTL8201E-VC-GR
RTL8201EL-VC-GR

SINGLE-CHIP/PORT 10/100MBPS ETHERNET PHYCEIVER WITH AUTO MDIX

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.7
29 December 2009
Track ID: JATR-2265-11

Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2008/06/18	First release.
1.1	2008/08/08	Revised Table 19, Register 17 Loopback, Bypass, Receiver Error Mask Register (LBREMR), page 17. Added section 8.5 LED and PHY Address Configuration, page 23. Revised section 8.11 3.3V Power Supply and Voltage Conversion Circuit, page 27. Added section 9.1.3 Power On Sequence, page 28. Added section 9.1.4 PHY Reset Sequence, page 29. Revised Table 34, Input Voltage: Vcc, page 30.
1.2	2008/11/14	Removed RMII function. Removed INTB function.
1.3	2008/12/16	Added RTL8201E(L)-VB-GR version and features (RMII and INTB).
1.4	2009/05/05	Added RTL8201E(L)-VC-GR version data. Revised Table 2 RMII Interface (RTL8201E(L)-VC Only), page 8. Revised Table 9 Reset and Other Pins, page 11. Added Table 24 Page 1 Register 16 Interrupt Status Register, page 18. Revised section 8.1.3 Interrupt (RTL8201EL-VC Only), page 22.
1.5	2009/07/03	Revised Table 22 Register 25 Test Register, page 18. Added Table 23 Register 31 Page Select Register, page 18. Revised Table 33 Power Dissipation (mW @ Whole System), page 29.
1.6	2009/12/02	Revised Table 22 Register 25 Test Register, page 18. Revised Table 23 Register 31 Page Select Register, page 18. Added section 9.2.4 RMII Reception Cycle Timing (REFCLK Input Mode; RTL8201E(L)-VC Only), page 34. Added section 9.2.5 RMII Reception Cycle Timing (REFCLK Output Mode; RTL8201E(L)-VC Only), page 35.
1.7	2009/12/29	Revised Table 13 Register 2 PHY Identifier Register 1, page 13. Revised Table 14 Register 3 PHY Identifier Register 2, page 14. Revised Table 29 Absolute Maximum Ratings, page 28.

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1. General Description

The RTL8201E(L) is a single-chip/single-port 10/100Mbps Ethernet PHYceiver that supports:

- MII (Media Independent Interface)
- RMII (Reduced Media Independent Interface; RTL8201E(L)-VC only)
- SNI (Serial Network Interface)

The RTL8201E(L) implements all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), with an auto MDIX function, 10Base-Tx Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU).

A PECL (Pseudo Emitter Coupled Logic) interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.

2. Features

- Supports MII and 7-wire SNI (Serial Network Interface)
- Supports RMII mode (RTL8201E(L)-VC only)
- 10/100Mbps operation
- Full/half duplex operation
- Twisted pair or fiber mode output
- Auto-Negotiation
- Supports power down mode
- Supports operation under Link Down Power Saving mode
- Supports Base Line Wander (BLW) compensation
- Supports auto MDIX
- Supports repeater mode
- Supports Interrupt function (RTL8201EL-VC only)
- Adaptive Equalization
- Network status LEDs
- Flow control support
- 25MHz crystal/oscillator as clock source
- IEEE 802.3/802.3u compliant
- Low power supply, 1.2V, and 3.3V; 1.2V is generated by an internal regulator
- 0.11µm CMOS process
- Packages:
  - 32-pin QFN 'Green' package (RTL8201E)
  - 48-pin LQFP 'Green' package (RTL8201EL)

3. Applications

- Network Interface Adapter
- MAU (Media Access Unit)
- CNR (Communication and Network Riser)
- ACR (Advanced Communication Riser)
- Ethernet hub
- Ethernet switch

In addition, the RTL8201E(L) can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection or Fiber PECL interface to an external 100Base-FX optical transceiver module.

4. Block Diagram

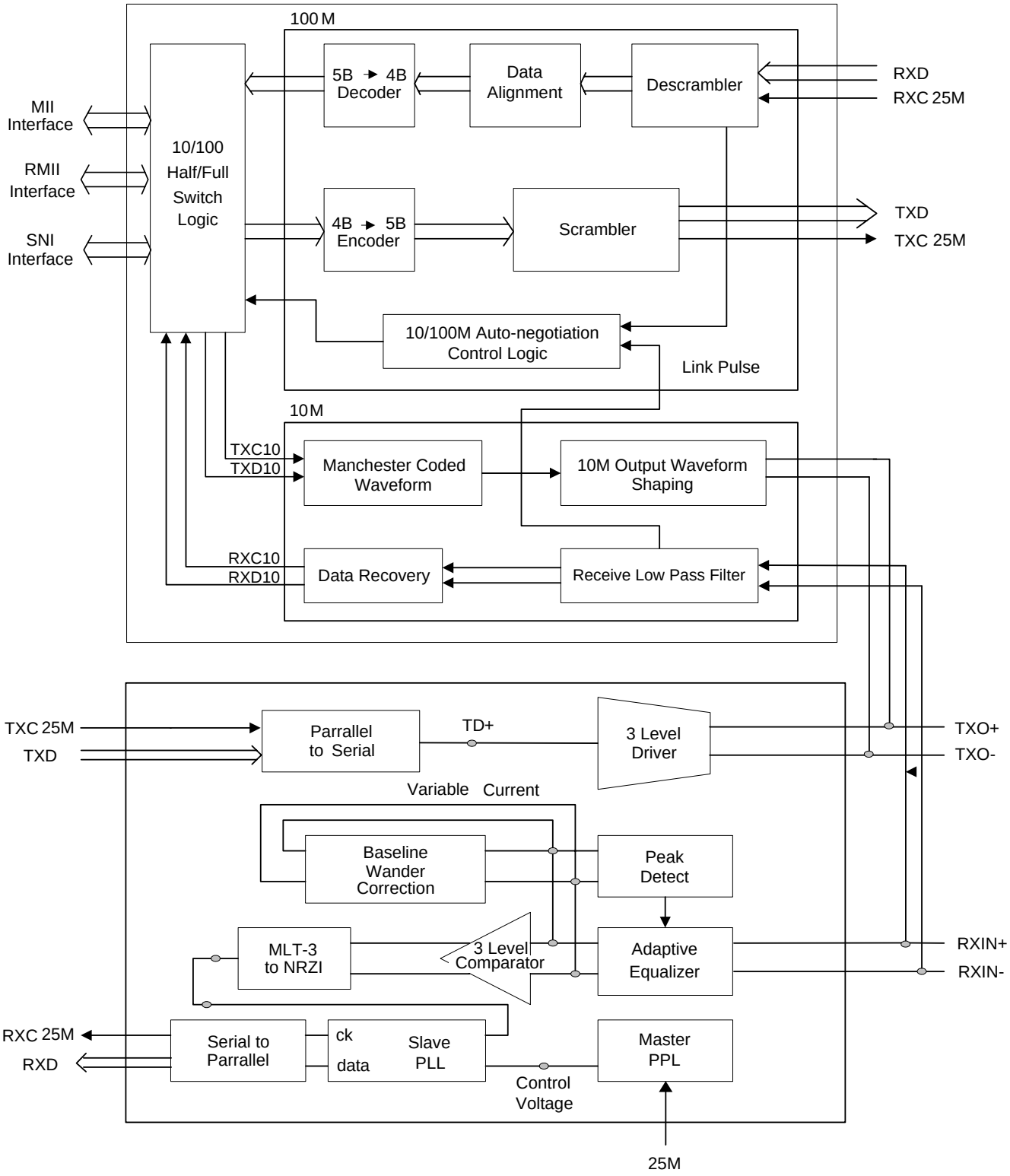


Figure 1. Block Diagram

5. Pin Assignments

5.1. RTL8201E QFN-32 Pin Assignments

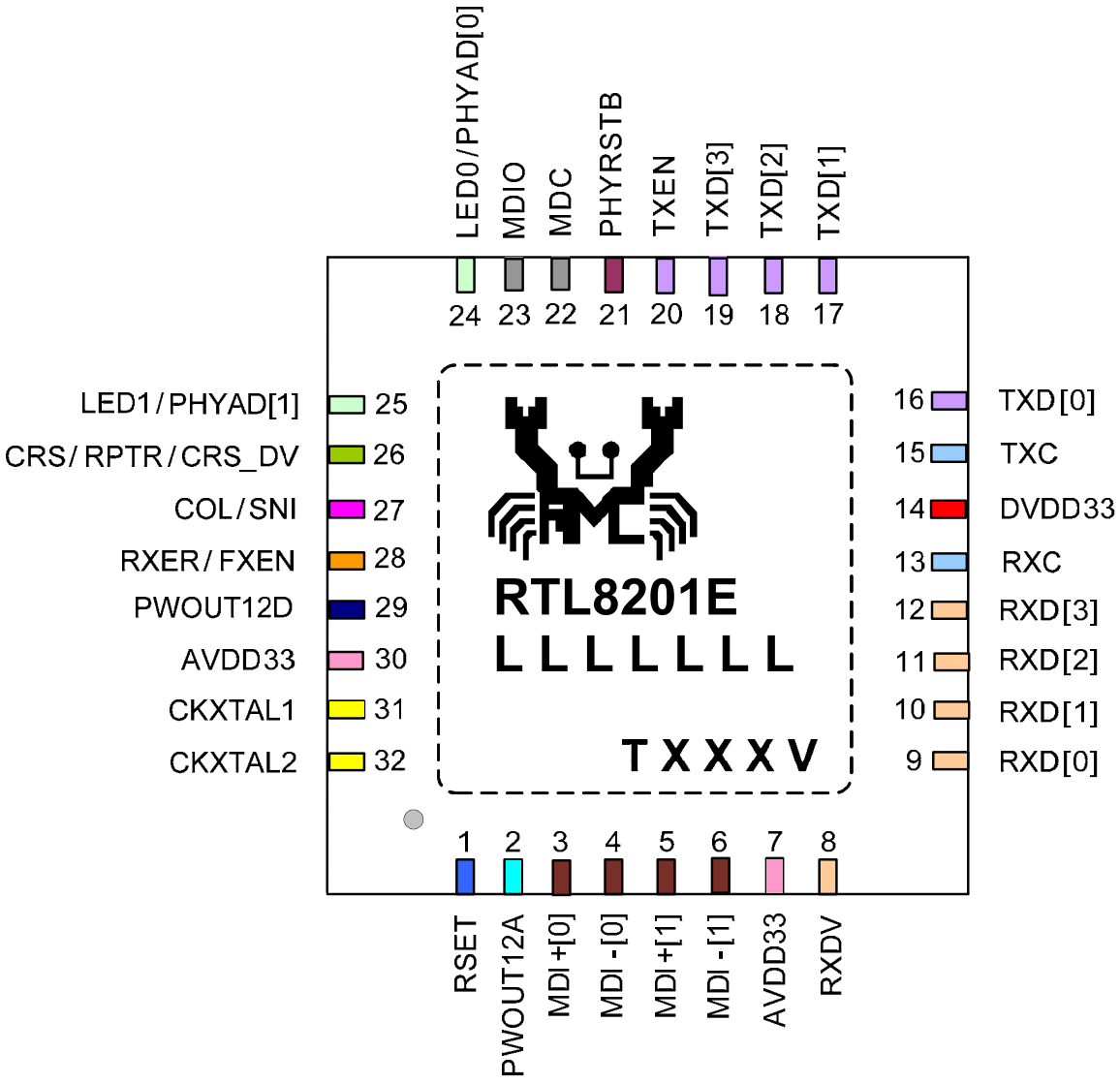


Figure 2. RTL8201E QFN-32 Pin Assignments

5.2. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. The version is shown in the location marked 'V'.

5.3. RTL8201EL LQFP-48 Pin Assignments

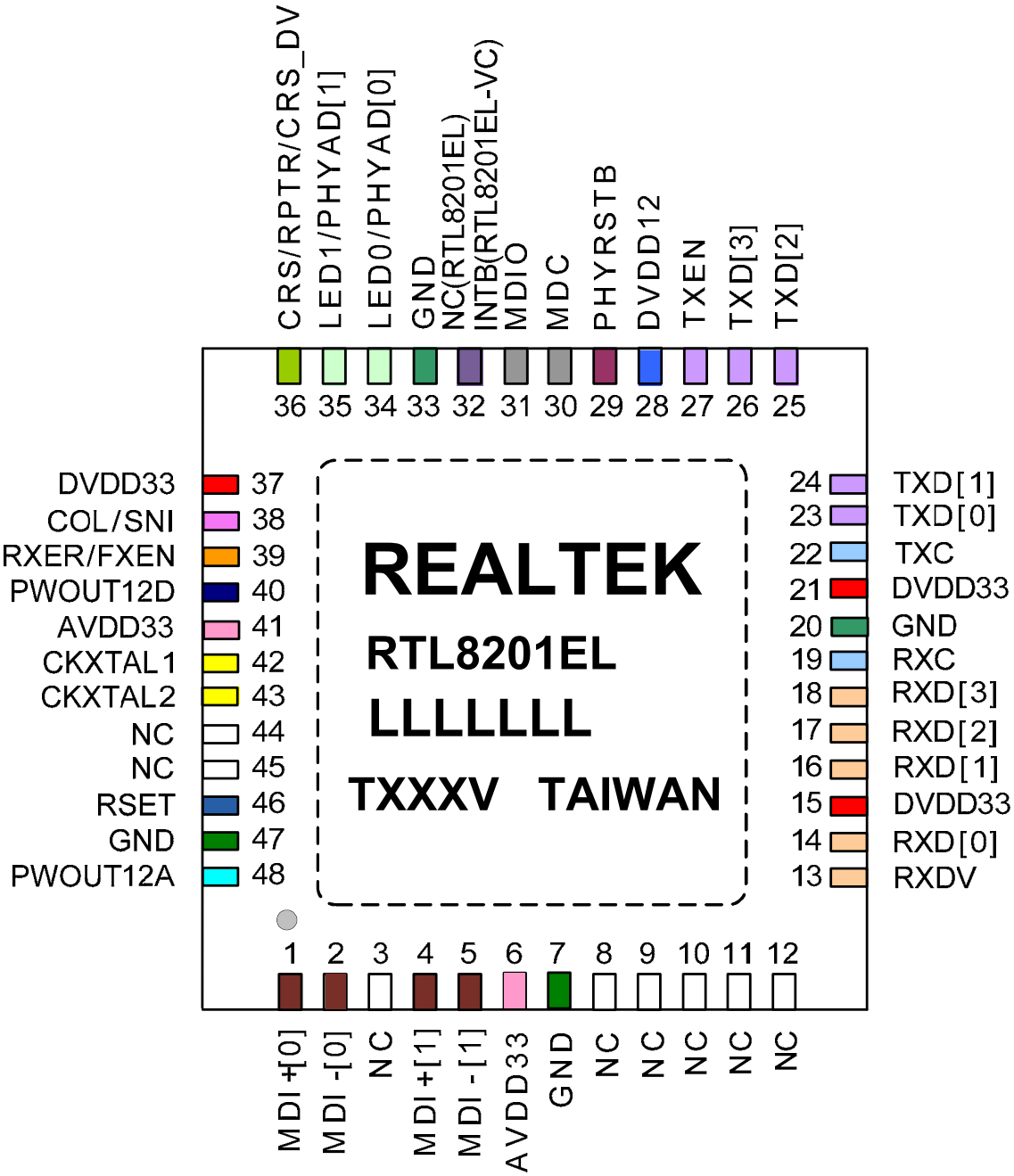


Figure 3. RTL8201EL LQFP-48 Pin Assignments

5.4. Green Package and Version Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 3. The version is shown in the location marked 'V'.

6. Pin Descriptions

I: Input

O: Output

P: Power

PU: Internal Pull up during power on reset

D: Open Drain output

LI: Latched Input during Power up or Reset

IO: Bi-directional input and output

HZ: High impedance during power on reset

PD: Internal Pull down during power on reset

6.1. MII Interface

Table 1. MII Interface

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
TXC	O/HZ	15	22	Transmit Clock. This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN.
TXEN	I/PD	20	27	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD[3:0]. An internal weakly pulled low resistor prevents the bus floating.
TXD[0:3]	I/PD	16, 17, 18, 19	23, 24, 25, 26	Transmit Data. The MAC will source TXD[0:3] synchronous with TXC when TXEN is asserted. An internal weakly pulled low resistor prevents the bus floating.
RXC	O/HZ	13	19	Receive Clock. This pin provides a continuous clock reference for RXDV and RXD[0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
COL/SNI	LI/O/ PD	27	38	Collision Detect. COL is asserted high when a collision is detected on the media. This pin's status is latched at power on reset to determine at which interface mode to operate: 0: MII/RMII mode 1: SNI mode This pin can be directly connected to GND or VCC. *Note: Only the RTL8201E(L)-VC supports RMII mode.*
CRS/RPTR/ CRS_DV	LI/O/ PD	26	36	Carrier Sense. This pin's signal is asserted high if the media is not in Idle state. At power on reset, this pin set high to put the RTL8201E(L) into repeater mode. This pin can be directly connected to GND or VCC.

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
RXDV	LI/O/ PD	8	13	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin. *Note: Only the RTL8201E(L)-VC supports RMII mode.*
RXD[0:3]	O/PD	9, 10, 11, 12	14, 16, 17, 18	Receive Data. These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY).
RXER/ FXEN	LI/O/ PD	28	39	Receive Error. If a 5B decode error occurs, such as invalid /J/K/, invalid /T/R/, or invalid symbol, this pin will go high. Fiber/UTP Enable. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.
MDC	I/PU	22	30	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.
MDIO	IO/PU	23	31	Management Data Input/Output. This pin provides the bi-directional signal used to transfer management information.

6.2. RMII Interface (RTL8201E(L)-VC Only)

Table 2. RMII Interface (RTL8201E(L)-VC Only)

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
TXC	IO	15	22	Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The direction is decided by Page 0 Register 25. The default direction is reference clock input mode.
CRS/RPTR/ CRS_DV	O	26	36	Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non-idle.
RXD[0:1]	O	9, 10	14, 16	Receive Data.
TXEN	I	20	27	Transmit Enable.
TXD[0:1]	I	16, 17	23, 24	Transmit Data.
RXER/FXEN	O	28	39	Receive Error. RX_ER is a required output of the PHY, but is an optional input for the MAC.

6.3. SNI (Serial Network Interface) 10Mbps Only

Table 3. SNI (Serial Network Interface) 10Mbps Only

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
COL/SNI	O/PD	27	38	Collision Detect.
RXD0	O/PD	9	14	Received Serial Data.
CRS/RPTR/ CRS_DV	O/PD	26	36	Carrier Sense.
RXC	O/HZ	13	19	Receive Clock. Resolved from received data.
TXD0	I/PD	16	23	Transmit Serial Data.
TXC	O/HZ	15	22	Transmit Clock. Generated by PHY.
TXEN	I/PD	20	27	Transmit Enable. For MAC to indicate transmit operation.

6.4. Clock Interface

Table 4. Clock Interface

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
CKXTAL2	O	32	43	25MHz Crystal Output. This pin provides the 25MHz crystal output. It must be left open when an external 25MHz oscillator drives X1.
CKXTAL1	I	31	42	25MHz Crystal Input. This pin provides the 25MHz crystal input. If a 25MHz oscillator is used, connect CKXTAL1 to the oscillator's output (see 9.3 Crystal Characteristics, page 39, for clock source specifications).

6.5. 10Mbps/100Mbps Network Interface

Table 5. 10Mbps/100Mbps Network Interface

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
MDI+[0] MDI-[0]	O	3 4	1 2	Transmit Output. Differential transmit output pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo-ECL level.
RSET	I	1	46	Transmit Bias Resistor Connection. This pin should be pulled to GND by a 2.49KΩ (1%) resistor to define driving current for the transmit DAC. The resistance value may be changed, depending on experimental results of the RTL8201E(L).
MDI+[1] MDI-[1]	I	5 6	4 5	Receive Input. Differential receive input pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.

6.6. Device Configuration Interface

Table 6. Device Configuration Interface

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
RXDV	LI/O /PD	8	13	RMII/MII Interface This pin's status is latched at power on reset to determine at which interface mode to operate: 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. *Note: Only the RTL8201E(L)-VC supports RMII mode.*

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
LED0/PHYAD[0] LED1/PHYAD[1]	LI/O /HZ	24 25	34 35	PHY Address. Sets the PHY address for the device.
CRS/RPTR/ CRS_DV	LI/O /PD	26	36	Repeater Mode. Set high to put the RTL8201E(L) into repeater mode. This pin can be directly connected to GND or VCC.
COL/SNI	LI/O /PD	27	38	MII/RMII/SNI Interface. This pin is latched to input at a power on or reset condition. Pull high to set the RTL8201E(L) into SNI mode operation. Set low for MII/RMII mode. This pin can be directly connected to GND or VCC. *Note: Only the RTL8201E(L)-VC supports RMII mode.*
RXER/FXEN	LI/O /PD	28	39	Fiber/UTP Interface. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.

6.7. LED Interface/PHY Address Configuration

Table 7. LED Interface/PHY Address Configuration

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
LED0/PHYAD[0]	LI/O/HZ	24	34	Link Indicator.
LED1/PHYAD[1]	LI/O/HZ	25	35	Receive/Transmit LED.

6.8. Power and Ground Pins

Table 8. Power and Ground Pins

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
AVDD33	P	7, 30	6, 41	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
DVDD33	P	14	15, 21, 37	3.3V Digital Power Input. 3.3V power supply for digital circuit.
DVDD12	P	-	28	1.2V Digital Power.
GND	P	-	7, 20, 33, 47	Ground. Should be connected to a larger GND plane.

6.9. Reset and Other Pins

Table 9. Reset and Other Pins

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
PHYRSTB	I/HZ	21	29	RESETB. Set low to reset the chip. For a complete reset, this pin must be asserted low for at least 10ms.
PWOUT12D PWOUT12A	O	29 2	40 48	Power Output. Be sure to connect a 0.1µF ceramic capacitor for decoupling purposes. The connection method is outlined in 8.11 3.3V Power Supply and Voltage Conversion Circuit, page 27.
INTB	D	-	32	Interrupt. Set low if link status change, duplex change, or auto negotiation fail. Active Low. This pin is an open-drain design, and for default value should be pulled high by an external 4.7KΩ. If not used, keep floating. *Note: Only the RTL8201EL-VC supports Interrupt pin.*

6.10. NC (Not Connected) Pins

Table 10. NC (Not Connected) Pins

Name	Type	Pin No. (QFN-32)	Pin No. (LQFP-48)	Description
NC	-	-	3, 8, 9, 10, 11, 12, 32, 44, 45 (Pin 32 is NC in RTL8201EL-GR Only)	Not Connected.

7. Register Descriptions

This section describes the functions and usage of the registers available in the RTL8201E(L). In this section the following abbreviations are used:

RO: Read Only RW: Read/Write

7.1. Register 0 Basic Mode Control Register

Table 11. Register 0 Basic Mode Control Register

Address	Name	Description	Mode	Default
0:15	Reset	This bit sets the status and control registers of the PHY in the default state. This bit is self-clearing. 1: Software reset 0: Normal operation	RW	0
0:14	Loopback	This bit enables loopback of transmit data nibbles TXD3:0 to the receive data path. 1: Enable loopback 0: Normal operation	RW	0
0:13	Spd_Set	This bit sets the network speed. 1: 100Mbps 0: 10Mbps After completing auto negotiation, this bit will reflect the Speed status. 1: 100Base-T 0: 10Base-T When 100Base-FX mode is enabled, this bit=1 and is read only.	RW	0
0:12	Auto Negotiation Enable	This bit enables/disables the NWay auto-negotiation function. 1: Enable auto-negotiation; bits 0:13 and 0:8 will be ignored 0: Disable auto-negotiation; bits 0:13 and 0:8 will determine the link speed and the data transfer mode, respectively When 100Base-FX mode is enabled, this bit=0 and is read only.	RW	1
0:11	Power Down	This bit turns down the power of the PHY chip, including the internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing the MAC. 1: Power down 0: Normal operation	RW	0
0:10	Reserved	Reserved.	-	-
0:9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset. 1: Re-start auto-negotiation 0: Normal operation	RW	0
0:8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 0:12=0). 1: Full duplex 0: Half duplex After completing auto-negotiation, this bit will reflect the duplex status. 1: Full duplex 0: Half duplex	RW	0
0:7~0	Reserved	Reserved.	-	-

7.2. Register 1 Basic Mode Status Register

Table 12. Register 1 Basic Mode Status Register

Address	Name	Description	Mode	Default
1:15	100Base-T4	1: Enable 100Base-T4 support 0: Suppress 100Base-T4 support	RO	0
1:14	100Base_TX_ FD	1: Enable 100Base-TX full duplex support 0: Suppress 100Base-TX full duplex support	RO	1
1:13	100Base_TX_HD	1: Enable 100Base-TX half duplex support 0: Suppress 100Base-TX half duplex support	RO	1
1:12	10Base_T_FD	1: Enable 10Base-T full duplex support 0: Suppress 10Base-T full duplex support	RO	1
1:11	10_Base_T_HD	1: Enable 10Base-T half duplex support 0: Suppress 10Base-T half duplex support	RO	1
1:10~7	Reserved	Reserved.	-	-
1:6	MF Preamble Suppression	The RTL8201E(L) will accept management frames with preamble suppressed. A minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications.	RO	1
1:5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	RO	0
1:4	Remote Fault	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault has been detected (see 8.12 Far End Fault Indication, page 27).	RO	0
1:3	Reserved	Reserved.	-	-
1:2	Link Status	1: Valid link established 0: No valid link established	RO	0
1:1~0	Reserved	Reserved.	-	-

7.3. Register 2 PHY Identifier Register 1

Table 13. Register 2 PHY Identifier Register 1

Address	Name	Description	Mode	Default
2:15~0	OUI_MSB	Organizationally Unique Identifier Bit 3:18	RO	001Ch

7.4. Register 3 PHY Identifier Register 2

Table 14. Register 3 PHY Identifier Register 2

Address	Name	Description	Mode	Default
3:15~10	OUI_LSB	Organizationally Unique Identifier Bit 19:24	RO	110010
3:9~4	Model Number	Model Number	RO	000001
3:3~0	Revision Number	Revision Number	RO	0101

7.5. Register 4 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Table 15. Register 4 Auto-Negotiation Advertisement Register (ANAR)

Address	Name	Description	Mode	Default
4:15	NP	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
4:14	ACK	1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception	RO	0
4:13	RF	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	RW	0
4:12~11	Reserved	Reserved.	-	-
4:10	RXFC	1: RX flow control is supported by local node 0: RX flow control not supported by local node	RW	0
4:9	T4	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	RO	0
4:8	TXFD	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	RW	1
4:7	100B-TX	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node	RW	1
4:6	10FD	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node	RW	1
4:5	10B-T	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node	RW	1
4:4~0	Selector[4:0]	Binary encoded selector supported by this node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.	RW	00001

7.6. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Table 16. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

Address	Name	Description	Mode	Default
5:15	NP	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
5:14	ACK	1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement	RO	0
5:13	RF	1: Link partner is indicating a remote fault 0: Link partner is not indicating a remote fault	RO	0
5:12	Reserved	Reserved.	-	-
5:11	TXFC	1: TX flow control is supported by Link partner 0: TX flow control not supported by Link partner	RO	0
5:10	RXFC	1: RX flow control is supported by Link partner 0: RX flow control not supported by Link partner	RO	0
5:9	T4	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner	RO	0
5:8	TXFD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	RO	0
5:7	100Base-TX	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner This bit will also be set if the link in 100Base is established by parallel detection.	RO	0
5:6	10FD	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner	RO	0
5:5	10Base-T	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner This bit will also be set if the link in 10Base-T is established by parallel detection.	RO	0
5:4~0	Selector[4:0]	Link Partner's Binary Encoded Node Selector. Currently only CSMA/CD 00001 is specified.	RO	00000

7.7. Register 6 Auto-Negotiation Expansion Register (ANER)

This register contains additional status for NWay auto-negotiation.

Table 17. Register 6 Auto-Negotiation Expansion Register (ANER)

Address	Name	Description	Mode	Default
6:15~5	Reserved	Reserved.	-	-
6:4	MLF	Indicates whether a Multiple Link Fault Has Occurred. 1: Fault occurred 0: No fault occurred	RO	0
6:3	LP_NP_ABLE	Indicates whether the Link Partner Supports Next Page Negotiation. 1: Supported 0: Not supported	RO	0
6:2	NP_ABLE	This bit indicates whether the local node is able to send additional Next Pages. Internal use only.	RO	0
6:1	PAGE_RX	This bit is set when a new link code word page has been received. It is automatically cleared when the auto-negotiation link partner's ability register (register 5) is read by management.	RO	0
6:0	LP_NW_ABLE	1: Link partner supports NWay auto-negotiation.	RO	0

7.8. Register 16 NWay Setup Register (NSR)

Table 18. Register 16 NWay Setup Register (NSR)

Address	Name	Description	Mode	Default
16:15~11	Reserved	Realtek Test Mode Internal Use. Do not change this field without Realtek's approval.	-	-
16:10	Testfun	1: Auto-negotiation speeds up internal timer	RW	0
16:9	NWLPBK	1: Set NWay to loopback mode	RW	0
16:8~3	Reserved	Reserved.	-	-
16:2	FLAGABD	1: Auto-negotiation experienced ability detect state	RO	0
16:1	FLAGPDF	1: Auto-negotiation experienced parallel detection fault state	RO	0
16:0	FLAGLSC	1: Auto-negotiation experienced link status check state	RO	0

7.9. Register 17 Loopback, Bypass, Receiver Error Mask Register (LBREMR)

Table 19. Register 17 Loopback, Bypass, Receiver Error Mask Register (LBREMR)

Address	Name	Description	Mode	Default
17:15	RPTR	Set to 1 to put the RTL8201E(L) into repeater mode.	RW	0
17:14	BP_4B5B	Assertion of this bit allows bypassing of the 4B/5B & 5B/4B encoder.	RW	0
17:13	BP_SCR	Assertion of this bit allows bypassing of the Scrambler/Descrambler.	RW	0
17:12	LDPS	Set to 1 to enable Link Down Power Saving mode.	RW	0
17:11	AnalogOFF	Set to 1 to power down the analog function of transmitter and receiver.	RW	0
17:10	BMODE_EN	Sets the inverse function of the Receive/Transmit LED.	RW	1
17:9	DIGILBK	Set to 1 to enable DSP loopback.	RW	0
17:8	F_Link_10	Used to logic force a good link in 10Mbps for diagnostic purposes.	RW	1
17:7	F_Link_100	Used to logic force a good link in 100Mbps for diagnostic purposes.	RW	1
17:6	JBEN	Set to 1 to enable jabber function in 10Base-T.	RW	1
17:5	CODE_err	Assertion of this bit causes a code error detection to be reported.	RW	0
17:4	PME_err	Assertion of this bit causes a pre-mature end error detection to be reported.	RW	0
17:3	LINK_err	Assertion of this bit causes a link error detection to be reported.	RW	0
17:2	PKT_err	Assertion of this bit causes a ‘detection of packet errors due to 722 ms time-out’ to be reported.	RW	0
17:1	FXMODE	This bit indicates whether Fiber Mode is enabled.	RW	0
17:0	SNIMODE	This bit indicates whether SNI Mode is enabled.	RW	0

7.10. Register 18 RX_ER Counter (REC)

Table 20. Register 18 RX_ER Counter (REC)

Address	Name	Description	Mode	Default
18:15~0	RXERCNT	This 16-bit counter increments by 1 for each invalid packet received. The value is valid while the link is established.	RO	0000

7.11. Register 19 SNR Display Register

Table 21. Register 19 SNR Display Register

Address	Name	Description	Mode	Default
19:15~4	Reserved	Realtek Test Mode Internal Use. Do not change this field without Realtek’s approval.	-	-
19:3~0	SNR_0	These 4-Bits Show the Signal to Noise Ratio Value.	RW	0000

7.12. Register 25 Test Register

Table 22. Register 25 Test Register

Address	Name	Description	Mode	Default
25:15	Reserved	Reserved for Internal Testing.	RW	0
25:14	PACKAGE_INDICATE	Package Type Indicator. 0: 48pin 1: 32pin	RW	0
25:13	RMII_RXD_TRIG	This Bit Sets the RXD Output from the REF_CLK Rising or Falling Edge. 0: RXD and CRS_DV output at REF_CLK falling edge 1: RXD and CRS_DV output at REF_CLK rising edge	RW	1
25:12	Reserved	Reserved for Internal Testing.	-	-
25:11	RMII_CLKIN	This Bit Sets the Type of TXC in RMII mode 0: Output 1: Input	RW	1
25:10	RMII Mode	This Bit Sets the RMII Mode. 1: RMII mode 0: MII mode	RW	0
25:9	RMII_CRS_SEL	This Bit Determines whether CRS can Toggle or Not. 0: Toggle 1: No Toggle	RW	0
25:8~7	PHYAD[1:0]	Reflects the PHY Address Defined by the External PHY Address Configuration Pins.	RO	01
25:6~2	Reserved	Reserved for Internal Testing.	RO	-
25:1	LINK10	1: 10Base-T link established 0: No 10Base-T link established	RO	0
25:0	LINK100	1: 100Base-FX or 100Base-TX link established 0: No 100Base link established	RO	0

7.13. Register 31 Page Select Register

Table 23. Register 31 Page Select Register

Address	Name	Description	Mode	Default
31:15~2	Reserved	Reserved for Internal Testing.	-	-
31:1~0	PAGE SEL	00: PAGE0 01: PAGE1 10: PAGE2	RW	00

7.14. Page 1 Register 16 Interrupt Status Register

Table 24. Page 1 Register 16 Interrupt Status Register

Address	Name	Description	Mode	Default
16:15	ANERR	Auto-Negotiation Error Interrupt	R	-
16:14	LNKSTS	Link Status Change Interrupt	R	-
16:13	DUPLEX	Duplex Mode Change Interrupt	R	-
16:12~0	Reserved	Reserved	-	-

8. Functional Description

The RTL8201E(L) PHYceiver is a physical layer device that integrates 10Base-T and 100Base-TX/ 100Base-FX functions, and some extra power management features. This device supports the following functions:

- MII interface with MDC/MDIO SMI management interface to communicate with the MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Flow control ability support to cooperate with MAC
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO
- 7-wire SNI (Serial Network Interface) support (only in 10Mbps mode)
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT-3
- Manchester Encode and Decode for 10Base-T operation
- Clock and Data recovery
- Adaptive Equalization
- Far End Fault Indication (FEFI) in fiber mode

8.1. MII and Management Interface

8.1.1. Data Transition

To set the RTL8201E(L) for MII mode operation, pull the COL/SNI pin low.

The MII (Media Independent Interface) is an 18-signal interface (as described in IEEE 802.3u) supplying a standard interface between the PHY and MAC layer.

This interface operates at two frequencies – 25MHz and 2.5MHz – to support 100Mbps/10Mbps bandwidth for both transmit and receive functions.

Transmission

The MAC asserts the TXEN signal. It then changes byte data into 4-bit nibbles and passes them to the PHY via TXD[3:0]. The PHY will sample TXD[3:0] synchronously with TXC – the transmit clock signal supplied by the PHY – during the interval TXEN is asserted.

Reception

The PHY asserts the RXEN signal. It passes the received nibble data RXD[3:0] clocked by RXC. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when the decoded signal in 5B is not IDLE, the CRS signal will assert. When 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble has been confirmed and will be de-asserted when the IDLE pattern has been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be de-asserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur, e.g., an invalid J/K, invalid T/R, or invalid symbol. This pin will go high for one or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame.

Note: The RTL8201E(L) does not use a TXER signal. This does not affect the transmit function.

8.1.2. Serial Management

The MAC layer device can use the MDC/MDIO management interface to control a maximum of 4 RTL8201E(L) devices, configured with different PHY addresses (00b to 11b).

During a hardware reset, the logic levels of pins 34/24 and 35/25 are latched into the RTL8201E(L) to be set as the PHY address for management communication via the serial interface. The read and write frame structure for the management interface is illustrated in Figure 4 and Figure 5.

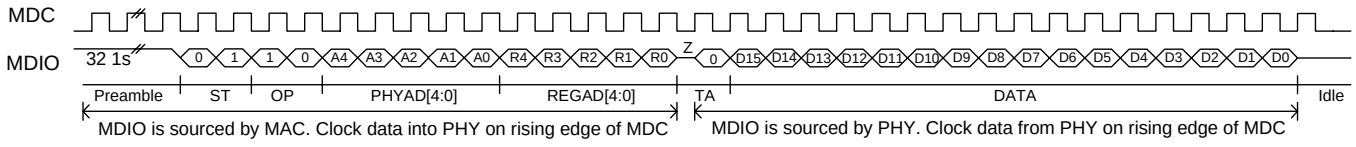


Figure 4. Read Cycle

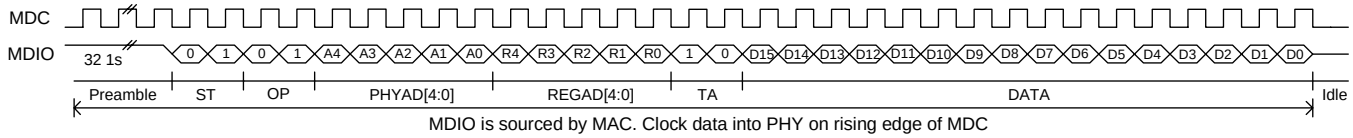


Figure 5. Write Cycle

Table 25. Serial Management

Name	Description
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

8.1.3. Interrupt (RTL8201EL-VC Only)

Whenever there is a status change on the media detected by the RTL8201EL-VC, the RTL8201EL-VC will drive the interrupt pin (INTB) low to issue an interrupt event. The MAC senses the status change and accesses the registers (P1:R16) through the MDC/MDIO interface in response.

Once these status registers (P1:R16) have been read by the MAC through the MDC/MDIO, the INTB is de-asserted. The RTL8201EL-VC interrupt function removes the need for continuous polling through the MDC/MDIO management interface.

8.2. Auto-Negotiation and Parallel Detection

The RTL8201E(L) supports IEEE 802.3u clause 28 Auto-negotiation for operation with other transceivers supporting auto-negotiation. The RTL8201E(L) can auto-detect the link partner's abilities and determine the highest speed/duplex configuration possible between the two devices. If the link partner does not support auto-negotiation, then the RTL8201E(L) will enable half duplex mode and enter parallel detection mode. The RTL8201E(L) will default to transmitting FLP (Fast Link Pulse) and wait for the link partner to respond. If the RTL8201E(L) receives a FLP, then the auto-negotiation process will go on. If it receives NLP (Normal Link Pulse), then the RTL8201E(L) will change to 10Mbps and half duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half duplex mode.

8.2.1. Setting the Medium Type and Interface Mode to MAC

Table 26. Setting the Medium Type and Interface Mode to MAC

FXEN	COL/SNI	RXDV	Operation Mode
H	L	L	Fiber Mode and MII Mode
H	L	H	Fiber Mode and RMII Mode
H	H	X	Fiber Mode and SNI Mode
L	L	L	UTP Mode and MII Mode
L	L	H	UTP Mode and RMII Mode
L	H	X	UTP Mode and SNI Mode

8.3. Flow Control Support

The RTL8201E(L) supports flow control indications. The MAC can program the MII register to indicate to the PHY that flow control is supported. When the MAC supports the Flow Control mechanism, the OS sets bit 10 of the ANAR register via the MAC using the MDC/MDIO SNI interface; then the RTL8201E(L) will add the ability to its NWay ability. If the Link partner also supports Flow Control, the RTL8201E(L) can recognize the Link partner's NWay ability by examining bit 10 of the ANLPAR (register 5).

8.4. Hardware Configuration and Auto-Negotiation

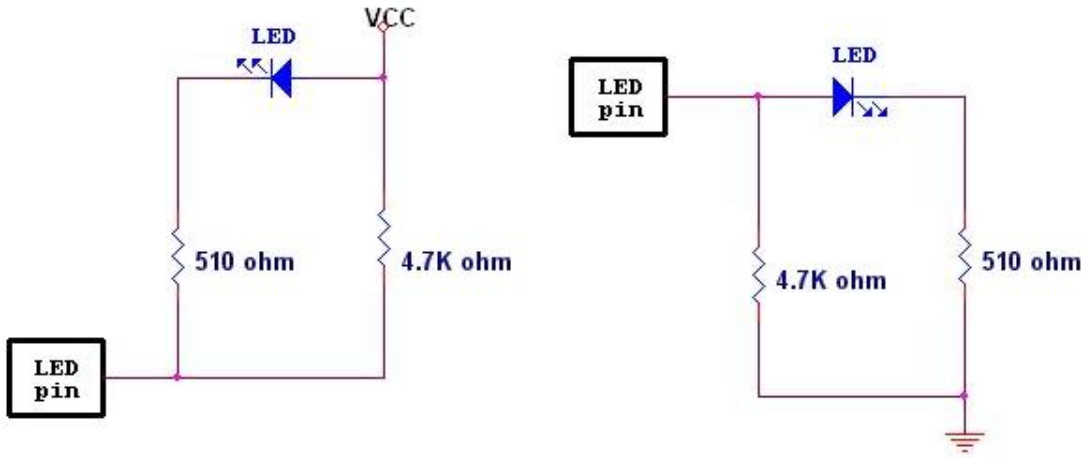
This section describes methods to configure the RTL8201E(L) and set the auto-negotiation mode. Table 27 shows the various pins and their settings.

Table 27. Auto-Negotiation Mode Pin Settings

Pin Name	Description
CRS/RPTR/ CRS_DV	Pull high to set the RTL8201E(L) into Repeater Mode. This pin is pulled low by default (see 8.9 Repeater Mode Operation, page 26).
COL/SNI	Pull low to set the RTL8201E(L) into MII/RMII Mode operation, which is the Default Mode for the RTL8201E(L). This pin pulled high will set the RTL8201E(L) into SNI mode operation. When set to SNI mode, the RTL8201E(L) will operate at 10Mbps (see section 8.6 Serial Network Interface, page 24).

8.5. LED and PHY Address Configuration

In order to reduce the pin count on the RTL8201E(L), the LED pins are duplexed with the PHY address pins. The external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, as Figure 6 (left-side) shows, if a given PHYAD input is resistively pulled high, then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



PHY Address[:]=Logical 1
LED Indication=Active low

PHY Address[:]=Logical 0
LED Indication=Active High

Figure 6. LED and PHY Address Configuration

8.6. Serial Network Interface

The RTL8201E(L) also supports the traditional 7-wire serial interface to operate with legacy MACs or embedded systems. To setup for this mode of operation, pull the COL/SNI pin high. In this mode, the RTL8201E(L) will set the default operation to 10Mbps and half-duplex mode. This interface consists of a 10Mbps transmit and receive clock generated by the PHY, 10Mbps transmit and receive serial data, transmit enable, collision detect, and carry sense signals.

8.7. Power Down, Link Down, and Power Saving Modes

Three types of Power Saving mode operation are supported. This section describes how to implement each mode through software.

Table 28. Power Saving Mode Pin Settings

Mode	Description
Analog Off	Setting bit 11 of register 17 to 1 will put the RTL8201E(L) into analog off state. In analog off state, the RTL8201E(L) will power down all analog functions such as transmit, receive, PLL, etc. However, the internal 25MHz crystal oscillator will not be powered down. Digital functions in this mode are still available which allows reacquisition of analog functions
LDPS	Setting bit 12 of register 17 to 1 will put the RTL8201E(L) into LDPS (Link Down Power Saving) mode. In LDPS mode, the RTL8201E(L) will detect the link status to decide whether or not to turn off the transmit function. If the link is off, FLP or 100Mbps IDLE/10Mbps NLP will not be transmitted. However, some signals similar to NLP will be transmitted. Once the receiver detects leveled signals, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This can cut power used by 60%~80% when the link is down.
PWD	Setting bit 11 of register 0 to 1 puts the RTL8201E(L) into power down mode. This is the maximum power saving mode while the RTL8201E(L) is still alive. In PWD mode, the RTL8201E(L) will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the RTL8201E(L) is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).

8.8. Media Interface

8.8.1. 100Base-TX Transmit and Receive Operation

100Base-TX Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 25MHz (TXC) is transformed into 5B symbol code (4B/5B encoding). Scrambling, serializing, and conversion to 125MHz, and NRZ to NRZI then takes place. After this process, the NRZI signal is passed to the MLT-3 encoder, then to the transmit line driver. The transmitter will first assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol, and finally a /T/R/ symbol known as the End-Of-Frame delimiter. For better EMI performance, the seed of the scrambler is based on the PHY address. In a hub/switch environment, each RTL8201E(L) will have different scrambler seeds and so spread the output of the MLT-3 signals.

100Base-TX Receive

The received signal is compensated by the adaptive equalizer to make up for signal loss due to cable attenuation and Inter Symbol Interference (ISI). Baseline Wander Correction monitors the process and dynamically applies corrections to the process of signal equalization. The Phase Locked Loop (PLL) then recovers the timing information from the signals and from the receive clock. With this, the received signal is sampled to form NRZI (Non-Return-to-Zero Inverted) data. The next steps are the NRZI to NRZ (Non-Return-to-Zero) process, unscrambling of the data, serial to parallel and 5B to 4B conversion, and passing of the 4B nibble to the MII interface.

8.8.2. 100Base-FX Fiber Transmit and Receive Operation

The RTL8201E(L) can be configured to 100Base-FX mode via hardware configuration. The hardware 100Base-FX setting takes priority over NWay settings. A scrambler is not required in 100Base-FX.

100Base-FX Transmit

Di-bits of TXD are processed as 100Base-TX except without a scrambler before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pair form.

100Base-FX Receive

The signal is received through PECL receiver inputs from the fiber transceiver and directly passed to the clock recovery circuit for data/clock recovery. The scrambler/de-scrambler is bypassed in 100Base-FX.

8.8.3. 10Base-T Transmit and Receive Operation

10Base-T Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC) is first fed to a parallel-to-serial converter, then the 10Mbps NRZ signal is sent to a Manchester encoder. The Manchester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a Start of Idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Finally, the encoded data stream is shaped by a band-limited filter embedded in the RTL8201E(L) and then transmitted.

10Base-T Receive

In 10Base-T receive mode, the Manchester decoder in the RTL8201E(L) converts the Manchester encoded data stream into NRZ data by decoding the data and stripping off the SOI pulse. Then the serial NRZ data stream is converted to a parallel 4-bit nibble signal (RXD[0:3]).

8.9. Repeater Mode Operation

Setting bit 15 of register 17 to 1, or pulling the RPTR pin high, sets the RTL8201E(L) into repeater mode. In repeater mode, the RTL8201E(L) will assert CRS high only when receiving a packet. In NIC mode, the RTL8201E(L) will assert CRS high both when transmitting and receiving packets. If using the RTL8201E(L) in a NIC or switch application, set to the default mode. NIC/Switch mode is the default setting and has the RPTR pin pulled low, or bit 15 of register 17 is set to 0.

8.10. Reset and Transmit Bias

The RTL8201E(L) can be reset by pulling the PHYRSTB pin low for about 10ms, then pulling the pin high. It can also be reset by setting bit 15 of register 0 to 1, and then setting it back to 0. Reset will clear the registers and re-initialize them. The media interface will disconnect and restart the auto-negotiation/parallel detection process.

The RSET pin must be pulled low by a 2.49KΩ resistor with 1% accuracy to establish an accurate transmit bias. This will affect the signal quality of the transmit waveform. Keep its circuitry away from other clock traces and transmit/receive paths to avoid signal interference.

8.11. 3.3V Power Supply and Voltage Conversion Circuit

The RTL8201E(L) is fabricated in a 0.11µm process. The core circuit needs to be powered by 1.2V, however, the digital IO and DAC circuits need a 3.3V power supply. Regulators are embedded in the RTL8201E(L) to convert 3.3V to 1.2V. An external 1.2V power supply is not suggested, as the internal regulators cannot be disabled, and two 1.2V power sources may conflict. As with many commercial voltage conversion devices, the 1.2V output pin (PWFBOUT) of this circuit requires the use of an output capacitor (0.1µF ceramic capacitor is recommended) as part of the device frequency compensation.

The analog and digital ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is the ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.

8.12. Far End Fault Indication

The MII Reg.1.4 (Remote Fault) is the Far End Fault Indication (FEFI) bit when 100FX mode is enabled, and indicates when a FEFI has been detected. FEFI is an alternative in-band signaling method which is composed of 84 consecutive '1's followed by one '0'. When the RTL8201E(L) detects this pattern three times, Reg.1.4 is set, which means the transmit path (the Remote side's receive path) has a problem. On the other hand, if an incoming signal fails to cause a 'Link OK', the RTL8201E(L) will start sending this pattern, which in turn causes the remote side to detect a Far End Fault. This means that the receive path has a problem from the point of view of the RTL8201E(L). The FEFI mechanism is used only in 100Base-FX mode.

9. Characteristics

9.1. DC Characteristics

9.1.1. Absolute Maximum Ratings

Table 29. Absolute Maximum Ratings

Item	Minimum	Maximum
Supply Voltage	-0.4V	3.7V
Storage Temperature	-55°C	125°C

9.1.2. Operating Conditions

Table 30. Operating Conditions

Item	Condition	Minimum	Typical	Maximum
Vcc 3.3V	3.3V Supply Voltage	2.97V	3.3V	3.63V
T_A	Ambient Operating Temperature	0°C	-	70°C

9.1.3. Power On Sequence

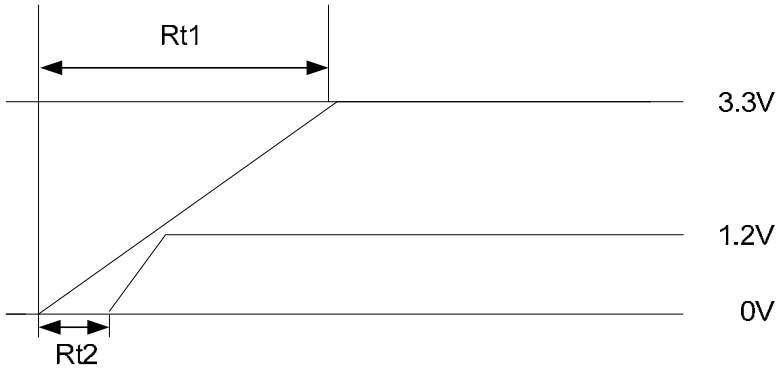


Figure 7. Power On Sequence

Table 31. Power On Sequence

Symbol	Description	Minimum	Maximum
Rt1	3.3V Rise Time	1ms	50ms
Rt2	1.2V Delay Time	300µs	1ms

The RTL8201E(L) needs 250ms power on time. After 250ms it can access the PHY register from MDC/MDIO.

9.1.4. PHY Reset Sequence

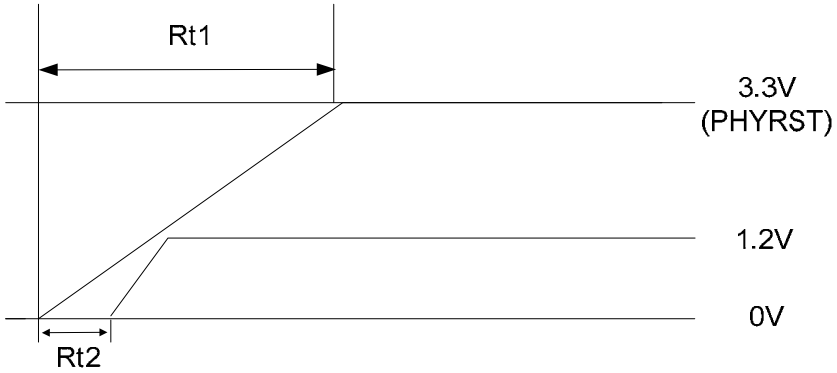


Figure 8. PHY Reset Sequence

Table 32. PHY Reset Sequence Operating Conditions

Symbol	Description	Minimum	Maximum
Rt1	3.3V Rise Time (PHYRST)	1ms	10ms
Rt2	1.2V Delay Time	300µs	1ms

9.1.5. Power Dissipation

Test Condition: The data was measured from an RTL8201EL Demo Board. The whole system power dissipation (including regulator loss) is shown in Table 33.

Table 33. Power Dissipation (mW @ Whole System)

Symbol	Condition	RTL8201E(L) Only	RTL8201E(L)-VC MII Mode	RTL8201E(L)-VC RMII Mode and TXC from MAC	RTL8201E(L)-VC RMII Mode and TXC from RTL8201E(L)-VC
P_{10IDLE}	10Base-T Idle	82.5	85.8	85.8	122.1
P_{10F}	10Base-T Full Duplex	217.8	224.4	214.5	244.2
$P_{100IDLE}$	100Base-T Idle	191.4	188.1	168.3	184.8
P_{100F}	100Base-T Full Duplex	207.9	198	188.1	221.1
P_{LDPS}	Link Down Power Saving	72.6	52.8	49.5	69.3
P_{PHYRST}	PHY Reset	3.3	3.3	3.3	3.3

9.1.6. Input Voltage: Vcc

Table 34. Input Voltage: Vcc

Symbol	Condition		Minimum	Maximum
TTL V_{IH}	Input High Voltage	-	0.5*Vcc	Vcc +0.5V
TTL V_{IL}	Input Low Voltage	-	-0.5V	0.7V
TTL V_{OH}	Output High Voltage	IOH=-8mA	0.65*Vcc	Vcc
TTL V_{OL}	Output Low Voltage	IOL=8mA	-	0.7V
TTL I_{OZ}	Tri-State Leakage	Vout=Vcc or GND	-110µA	10µA
I_{IN}	Input Current	Vin=Vcc or GND	-1µA	10µA
I_{PL}	Input Current with Internal Weakly Pulled Low Resistor	Vin=Vcc or GND	-1µA	100µA
I_{PH}	Input Current with Internal Weakly Pulled High Resistor	Vin=Vcc or GND	-110µA	10µA
PECL V_{IH}	PECL Input High Voltage	-	Vdd -1.16V	Vdd -0.88V
PECL V_{IL}	PECL Input Low Voltage	-	Vdd -1.81V	Vdd -1.47V
PECL V_{OH}	PECL Output High Voltage	-	Vdd -1.02V	-
PECL V_{OL}	PECL Output Low Voltage	-	-	Vdd -1.62V

9.2. AC Characteristics

9.2.1. MII Transmission Cycle Timing

Table 35. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
T_1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
T_2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	5	-	-	ns
t_5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	-	-	ns
		10Mbps	0	-	-	ns
t_6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t_7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns
t_8	Transmit Latency	100Mbps	60	70	140	ns
		10Mbps	-	-	2000	ns
t_9	Sampled TXEN Inactive to End of Frame	100Mbps	-	100	170	ns
		10Mbps	-	-	-	ns

Figure 9 and Figure 10 and show an example of a packet transfer from MAC to PHY on the MII interface.

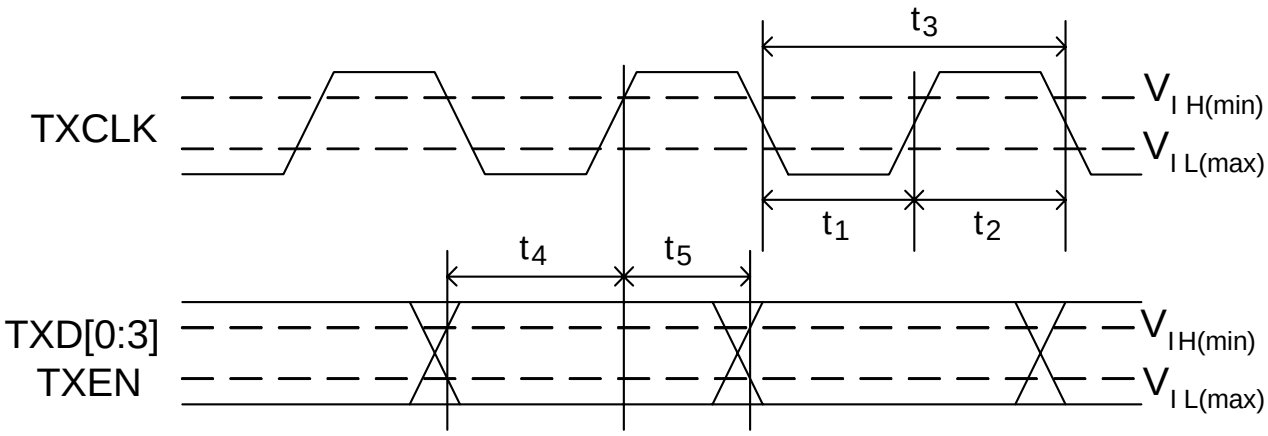


Figure 9. MII Transmission Cycle Timing-1

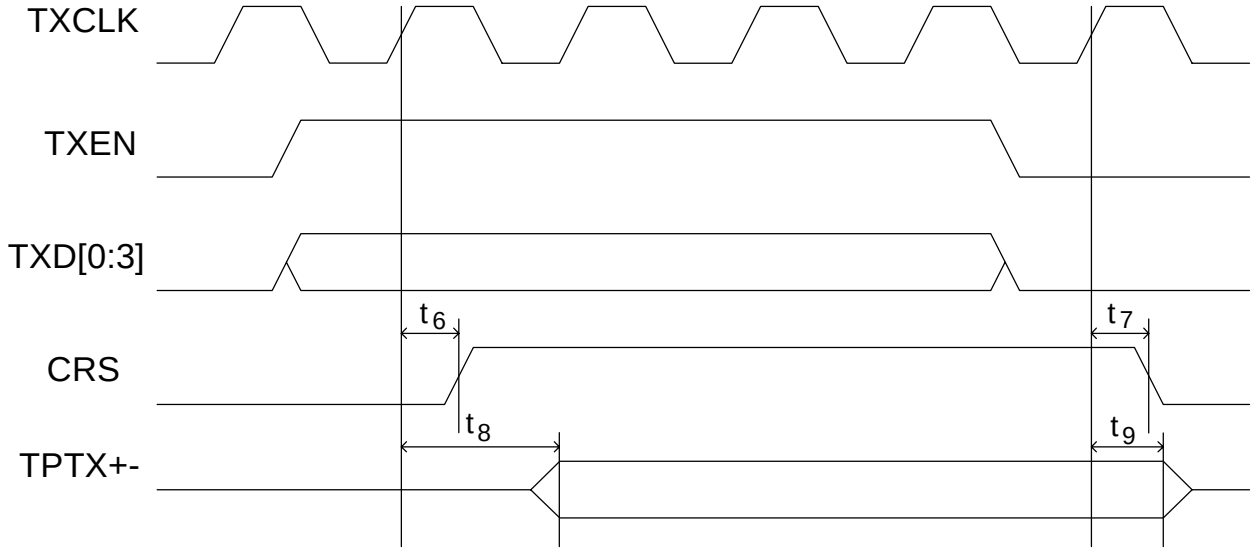


Figure 10. MII Transmission Cycle Timing-2

9.2.2. MII Reception Cycle Timing

Table 36. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t_3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	RXER, RXDV, RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t_5	RXER, RXDV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t_6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t_7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t_8	Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t_9	End of Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

Figure 11 and Figure 12 show an example of a packet transfer from PHY to MAC on the MII interface.

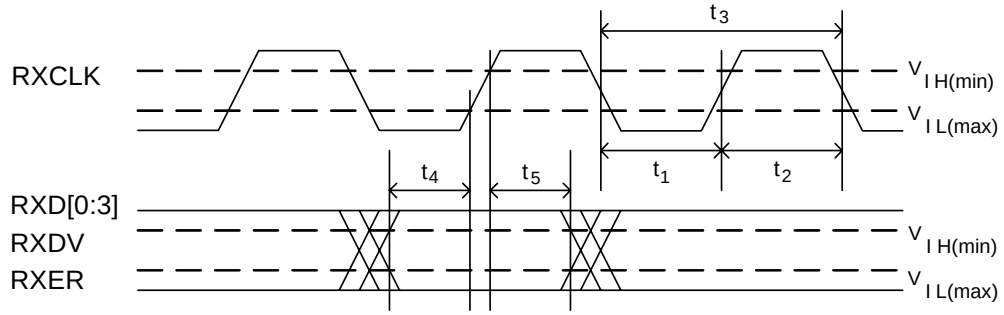


Figure 11. MII Reception Cycle Timing-1

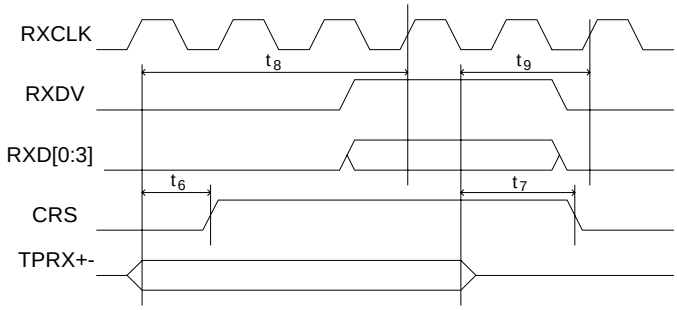


Figure 12. MII Reception Cycle Timing-2

9.2.3. RMII Transmission Cycle Timing (RTL8201E(L)-VC Only)

Table 37. RMII Transmission Cycle Timing (RTL8201E(L)-VC Only)

Symbol	Description	Minimum	Typical	Maximum	Unit
REF_CLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REF_CLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_txd_rmii	TXD/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_txd_rmii	TXD/TXEN Hold Time from REFCLK	2	-	-	ns

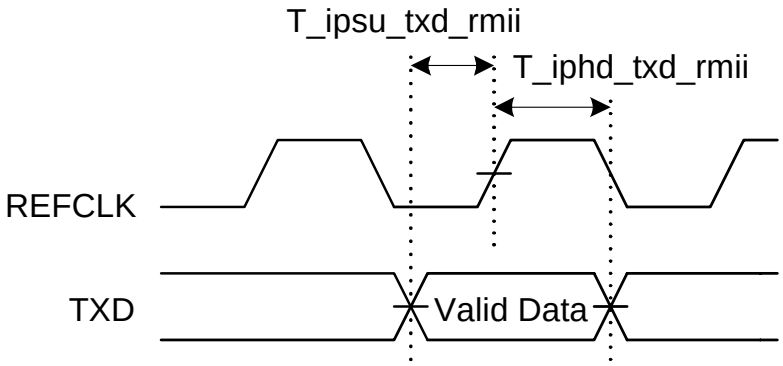


Figure 13. RMII Transmission Cycle Timing

9.2.4. RMII Reception Cycle Timing (REFCLK Input Mode; RTL8201E(L)-VC Only)

9.2.4.1 REFCLK Rising Edge Output Data

Reg25, bit13 = 1 (Default)

RXD/CRS_DV from the REFCLK delay time is as shown in Table 38.

Table 38. RMII Reception Cycle Timing (REFCLK Rising Edge) (RTL8201E(L)-VC Only)

Symbol	Description	Minimum	Typical	Maximum	Unit
T_ipd_rxd_rmii	RXD/CRS_DV Delay Time from REFCLK	6.5	-	9.1	ns
T_Cycle	REFCLK Clock Cycle Time	-	20	-	ns

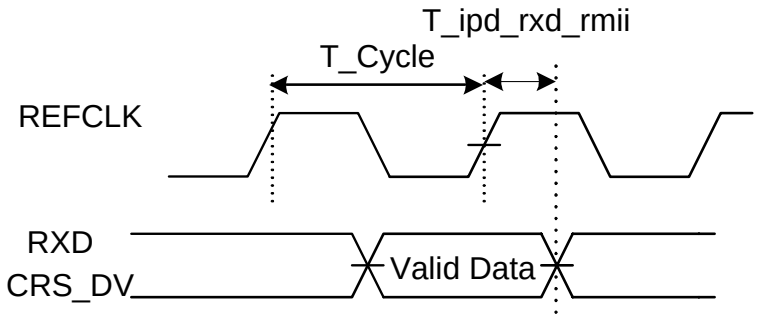


Figure 14. REFCLK Rising Edge Output Data Cycle Timing (REFCLK Input Mode)

9.2.4.2 REFCLK Falling Edge Output Data

Reg25, bit13 = 0

We recommend this mode NOT be used, as the RXD/CRS_DV from REFCLK setup time is insufficient.

RXD/CRS_DV from the REFCLK delay time is as shown in Table 39.

Table 39. RMII Reception Cycle Timing (REFCLK Falling Edge) (RTL8201E(L)-VC Only)

Symbol	Description	Minimum	Typical	Maximum	Unit
T_ipd_rxd_rmii	RXD/CRS_DV Delay Time from REFCLK	16.2	-	18.6	ns
T_Cycle	REFCLK Clock Cycle Time	-	20	-	ns

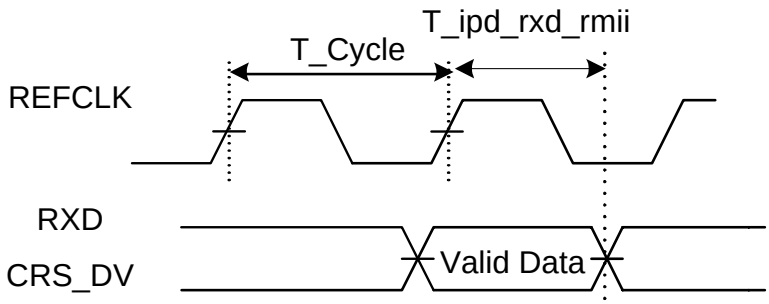


Figure 15. REFCLK Falling Edge Output Data Cycle Timing (REFCLK Input Mode)

9.2.5. RMII Reception Cycle Timing (REFCLK Output Mode; RTL8201E(L)-VC Only)

9.2.5.1 REFCLK Rising Edge Output Data

Reg25, bit13 = 1 (Default)

We recommend this mode NOT be used, as the RXD/CRS_DV from REFCLK delay time is insufficient.

RXD/CRS_DV from the REFCLK delay time is as shown in Table 40.

Table 40. RMII Reception Cycle Timing (REFCLK Rising Edge) (RTL8201E(L)-VC Only)

Symbol	Description	Minimum	Typical	Maximum	Unit
T_ipd_rxd_rmii	RXD/CRS_DV Delay Time from REFCLK	3	-	5	ns
T_Cycle	REFCLK Clock Cycle Time	-	20	-	ns

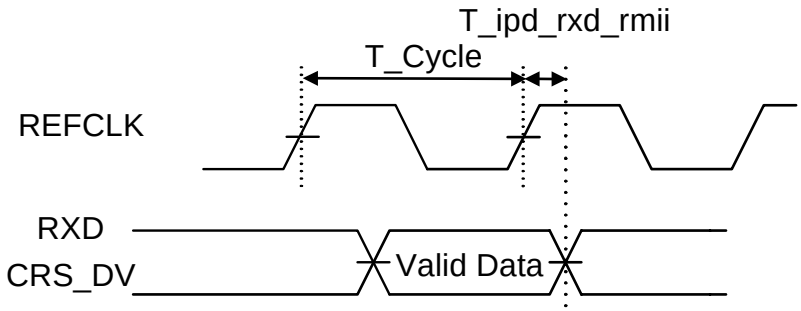


Figure 16. REFCLK Rising Edge Output Data Cycle Timing (REFCLK Output Mode)

9.2.5.2 REFCLK Falling Edge Output Data

Reg25, bit13 = 0

RXD/CRS_DV from the REFCLK delay time is as shown in Table 41.

Table 41. RMII Reception Cycle Timing (REFCLK Falling Edge) (RTL8201E(L)-VC Only)

Symbol	Description	Minimum	Typical	Maximum	Unit
T_ipd_rxd_rmii	RXD/CRS_DV Delay Time from REFCLK	12.6	-	15.6	ns
T_Cycle	REFCLK Clock Cycle Time	-	20	-	ns

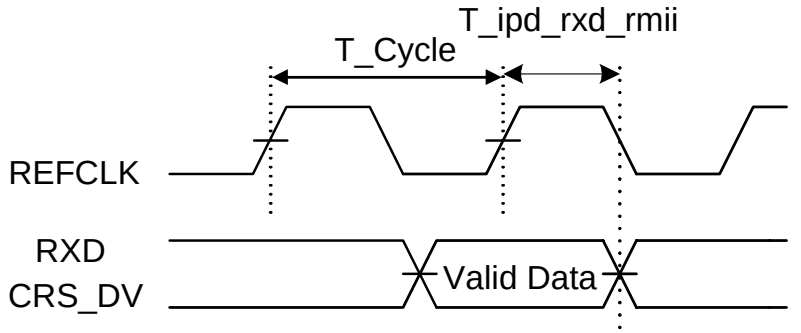


Figure 17. REFCLK Falling Edge Output Data Cycle Timing (REFCLK Output Mode)

9.2.6. SNI Transmission Cycle Timing

Table 42. SNI Transmission Cycle Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	TXCLK High Pulse Width	36	-	ns
t_2	TXCLK Low Pulse Width	36	-	ns
t_3	TXCLK Period	80	120	ns
t_4	TXEN, TXD0 Setup to TXCLK Rising Edge	20	-	ns
t_5	TXEN, TXD0 Hold after TXCLK Rising Edge	10	-	ns
t_8	Transmit Latency	-	50	ns

Figure 18 and Figure 19 show an example of a packet transfer from MAC to PHY on the SNI interface.

Note: SNI mode only runs at 10Mbps.

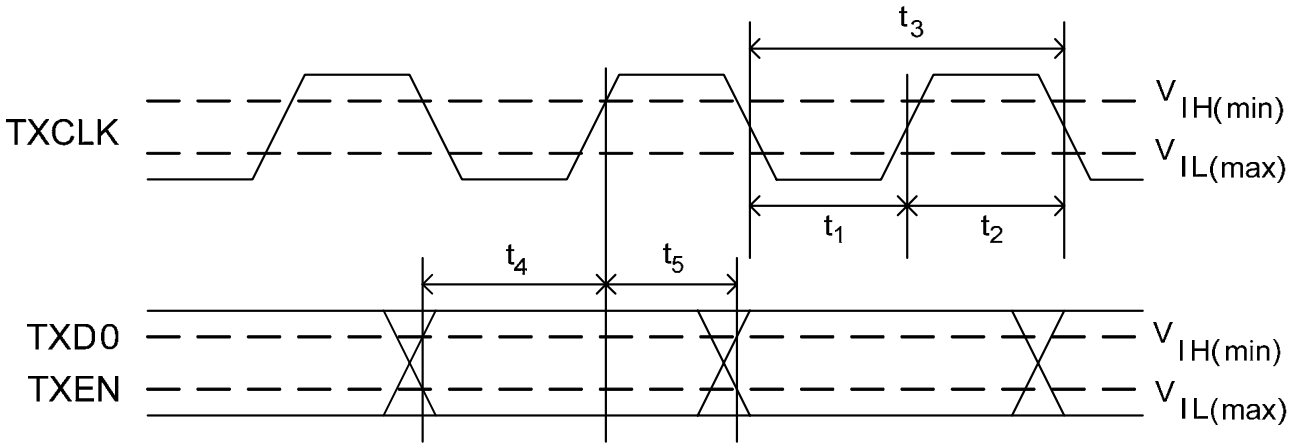


Figure 18. SNI Transmission Cycle Timing-1

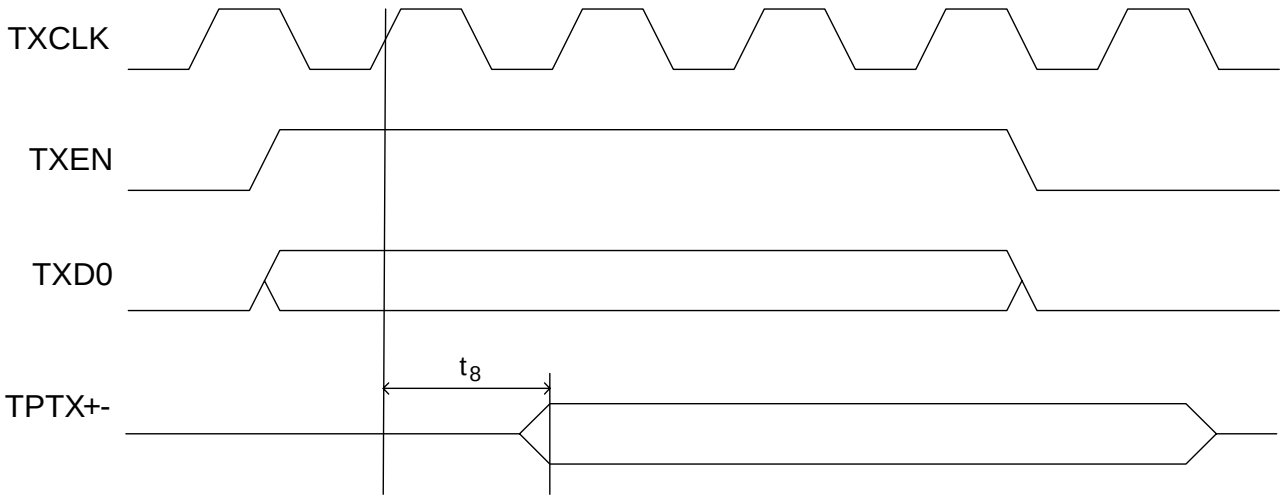


Figure 19. SNI Transmission Cycle Timing-2

9.2.7. SNI Reception Cycle Timing

Table 43. SNI Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
t_1	RXCLK High Pulse Width	36	-	-	ns
t_2	RXCLK Low Pulse Width	36	-	-	ns
t_3	RXCLK Period	80	-	120	ns
t_4	RXD0 Setup to RXCLK Rising Edge	40	-	-	ns
t_5	RXD0 Hold after RXCLK Rising Edge	40	-	-	ns
t_6	Receive Frame to CRS High	-	-	50	ns
t_7	End of Receive Frame to CRS Low	-	-	160	ns
t_8	Decoder Acquisition Time	-	600	1800	ns

Figure 20 and Figure 21 show an example of a packet transfer from PHY to MAC on the SNI interface.

Note: SNI mode only runs at 10Mbps.

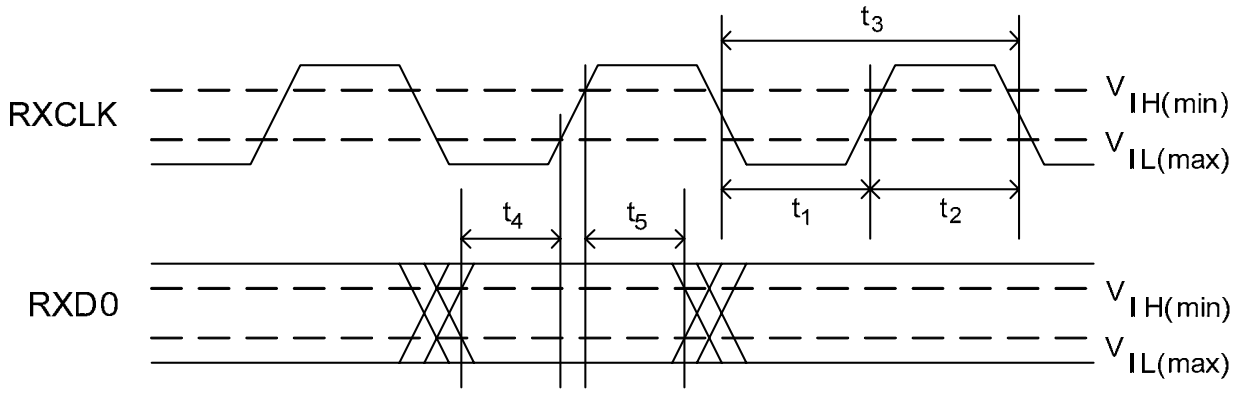


Figure 20. SNI Reception Cycle Timing-1

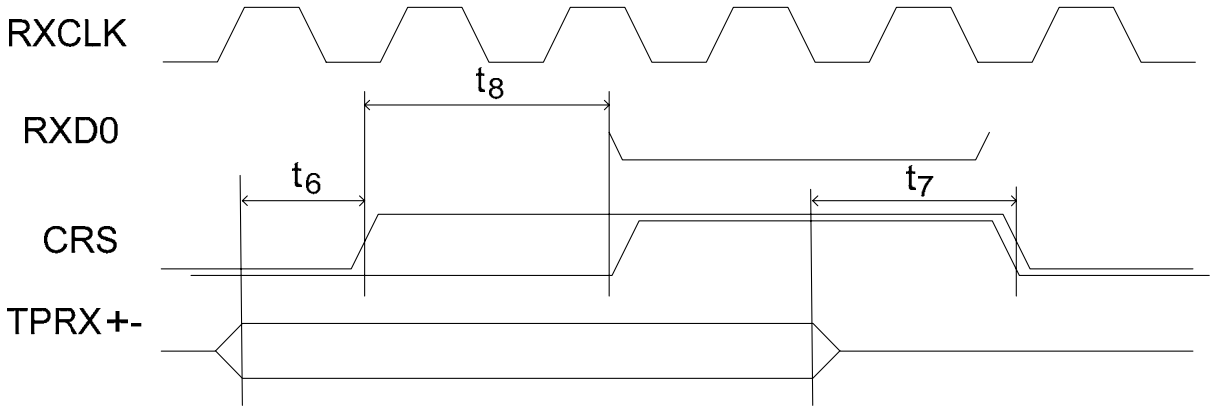


Figure 21. SNI Reception Cycle Timing-2

9.2.8. MDC/MDIO Timing

Table 44. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC High Pulse Width	160	-	ns
t_2	MDC Low Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

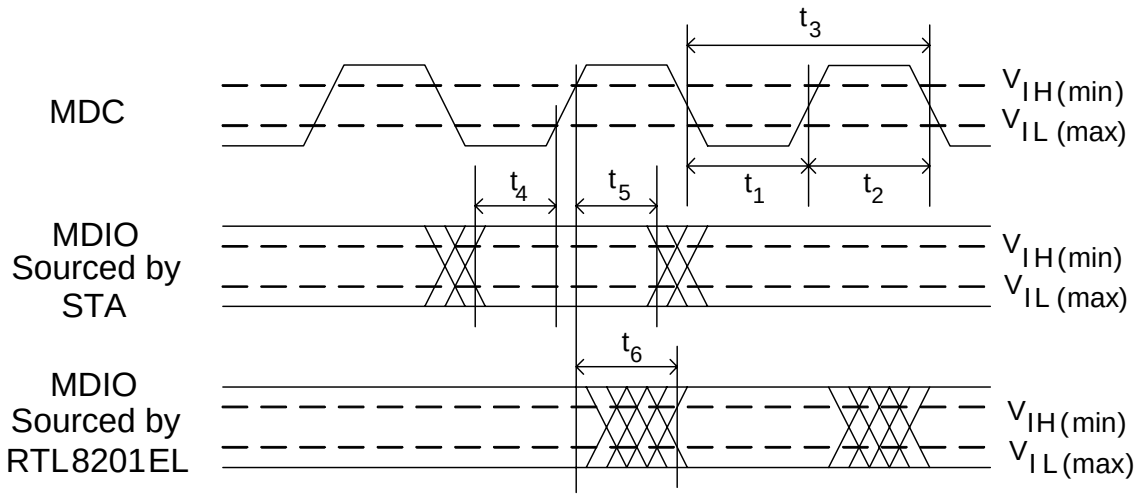


Figure 22. MDC/MDIO Timing

9.2.9. Transmission without Collision

Figure 23 shows an example of a packet transfer from MAC to PHY.

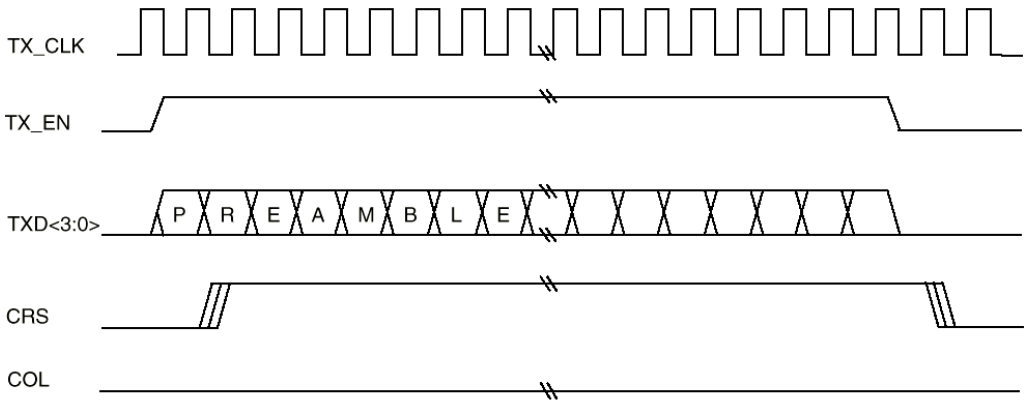


Figure 23. MAC to PHY Transmission Without Collision

9.2.10. Reception without Error

Figure 24 shows an example of a packet transfer from PHY to MAC.

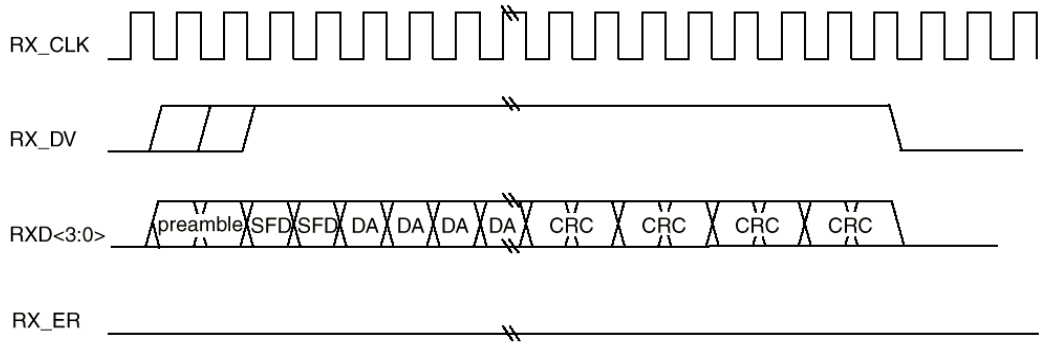


Figure 24. PHY to MAC Reception Without Error

9.3. Crystal Characteristics

Table 45. Crystal Characteristics

Parameter	Range
Nominal Frequency	25.000MHz
Oscillation Mode	Base wave
Frequency Tolerance at 25°C	±50ppm
Frequency Tolerance at -20~70°C	±30ppm
Operating Temperature Range	-10°C ~ +70°C
Equivalent Series Resistance	30ohm Max.
Drive Level	0.1mV
Load Capacitance	20pF
Shunt Capacitance	7pF Max.
Insulation Resistance	Mega ohm Min./DC 100V
Test Impedance Meter	Saunders 250A
Aging Rate Per Year	±0.0003%
Broadband Peak to Peak Jitter[1, 2]	500ps

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

9.4. Oscillator Requirements

Table 46. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	Ta = 0°C~+70°C	-30	-	30	ppm
Frequency Tolerance	Ta = 25°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak to Peak Jitter[1, 2]	-	-	-	500	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

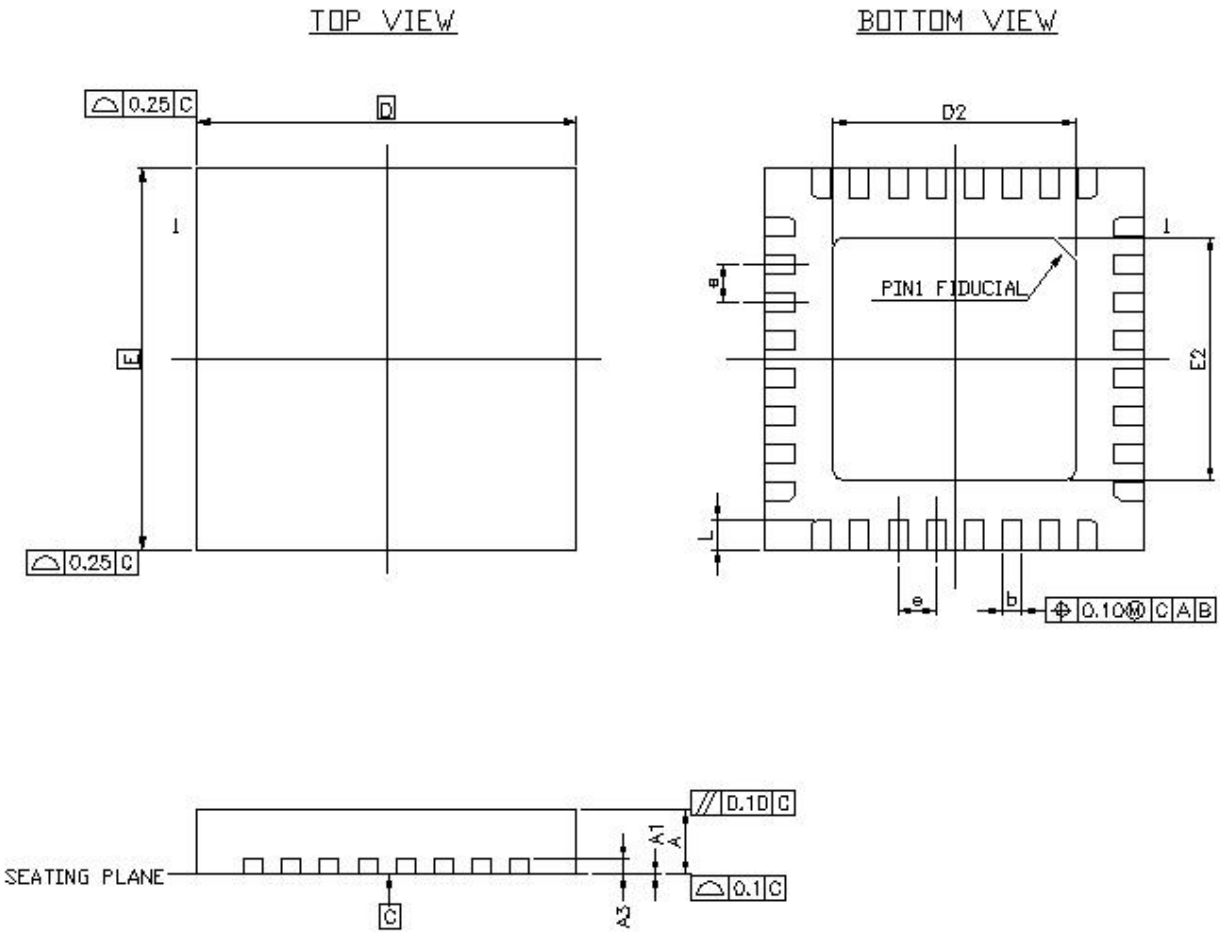
9.5. Transformer Characteristics

Table 47. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1 CT	1:1 CT
Inductance (min.)	350µH @ 8mA	350µH @ 8mA

10. Mechanical Dimensions

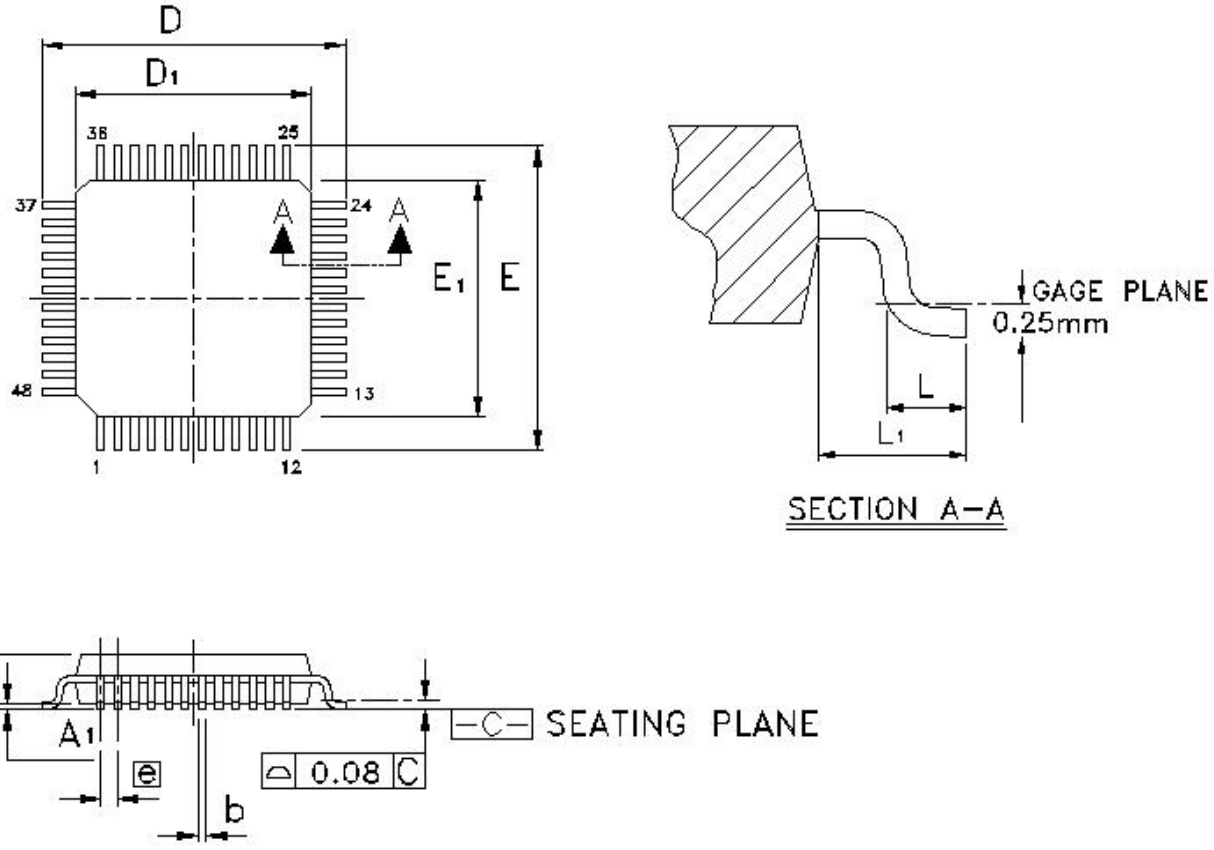
10.1. RTL8201E (32-Pin QFN)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.85	1.00	0.030	0.034	0.039
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
c	-	-	0.6	-	-	0.024
D/E		5.00 BSC			0.197 BSC	
D_2/E_2	3.10	3.35	3.60	0.122	0.132	0.142
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

10.2. RTL8201EL (48-Pin LQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	0.15	0.002	-	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D/E	9.00 BSC			0.354 BSC		
D_1/E_1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-026.

11. Ordering Information

Table 48. Ordering Information

Part Number	Package	Status
RTL8201E-GR	32-Pin QFN with 'Green' Package	Mass Production
RTL8201EL-GR	48-Pin LQFP with 'Green' Package	Mass Production
RTL8201E-VC-GR	RTL8201E-GR Version C (adds RMII and INTB support)	Mass Production
RTL8201EL-VC-GR	RTL8201EL-GR Version C (adds RMII and INTB support)	Mass Production

Note: See page 4 & 5 for package identification.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan.
Tel: 886-3-578-0211 Fax: 886-3-577-6047
www.realtek.com