TJA1028

LIN transceiver with integrated voltage regulator

Rev. 1 — 21 September 2010 Product data sheet

1. General description

The TJA1028 is a LIN 2.0/2.1/SAE J2602 transceiver with an integrated low-drop voltage regulator. The voltage regulator can deliver up to 70 mA and is available in 3.3 V and 5.0 V variants. TJA1028 facilitates the development of compact nodes in LIN bus systems. To support robust designs, the TJA1028 offers strong ElectroStatic Discharge (ESD) performance and can withstand high voltages on the LIN bus. In order to minimize current consumption, the TJA1028 supports a Sleep mode in which the LIN transceiver and the voltage regulator are powered down while still having wake-up capability via the LIN bus.

2. Features and benefits

- LIN 2.0/2.1 compliant
- SAE J2602 compliant
- Downward compatible with LIN 1.3
- Internal LIN slave termination resistor
- Voltage regulator offering 5 V or 3.3 V, 70 mA capability
- ±2 % voltage regulator accuracy over specified temperature and supply ranges
- Voltage regulator output undervoltage detection with reset output
- Voltage regulator is short-circuit proof to ground
- Robust ESD performance; ±6 kV according to IEC61000-4-2 for pins V_{BAT} and LIN
- Pins LIN and V_{BAT} protected against transients in the automotive environment (ISO 7637)
- Very low LIN bus leakage current of < 2 μA when battery not connected
- LIN pin short-circuit proof to battery and ground
- Transmit data (TXD) dominant time-out function
- Thermally protected
- Very low ElectroMagnetic Emission (EME)
- High ElectroMagnetic Immunity (EMI)
- Typical Standby mode current of 45 μA
- Typical Sleep mode current of 12 μA
- LIN bus wake-up function
- K-line compatible
- Pb-free; Restriction of Hazardous Substances (RoHS), and dark green compliant

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1028T/xxx/xx[1][2]	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

[1] TJA1028T/5V0/xx for the versions with the 5 V regulator; TJA1028T/3V3/xx for the versions with the 3.3 V regulator.

[2] TJA1028T/xxx/20 for the normal slope versions that support baud rates up to 20 kBd; TJA1028T/xxx/10 for the low slope versions that support baud rates up to 10.4 kBd (SAE J2602)

4. Block diagram

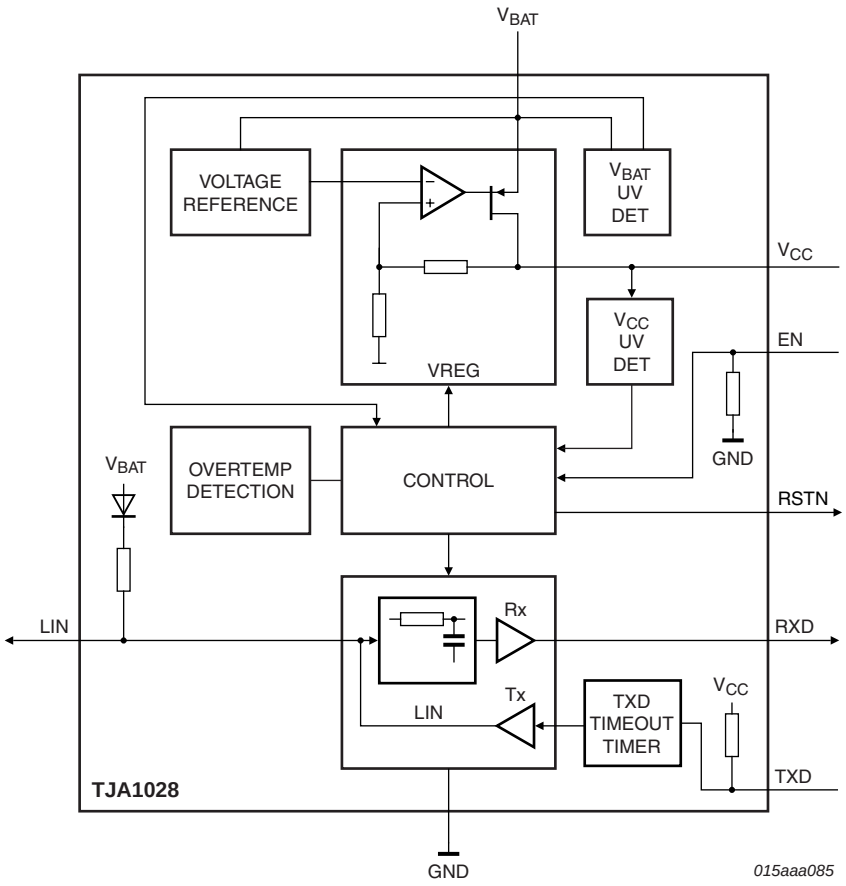


Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

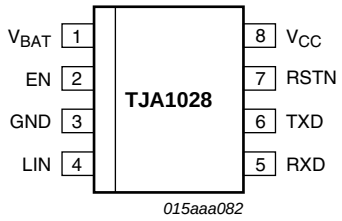


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{BAT}	1	battery supply for the TJA1028
EN	2	enable input
GND	3	ground
LIN	4	LIN bus line
RXD	5	LIN receive data output
TXD	6	LIN transmit data input
RSTN	7	reset output (active LOW)
V_{CC}	8	voltage regulator output

6. Functional description

The TJA1028 combines the functionality of a LIN transceiver and a voltage regulator in a single chip and offers wake-up by bus activity. The voltage regulator is designed to power the Electronic Control Unit's (ECU) microcontroller and its peripherals.

The TJA1028 is the interface between a LIN master/slave protocol controller and the physical bus in a Local Interconnect Network (LIN). The TJA1028 is LIN 2.0/2.1/SAE J2602 compliant and achieves optimum ElectroMagnetic Compatibility (EMC) performance by wave shaping the LIN output.

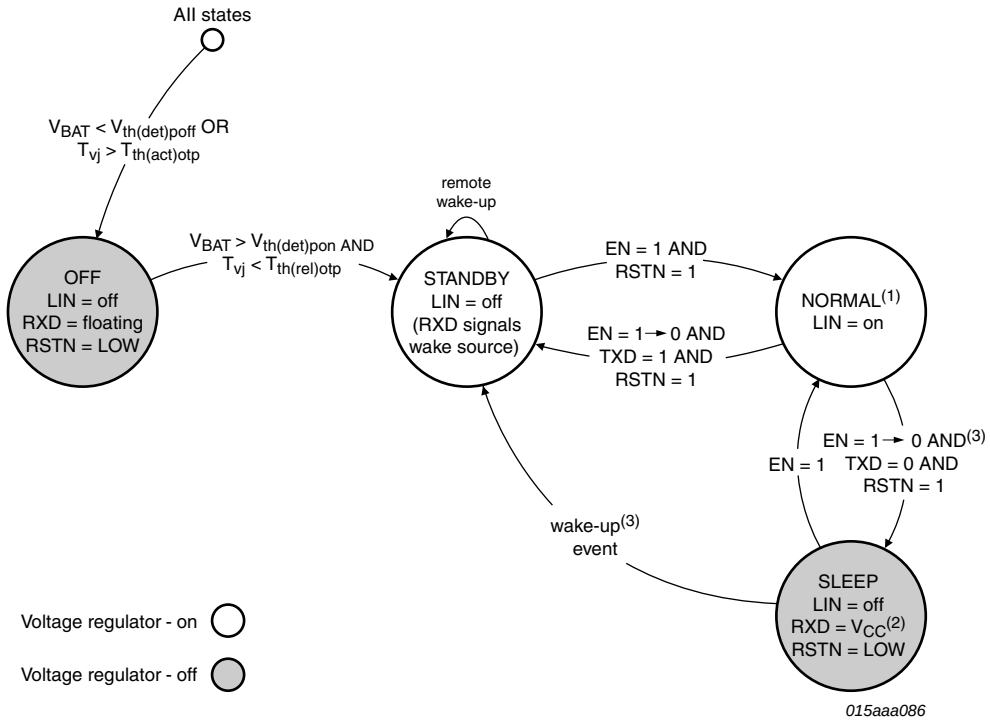
The TJA1028T/xxx/20 versions are optimized for a speed of 20 kBd, the maximum specified in the LIN standard. The TJA1028T/xxx/10 versions are optimized for a transmission speed of 10.4 kBd, as specified in SAE J2602.

6.1 Operating modes

The TJA1028 supports four operating modes: Normal, Standby, Sleep and Off. The operating modes, and the transitions between modes, are illustrated in Figure 3.

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(1) In Normal mode, the LIN transmitter is enabled - but if EN and/or RSTN go LOW, the LIN transmitter will be disabled. Remote wake-up signalling will be activated.

(2) Until V_{CC} drops below 2 V.

(3) If a wake-up event and a go-to-sleep event occur simultaneously, the device will switch directly to Standby mode without initiating a reset.

Fig 3. State diagram

6.1.1 Off mode

The TJA1028 switches to Off mode from all other modes if the battery supply voltage drops below the power-off detection threshold ($V_{th(det)poff}$) or the junction temperature exceeds the overtemperature protection shutdown temperature ($T_{th(act)otp}$).

The voltage regulator and the LIN physical layer are disabled in Off mode, and pin RSTN is forced LOW.

6.1.2 Standby mode

Standby mode is a low-power mode that guarantees very low current consumption.

The TJA1028 switches from Off mode to Standby mode as soon as the battery supply voltage rises above the power-on detection threshold ($V_{BAT} > V_{th(det)pon}$), provided the junction temperature is below the overtemperature protection release threshold ($T_{vj} < T_{th(rel)otp}$).

The TJA1028 switches to Standby mode from Normal mode during the mode select window if TXD is HIGH and EN is LOW (see Section 6.1.5), provided RSTN = 1.

A remote wake-up event will trigger a transition to Standby mode from Sleep mode. The remote wake-up event will be signalled by a continuous LOW level on pin RXD.

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In Standby mode, the voltage regulator is on, the LIN physical layer is disabled and remote wake-up detection is active. The wake-up source is indicated by the level on RXD (LOW indicates a remote wake-up).

6.1.3 Normal mode

If the EN pin is pulled HIGH while the TJA1028 is in Standby mode (with RSTN = 1) or Sleep mode, the device will enter Normal mode. The LIN physical layer and the voltage regulator are enabled in Normal mode.

6.1.3.1 The LIN transceiver in Normal mode

The LIN transceiver is activated when the TJA1028 enters Normal mode.

In Normal mode, the transceiver can transmit and receive data via the LIN bus. The receiver detects data streams on the LIN pin and transfers them to the microcontroller via pin RXD. LIN recessive is represented by a HIGH level on RXD, LIN dominant by a LOW level.

The transmit data streams of the protocol controller at the TXD input are converted by the transmitter into bus signals with optimized slew rate and wave shaping to minimize EME. A LOW level at the TXD input is converted to a LIN dominant level while a HIGH level is converted to a LIN recessive level.

6.1.4 Sleep mode

Sleep mode features extremely low power consumption.

The TJA1028 switches to Sleep mode from Normal mode during the mode select window if TXD and EN are both LOW (see Section 6.1.5), provided RSTN = 1.

The voltage regulator and the LIN physical layer are disabled in Sleep mode. Pin RSTN is forced LOW. Remote wake-up detection is active.

6.1.5 Transition from Normal to Sleep or Standby mode

When EN is driven LOW in Normal mode, the TJA1028 disables the transmit path. The mode select window opens $t_{msel(min)}$ after EN goes LOW, and remains open until $t_{msel(max)}$ after EN goes LOW (see Figure 4).

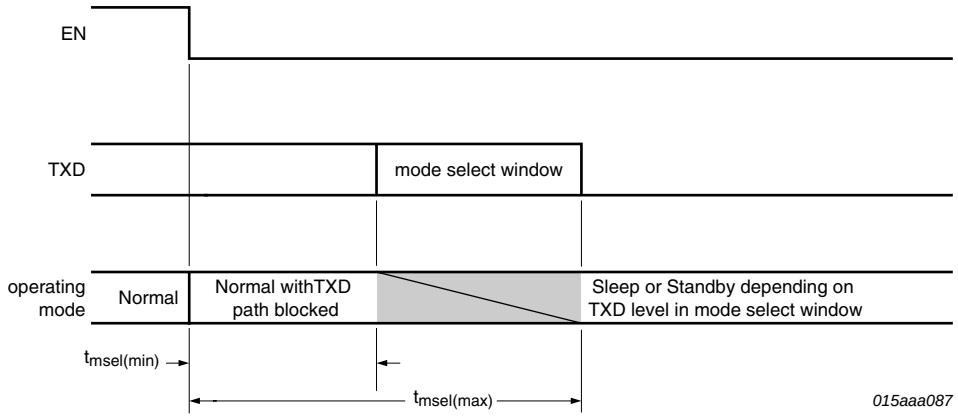
The TXD pin is sampled in the mode select window. A transition to Standby mode is triggered if TXD is HIGH, or to Sleep mode if TXD is LOW.

To avoid complicated timing in the application, EN and TXD can be pulled LOW at the same time without having any effect on the LIN bus. In order to ensure that the remote wake-up time ($t_{wake(busdom)min}$) is not reset on a transition to Sleep mode, TXD should be pulled LOW at least $t_{d(EN-TXD)}$ after EN goes LOW. This is guaranteed by design.

The user must ensure the appropriate level is present on pin TXD while the mode select window is open.

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TXD is sampled during the mode select window. The TJA1028 switches to Standby (TXD HIGH) or Sleep (TXD LOW) mode after sampling.

Fig 4. Transition from Normal to Sleep/Standby mode

6.2 Power supplies

6.2.1 Battery (pin V_{BAT})

The TJA1028 contains a single supply pin, V_{BAT}. An external diode is needed in series to protect the device against negative voltages. The operating range is from 4.5 V to 28 V. The TJA1028 can handle voltages up to 40 V (max). If the voltage at pin V_{BAT} falls below the power-off detection threshold, $V_{th(det)poff}$, the TJA1028 switches to Off mode, shutting down the internal logic and the voltage regulator and disabling the LIN transmitter. The TJA1028 exits Off mode as soon as the voltage rises above the power-on detection threshold, $V_{th(det)pon}$, provided the junction temperature is below the overtemperature protection release threshold ($T_{th(rel)otp}$).

6.2.2 Voltage regulator (pin V_{CC})

The TJA1028 contains a voltage regulator supplied via pin V_{BAT}, which delivers up to 70 mA. It is designed to supply the microcontroller and its periphery via pin V_{CC}.

The output voltage on pin V_{CC} is monitored continuously and a system reset signal is generated (pin RSTN goes LOW) if an undervoltage event is detected ($V_{CC} < V_{uvd}$).

6.3 LIN transceiver

The transceiver is the interface between a LIN master/slave protocol controller and the physical bus in a Local Interconnect Network (LIN). It is primarily intended for in-vehicle sub-networks using baud rates from 2.4 kBd up to 20 kBd and is LIN 2.0/LIN 2.1/SAE J2602 compliant.

6.4 Remote wake-up

A remote wake-up is triggered by a falling edge on pin LIN, followed by LIN remaining LOW for at least $t_{wake(busdom)min}$, followed by a rising edge on pin LIN (see Figure 5).

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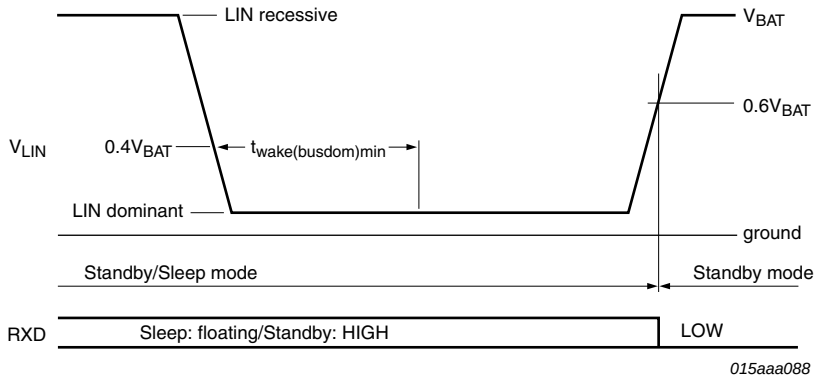


Fig 5. Remote wake-up behavior

The remote wake-up request is communicated to the microcontroller in Standby mode by a continuous LOW level on pin RXD.

Note that $t_{wake(busdom)min}$ is measured in Sleep and Standby modes, and in Normal mode if TXD is HIGH.

6.5 Fail-safe features

6.5.1 General fail-safe features

The following general fail-safe features have been implemented:

- An internal pull-up towards V_{CC} on pin TXD guarantees a recessive bus level if the pin is left floating by a bad soldering joint or floating microcontroller port pin.
- The current in the transmitter output stage is limited in order to protect the transmitter against short circuits to pin V_{BAT}.
- A loss of power (pins V_{BAT} and GND) has no impact on the bus line or on the microcontroller. There will be no reverse currents from the bus.
- The LIN transmitter is automatically disabled when either EN or RSTN is LOW.
- After a transition to Normal mode, the LIN transmitter is only enabled if a recessive level is present on pin TXD.

6.5.2 TXD dominant time-out function

A TXD dominant time-out timer circuit prevents the bus line being driven to a permanent dominant state (blocking all network communications) if TXD is forced permanently LOW by a hardware or software application failure. The timer is triggered by a negative edge on the TXD pin. If the pin remains LOW for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, driving the bus line to a recessive state. The timer is reset by a positive edge on the TXD pin.

6.5.3 Temperature protection

The temperature of the IC is monitored in Normal, Standby and Off modes. If the temperature is too high ($T_{vj} > T_{th(act)otp}$), the TJA1028 will switch to Off mode (if in Standby or Normal mode). The voltage regulator and the LIN transmitter will be switched off and the RSTN pin driven LOW.

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When the temperature falls below the overtemperature protection release threshold ($T_{vj} < T_{th(rel)otp}$), the TJA1028 switches to Standby mode.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	battery supply voltage	DC; continuous		–0.3	+40	V
V_x	voltage on pin x	DC value				
		pin V_{CC}		–0.3	+7	V
		pins TXD, RXD, RSTN and EN		–0.3	V_{CC} + 0.3	V
		pin LIN; with respect to GND and V_{BAT}		–40	+40	V
V_{ESD}	electrostatic discharge voltage	HBM	[1]			
		at pins V_{BAT} and LIN	[2]	–8	+8	kV
		at any other pin		–2	+2	kV
		IEC 61000-4-2	[3]			
		at pins LIN and V_{BAT}		–8	+8	kV
		MM	[4]			
		at any pin		–250	+250	V
		CDM	[5]			
		at corner pins		–750	+750	V
		at any other pin		–500	+500	V
V_{trt}	transient voltage	on pin V_{BAT}; via reverse polarity diode/capacitor	[6]	–150	+100	V
		on pin LIN; via 1 nF coupling capacitor				

[1] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[2] V_{CC} and V_{BAT} connected to GND, emulating application circuit.

[3] ESD performance of pins LIN and V_{BAT} according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house.

[4] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 µH, 10 Ω).

[5] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

[6] Verified by an external test house to ensure pins can withstand ISO 7637 part 2 automotive transient test pulses 1, 2a, 3a and 3b.

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8; single-layer board	[1]	132	K/W
		SO8; four-layer board	[2]	93	K/W

[1] According to JEDEC JESD51-2 and JESD51-3 at natural convection on 1s board.

[2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board; board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer.

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9. Static characteristics

Table 5. Static characteristics

V_{BAT} = 5.5 V to 28 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply; pin V_{BAT}							
I_{BAT}	battery supply current	Standby mode; $V_{LIN} = V_{BAT}$		-	45	59	µA
		Sleep mode; $V_{LIN} = V_{BAT}$		-	12	18	µA
		Normal mode; bus recessive $V_{LIN} = V_{BAT}$; $V_{RXD} = V_{CC}$; V_{RSTN} = HIGH		-	850	1800	µA
		Normal mode; bus dominant V_{BAT} = 12 V; V_{TXD} = 0 V; V_{RSTN} = HIGH		-	2.0	4.5	mA
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} = 2 V to 28 V		-	-	5.25	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} = 2 V to 28 V		3	-	4.5	V
$V_{hys(det)pon}$	power-on detection hysteresis voltage	V_{BAT} = 2 V to 28 V		50	-	-	mV
Supply; pin V_{CC}							
V_{CC}	supply voltage	$V_{CC(nom)}$ = 5 V; I_{CC} = −70 mA to 0 mA		4.9	5	5.1	V
		$V_{CC(nom)}$ = 3.3 V; V_{BAT} = 4.5 V to 28 V I_{CC} = −70 mA to 0 mA		3.234	3.3	3.366	V
I_{Olim}	output current limit	V_{CC} = 0 V to 5.5 V		−250	-	−70	mA
V_{uvd}	undervoltage detection voltage	$V_{CC(nom)}$ = 5 V		4.5	-	4.75	V
		$V_{CC(nom)}$ = 3.3 V		2.97	-	3.135	V
V_{uvr}	undervoltage recovery voltage	$V_{CC(nom)}$ = 5 V		4.6	-	4.9	V
		$V_{CC(nom)}$ = 3.3 V		3.036	-	3.234	V
$R_{(VBAT-VCC)}$	resistance between pin V_{BAT} and pin V_{CC}	$V_{CC(nom)}$ = 5 V; V_{BAT} = 4.5 V to 5.5 V I_{V1} = −70 mA to −5 mA regulator in saturation	[1]	-	-	5	Ω
C_o	output capacitance	ESR < 5 Ω	[1]	1.8	10	-	µF
LIN transmit data input; pin TXD							
$V_{th(sw)}$	switching threshold voltage	V_{CC} = 2.97 V to 5.5 V		0.3 × V_{CC}	-	0.7 × V_{CC}	V
$V_{hys(i)}$	input hysteresis voltage	V_{CC} = 2.97 V to 5.5 V		200	-	-	mV
R_{pu}	pull-up resistance			5	12	25	kΩ
LIN receive data output; pin RXD							
I_{OH}	HIGH-level output current	Normal mode $V_{LIN} = V_{BAT}$; $V_{RXD} = V_{CC}$ − 0.4 V		-	-	−0.4	mA
I_{OL}	LOW-level output current	Normal mode V_{LIN} = GND; V_{RXD} = 0.4 V		0.4	-	-	mA
Enable input; pin EN							
$V_{th(sw)}$	switching threshold voltage			0.8	-	2	V
R_{pd}	pull-down resistance			50	130	400	kΩ

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Table 5. Static characteristics *...continued*

V_{BAT} = 5.5 V to 28 V; T_{vj} = –40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset output; pin RSTN							
R_{pu}	pull-up resistance	$V_{RSTN} = V_{CC} - 0.4$ V V_{CC} = 2.97 V to 5.5 V		3	-	12	kΩ
I_{OL}	LOW-level output current	V_{RSTN} = 0.4 V; V_{CC} = 2.97 V to 5.5 V –40 °C < T_{vj} < 195 °C		3.2	-	40	mA
V_{OL}	LOW-level output voltage	V_{CC} = 2.5 V to 5.5 V –40 °C < T_{vj} < 195 °C		0	-	0.5	V
V_{OH}	HIGH-level output voltage	–40 °C < T_{vj} < 195 °C		0.8 × V_{CC}	-	V_{CC} + 0.3	V
LIN bus line; pin LIN							
I_{BUS_LIM}	current limitation for driver dominant state	$V_{BAT} = V_{LIN}$ = 18 V; V_{TXD} = 0 V		40	-	100	mA
$I_{BUS_PAS_rec}$	receiver recessive input leakage current	V_{LIN} = 18 V; V_{BAT} = 5.5 V; $V_{TXD} = V_{CC}$		-	-	2	µA
$I_{BUS_PAS_dom}$	receiver dominant input leakage current including pull-up resistor	Normal mode $V_{TXD} = V_{CC}$; V_{LIN} = 0 V; V_{BAT} = 12 V		–600	-	-	µA
$I_{L(log)}$	loss of ground leakage current	V_{BAT} = 18 V; V_{LIN} = 0 V		–750	-	+10	µA
$I_{L(lob)}$	loss of battery leakage current	V_{BAT} = 0 V; V_{LIN} = 18 V		-	-	2	µA
$V_{rec(RX)}$	receiver recessive voltage	V_{BAT} = 5.5 V to 18 V		0.6 × V_{BAT}	-	-	V
$V_{dom(RX)}$	receiver dominant voltage	V_{BAT} = 5.5 V to 18 V		-	-	0.4 × V_{BAT}	V
$V_{th(cntr)RX}$	receiver center threshold voltage	V_{BAT} = 5.5 V to 18 V $V_{th(cntr)RX} = (V_{th(rec)RX} + V_{th(dom)RX})/2$	[2]	0.475 × V_{BAT}	0.5 × V_{BAT}	0.525 × V_{BAT}	V
$V_{th(hys)RX}$	receiver hysteresis threshold voltage	V_{BAT} = 5.5 V to 18 V $V_{th(hys)RX} = V_{th(rec)RX} - V_{th(dom)RX}$	[2]	0.05 × V_{BAT}	0.15 × V_{BAT}	0.175 × V_{BAT}	V
C_{LIN}	capacitance on pin LIN		[1]	-	-	30	pF
$V_{O(dom)}$	dominant output voltage	Normal mode V_{TXD} = 0 V; V_{BAT} = 7 V		-	-	1.4	V
		Normal mode V_{TXD} = 0 V; V_{BAT} = 18 V		-	-	2.0	V
R_{slave}	slave resistance	between pin LIN and V_{BAT} V_{LIN} = 0 V; V_{BAT} = 12 V		20	30	60	kΩ
Temperature protection							
$T_{th(act)otp}$	overtemperature protection activation threshold temperature			165	180	195	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature			126	138	150	°C

[1] Guaranteed by design; not tested.

[2] See Figure 7.

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10. Dynamic characteristics

Table 6. Dynamic characteristics

V_{BAT} = 5.5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Duty cycles							
δ1	duty cycle 1	$V_{th(rec)RX(max)}$ = 0.744V_{BAT} $V_{th(dom)RX(max)}$ = 0.581V_{BAT} t_{bit} = 50 µs V_{BAT} = 7 V to 18 V	[2][3] [4][5]	0.396	-	-	
		$V_{th(rec)RX(max)}$ = 0.76V_{BAT} $V_{th(dom)RX(max)}$ = 0.593V_{BAT} t_{bit} = 50 µs V_{BAT} = 5.5 V to 7.0 V	[2][3] [4][5]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)RX(min)}$ = 0.422V_{BAT} $V_{th(domRX)(min)}$ = 0.284V_{BAT} t_{bit} = 50 µs V_{BAT} = 7.6 V to 18 V	[2][4] [5][6]	-	-	0.581	
		$V_{th(rec)RX(min)}$ = 0.41V_{BAT} $V_{th(dom)RX(min)}$ = 0.275V_{BAT} t_{bit} = 50 µs V_{BAT} = 6.1 V to 7.6 V	[2][4] [5][6]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)RX(max)}$ = 0.778V_{BAT} $V_{th(dom)RX(max)}$ = 0.616V_{BAT} t_{bit} = 96 µs V_{BAT} = 7 V to 18 V	[3][4] [5]	0.417	-	-	
		$V_{th(rec)RX(max)}$ = 0.797V_{BAT} $V_{th(dom)RX(max)}$ = 0.630V_{BAT} t_{bit} = 96 µs V_{BAT} = 5.5 V to 7 V	[3][4] [5]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)RX(min)}$ = 0.389V_{BAT} $V_{th(dom)RX(min)}$ = 0.251V_{BAT} t_{bit} = 96 µs V_{BAT} = 7.6 V to 18 V	[4][5] [6]	-	-	0.590	
		$V_{th(rec)RX(min)}$ = 0.378V_{BAT} $V_{th(dom)RX(min)}$ = 0.242V_{BAT} t_{bit} = 96 µs V_{BAT} = 6.1 V to 7.6 V	[4][5] [6]	-	-	0.590	
Timing characteristics							
$t_{PD(RX)r}$	rising receiver propagation delay	C_{RXD} = 20 pF		-	-	6	µs
$t_{PD(RX)f}$	falling receiver propagation delay	C_{RXD} = 20 pF		-	-	6	µs
$t_{PD(RX)sym}$	receiver propagation delay symmetry	C_{RXD} = 20 pF		−2	-	+2	µs
$t_{wake(busdom)min}$	minimum bus dominant wake-up time	Sleep mode		30	80	150	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V		6	-	20	ms
t_{msel}	mode select time			3	-	20	µs
$t_{d(EN-TXD)}$	delay time from EN to TXD		[7]	0	-	1	µs
Reset output; pin RSTN							
t_{rst}	reset time			2	-	8	ms

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[1] All parameters are guaranteed by design over the virtual junction temperature range. Products are 100 % tested at 125 °C ambient temperature at wafer level (pre-testing). Cased products are 100 % tested at 25 °C ambient temperature (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Not applicable to the low slope versions (TJA1028T/xxx/10) of the TJA1028.

[3] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 7.

[4] Bus load conditions are: C_L = 1 nF and R_L = 1 kΩ; C_L = 6.8 nF and R_L = 660 Ω; C_L = 10 nF and R_L = 500 Ω.

[5] For V_{BAT} > 18 V, the LIN transmitter might be suppressed. If TXD is HIGH then the LIN transmitter output is recessive.

[6] $\delta 2, \delta 4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 7.

[7] Guaranteed by design; not tested.

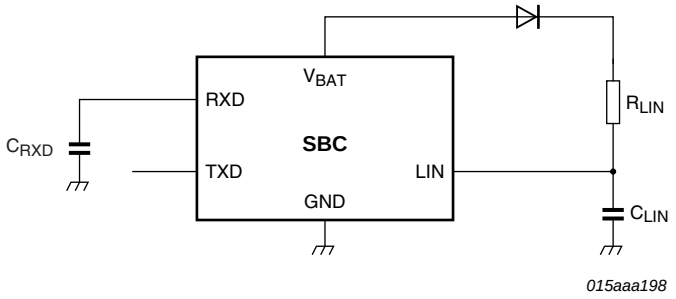


Fig 6. Timing test circuit for LIN transceiver

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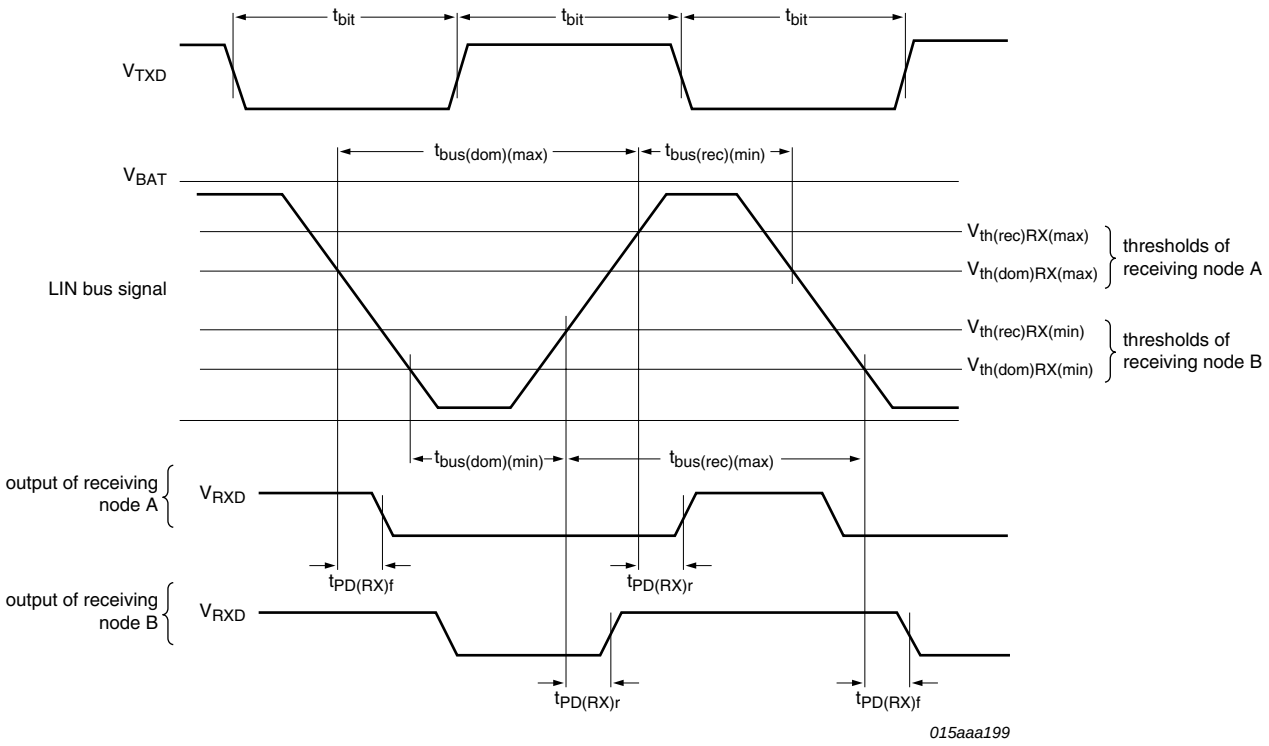


Fig 7. LIN transceiver timing diagram

11. Test information

11.1 Quality information

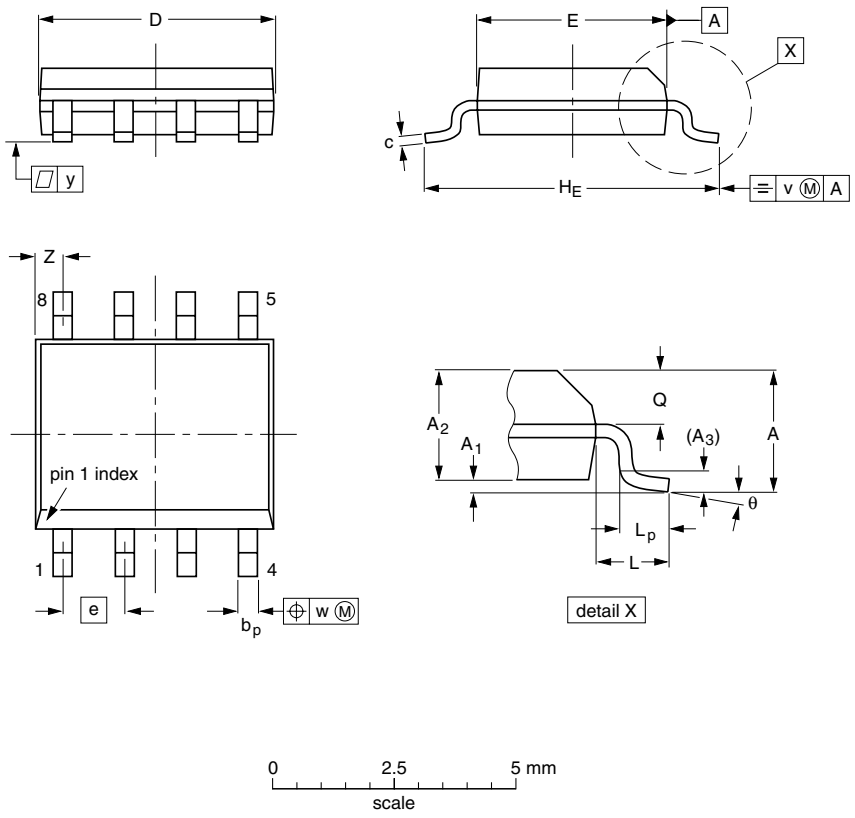
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 8. Package outline SOT96-1 (SO8)

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13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1028 v.1	20100921	Product data sheet	-	-

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14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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