NXP Semiconductors
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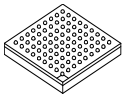
MIMX8ML8CVNKZAB **MIMX8ML6CVNKZAB**
MIMX8ML4CVNKZAB **MIMX8ML3CVNKZAB**

i.MX 8M Plus Applications Processor Datasheet for Industrial Products



Package Information
Bare die Package
FCBGA 15 x 15 mm, 0.5 mm pitch

Ordering Information
See Table 3 on page 7

1 i.MX 8M Plus introduction

The i.MX 8M Plus family focuses on neural processing unit (NPU) and vision system, advance multimedia, and industrial automation with high reliability.

The i.MX 8M Plus is a powerful quad Arm® Cortex®-A53 processor with speed up to 1.6 GHz integrated with a NPU of 2.3 TOPS that greatly accelerate machine learning inference. The vision engine is composed of two camera inputs and a HDR-capable Image Signal Processor (ISP) capable of 375 MPixels/s.
The advanced multimedia capabilities include 1080p60 video encode and decode H.265 and H.264. A 3D and 2D graphic acceleration supporting 1 GPixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces for Immersive Audio and Voice systems.
For industrial applications, real time control is enabled by an integrated 800 MHz Arm® Cortex®-M7. Robust control networks are possible via CAN-FD interfaces. And a dual Gb Ethernet, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency. High industrial system reliability for safety is leveraged by DRAM Inline ECC as well as ECC support on internal software-accessible SRAMs.

The i.MX 8M Plus is very versatile presenting multiple displays and high-speed interfaces as well as multiple memory interfaces.
It is built to meet the needs for Smart Home, Building, City and Industry 4.0 applications.

Table 1. Features (Sheet 1 of 4)

Subsystem	Features
Cortex®-A53 MPCore platform	Quad Cortex®-A53 processors operation up to 1.6 GHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Media Processing Engine (MPE) with Arm® NEON™ technology supporting the Advanced Single Instruction Multiple Data architecture • Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
	Support of 64-bit Arm® v8-A architecture
	512 KB unified L2 cache
Cortex®-M7 core platform	• Microcontroller available for customer application • Real-time processing • Cortex®-A53 complex off loading • Low power operation
	Cortex®-M7 CPU operating up to 800 MHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • 256 KB tightly coupled memory (TCM)
Image Sensor Processor (ISP)	375 Mpixel/s HDR ISP supporting configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80
External memory interface	32-bit DRAM interfaces: • LPDDR4-4000 • DDR4-3200 • Inline ECC on the DDR bus
	8-bit NAND-Flash, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
	eMMC 5.1 Flash (2 interfaces: uSDHC1 and uSDHC3)
	SPI NOR Flash (3 interfaces)
	FlexSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices. It also supports both Serial NOR and Serial NAND flash using the FlexSPI.
On-chip memory	Boot ROM (256 KB)
	On-chip RAM (868 KB): • OCRAM_A: 256 KB inside AUDIOMIX • OCRAM: 576 KB inside SUPERMIX • OCRAM_S: 36 KB inside SUPERMIX

Table 1. Features (continued) (Sheet 2 of 4)

Subsystem	Features
Graphic Processing Unit	• GC7000UL with OpenCL and Vulkan support • 2 shaders • 166 million triangles/sec • 1.0 giga pixel/sec • 16 GFLOPs 32-bit • Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan • Core clock frequency of 1000 MHz • Shader clock frequency of 1000 MHz • GC520L for 2D acceleration • Render target compatibility between 3D and 2D GPU (super tile status buffer)
Video Processing Unit	Video Decode • 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) • 1080p60 VP9 Profile 0, 2 • 1080p60 VP8 • 1080p60 AVC/H.264 Baseline, Main, High decoder Video Encode • 1080p60 AVC/H.264 encoder • 1080p60 HEVC/H.265 encoder
Neutral Processing Unit (NPU)	2.3 TOP/s Neural Network performance • Keyword detect, noise reduction, beamforming • Speech recognition (i.e. Deep Speech 2) • Image recognition (i.e. ResNet-50)
HDMI 2.0a Tx	HDMI 2.0a Tx supporting one display • Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30 • Pixel clock up to 297 MHz Audio support • 32-channel audio output support • 1 SPDIF audio eARC input support
LCDIF Display Controller	Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously. • One LCDIF drives MIPI DSI, up to UWHD and WUXGA • One LCDIF drives LVDS Tx, up to 1920x1080p60 • One LCDIF drives HDMI Tx, up to 4kp30
MIPI Interface	4-lane MIPI DSI interface Two instances of 4-lane MIPI CSI interface and HDR ISP • 2x ISP supporting 375 Mpixel/s aggregate performance and up to 3-exposure HDR processing. •When one camera is used, support up to 12MP@30fps or 4kp45 •When two cameras are used, each supports up to 1080p80 • Maximum resolution limited to resolutions achievable with a 250 MHz pixel clock and active pixel rate of 200 Mpixel/s with 24-bit RGB. This includes resolutions such as: •1080 p60 •WUXGA (1920X1200) at 60 Hz •1920x1440 at 60 Hz •UWHD (2560X1080) at 60 Hz •MIPI DSI: WQHD (2560x1440) can be supported by reduced blanking mode

Table 1. Features (continued) (Sheet 3 of 4)

Subsystem	Features
Audio	• Cadence® Tensilica® HiFi 4 DSP, operating up to 800 MHz • SPDIF input and output, including a raw capture input mode • Six external synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1RX lane. • All ports support 49.152 MHz BCLK. • ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate, and 1/16 to 8x sample rate conversion ratio. • eARC/ARC • 8-channel PDM mic input
GPIO and pin multiplexing	General-purpose input/output (GPIO) modules with interrupt capability
	Input/output multiplexing controller (IOMUXC) to provide centralized pad control
Power management	Temperature sensor with programmable trip points
	Flexible power domain partitioning with internal power switches to support efficient power management
Connectivity	One PCIe Express (PCIe) Single Lane supporting PCIe Gen3 • Dual Mode operation to function as root complex or endpoint • Integrated PHY interface • Supports L1 low power sub-state
	Two USB 3.0 Type C controllers with integrated PHY (also supported USB 2.0) interfaces: • Spread spectrum clock support
	Three Ultra Secure Digital Host Controller (uSDHC) interfaces • eMMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec • SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec • Support for SDXC (extended capacity)
	Two Ethernet controllers (both capable of simultaneous operation) • One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588 • One Gigabit Ethernet controller with support for TSN in addition to EEE, Ethernet AVB, and IEEE 1588
	Two Controller Area Network (FlexCAN) modules, each optionally supporting flexible data-rate (FD) **Note:** Legacy CAN mode supports both Mailbox (MB) and RX FIFO (with DMA support) operation. Flexible Data (FD) mode supports MB operation only. There is no enhanced RX FIFO or DMA support in FD mode.
	Four Universal Asynchronous Receiver/Transmitter (UART) modules
	Six I2C modules
	Three SPI modules

Table 1. Features (continued) (Sheet 4 of 4)

Subsystem	Features
Security	Resource Domain Controller (RDC) • Supports 4 domains and up to 8 regions of DDR
	Arm® TrustZone® (TZ) architecture: • Cortex®-A53 MPCore TrustZone® support
	On-chip RAM (OCRAM) secure region protection using OCRAM controller
	High Assurance Boot (HAB)
	Cryptographic Acceleration and Assurance Module (CAAM) • Capable to support Widevine and PlayReady content protection • Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms • Real-time integrity checker (RTIC) • DRM support for RSA, AES, 3DES, DES • True random number generation (RNG) • Manufacturing protection support
	Secure Non-Volatile Storage (SNVS) • Secure real-time clock (RTC)
	Secure JTAG Controller (SJC)
System debug	Arm® CoreSight™ debug and trace technology
	Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
	Unified trace capability for quad core Cortex®-A53 and Cortex®-M7 CPUs
	Cross Triggering Interface (CTI)
	Support for 5-pin (JTAG) debug interface

NOTE

The actual feature set depends on the part numbers as described in Table 3.

1.1 Block diagram

Figure 1 shows the functional modules in the i.MX 8M Plus processor system.

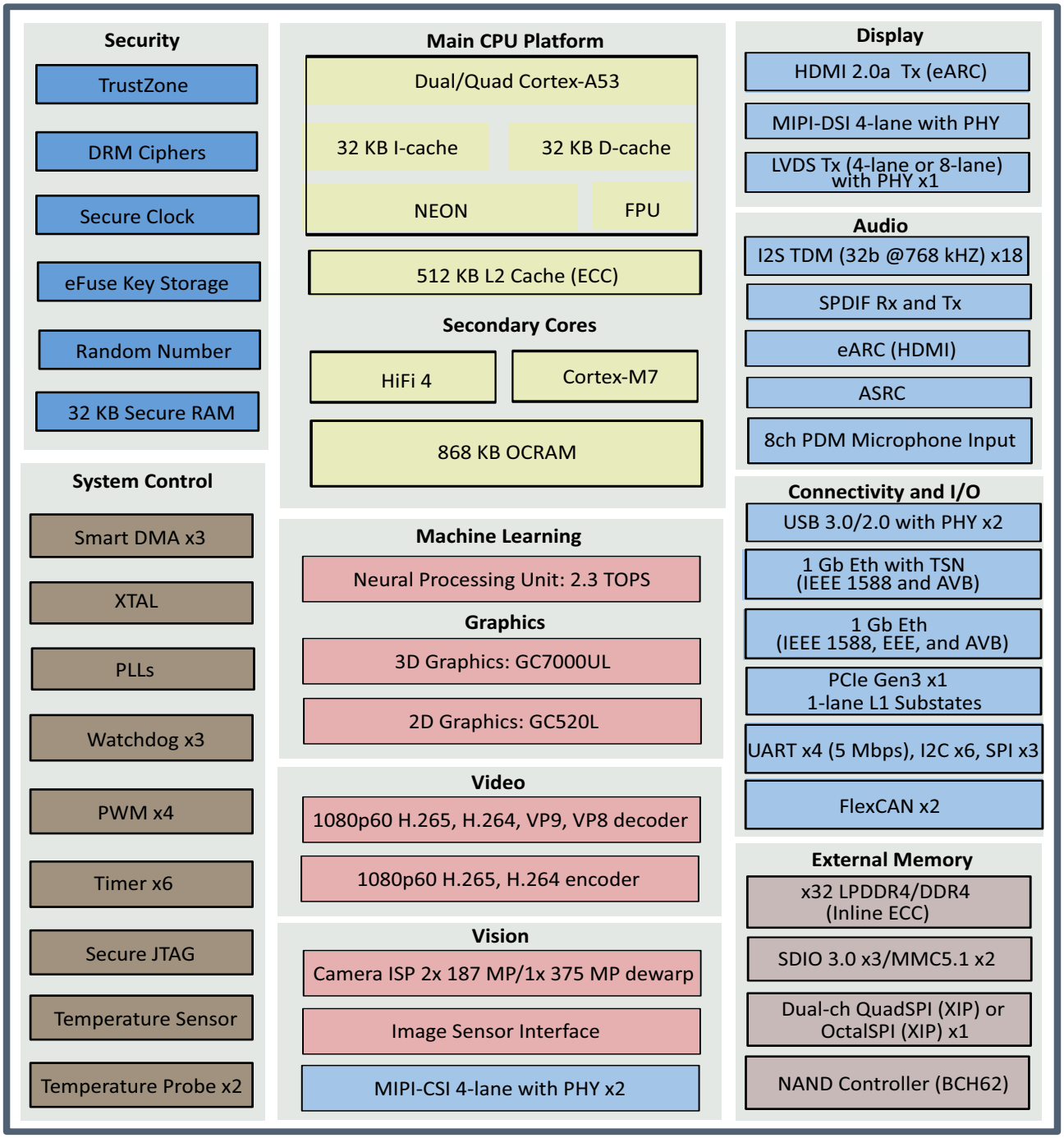


Figure 1. i.MX 8M Plus system block diagram

NOTE

Some modules shown in this block diagram are not offered on all derivatives. See Table 2 for exceptions.

Table 2. Modules supported

Key Modules	8CVN	6CVN	4CVN	3CVN	8DVN	6DVN	4DVN	3DVN
Cortex® A53	4x	4x	4x	2x	4x	4x	4x	2x
VPU	1x	1x	N/A	1x	1x	1x	N/A	1x
NPU	1x	N/A	N/A	1x	1x	N/A	N/A	1x
ISP	1x	1x	N/A	1x	1x	1x	N/A	1x
HiFi 4	1x	N/A	N/A	1x	1x	N/A	N/A	1x

1.2 Ordering information

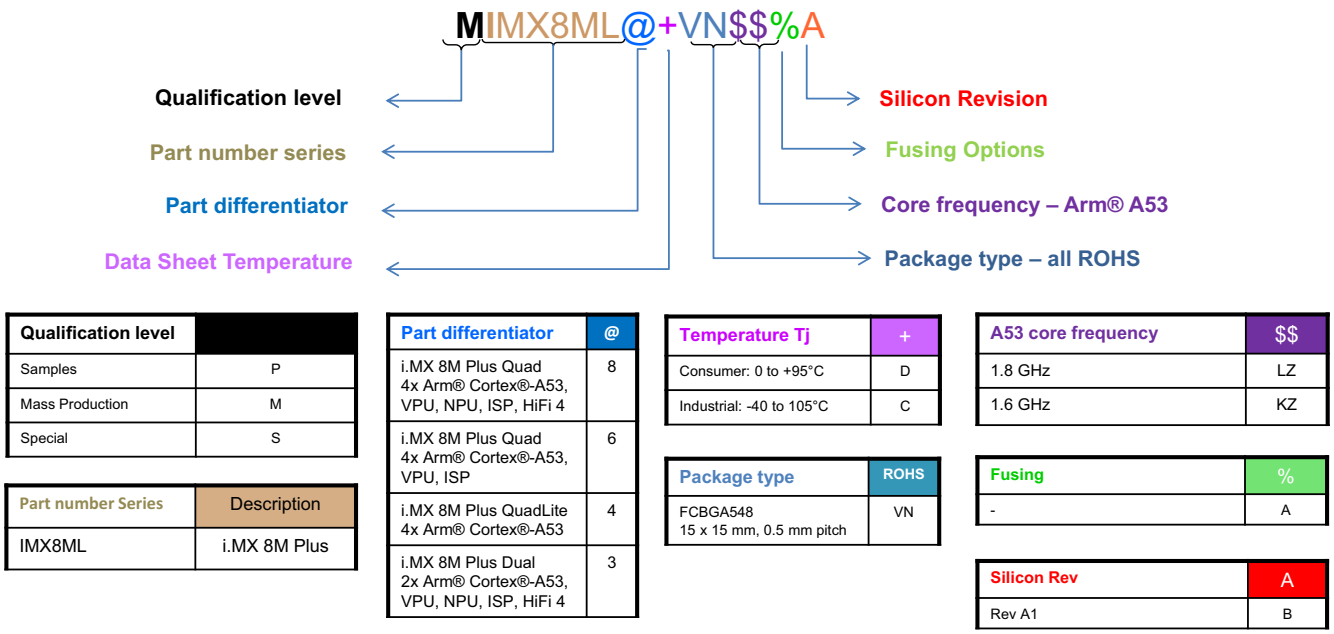
Table 3 shows examples of orderable sample part numbers covered by this data sheet. This table does not include all possible orderable part numbers. If your desired part number is not listed in the table, or you have questions about available parts, contact your NXP representative.

Table 3. Orderable part numbers

Part number	Device description	Part differentiator description	Number of A53 Cores	A53 speed	Qualification tier	Temperature T_j (°C)	Package description
MIMX8ML8CVNKZAB	i.MX 8M Plus Quad	NPU, ISP, VPU, HiFi 4, CAN-FD	4	1.6 GHz	Industrial	-40 to 105	15 x 15 mm, 0.5 pitch, FCBGA
MIMX8ML6CVNKZAB	i.MX 8M Plus Quad	ISP, VPU, CAN-FD	4	1.6 GHz	Industrial	-40 to 105	15 x 15 mm, 0.5 pitch, FCBGA
MIMX8ML4CVNKZAB	i.MX 8M Plus QuadLite	CAN-FD	4	1.6 GHz	Industrial	-40 to 105	15 x 15 mm, 0.5 pitch, FCBGA
MIMX8ML3CVNKZAB	i.MX 8M Plus Dual	NPU, ISP, VPU, HiFi 4, CAN-FD	2	1.6 GHz	Industrial	-40 to 105	15 x 15 mm, 0.5 pitch, FCBGA

Figure 2 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.

Contact an NXP representative for additional details.



Qualification level	
Samples	P
Mass Production	M
Special	S

Part number Series	Description
IMX8ML	i.MX 8M Plus

Part differentiator	@
i.MX 8M Plus Quad 4x Arm® Cortex®-A53, VPU, NPU, ISP, HiFi 4	8
i.MX 8M Plus Quad 4x Arm® Cortex®-A53, VPU, ISP	6
i.MX 8M Plus QuadLite 4x Arm® Cortex®-A53	4
i.MX 8M Plus Dual 2x Arm® Cortex®-A53, VPU, NPU, ISP, HiFi 4	3

Temperature Tj	+
Consumer: 0 to +95°C	D
Industrial: -40 to 105°C	C

Package type	ROHS
FCBGA548 15 x 15 mm, 0.5 mm pitch	VN

A53 core frequency	$$
1.8 GHz	LZ
1.6 GHz	KZ

Fusing	%
-	A

Silicon Rev	A
Rev A1	B

Figure 2. Part number nomenclature—i.MX 8M Plus family of processors

2 Modules list

The i.MX 8M Plus family of processors contains a variety of digital and analog modules. Table 4 describes these modules in alphabetical order.

Table 4. i.MX 8M Plus modules list

Block mnemonic	Block name	Brief description
APBH-DMA	NAND Flash and BCH ECC DMA Controller	DMA controller used for GPMI2 operation.
Arm	Arm Platform	The Arm Core Platform includes a quad Cortex-A53 core and a Cortex-M7 core. The Cortex-A53 core includes associated sub-blocks, such as the Level 2 Cache Controller, Snoop Control Unit (SCU), General Interrupt Controller (GIC), private timers, watchdog, and CoreSight debug modules. The Cortex-M7 core is used as a customer microcontroller.
ASRC	Asynchronous Sample Rate Converter	The Asynchronous Sample Rate Converter (ASRC) can process 4 groups of audio channels with an independent time-base simultaneously. A group of channels with the same time-base (or resampling ration) is referred to as a context. Each context has independent processing pipelines. Contexts can be configured to start and stop at any time without affecting the processing of other contexts. The ASRC supports up to 32 audio channels, which can either be assigned to a single context or spread across multiple contexts.
BCH	Binary-BCH ECC Processor	The BCH module provides up to 62-bit ECC encoder/decoder for NAND Flash controller (GPMI).
CAAM	Cryptographic accelerator and assurance module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The PRNG is certifiable by the Cryptographic Algorithm Validation Program (CAVP) of the National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 8M Plus processors, the secure memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 8M Plus platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interface	Cross Trigger Interface (CTI) allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A53 core platform.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.

Table 4. i.MX 8M Plus modules list (continued)

Block mnemonic	Block name	Brief description
DDRC	Double Data Rate Controller	The DDR Controller has the following features: • Supports 32-bit LPDDR4-4000 and DDR4-3200 • Supports up to 8 Gbyte DDR memory space
eCSPI1 eCSPI2 eCSPI3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes.
eDMA	Enhanced Direct Memory Access	• There is one enhanced DMAs (eDMA). • The eDMA is a 32-channel DMA engine • It is provided specifically for copying between memory and memory (most likely such as between two of DRAM, OCRAM_A, and Audio DSPs TCM). • It separates the 32 channels into separate 64 KByte regions in the system memory map for virtualization and partitioning purpose. • There are no DMA requests connected to eDMA from any peripheral. It is generally controlled by the Audio DSP (or potentially the Cortex-A53 or Cortex_M7).
ENET	Ethernet Controller	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM) for details.
ENET_QOS	Ethernet QoS Controller	The ENET_QOS is compliant with the IEEE 802.3–2015 specification and can be used in applications, such as AV bridges, AV nodes, switches, data center bridges and nodes, and network interface cards. It enables a host to transmit and receive data over Ethernet in compliance with the IEEE802.3–2015. A separate 1 Gbit Ethernet QoS with TSN supports the same features as ENET and also following features: • 802.1Qbv Enhancements to Scheduling Traffic • 802.1Qbu Frame preemption • Time Based Scheduling
FlexCAN1 FlexCAN2	Flexible Controller Area Network	Communication controller implementing the CAN with Flexible Data rate (CAN FD) protocol and the CAN protocol according to the CAN 2.0B protocol specification.
FlexSPI	FlexSPI	The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi master access with priority and flexible and configurable buffer for each master
GIC	Generic Interrupt Controller	The GIC handles all interrupts from the various subsystems and is ready for virtualization.

Table 4. i.MX 8M Plus modules list (continued)

Block mnemonic	Block name	Brief description
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	The GPMI module supports up to 4x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2 GPT3 GPT4 GPT5 GPT6	General Purpose Timer	Each GPT is a 32-bit “free-running” or “set-and-forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set-and-forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2D	Graphics Processing Unit-2D	This Graphic Processing Unit defines a high-performance, multi-pipe 2D raster graphics core that accelerates the 2D graphics display.
GPU3D	Graphics Processing Unit-3D	The GPU3D provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays.
I2C1 I2C2 I2C3 I2C4 I2C5 I2C6	I^2C Interface	I^2C provides serial interface for external devices. Data rates of up to 320 kbps are supported.
IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.
LCDIF	LCD interface	The LCD Interface (LCDIF) is a general purpose display controller used to drive a wide range of display devices varying in size and capability.
LDB	LVDS Display Bridge	LVDS Display Bridge is used to connect the LCDIF to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MIPI CSI1 MIPI CSI2 (four-lane)	MIPI Camera Serial Interface	This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps.
MIPI DSI (four-lane)	MIPI Display Serial Interface	This module provides a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps.

Table 4. i.MX 8M Plus modules list (continued)

Block mnemonic	Block name	Brief description
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility.
OCRAM	On-Chip Memory controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. In i.MX 8M Plus processors, the OCRAM is used for controlling the 868KB multimedia RAM through AXI bus.
PCIe	PCI Express 3.0	The PCIe IP provides PCI Express Gen 3 functionality.
PMU	Power Management Unit	Integrated power management unit. Used to provide power to various SoC domains.
PWM1 PWM2 PWM3 PWM4	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
SAI1 SAI2 SAI3 SAI5 SAI6 SAI7	Synchronous Audio Interface	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 4. i.MX 8M Plus modules list (continued)

Block mnemonic	Block name	Brief description
SDMA	Smart Direct Memory Access	The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	Secure JTAG Controller	The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 8M Plus family of processors uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE 1149.1 and IEEE 1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 8M Plus SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation Detection and reporting.
SPDIF1	Sony Philips Digital Interconnect Format	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
System Bus (NoC)	Network-on-Chip	The module is used as central inter-connect fabric, which runs at approximately 1/4 of the DRAM data rate, and links the bus master to DRAM controller for high-throughput DRAM access. Multiple additional NoCs as the high-performance inter-connect bus fabric for high-speed initiators.
TEMPSENSOR	Temperature Sensor	Temperature sensor
TZASC	Trust-Zone Address Space Controller	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.

Table 4. i.MX 8M Plus modules list (continued)

Block mnemonic	Block name	Brief description
UART1 UART2 UART3 UART4	UART Interface	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud
uSDHC1 uSDHC2 uSDHC3	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	i.MX 8M Plus SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to support: • SD/SDIO standard, up to version 3.0. • MMC standard, up to version 5.1. • 1.8 V and 3.3 V operation, but do not support 1.2 V operation. • 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode.
USB 3.0	2x USB 3.0 controllers and PHYs	Two USB controllers and PHYs that support USB 3.0. Each USB instance contains: • USB 3.0 core, which can operate in 2.0 mode
VPU	Video Processing Unit	A high performing video processing unit (VPU), which covers many SD-level and HD-level video decoders. See the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM) for a complete list of the VPU's decoding and encoding capabilities.
WDOG1 WDOG2 WDOG3	Watchdog	The watchdog (WDOG) timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator interface	The XTALOSC module enables connectivity to an external crystal oscillator device. In a typical application use case, it is used for a 24 MHz oscillator.

2.1 Unused input and output guidance

If a function of the i.MX 8M Plus is not used, the I/Os and power rails of that function can be terminated to reduce overall board power. Table 5 is recommended connectivities for LVDS, PCIe, HDMI, eARC, and other digital I/Os. Table 6 is recommended connectivities for MIPI. Table 7 is recommended connectivities for USB.

Table 5. Unused function strapping recommendations

Function	Ball name	Recommendations if Unused
LVDS	VDD_LVDS_1P8, LVDS1_CLK_P, LVDS1_CLK_N, LVDS1_Dx_P, LVDS1_Dx_N, LVDS2_CLK_P, LVDS2_CLK_N, LVDS2_Dx_P, LVDS2_Dx_N,	Not connected
PCIe	VDD_PCI_1P8, VDD_PCI_0P8, PCIE_TXN_P, PCIE_TXN_N, PCIE_RXN_P, PCIE_RXN_N, PCIE_REF_PAD_CLK_P, PCIE_REF_PAD_CLK_N, PCIE_RESREF	Not connected

Table 5. Unused function strapping recommendations (continued)

Function	Ball name	Recommendations if Unused
HDMI	VDD_HDMI_1P8, VDD_HDMI_0P8, HDMI_TXC_P, HDMI_TXC_N, HDMI_TXx_P, HDMI_TXx_N, HDMI_REXT	Not connected
eARC	VDD_EARC_1P8	Tie to ground using a 10K resistor
	EARC_AUX, EARC_N_HPD, EARC_P_UTIL	Not connected
Digital I/O supplies	NVCC_SAI2_SAI3_SPDIF, NVCC_ECSPI_HDMI, NVCC_ENET, NVCC_GPIO, NVCC_I2C_UART, NVCC_JTAG, NVCC_NAND, NVCC_SAI1_SAI5, NVCC_SD1, NVCC_SD2, NVCC_CLK	Not connected if entire bank not used

Table 6. MIPI strapping recommendations

Function	Ball name	Recommendations
MIPI_CSI1, MIPI_CSI2 and MIPI_DSI	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	VDD_MIPI_1P2_CAP, MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Not connected
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N, MIPI_CSI2_CLK_P, MIPI_CSI2_CLK_N, MIPI_CSI2_Dx_P, MIPI_CSI2_Dx_N, MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N	Function
Only MIPI_CSI1 and MIPI_CSI2	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	MIPI_VREG1_CAP	Not connected
	VDD_MIPI_1P2_CAP	Connect to outside cap
	MIPI_TEST_DNU	Not connected
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N, MIPI_CSI2_CLK_P, MIPI_CSI2_CLK_N, MIPI_CSI2_Dx_P, MIPI_CSI2_Dx_N,	Function
	MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N	Not connected
Only MIPI_CSI1 and MIPI_DSI	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	VDD_MIPI_1P2_CAP, MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Not connected
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N	Function
	MIPI_CSI2_CLK_P, MIPI_CSI2_CLK_N, MIPI_CSI2_Dx_P, MIPI_CSI2_Dx_N	Tied to ground
	MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N	Function

Table 6. MIPI strapping recommendations (continued)

Function	Ball name	Recommendations
Only MIPI_CSI2 and MIPI_DSI	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	VDD_MIPI_1P2_CAP, MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Not connected
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N	Tied to ground
	MIPI_CSI2_CLK_P, MIPI_CSI2_CLK_N, MIPI_CSI2_Dx_P, MIPI_CSI2_Dx_N	Function
	MIPI_DSI_CLK_P, MIPI_DSI_CLK_N, MIPI_DSI_Dx_P, MIPI_DSI_Dx_N	Function
Only MIPI_DSI	VDD_MIPI_1P8, VDD_MIPI_0P8	Supply
	VDD_MIPI_1P2_CAP, MIPI_VREG1_CAP	Connect to outside cap
	MIPI_TEST_DNU	Not connected
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N	Tied to ground
	MIPI_CSI2_CLK_P, MIPI_CSI2_CLK_N, MIPI_CSI2_Dx_P, MIPI_CSI2_Dx_N	Tied to ground
MIPI_CSI1, MIPI_CSI2 and MIPI_DSI are not used	VDD_MIPI_1P8, VDD_MIPI_0P8	Not connected
	VDD_MIPI_1P2_CAP, MIPI_VREG1_CAP	Not connected
	MIPI_TEST_DNU	Not connected
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N	Not connected
	MIPI_CSI2_CLK_P, MIPI_CSI2_CLK_N, MIPI_CSI2_Dx_P, MIPI_CSI2_Dx_N	Not connected

Table 7. USB strapping recommendations

Function	Ball name	Recommendations
USB1 and USB2	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P, USB1_D_N, USB1_TX_P, USB1_TX_N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P, USB1_RX_N	Function connection
	USB2_VBUS, USB2_D_P, USB2_D_N, USB2_TX_P, USB2_TX_N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P, USB2_RX_N	Function connection
USB1	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P, USB1_D_N, USB1_TX_P, USB1_TX_N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P, USB1_RX_N	Function connection
	USB2_VBUS, USB2_D_P, USB2_D_N, USB2_TX_P, USB2_TX_N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P, USB2_RX_N	Ground *RX_P and *RX_N, others are not connected
USB2	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P, USB1_D_N, USB1_TX_P, USB1_TX_N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P, USB1_RX_N	Ground *RX_P and *RX_N, others are not connected
	USB2_VBUS, USB2_D_P, USB2_D_N, USB2_TX_P, USB2_TX_N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P, USB2_RX_N	Function connection

Table 7. USB strapping recommendations (continued)

Function	Ball name	Recommendations
USB1 and USB2 are not used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Not connected
	USB1_VBUS, USB1_D_P, USB1_D_N, USB1_TX_P, USB1_TX_N, USB1_DNU, USB1_TXRTUNE, USB1_RX_P, USB1_RX_N	Ground *RX_P and *RX_N, others are not connected
	USB2_VBUS, USB2_D_P, USB2_D_N, USB2_TX_P, USB2_TX_N, USB2_DNU, USB2_TXRTUNE, USB2_RX_P, USB2_RX_N	Ground *RX_P and *RX_N, others are not connected

If there are any questions, visit the web page NXP.com/IMX 8 Processors or contact an NXP representative for details.

3 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 8M Plus family of processors.

3.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 8 for a quick reference to the individual tables and sections.

Table 8. i.MX 8M Plus chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 18
Thermal resistance	on page 20
Operating ranges	on page 23
External clock sources	on page 28
Estimated power supply maximum currents	on page 31
Power modes	on page 32
Power supplies requirements and restrictions	on page 34

3.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under Table 9 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 9. Absolute maximum ratings

Parameter description	Symbol	Min	Max	Unit	Notes
Core supply voltages	VDD_ARM VDD_SOC	-0.3	1.15	V	—
GPIO supply voltage	NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_JTAG, NVCC_ENET, NVCC_SAI1_SAI5, NVCC_SAI2_SAI3_SPDIF, NVCC_ECSPI_HDMI, NVCC_GPIO, NVCC_I2C_UART, NVCC_CLK	-0.3	3.8	V	—
SNVS IO supply voltage	NVCC_SNVS_1P8	-0.3	2.15	V	—

Table 9. Absolute maximum ratings (continued)

Parameter description	Symbol	Min	Max	Unit	Notes
DDR I/O supply voltage	NVCC_DRAM	-0.3	1.575	V	—
Arm PLL supply voltage	VDD_ARM_PLL_0P8	-0.3	1.15	V	—
	VDD_ARM_PLL_1P8	-0.3	2.15	V	—
PCIe PHY supply voltage	VDD_PCI_0P8	-0.3	1.15	V	—
	VDD_PCI_1P8	-0.3	2.15	V	—
MIPI PHY supply voltage	VDD_MIPI_0P8	-0.3	1.15	V	—
	VDD_MIPI_1P8	-0.3	2.15	V	—
USB PHY supply voltage	VDD_USB_0P8	-0.3	1.15	V	—
	VDD_USB_1P8	-0.3	2.15	V	—
	VDD_USB_3P3	-0.3	3.95	V	—
USB_VBUS input detected	USB1_VBUS, USB2_VBUS	-0.3	3.95	V	—
XTAL supply voltage	VDD_24M_XTAL_1P8	-0.3	2.15	V	—
Input/output voltage range	V_{in}/V_{out}	-0.3	OVDD[1] + 0.3	V	—
Storage temperature range	$T_{STORAGE}$	-40	150	^{o}C	—

1 OVDD is the I/O supply voltage.

Table 10. Electrostatic discharge and latch up ratings

Parameter description		Rating	Reference	Comment
Electrostatic Discharge (ESD)	Human Body Model (HBM)	±1000 V	JS-001-2017	—
	Charged Device Model (CDM)	±250 V	JS-002-2018	—
Latch UP (LU)	Immunity level: • Class I@ 25 ^{o}C ambient temperature • Class II @ 105 ^{o}C ambient temperature	 A A	JESD78E	—

3.1.2 Thermal resistance

3.1.2.1 15 x 15 mm FCPBGA package thermal characteristics

Table 11 displays the 15 x 15 mm FCPBGA package thermal resistance data.

Table 11. 15 x 15 mm FCPBGA thermal resistance data

Rating[1]	Board Type[2]	Symbol	Value	Unit
Junction to Ambient Thermal Resistance[3]	JESD51-9, 2s2p	$R_{\theta JA}$	21.1	°C/W
Junction-to-Top of Package Thermal Characterization parameter[3]	JESD51-9, 2s2p	Ψ_{JT}	0.98	°C/W
Junction to Case Thermal Resistance[4]	JESD51-9, 1s	$R_{\theta JC}$	0.24	°C/W

1 The ratings were generated using a non-uniformly powered die.

2 Thermal test board meets JEDEC specification for this package (JESD51-9). PCB has no thermal vias under the package.

3 Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

4 Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers t the package top side surface.

3.1.3 Power architecture

The power architecture of the chip is defined based on the assumption that lowest-cost system are constructed for case where the PMIC is always used to supply all the power rails to the processor.

The digital logic inside chip will be supplied with two supplies: VDD_ARM and VDD_SOC.

- VDD_ARM is for the Cortex®-A53 platform.
- VDD_SOC is for the rest of the modules in SoC.

The VDD_SOC can be nominal or overdrive voltage, the VDD_ARM can be nominal, overdrive or super-overdrive. To support system with VDD_ARM at super-overdrive voltage, it is recommended to use two external DCDC or DC-DC supplies, first one for VDD_ARM and the second one for VDD_SOC. However, for cost-optimized solutions, the two supplies can be tied together in customer systems. VDD_ARM can support DVFS for SoCs that choose to enable it. VDD_SOC does not support fast on-the-fly DVFS, but can support mode-based dynamic voltage for SoCs that choose to enable it.

The GPIO pads will have external power supply for 3.3 V and 1.8 V IO voltage. The IO pad core voltage will be supplied directly by VDD_SOC. For 3.3 V IO pad, its 3.3 V IO supply (NVCC) and 1.8 V pre-driver supply (PVCC_1P8) should be always meet NVCC - PVCC < 2 V requirement during power up and power down. For 1.8 V IO pad, its 1.8 V PVCC can be shorted together with NVCC.

The DRAM controller and PHY have four external power supplies: VDD_SOC supplies controller and PHY digital logic, VDD_DRAM_PLL_1P8 / VDD_DRAM_PLL_0P8 for PHY analog circuit, and NVCC_DRAM for IO.

For all the integrated analog modules, their 1.8 V analog power and 0.85 V/0.95 V digital power will be supplied externally through power pads. These supplies are separated with other power pads on the

package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For all the integrated PCIe PHY, LVDS PHY, MIPI PHY, and USB PHY, their 3.3 V (where supported), 1.8 V and 0.85/0.95 V power will be supplied externally through power pads. The powers to those PHYs are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC. A LDO will be integrated to generate the 1.2 V required for the MIPI PHY. The MIPI PHY also has integrated within its PHY and LDO to generate its 0.4V supply. External capacitors are required for both the 1.2 V and 0.4 V internal LDO regulators.

For SNVS/RTC, the 1.8 V IO pre-driver supply and 1.8 V IO pad supply will also be supplied externally. The 0.8 V SNVS_LP core domain logic is supplied by an internal LDO.

Figure 3 is the power architecture diagram. Note it only shows supplies, and does not show capacitors that may be required for internal LDO regulators.

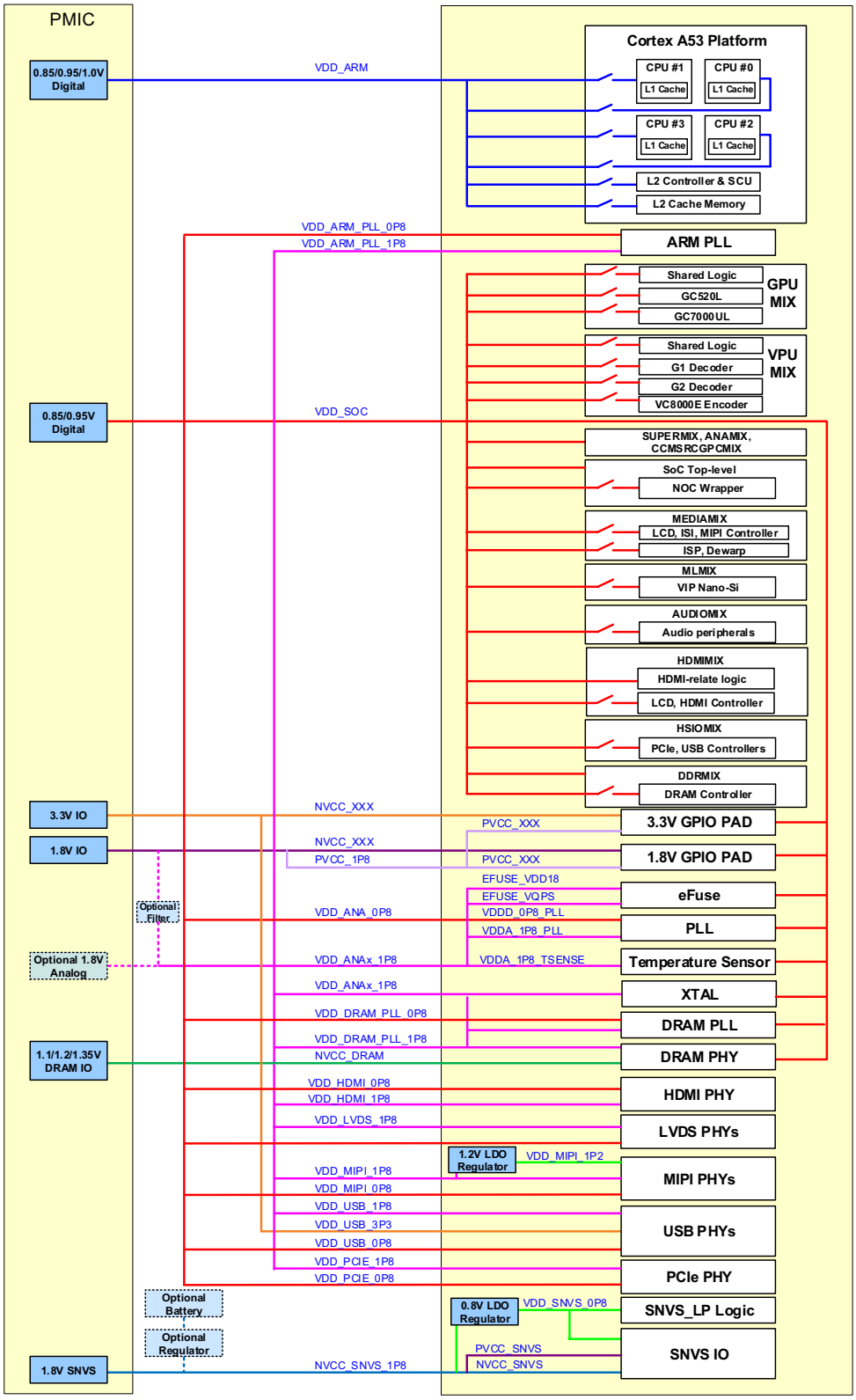


Figure 3. Power architecture of i.MX 8M Plus family of processors

3.1.4 Operating ranges

Table 12 provides the operating ranges of the i.MX 8M Plus of processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM).

Table 12. Operating ranges

Parameter description	Symbol	Min	Typ	Max[1,2]	Unit	Comment
Power supply for Quad-A53	VDD_ARM	0.805	0.850	0.950	V	Power supply for Cortex®-A53, nominal mode, 1.2 GHz
		0.900	0.950	1.000	V	Power supply for Cortex®-A53, overdrive mode, 1.6 GHz
Power supply for SoC logic	VDD_SOC	0.805	0.850	0.900	V	Power supply for SOC, nominal mode
		0.900	0.950	1.000	V	Power supply for SOC, overdrive mode
DDR I/O supply voltage	NVCC_DRAM	1.140	1.200	1.260	V	DDR4
		1.045	1.100	1.155	V	LPDDR4
SNVS supply voltage	NVCC_SNVS_1P8	1.710	1.800	1.950	V	I/O supply and I/O Pre-driver supply for GPIO in SNVS bank
Supply for analog PLLs	VDD_ANA1_0P8	0.805	0.850	0.900	V	Power supply for ANAMIX PLL, nominal mode
		0.900	0.950	1.000	V	Power supply for ANAMIX PLL, overdrive mode
1.8 V supply for PLLs, eFuse, and Temperature Sensor	VDD_ANAx_1P8	1.710	1.800	1.890	V	—
1.8 V supply for 24 MHz XTAL	VDD_24M_XTAL_1P8	1.710	1.800	1.890	V	—
USB PHY supply voltage	VDD_USB_0P8	0.805	0.850	0.900	V	Digital supply for USB PHY, nominal mode
		0.900	0.950	1.000	V	Digital supply for USB PHY, overdrive mode
	VDD_USB_3P3	3.069	3.300	3.630	V	3.3 V supply for USB PHY
	VDD_USB_1P8	1.710	1.800	1.890	V	1.8 V supply for USB PHY
USBx_VBUS supply voltage	USBx_VBUS	1.34	—	3.6	V	3.3 V supply for USB
PCIe PHY supply voltage	VDD_PCI_0P8	0.805	0.850	0.900	V	Digital supply for PCIe PHY, nominal mode
		0.900	0.950	1.000	V	Digital supply for PCIe PHY, overdrive mode
	VDD_PCI_1P8	1.710	1.800	1.890	V	1.8 V supply for PCIe PHY

Table 12. Operating ranges (continued)

Parameter description	Symbol	Min	Typ	Max[1,2]	Unit	Comment
HDMI supply voltage	VDD_HDMI_0P8	0.805	0.850	0.900	V	Digital supply for HDMI PHY, nominal mode
		0.900	0.950	1.000	V	Digital supply for HDMI PHY, overdrive mode
	VDD_HDMI_1P8	1.710	1.800	1.890	V	Digital supply for HDMI PHY, overdrive mode
LVDS supply voltage	VDD_LVDS_1P8	1.710	1.800	1.890	V	1.8 V supply for LVDS PHY
MIPI PHY supply voltage	VDD_MIPI_0P8	0.805	0.850	0.900	V	Digital supply for MIPI PHY, nominal mode
		0.900	0.950	1.000	V	Digital supply for MIPI PHY, overdrive mode
	VDD_MIPI_1P8	1.710	1.800	1.890	V	1.8 V supply for MIPI PHY
Arm PLL supply voltage	VDD_ARM_PLL_0P8	0.805	0.850	0.900	V	0.85 V supply for Arm PLL, nominal mode
		0.900	0.950	1.000	V	0.95 V supply for Arm PLL, overdrive mode
	VDD_ARM_PLL_1P8	1.710	1.800	1.890	V	1.8 V supply for Arm PLL
DRAM PLL supply voltage	VDD_DRAM_PLL_0P8	0.805	0.850	0.900	V	0.85 V supply for Arm PLL, nominal mode
		0.900	0.950	1.000	V	0.95 V supply for Arm PLL, overdrive mode
	VDD_DRAM_PLL_1P8	1.710	1.800	1.890	V	1.8 V supply for DRAM PLL
SAI PLL supply voltage	VDD_SAI_PLL_0P8	0.805	0.850	0.900	V	0.85 V supply for SAI PLL
		0.900	0.950	1.000	V	0.95 V supply for SAI PLL, overdrive mode
	VDD_SAI_PLL_1P8	1.710	1.800	1.890	V	1.8 V supply for SAI PLL
AVPLL supply voltage	VDD_AVPLL_1P8	1.710	1.800	1.890	V	1.8 V supply for AVPLL
EARC supply voltage	VDD_EARC_1P8	1.710	1.800	1.890	V	1.8 V supply for EARC

Table 12. Operating ranges (continued)

Parameter description	Symbol	Min	Typ	Max[1,2]	Unit	Comment
GPIO supply voltages	PVCC_1P8	1.650	1.800	1.950	V	Power supply for GPIO pre-driver
	NVCC_SD1, NVCC_SD2, NVCC_NAND, NVCC_JTAG, NVCC_ENET, NVCC_SAI1_SAI5, NVCC_SAI2_SAI3_SPDIF,NVCC_ECSPI_HDMI, NVCC_GPIO, NVCC_I2C_UART, NVCC_CLK	1.650	1.800	1.950	V	Power supply for GPIO when it is in 1.8 V mode
		3.000	3.300	3.600	V	Power supply for GPIO when it is in 3.3 V mode
Junction temperature, Industrial	T_J	-40	—	+105	°C	See Table 3 for complete list of junction temperature capabilities.

1 Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This results in an optimized power/speed ratio.

2 Overdrive maximum voltage includes all the nominal frequencies.

3.1.5 Maximum frequency of modules

Table 13 provides the maximum frequency of modules in the i.MX 8M Plus of processors.

Table 13. Maximum frequency of modules (Sheet 1 of 4)

Clock root	Nominal mode	Overdrive mode	Unit
ARM_A53_CLK_ROOT	1000	1000	MHz
ARM_M7_CLK_ROOT	600	800	MHz
ML_CLK_ROOT	800	1000	MHz
GPU3D_CORE_CLK_ROOT	800	1000	MHz
GPU3D_SHADER_CLK_ROOT	800	1000	MHz
GPU2D_CLK_ROOT	800	1000	MHz
AUDIO_AXI_CLK_ROOT	600	800	MHz
HSIO_AXI_CLK_ROOT	400	500	MHz
MEDIA_ISP_CLK_ROOT	400	500	MHz
ENET_AXI_CLK_ROOT	266	266	MHz
NAND_USDHC_BUS_CLK_ROOT	266	266	MHz
VPU_BUS_CLK_ROOT	600	800	MHz
MEDIA_AXI_CLK_ROOT	400	500	MHz
MEDIA_APB_CLK_ROOT	200	200	MHz

Table 13. Maximum frequency of modules (continued) (Sheet 2 of 4)

Clock root	Nominal mode	Overdrive mode	Unit
HDMI_APB_CLK_ROOT	133	133	MHz
HDMI_AXI_CLK_ROOT	400	500	MHz
GPU_AXI_CLK_ROOT	600	800	MHz
GPU_AHB_CLK_ROOT	300	400	MHz
NOC_CLK_ROOT	800	1000	MHz
NOC_IO_CLK_ROOT	600	800	MHz
ML_AXI_CLK_ROOT	800	800	MHz
ML_AHB_CLK_ROOT	300	400	MHz
AHB_CLK_ROOT	133.333	133.333	MHz
IPG_CLK_ROOT	66.667	66.667	MHz
AUDIO_AHB_CLK_ROOT	400	400	MHz
MEDIA_DISP2_CLK_ROOT	170	170	MHz
DRAM_ALT_CLK_ROOT	666.667	666.667	MHz
DRAM_APB_CLK_ROOT	200	200	MHz
VPU_G1_CLK_ROOT	600	800	MHz
VPU_G2_CLK_ROOT	500	700	MHz
CAN1_CLK_ROOT	80	80	MHz
CAN2_CLK_ROOT	80	80	MHz
MEMREPAIR_CLK_ROOT	24	24	MHz
PCIE_PHY_CLK_ROOT	250	250	MHz
PCIE_AUX_CLK_ROOT	10	10	MHz
I2C5_CLK_ROOT	66	66	MHz
I2C6_CLK_ROOT	66	66	MHz
SAI1_CLK_ROOT	66	66	MHz
SAI2_CLK_ROOT	66	66	MHz
SAI3_CLK_ROOT	66	66	MHz
SAI5_CLK_ROOT	66	66	MHz
SAI6_CLK_ROOT	66	66	MHz
ENET_QOS_CLK_ROOT	125	125	MHz
ENET_QOS_TIMER_CLK_ROOT	200	200	MHz
ENET_REF_CLK_ROOT	125	125	MHz
ENET_TIMER_CLK_ROOT	125	125	MHz
ENET_PHY_REF_CLK_ROOT	125	125	MHz

Table 13. Maximum frequency of modules (continued) (Sheet 3 of 4)

Clock root	Nominal mode	Overdrive mode	Unit
NAND_CLK_ROOT	500	500	MHz
QSPI_CLK_ROOT	400	400	MHz
USDHC1_CLK_ROOT	400	400	MHz
USDHC2_CLK_ROOT	400	400	MHz
I2C1_CLK_ROOT	66	66	MHz
I2C2_CLK_ROOT	66	66	MHz
I2C3_CLK_ROOT	66	66	MHz
I2C4_CLK_ROOT	66	66	MHz
UART1_CLK_ROOT	80	80	MHz
UART2_CLK_ROOT	80	80	MHz
UART3_CLK_ROOT	80	80	MHz
UART4_CLK_ROOT	80	80	MHz
ECSPI1_CLK_ROOT	80	80	MHz
ECSPI2_CLK_ROOT	80	80	MHz
PWM1_CLK_ROOT	66	66	MHz
PWM2_CLK_ROOT	66	66	MHz
PWM3_CLK_ROOT	66	66	MHz
PWM4_CLK_ROOT	66	66	MHz
GPT1_CLK_ROOT	100	100	MHz
GPT2_CLK_ROOT	100	100	MHz
GPT3_CLK_ROOT	100	100	MHz
GPT4_CLK_ROOT	100	100	MHz
GPT5_CLK_ROOT	100	100	MHz
GPT6_CLK_ROOT	100	100	MHz
TRACE_CLK_ROOT	133	133	MHz
WDOG_CLK_ROOT	66	66	MHz
IPP_DO_CLKO1	200	200	MHz
IPP_DO_CLKO2	200	200	MHz
HDMI_FDCC_TST_CLK_ROOT	200	300	MHz
HDMI_REF_266M_CLK_ROOT	266	266	MHz
USDHC3_CLK_ROOT	400	400	MHz
MEDIA_CAM1_PIX_CLK_ROOT	400	500	MHz
MEDIA_MIPI_PHY1_REF_CLK_ROOT	300	300	MHz

Table 13. Maximum frequency of modules (continued) (Sheet 4 of 4)

Clock root	Nominal mode	Overdrive mode	Unit
MEDIA_DISP1_PIX_CLK_ROOT	250	250	MHz
MEDIA_CAM2_PIX_CLK_ROOT	277	277	MHz
MEDIA_LDB_CLK_ROOT	595	595	MHz
MEDIA_MIPI_TST_BYTE_CLK	200	200	MHz
ECSPI3_CLK_ROOT	80	80	MHz
PDM_CLK_ROOT	200	200	MHz
VPU_VC8000E_CLK_ROOT	400	500	MHz
SAI7_CLK_ROOT	66	66	MHz
DDR4-3200	3200	3200	MT/s
LPDDR4-4000	3200	4000	MT/s
NOC_GIC	400	500	MHz
MAIN_AXI	400	400	MHz

3.1.6 External clock sources

Each i.MX 8M Plus processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 14 shows the interface frequency requirements.

Table 14. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent.

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.

The typical values shown in Table 14 are required for use with NXP software to ensure precise time keeping and USB operation.

When connecting external input clock to OSC32K, following connections are recommended:

- 1.8 V square waveform to RTC_XTALI
- RTC_XTALO is connected to NVCC_SNVS_1P8 (1.8 V) through a 100 Kohm resistor.

i.MX 8M Plus has an integrated ring oscillator that allows the system to have an immediate clock. This clock automatically switches to OSC32K XTAL when available. Additionally, if the clock monitor determines that the OSC32K oscillation is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator of lesser frequency accuracy.

CAUTION

The internal ring oscillator is not meant to be used in customer applications, due to gross frequency variation over wafer processing, temperature, and supply voltage. These variations will cause timing issues to many different circuits that use the internal ring oscillator for reference; and, if this timing is critical, application issues will occur. To prevent application issues, it is recommended to only use an external crystal or an accurate external clock. If this recommendation is not followed, NXP cannot guarantee full compliance of any circuit using this clock.

Table 15 shows the external input clock for OSC32K.

Table 15. External input clock for OSC32K

	Symbol	Min	Typ	Max	Unit
Frequency	f	—	32.768	—	kHz
RTC_XTALI	V_{IH}	0.7 x NVCC_SNVS_1P8	—	NVCC_SNVS_1P8	V
	V_{IL}	0	—	0.3 x NVCC_SNVS_1P8	V
	I_{IH}	-12	—	12	µA
	I_{IL}	-12	—	12	µA

When connecting to 24 MHz clock, following connections are recommended:

- 1.8 V square waveform to XTALI_24M
- XTALO_24M is connected to VDD_24M_XTAL_1P8 through a 400 ohm resistor.

Table 16 shows the external input clock for 24 MHz.

Table 16. External input clock for 24 MHz

	Symbol	Min	Typ	Max	Unit
Frequency	f	—	24	—	MHz
XTALI_24M	V_{IH}	0.7 x V_{dd}	—	V_{dd} + 0.3	V
	V_{IL}	-0.3	—	0.3 x V_{dd}	V
	I_{IH}	-12	—	12	µA
	I_{IL}	-12	—	12	µA

3.1.6.1 On-chip OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator.

Table 17. 32K crystal specifications

Parameter Description	Min	Typ	Max	Unit
Frequency	—	32.768	—	kHz
Cload[1]	—	12.5	—	pF
Drive level[2]	—	—	1	μW
ESR[3]	—	70K	—	—
Rf (feedback resistor)[4]	4.7	—	—	MΩ
Rs (series resistor)[5]	0	—	1	MΩ

1 CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency. CL is given by the following formula: CL = {CL1 x CL2 / (CL1 + CL2)} + PCB strays

2 Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

3 ESR is the equivalent series resistance of the crystal.

4 Rf is the feedback resistor to bias the amplifier. A larger value of Rf is preferred at lower frequencies.

5 Rs is the series resistor to limit amplifier gain and reduce power dissipation in the crystal.

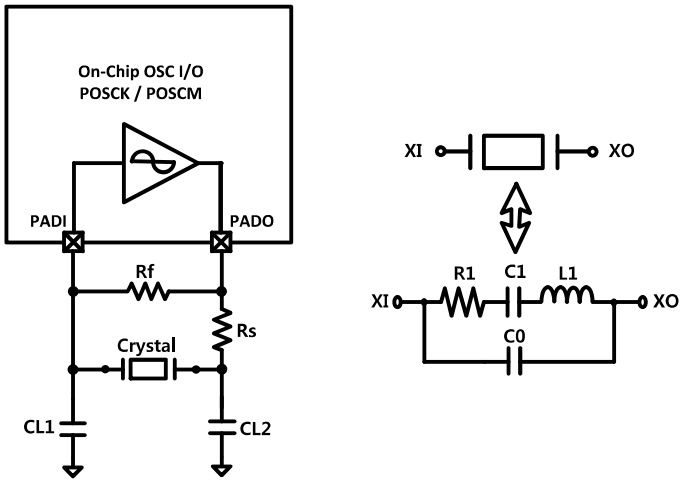


Figure 4. Crystal model and external components

3.1.6.2 On-chip OSC24M

This block implements an amplifier that when combined with a suitable 24 MHz external quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from VDD_24M_XTAL_1P8.

Table 18. 24M rystal specifications

Parameter Description	Min	Typ	Max	Unit
Frequency	—	24	—	MHz
Cload[1]	—	12	—	pF
Drive level[2]	—	—	100	μW
ESR[3]	—	60	—	—
Rf (feedback resistor)[4]	500	—	—	KΩ
Rs (series resistor)[5]	0	—	500	KΩ

1 CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency. CL is given by the following formula: CL = {CL1 x CL2 / (CL1 + CL2)} + PCB strays

2 Actual working drive level is depend on real design. Please contact crystal vendor for selecting drive level of crystal.

3 ESR is the equivalent series resistance of the crystal.

4 Rf is the feedback resistor to bias the amplifier. A larger value of Rf is preferred at lower frequencies.

5 Rs is the series resistor to limit amplifier gain and reduce power dissipation in the crystal.

3.1.7 Estimated power supply maximum currents

Power consumption is highly dependent on the application. The table below represents the estimated maximum current on the power supply rails and should be used as a guideline for power supply selection. The data below is based on a combination of design simulation and characterization data based on typical datasheet voltages. Actual power consumption for typical use cases are lower than values presented on the table below.

Table 19. Estimated power supply maximum currents (Sheet 1 of 2)

Power rail	Max current	Unit
VDD_ARM	2200	mA
VDD_SOC	5000	mA
Misc_0P8[1]	330	mA
Misc_1P8[1]	300	mA
VDD_USB_3P3	56	mA
NVCC_SNVS_1P8	2	mA
DRAM_VREF	50	μA

Table 19. Estimated power supply maximum currents (continued) (Sheet 2 of 2)

Power rail	Max current	Unit
NVCC_<XXX>	I_{max} = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.	
NVCC_DRAM		

[1] See Table 20, "Group name"

Table 20. Group name

Misc_0P8	VDD_ANA1_0P8 VDD_ARM_PLL_0P8 VDD_DRAM_0P8 VDD_HDMI_0P8 VDD_MIPI_0P8 VDD_PCI_0P8 VDD_SAI_PLL_0P8 VDD_USB_0P8
Misc_1P8	VDD_24M_XTAL_1P8 VDD_ANA0_1P8 VDD_ANA1_1P8 VDD_ANA2_1P8 VDD_ARM_PLL_1P8 VDD_AVPLL_1P8 VDD_DRAM_PLL_1P8 VDD_EARC_1P8 VDD_HDMI_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_PCI_1P8 VDD_SAI_PLL_1P8 VDD_USB_1P8

3.1.8 Power modes

The i.MX 8M Plus supports the following power modes:

- RUN Mode: All external power rails are on, CPU is active and running; other internal modules can be on/off based on application.
- IDLE Mode: When there is no thread running and all high-speed devices are not active, the CPU can automatically enter this mode. The CPU can be in the power-gated state but with L2 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated but still remains powered. The M7 core can remain running. Compared with RUN mode, all the external power rails from the PMIC remain the same, and most of the modules still remain in their state.

- SUSPEND Mode: The most efficient power saving mode where all the clocks are off and all the unnecessary power supplies are off.
- SNVS Mode: This mode is also called RTC mode. Only the power for the SNVS domain remains on to keep RTC and SNVS logic alive.
- OFF Mode: All power rails are off.

Table 21. Chip power in different LP mode

Mode	Supply	Typ.[1]	Unit
SUSPEND	VDD_SOC	13.40	mW
	NVCC_DRAM	2.20	
	NVCC_SNVS_1P8	0.30	
	PVCC	0.70	
	NVCC	0.70	
	VDD_ANA_0P8	1.90	
	VDD_ANA_1P8	1.30	
	Total[2]	19.20	

1 All the power numbers defined in the table are based on typical silicon at 25°C. Use case dependent

2 Sum of the listed supply rails.

Table 22 summarizes the external power supply states in all the power modes.

Table 22. The power supply states

Power rail	OFF	SNVS	SUSPEND	IDLE	RUN
VDD_ARM	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
Misc_1P8[1]	OFF	OFF	ON	ON	ON
Misc_0P8[1]	OFF	OFF	ON	ON	ON
VDD_DRAM_PLL_1P8 VDD_DRAM_PLL_0P8	OFF	OFF	ON	ON	ON
NVCC_SNVS	OFF	ON	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
NVCC_DRAM	OFF	OFF	ON	ON	ON
DRAM_VREF	OFF	OFF	OFF	ON	ON

1 See Table 20, "Group name"

3.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

3.2.1 Power-up sequence

Figure 5 illustrates the power-up sequence of i.MX 8M Plus processor.

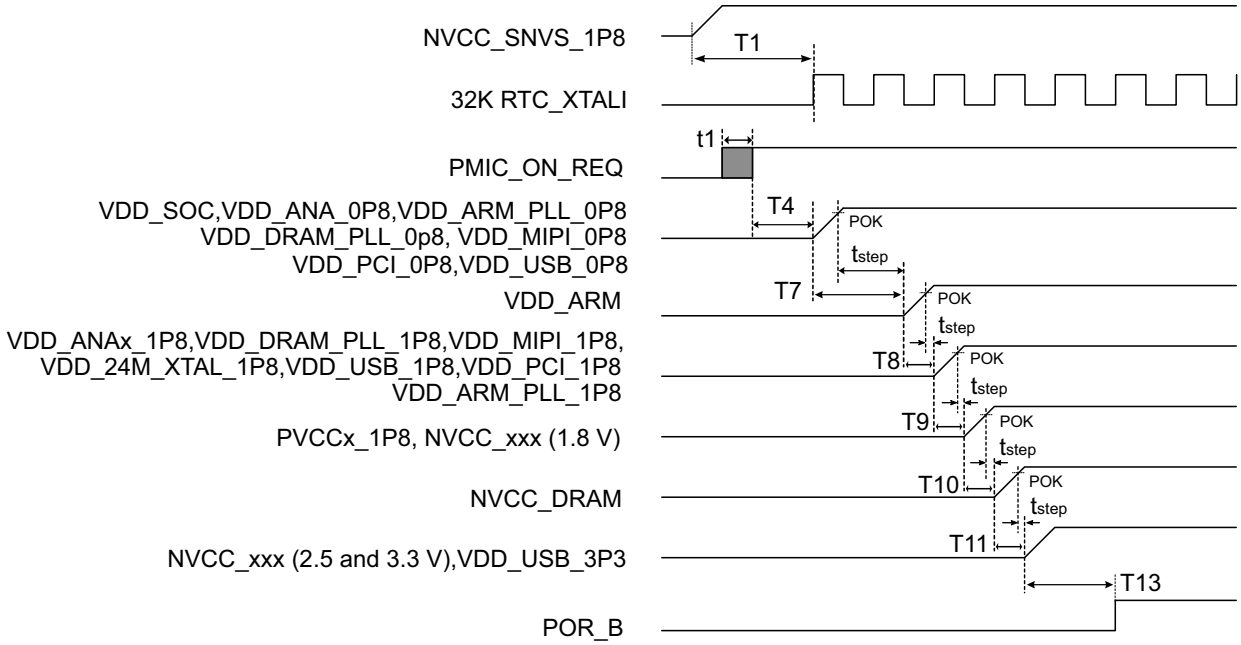


Figure 5. The power-up sequence

Table 23 represents the timing parameters of the power-up sequence.

Table 23. Power-up sequence

	Description	Min	Typ	Max	Unit
T1	Delay from NVCC_SNVS_1P8 to stable 32K existed	0	2	—	ms
T4	Delay from PMIC_ON_REQ assert to VDD_SOC and analog 0.8 V on	0	20	—	ms
T7	Delay from VDD_SOC and analog 0.8 V assert to VDD_ARM on	0	—	—	ms
T8	Delay from VDD_ARM assert to analog 1.8 V on	1	—	—	ms
T9	Delay from analog 1.8 V assert to digital 1.8 V on	0	—	—	ms
T10	Delay from digital 1.8 V assert to NVCC_DRAM on	1	—	—	ms
T11	Delay from NVCC_DRAM assert to digital 2.5 V and 3.3 V on	0	—	—	ms
T13	Delay from digital 2.5 V and 3.3 V assert to POR_B de-assert	0	20	—	ms
t_{step}	Typical delay from POK[1] of one supply to start of next supply	—	2	—	
t1	Uncertain period before PMIC_ON_REQ assert during NVCC_SNVS_1P8 ramp up.				
	For ramp up requirement, only VDD_ANA0_1P8 has 5 μs minimum requirement, others do not have such requirement. During power-up, make sure NVCC_xxx - PVCCx_1P8 < 2 V.				

1 Power good at 85% of typical value

3.2.2 Power-down sequence

Figure 6 illustrates the power-down sequence of i.MX 8M Plus processor.

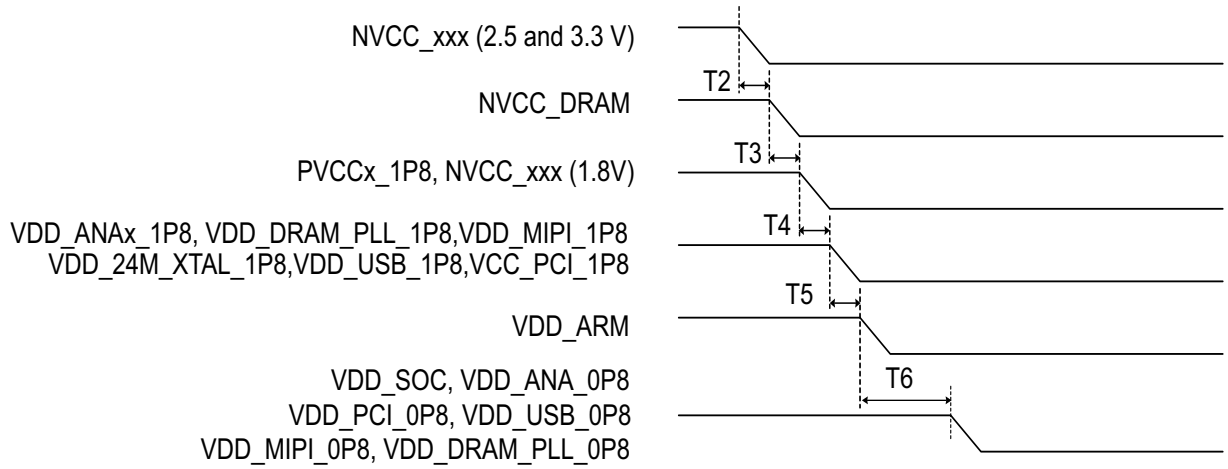


Figure 6. The power-down sequence

Table 24 represents the timing parameters of the power-down sequence.

Table 24. Power-down sequence

	Description	Min	Typ	Max	Unit
T2	Delay from digital 2.5 V and 3.3 V off to NVCC_DRAM off	0	8	—	ms
T3	Delay from NVCC_DRAM off to digital 1.8 V off	0	8	—	ms
T4	Delay from digital 1.8 V off to analog 1.8 V off	0	8	—	ms
T5	Delay from analog 1.8 V off to VDD_ARM off	0	8	—	ms
T6	Delay from VDD_ARM off to VDD_SOC off	0	8	—	ms
	During power-down, make sure NVCC_xxx - PVCCx_1P8 < 2 V.				

3.3 PLL electrical characteristics

Table 25. PLL electrical parameters

PLL type	Parameter	Value
AUDIO_PLL1	Clock output range	650 MHz — 1.3 GHz
	Reference clock	24 MHz
	Lock time	50 μs
	Jitter	±1% of output period, ≥ 50 ps
AUDIO_PLL2	Clock output range	650 MHz — 1.3 GHz
	Reference clock	24 MHz
	Lock time	50 μs
	Jitter	±1% of output period, ≥ 50 ps
VIDEO_PLL1	Clock output range	650 MHz — 1190 MHz
	Reference clock	24 MHz
	Lock time	50 μs
AV_PLL	Clock output range	552 MHz — 1368 MHz
	Reference clock	24 MHz
	Lock time	70 μs
SAI_PLL	Clock output range	25 MHz — 100 MHz
	Reference clock	24 MHz
	Lock time	50 μs
HSIO_PLL	Clock output range	100 MHz
	Reference clock	24 MHz
	Lock time	20 μs

Table 25. PLL electrical parameters (continued)

PLL type	Parameter	Value
SYS_PLL1	Clock output range	800 MHz
	Reference clock	24 MHz
	Lock time	70 μs
SYS_PLL2	Clock output range	1 GHz
	Reference clock	24 MHz
	Lock time	70 μs
SYS_PLL3	Clock output range	600 MHz — 1 GHz
	Reference clock	24 MHz
	Lock time	70 μs
ARM_PLL	Clock output range	800 MHz —1800 MHz
	Reference clock	24 MHz
	Lock time	70 μs
DRAM_PLL1	Clock output range	400 MHz — 1067 MHz
	Reference clock	24 MHz
	Lock time	50 μs
GPU_PLL	Clock output range	800 MHz —1000 MHz
	Reference clock	24 MHz
	Lock time	70 μs
VPU_PLL	Clock output range	400 MHz — 800 MHz
	Reference clock	24 MHz
	Lock time	70 μs

3.4 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR4 and DDR4 modes
- LVDS I/O

3.4.1 General purpose I/O (GPIO) DC parameters

Table 26 shows DC parameters for GPIO pads. The parameters in Table 26 are guaranteed per the operating ranges in Table 12, unless otherwise noted.

Table 26. GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	$V_{OH\ (1.8\ V)}$	I_{OH} = 1.6/3.2/6.4/9.6 mA (1.8 V) I_{OH} = 2/4/8/12 mA (3.3 V)	0.8 x V_{DD}	—	V_{DD}	V
	$V_{OH\ (3.3\ V)}$		0.8 x V_{DD}	—	V_{DD}	V
Low-level output voltage	$V_{OL\ (1.8\ V)}$	I_{OL} = 1.6/3.2/6.4/9.6 mA (1.8 V) I_{OL} = 2/4/8/12 mA (3.3 V)	0	—	0.2 x V_{DD}	V
	$V_{OL\ (3.3\ V)}$		0	—	0.2 x V_{DD}	V
High-level input voltage	V_{IH}	—	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}	—	-0.3	—	0.3 x V_{DD}	V
Pull-up resistor	—	V_{DD} = 1.65 - 1.95V Temp = 0 - 95 °C	12	22	49	KΩ
Pull-down resistor	—		13	23	48	KΩ
Pull-up resistor	—	V_{DD} = 3.0 - 3.6V Temp = 0 - 95 °C	18	37	72	KΩ
Pull-down resistor	—		24	43	87	KΩ
High level input current	IIH	—	-4	—	4	μA
Low level input current	IIL	—	-0.7	—	0.7	μA

Table 27. Additional leakage parameters

Parameter	Symbol	Pins	Min	Max	Unit
High level input current	IIH	USBx_Dx	-30	30	μA
		MIPI_CSI	-4	4	
		ONOFF, POR_B	-1	1	
Low level input current	IIL	USBx_Dx	-6	6	μA
		MIPI_CSI, ONOFF, POR_B	-0.7	0.7	

3.4.2 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR 4 and DDR4 operational modes. The DDR Memory Controller (DDRMC) is compliant with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 8M Plus application processor.

3.4.3 LVDS I/O DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

Table 28 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 28. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V_{OD}	Rload = 100 Ω between padP and pad N	250	450	mV
Output High Voltage	V_{OH}	I_{OH} = 0 mA	1.25	1.6	V
Output Low Voltage	V_{OL}	I_{OL} = 0 mA	0.9	1.25	V
Offset Voltage	V_{OS}	—	1.125	1.375	V

3.5 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR4 and DDR4 modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 7 and Figure 8.

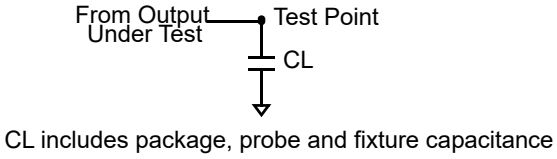


Figure 7. Load circuit for output

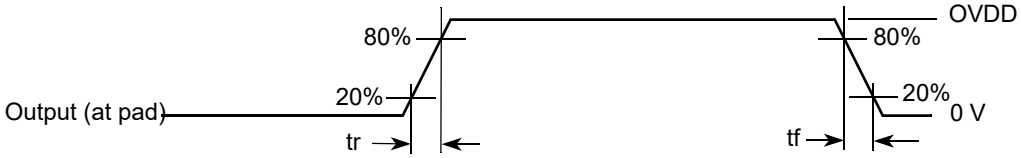


Figure 8. Output transition time waveform

3.5.1 General purpose I/O AC parameters

This section presents the I/O AC parameters for GPIO in different modes. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. Maximum frequency of operation for input

Maximum frequency (MHz)	
VDD = 1.8 V, CL = 50 pF	**VDD = 3.3 V, CL = 50 pF**
450	440

Table 30. Maximum frequency of operation for output

Parameter			Maximum Frequency (MHz)			
			VDD = 1.8 V		VDD = 3.3 V	
dse[2:0]	sre[1:0]	Driver type	CL = 10 pF	CL = 20 pF	CL = 10 pF	CL = 20 pF
00X	0X	1x Slow Slew	150	80	120	65
00X	1X	1x Fast Slew	150	80	120	65
10X	0X	2x Slow Slew	160	90	150	80
10X	1X	2x Fast Slew	160	90	150	80
01X	0X	4x Slow Slew	200	100	180	90
01X	1X	4x Fast Slew	200	100	180	90
11X	0X	6x Slow Slew	250	130	200	100
11X	1X	6x Fast Slew	250	130	200	100

3.5.2 DDR I/O AC electrical characteristics

The DDR I/O pads support LPDDR 4 and DDR4 operational modes. The DDR Memory Controller (DDRMC) is compliant with JEDEC-compliant SDRAMs.

DDRMC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 8M Plus application processor.

3.5.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 9.

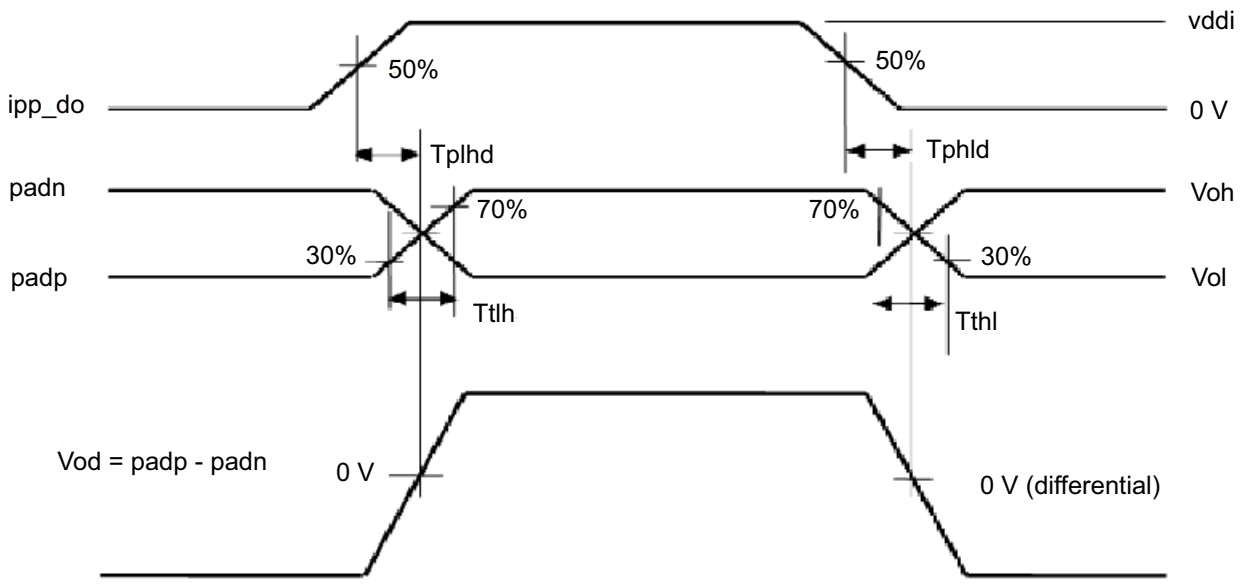


Figure 9. Output transition time waveform

Table 31 shows the AC parameters for (LVDS) I/O.

Table 31. LVDS I/O AC parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω Cload = 2 pF	—	—	0.25	ns
Transition Low to High time[2]	t_{TLH}		—	—	0.5	
Transition High to Low time	t_{THL}		—	—	0.5	
Operating frequency	f	—	—	600	800	MHz
Offset voltage imbalance	V_{os}	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} – t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20–80% from output voltage.

3.6 Output buffer impedance parameters

This section defines the I/O impedance parameters of the i.MX 8M Plus family of processors for the following I/O types:

- Differential I/O (CCM_CLK1)
- Double Data Rate I/O (DDR) for LPDDR4 and DDR4 modes

NOTE

DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 10).

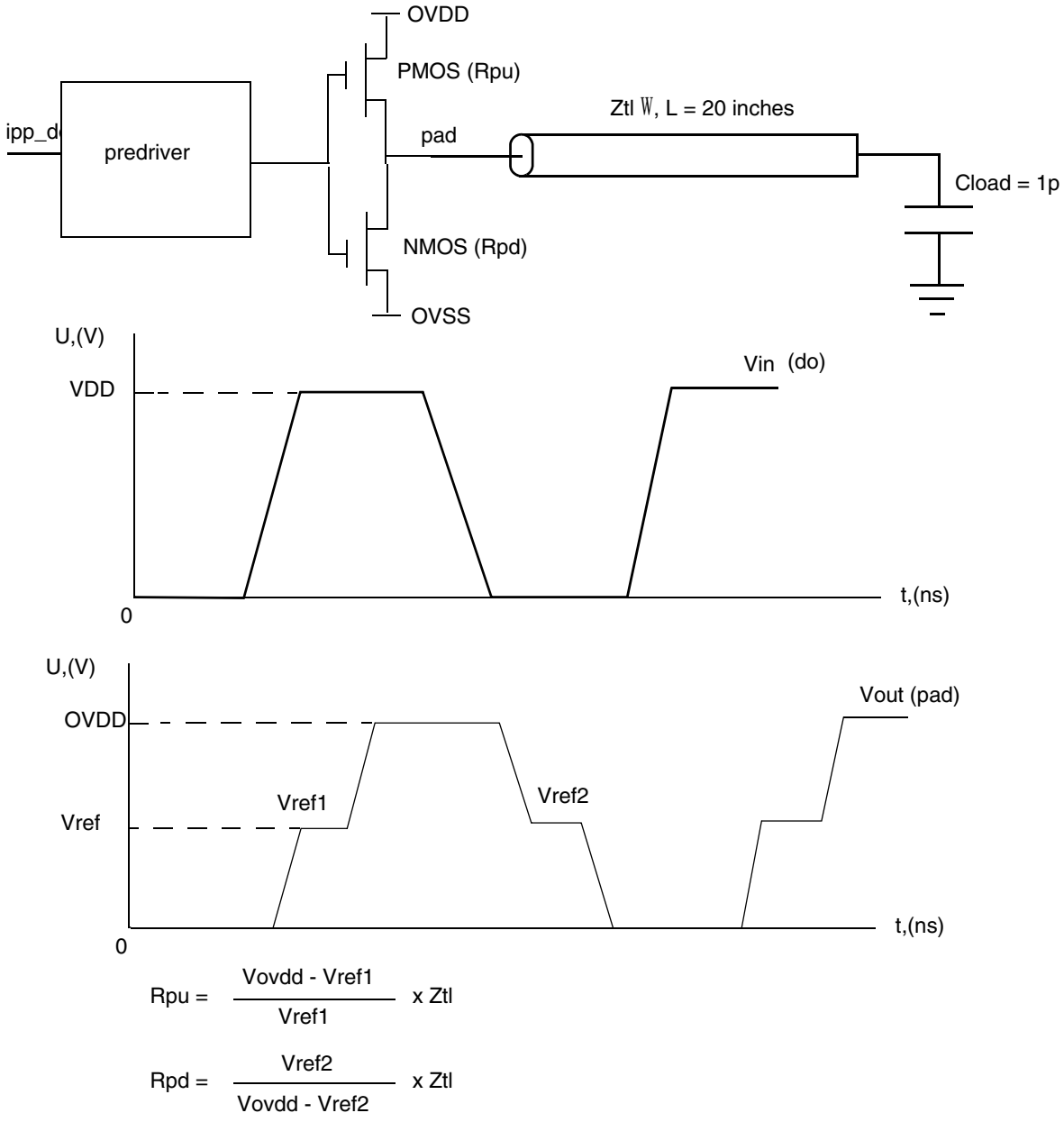


Figure 10. Impedance matching load for measurement

3.6.1 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001) for details.

3.6.2 DDR I/O output buffer impedance

Table 32 shows DDR I/O output buffer impedance of i.MX 8M Plus family of processors.

Table 32. DDR I/O output buffer impedance

Parameter	Symbol	Test Conditions DSE (Drive Strength)	Typical		Note	Unit
			NVCC_DRAM = 1.2 V (DDR4)	NVCC_DRAM = 1.1 V (LPDDR4)		
Output Driver Impedance[1, 2, 3]	Rdrv	000000	Hi-Z	Hi-Z	—	Ω
		000001	480	480	—	
		000010	240	240	—	
		000011	160	160	—	
		001000	120	120	—	
		001001	96	96	—	
		001010	80	80	—	
		001011	68	68	—	
		011000	60	60	[4]	
		011001	53	53	[4]	
		011010	48	48	—	
		011011	43	43	—	
		111000	40	40	[4]	
		111001	36	36	—	
		111010	34	34	[4]	
		111011	32	32	—	
		111110	30	30	—	
		111111	28	28	[4]	

1 Output driver impedance is controlled across PVTs using ZQ calibration procedure.

2 Calibration is done against 240 Ω external reference resistor.

3 Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4 Output driver impedance values are included in the IBIS model.

3.7 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 8M Plus processor.

3.7.1 Reset timings parameters

Figure 11 shows the reset timing and Table 33 lists the timing parameters.

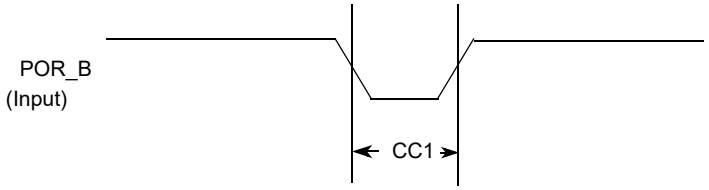


Figure 11. Reset timing diagram

Table 33. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid. **Note:** POR_B rise/fall times must be 5 ns or less.	1	—	RTC_XTALI cycle

3.7.2 WDOG Reset timing parameters

Figure 12 shows the WDOG reset timing and Table 34 lists the timing parameters.

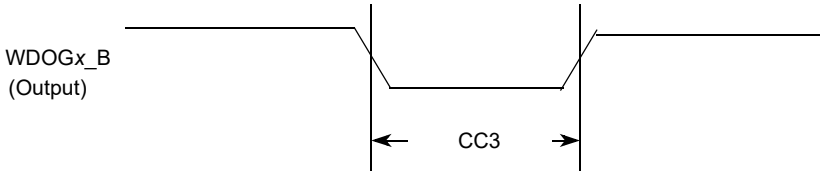


Figure 12. WDOG*x*_B timing diagram

Table 34. WDOG*x*_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μs.

NOTE

WDOG*x*_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM) for detailed information.

3.7.3 DDR SDRAM–specific parameters (LPDDR4 and DDR4)

The i.MX 8M Plus Family of processors have been designed and tested to work with JEDEC JESD209-4A–compliant LPDDR4 memory and JESD79-4A compliant DDR4 memory. Timing diagrams

and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation; PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-8-processors:IMX8-SERIES .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 35. i.MX 8M Plus DRAM controller supported SDRAM configurations

Parameter	LPDDR4	DDR4
Number of Controllers	1	1
Number of Channels	2	N/A
Number of Chip Selects	2	1
Bus Width	32 bit	32 bit
Maximum Clock Frequency	4000 MT/s	3200 MT/s

3.7.3.1 Clock/data/command/address pin allocations

These processors uses generic names for clock, data, and command address bus (DCF—DRAM controller functions); see Table 79 for details about mapping of clock, data, and command address signals of LPDDR4 and DDR4 modes.

3.8 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

3.8.1 ECSPI timing parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

3.8.1.1 ECSPI Master mode timing

Figure 13 depicts the timing of ECSPI in master mode. Table 36 lists the ECSPI master mode timing characteristics.

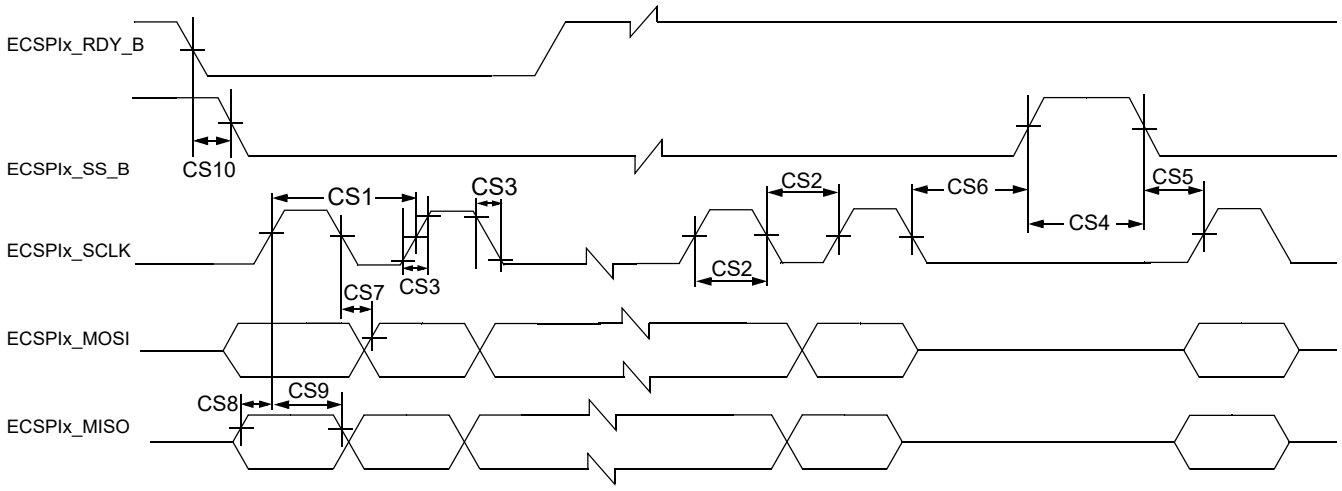


Figure 13. ECSPI Master mode timing diagram

Table 36. ECSPI Master mode timing parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	See Table 37	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	21.5 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	Half ECSPIx_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-1	1	ns
CS8	ECSPIx_MISO Setup Time	t_{Smiso}	1.23	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	3.09	—	ns
CS10	RDY to ECSPIx_SS_B Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 3.5, I/O AC parameters.

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

Table 37 lists the ECSPI Read and Write frequency.

Table 37. ECSPI Master Read and Write frequency

Instance	Mux mode	Master Read frequency	Master Write frequency	Unit
ECSPI1	Mux behind I2C1/I2C2	25	50	MHz
	Mux behind ECSPI1	30	60	MHz
ECSPI2	Mux behind SD2	30	60	MHz
	Mux behind ECSPI2	25	50	MHz
	Mux behind I2C3/I2C4	20	40	MHz
ECSPI3	Mux behind UART1/UART2	25	50	MHz

3.8.1.2 ECSPI Slave mode timing

Figure 14 depicts the timing of ECSPI in Slave mode. Table 38 lists the ECSPI Slave mode timing characteristics.

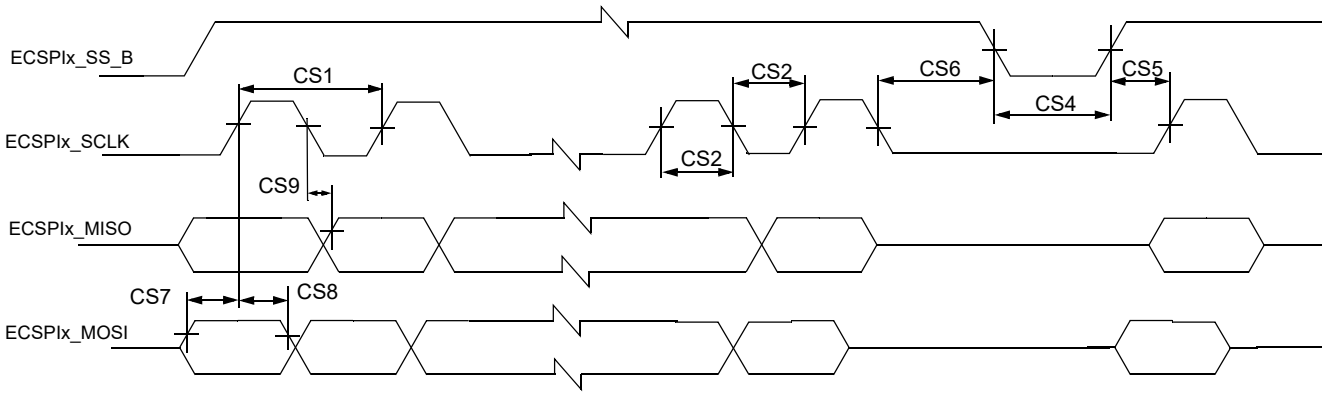


Figure 14. ECSPI Slave mode timing diagram

Table 38. ECSPI Slave mode timing parameters (Sheet 1 of 2)

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns

Table 38. ECSPI Slave mode timing parameters (continued) (Sheet 2 of 2)

ID	Parameter	Symbol	Min	Max	Unit
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

3.8.2 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC5.1 (single data rate) timing, eMMC5.1/SD3.0 (dual data rate) timing and SDR50/SDR104 AC timing.

3.8.2.1 SD3.0/eMMC5.1 (single data rate) AC timing

Figure 15 depicts the timing of SD3.0/eMMC5.1, and Table 39 lists the SD3.0/eMMC5.1 timing characteristics.

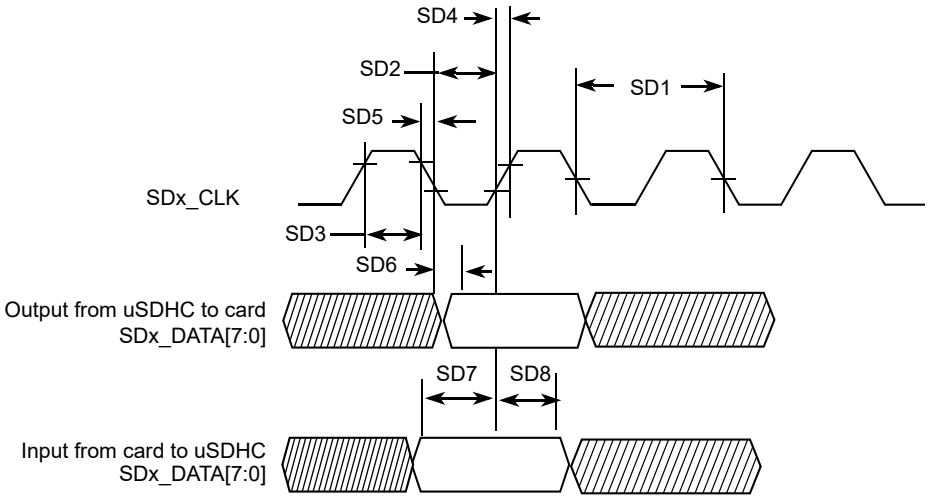


Figure 15. SD3.0/eMMC5.1 (SDR) timing

Table 39. SD3.0/eMMC5.1 (SDR) interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns

Table 39. SD3.0/eMMC5.1 (SDR) interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0 — 25 MHz. In High-speed mode, clock frequency can be any value between 0 — 50 MHz.

3 In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0 — 20 MHz. In High-speed mode, clock frequency can be any value between 0 — 52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

3.8.2.2 eMMC5.1/SD3.0 (dual data rate) AC timing

Figure 16 depicts the timing of eMMC5.1/SD3.0 (DDR). Table 40 lists the eMMC5.1/SD3.0 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

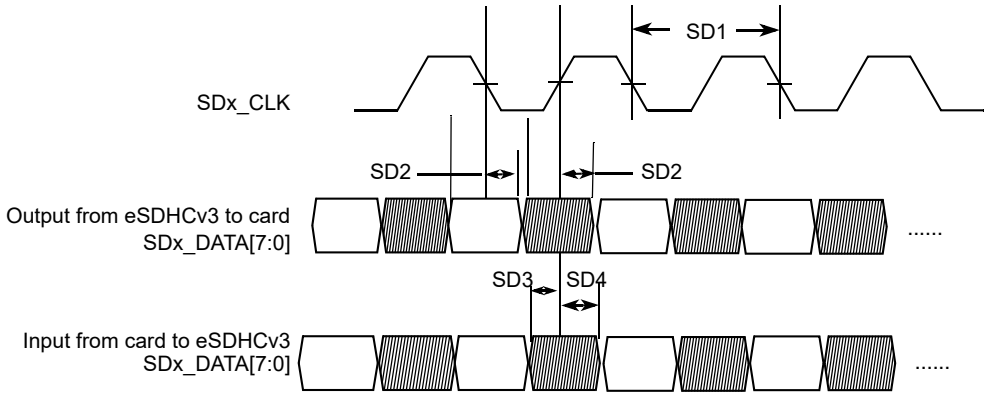


Figure 16. eMMC5.1/SD3.0 (DDR) timing

Table 40. eMMC5.1/SD3.0 (DDR) interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz

Table 40. eMMC5.1/SD3.0 (DDR) interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.7	6.9	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.3	—	ns

3.8.2.3 HS400 DDR AC timing

Figure 17 depicts the timing of HS400 mode, and Table 41 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 43 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

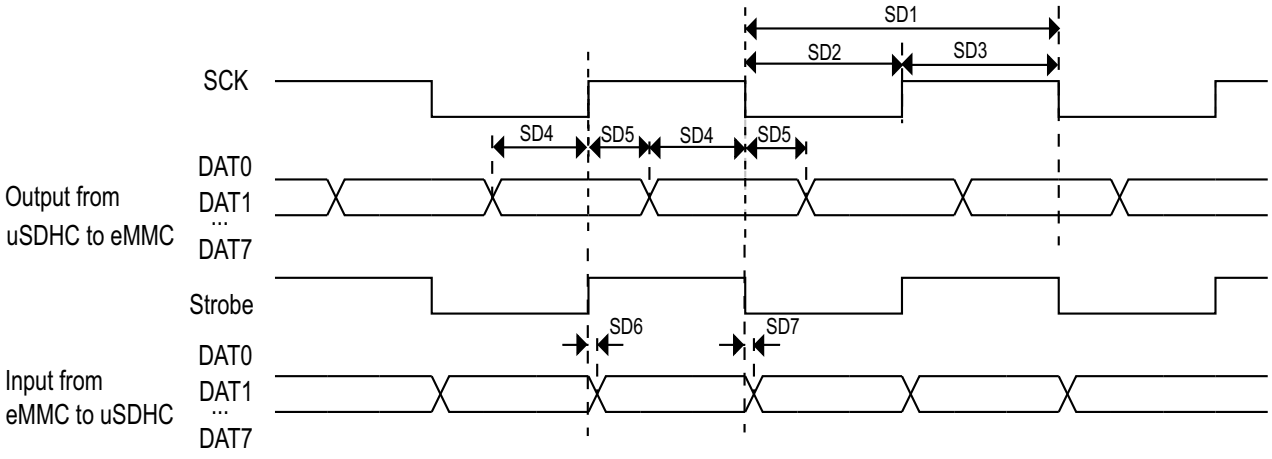


Figure 17. HS400 timing

Table 41. HS400 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	200	MHz
SD2	Clock low time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock high time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					

Table 41. HS400 interface timing specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD4	Output skew from data of edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output skew from edge of SCk to data	t_{OSkew2}	0.45	—	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

3.8.2.4 HS200 Mode AC timing

Figure 18 depicts the timing of HS200 mode, and Table 42 lists the HS200 timing characteristics.

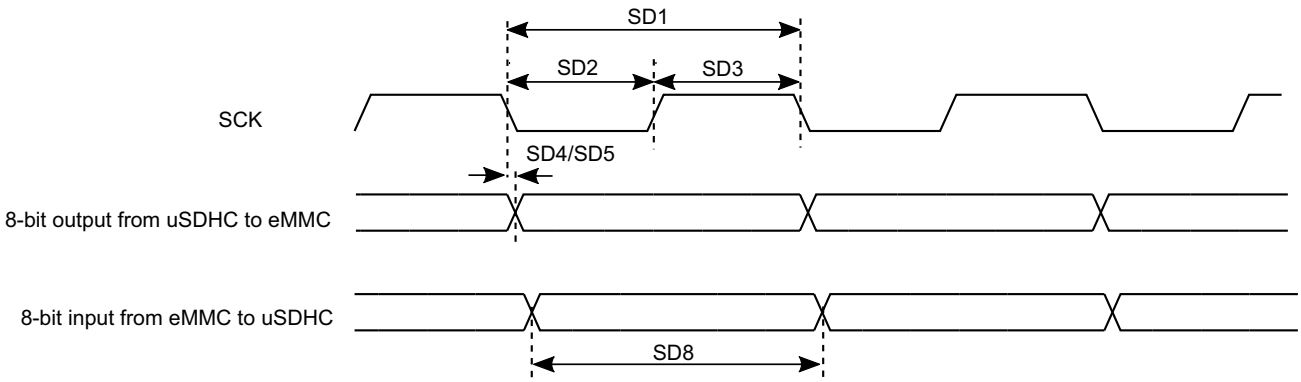


Figure 18. HS200 timing

Table 42. HS200 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.3 x t_{CLK}	0.7 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.3 x t_{CLK}	0.7 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1] HS200 is for 8 bits while SDR104 is for 4 bits.

3.8.2.5 SDR50/SDR104 AC timing

Figure 19 depicts the timing of SDR50/SDR104, and Table 43 lists the SDR50/SDR104 timing characteristics.

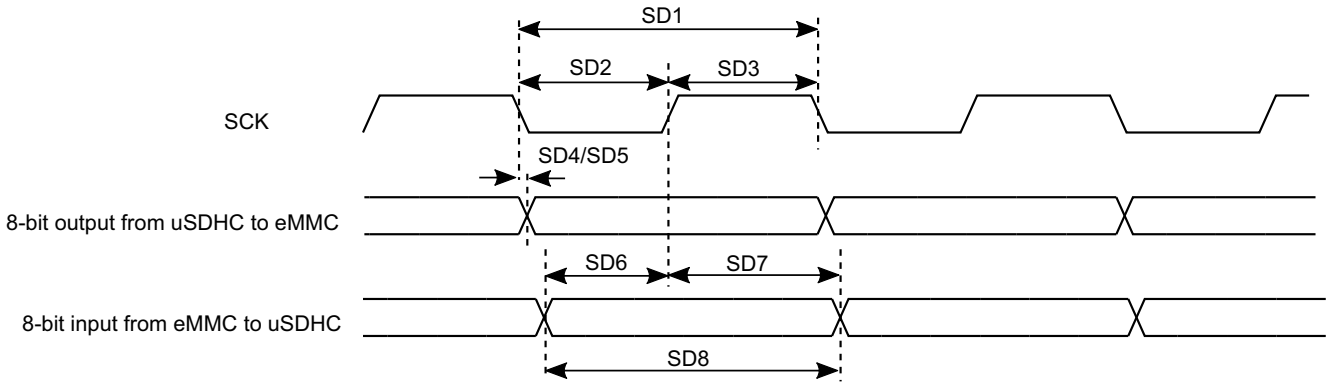


Figure 19. SDR50/SDR104 timing

Table 43. SDR50/SDR104 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 x t_{CLK}	0.54 x t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.4	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	uSDHC Output Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

[1] Data window in SDR100 mode is variable.

3.8.2.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.5/5.0/5.1 can be 1.8 V or 3.3 V depending on the working mode. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in Table 26, "GPIO DC parameters," on page 38.

3.8.3 Ethernet controller (ENET) AC electrical specifications

Ethernet supports the following key features:

- Support ENET AVB
- Support IEEE 1588
- Support Energy Efficient Ethernet (EEE)
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation

The following sections introduce the ENET AC electrical specifications.

3.8.3.1 ENET1 signal mapping

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 44. ENET1 signal mapping (Sheet 1 of 2)

Pad name	Description	Mode	Alt mode	Direction	Comments
GPIO1_IO00	ENET_PHY_REF_CLK_ROOT	RGMII	ALT1	O	Reference clock for PHY.
SAI1_RXFS	enet1.1588_EVENT0_IN	RMII/RGMII	ALT4	I	Capture/compare block input/output event bus signal. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software. When configured for compare, the corresponding signal 1588_EVENT is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn. An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TSCRn[TDRE] is set.
SAI1_RXC	enet1.1588_EVENT0_OUT	RMII/RGMII	ALT4	O	—
SAI1_RXD0	enet1.1588_EVENT1_IN	RMII/RGMII	ALT4	I	—
SAI1_RXD1	enet1.1588_EVENT1_OUT	RMII/RGMII	ALT4	O	—
SAI1_RXD2	enet1.MDC	RMII/RGMII	ALT4	O	—
SAI1_RXD3	enet1.MDIO	RMII/RGMII	ALT4	I/O	—
SAI1_RXD4	enet1.RGMII_RD0	RMII/RGMII	ALT4	I	—
SAI1_RXD5	enet1.RGMII_RD1	RMII/RGMII	ALT4	I	—
SAI1_RXD6	enet1.RGMII_RD2	RGMII	ALT4	I	Only used for RGMII
SAI1_RXD7	enet1.RGMII_RD3	RGMII	ALT4	I	Only used for RGMII

Table 44. ENET1 signal mapping (continued) (Sheet 2 of 2)

Pad name	Description	Mode	Alt mode	Direction	Comments
SAI1_TXFS	RMII.RX_EN (CRS_DV); enet1.RGMII_RX_CTL	RMII/RGMII	ALT4	I	—
SAI1_TXC	enet1.RGMII_RXC	RGMII	ALT4	I	—
SAI1_TXD0	enet1.RGMII_TD0	RMII/RGMII	ALT4	O	—
SAI1_TXD1	enet1.RGMII_TD1	RMII/RGMII	ALT4	O	—
SAI1_TXD2	enet1.RGMII_TD2	RGMII	ALT4	O	Only used for RGMII
SAI1_TXD3	enet1.RGMII_TD3	RGMII	ALT4	O	Only used for RGMII
SAI1_TXD4	RMII.TX_EN; enet1.RGMII_TX_CTL	RMII/RGMII	ALT4	O	For RMII—SAI1_TXD4 works as RMII.TX_EN. For RGMII—SAI1_TXD4 works as enet1.RGMII_TX_CTL.
SAI1_TXD5	enet1.RGMII_TXC	RGMII	ALT4	O	—
SAI1_TXD6	enet1.RX_ER	RMII	ALT4	I	—
SAI1_TXD7	enet1.TX_ER	RMII	ALT4	O	—
SAI1_MCLK	enet1.RMII_CLK	RMII	ALT4	I/O	Used as RMII clock, there are two RMII clock schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock.
SD1_CLK	enet1.MDC	RMII	ALT1	O	—
SD1_CMD	enet1.MDIO	RMII	ALT1	I/O	—
SD1_DATA0	enet1.RGMII_TD1	RMII	ALT1	O	—
SD1_DATA1	enet1.RGMII_TD0	RMII	ALT1	O	—
SD1_DATA2	enet1.RGMII_RD0	RMII	ALT1	I	—
SD1_DATA3	enet1.RGMII_RD1	RMII	ALT1	I	—
SD1_DATA4	RMII.TX_EN	RMII	ALT1	O	—
SD1_DATA5	enet1.TX_ER	RMII	ALT1	O	—
SD1_DATA6	RMII.RX_EN (CRS_DV)	RMII	ALT1	I	—
SD1_DATA7	enet1.RX_ER	RMII	ALT1	I	—
SD1_RESET_B	enet1.RMII_CLK	RMII	ALT1	I/O	Used as RMII clock, there are two RMII clock schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock

3.8.3.2 RMII mode timing

In RMII mode, enet1.RMII_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock.

Figure 20 shows RMII mode timings. Table 45 describes the timing parameters (M16–M21) shown in the figure.

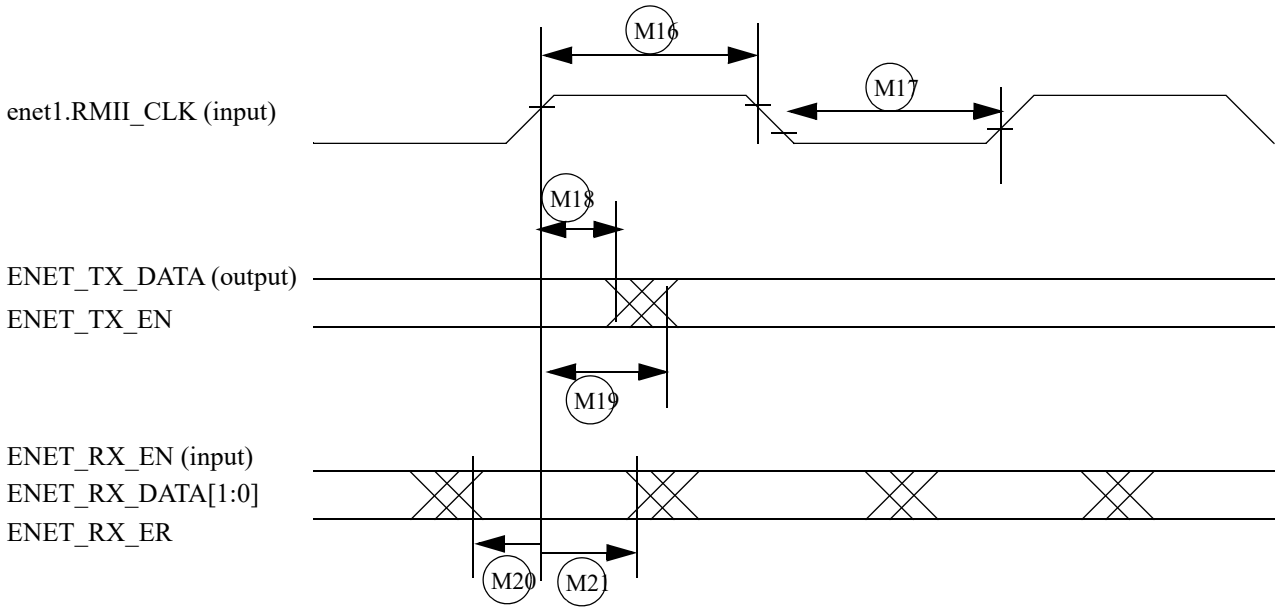


Figure 20. RMII mode signal timing diagram

Table 45. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

3.8.3.3 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 46. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

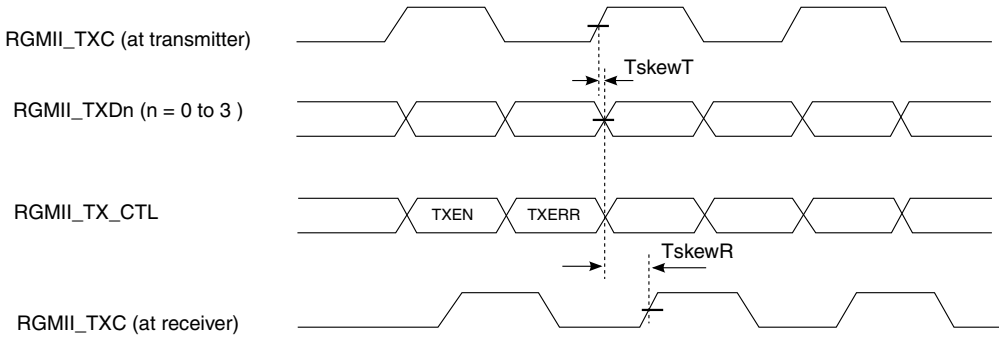


Figure 21. RGMII transmit signal timing diagram original

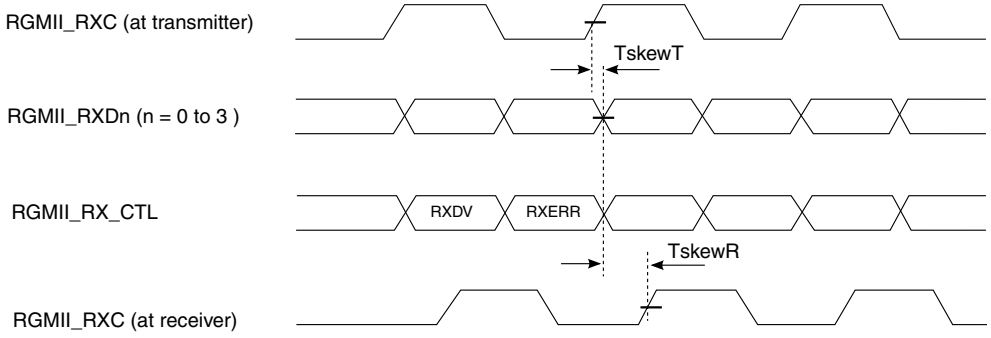


Figure 22. RGMII receive signal timing diagram original

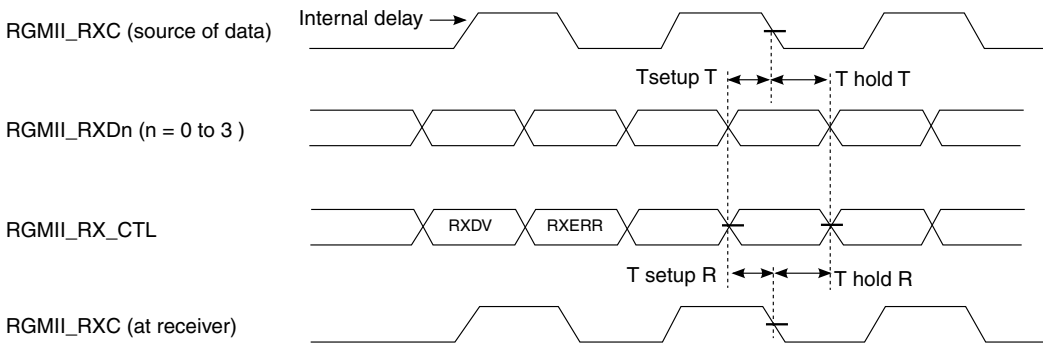


Figure 23. RGMII receive signal timing diagram with internal delay

3.8.4 Ethernet Quality-of-Service (QOS) electrical specifications

Ethernet QOS supports the following Time Sensitive Networking (TSN) features:

- 802.1Qbv Enhancements to Scheduling Traffic
- 802.1Qbu Frame preemption
- Time based Scheduling
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation

3.8.4.1 Ethernet QOS signal mapping

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 47. ENET QOS signal mapping

Pad name	Description	Mode	Alt mode	Direction	Comments
GPIO1_IO06	enet_qos.MDC	RMII/RGMII	ALT1	O	—
GPIO1_IO07	enet_qos.MDIO	RMII/RGMII	ALT1	I/O	—

Table 47. ENET QOS signal mapping (continued)

Pad name	Description	Mode	Alt mode	Direction	Comments
GPIO1_IO08	enet_qos.1588_EVENT0_IN; enet_qos.1588_EVENT0_AUX_IN	RMII/RGMII	ALT1/ALT4	I	Capture/compare block input/output event bus signal. When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software. When configured for compare, the corresponding signal 1588_EVENT is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn. An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TSCRn[TDRE] is set. ALT1 is for enet_qos.1588_EVENT1_IN. ALT4 is for enet_qos.1588_EVENT1_AUX_IN.
GPIO1_IO09	enet_qos.1588_EVENT0_OUT	RMII/RGMII	ALT1	O	—
ENET_MDC	enet_qos.MDC	RMII/RGMII	ALT0	O	—
ENET_MDIO	enet_qos.MDIO	RMII/RGMII	ALT0	I/O	—
ENET_TD3	enet_qos.RGMII_TD3	RGMII	ALT0	O	Only used for RGMII
ENET_TD2	RMII.REF_CLK; enet_qos.RGMII_TD2	RMII/RGMII	ALT1/ALT0	I/O	ALT0 is only for RGMII TD2 output, ALT1 is for RMII clock. Used as RMII clock and RGMII data, there are two RMII clock schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock.
ENET_TD1	enet_qos.RGMII_TD1	RMII/RGMII	ALT0	O	—
ENET_TD0	enet_qos.RGMII_TD0	RMII/RGMII	ALT0	O	—
ENET_TX_CTL	RMII.TX_EN; enet_qos.RGMII_TX_CTL	RMII/RGMII	ALT0	O	—

Table 47. ENET QOS signal mapping (continued)

Pad name	Description	Mode	Alt mode	Direction	Comments
ENET_TXC	enet_qos.RMII_TXER enet_qos.RGMII_ TXC;	RMII/RGMII	ALT1/ALT0	O	For RMII—ENET_TXC works as RMII.TX_ER in the ALT1 mode. For RGMII—ENET_TXC works as RGMII.TX_CLK in the ALT0 mode.
ENET_RX_CTL	RMII.RX_EN (CRS_DV); enet_qos.RGMII_RC_CTL	RMII/RGMII	ALT0	I	—
ENET_RXC	RMII_RXER; enet_qos.RGMII_RXC	RMII/RGMII	ALT1/ALT0	I	For RMII—ENET_RXC works as RMII.RX_ER in the ALT1 mode. For RGMII—ENET_RXC works as RGMII.RX_CLK in the ALT0 mode.
ENET_RD0	enet_qos.RGMII_RD0	RMII/RGMII	ALT0	I	—
ENET_RD1	enet_qos.RGMII_RD1	RMII/RGMII	ALT0	I	—
ENET_RD2	enet_qos.RGMII_RD2	RGMII	ALT0	I	Only used for RGMII.
ENET_RD3	enet_qos.RGMII_RD3	RGMII	ALT0	I	Only used for RGMII.
I2C1_SCL	enet_qos.MDC	RMII/RGMII	ALT1	O	—
I2C1_SDA	enet_qos.MDIO	RMII/RGMII	ALT1	I/O	—
I2C2_SCL	enet_qos.1588_EVENT1_IN; enet_qos.1588_EVENT1_AUX_IN	RMII/RGMII	ALT1/ALT4	I	ALT1 is for enet_qos.1588_EVENT1_IN. ALT4 is for enet_qos.1588_EVENT1_AUX_IN.
I2C2_SDA	enet_qos.1588_EVENT1_OUT	RMII/RGMII	ALT1	O	—
SAI2_MCLK	enet_qos.1588_EVENT3_IN; enet_qos.1588_EVENT3_AUX_IN	RMII/RGMII	ALT2/ALT4	I	ALT2 is for enet_qos.1588_EVENT3_IN. ALT4 is for enet_qos.1588_EVENT3_AUX_IN.
SAI2_RXD0	enet_qos.1588_EVENT2_OUT	RMII/RGMII	ALT2	O	—
SAI2_TXD0	enet_qos.1588_EVENT2_IN; enet_qos.1588EVENT2_AUX_IN	RMII/RGMII	ALT2/ALT4	I	ALT2 is for enet_qos.1588_EVENT2_IN. ALT4 is for enet_qos.1588_EVENT2_AUX_IN.
SAI2_TXFS	enet_qos.1588_EVENT3_OUT	RMII/RGMII	ALT2	O	—

3.8.4.2 RMII mode timing

In RMII mode, enet1.RMII_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock.

Figure 24 shows RMII mode timings. Table 48 describes the timing parameters (M16–M21) shown in the figure.

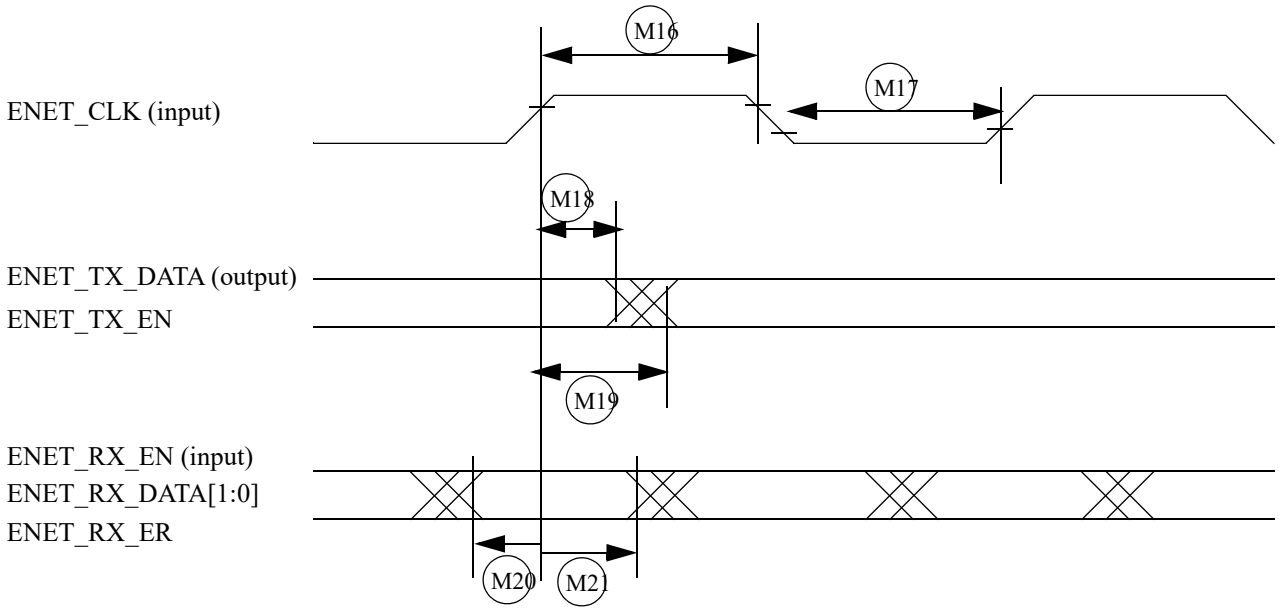


Figure 24. RMII mode signal timing diagram

Table 48. RMII signal timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid	—	15	ns
M20	ENET_RX_DATAD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RX_DATAD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

3.8.4.3 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 49. RGMII signal switching specifications[1]

Symbol	Description	Min.	Max.	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

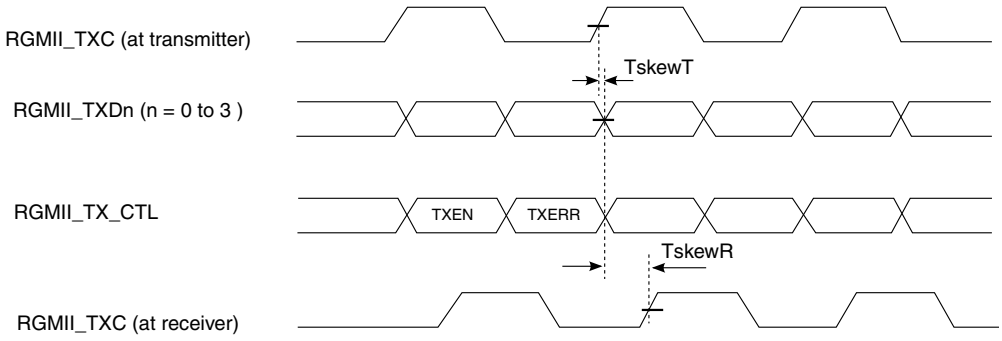


Figure 25. RGMII transmit signal timing diagram original

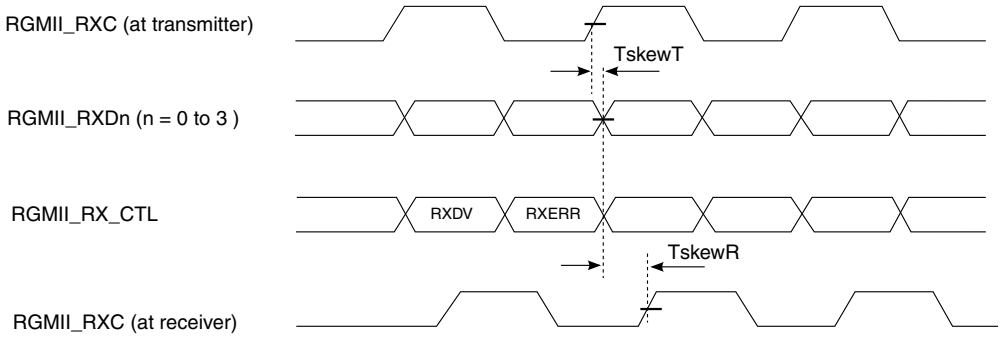


Figure 26. RGMII receive signal timing diagram original

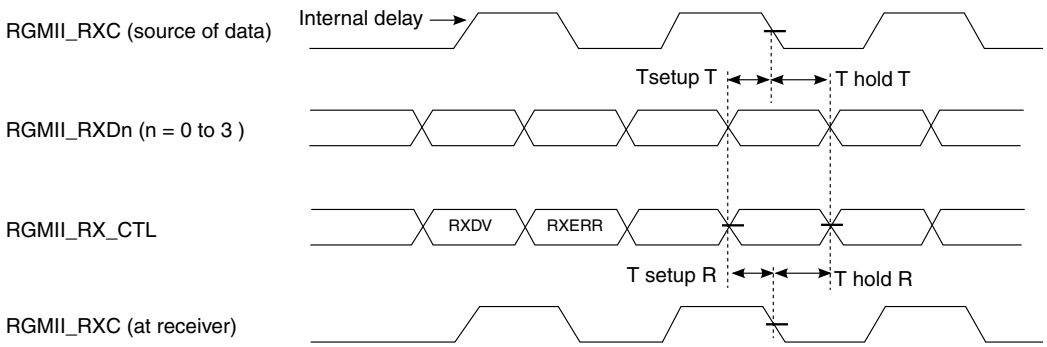


Figure 27. RGMII receive signal timing diagram with internal delay

3.8.5 General-purpose media interface (GPMI) timing

The i.MX 8M Plus GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous Timing mode, Source Synchronous Timing mode and Toggle Timing mode separately, as described in the following subsections.

3.8.5.1 Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 28 through Figure 31 depicts the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 50 describes the timing parameters (NF1–NF17) that are shown in the figures.

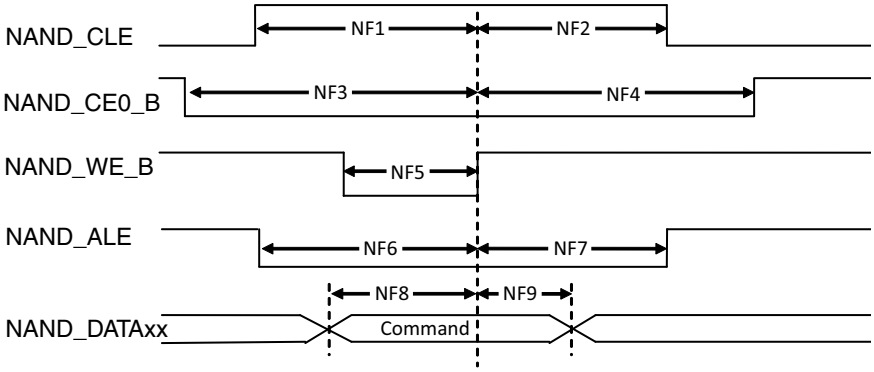


Figure 28. Command Latch cycle timing diagram

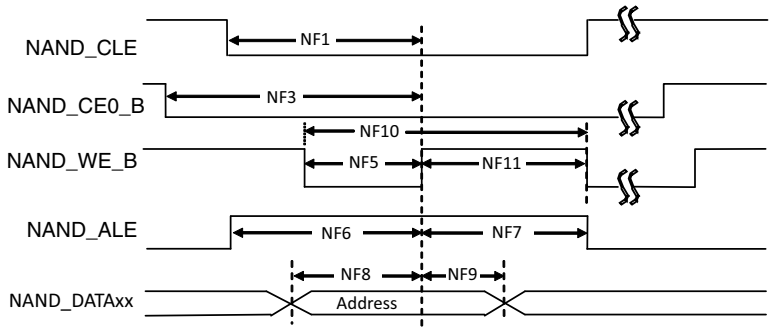


Figure 29. Address Latch cycle timing diagram

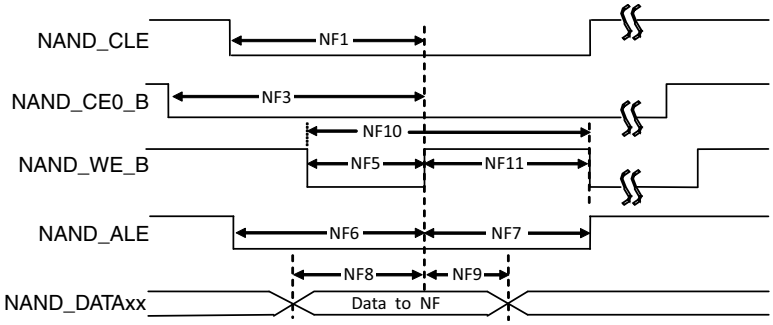


Figure 30. Write Data Latch cycle timing diagram

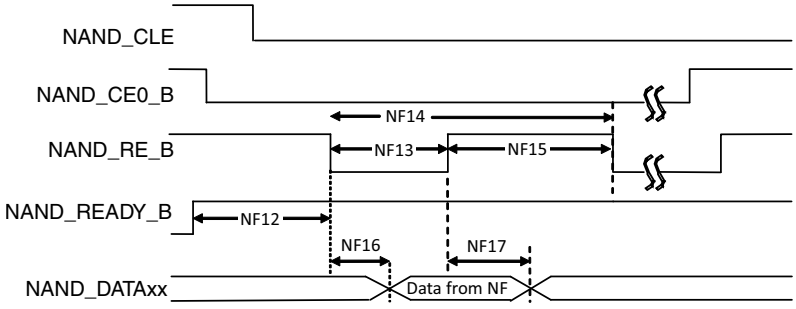


Figure 31. Read Data Latch cycle timing diagram (Non-EDO Mode)

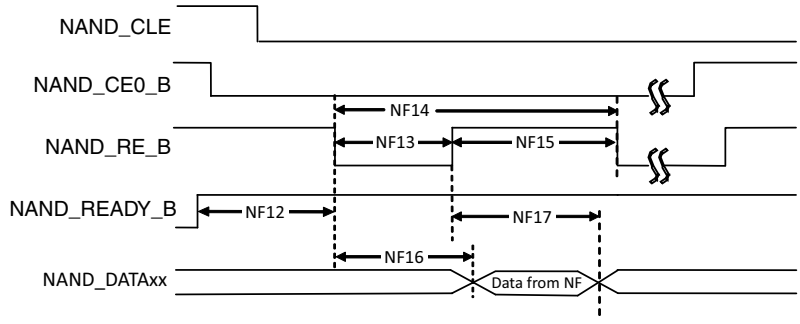


Figure 32. Read Data Latch cycle timing diagram (EDO mode)

Table 50. Asynchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see notes[2,3]]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		ns
NF3	NAND_CE0_B setup time	tCS	(AS + DS + 1) × T [see notes[3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	(DH+1) × T - 1 [see note[2]]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes[3,2]]		ns
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		ns
NF8	Data setup time	tDS	DH × T - 0.26 [see note[2]]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see note[2]]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see note[2]]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see note[2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see note[2]]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see note[2]]		ns
NF15	NAND_RE_B high hold time	tREH	DS × T [see note[2]]		ns
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see notes[5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see notes[5,6]]	—	ns

1 GPMI's Asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075 ns (half of maximum p-p jitter).

4 NF12 is guaranteed by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 31), NF16/NF17 are different from the definition in non-EDO mode (Figure 30). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI samples NAND_DATAxx at the rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 8M Plus Applications Processor Reference Manual* [IMX8MPRM]). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.8.5.2 Source synchronous mode AC timing (ONFI 2.x compatible)

Figure 33 to Figure 35 show the write and read timing of Source Synchronous mode.

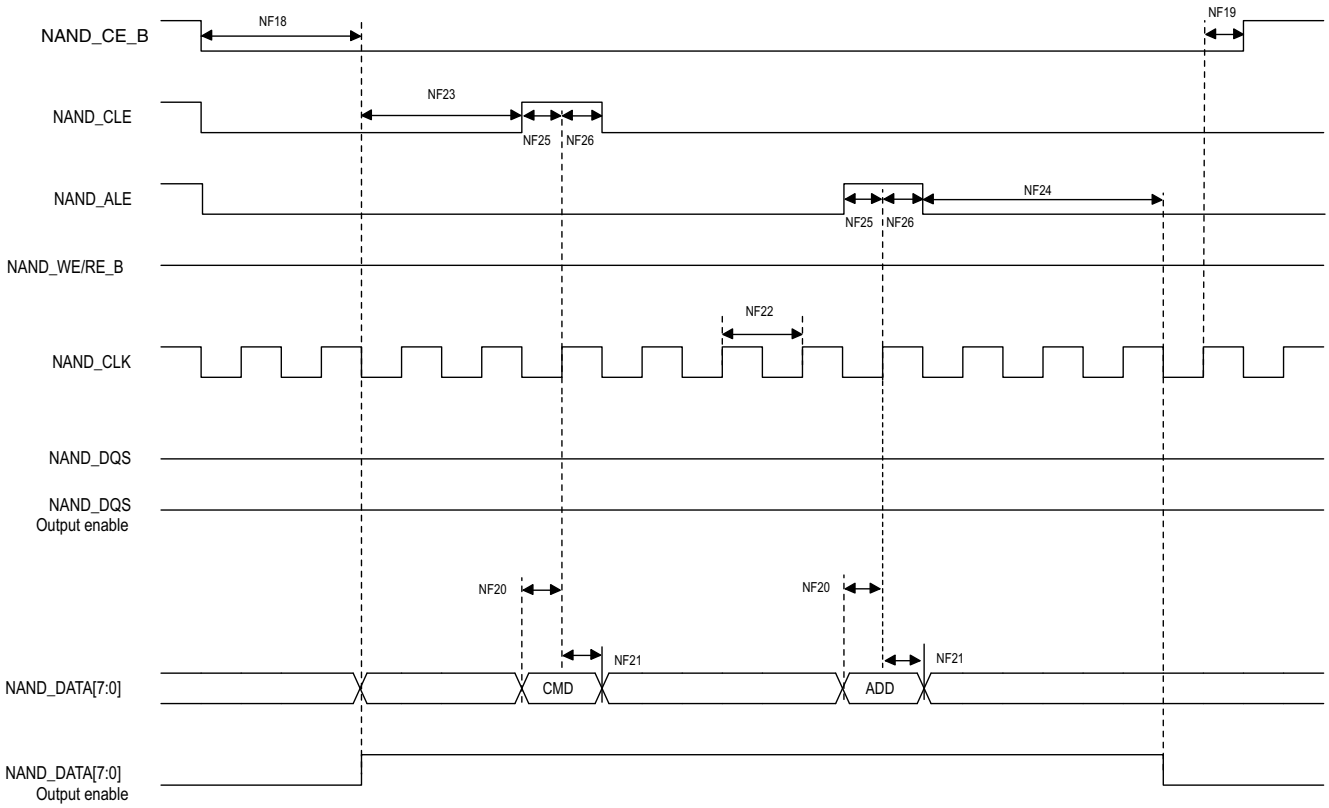


Figure 33. Source Synchronous mode command and address timing diagram

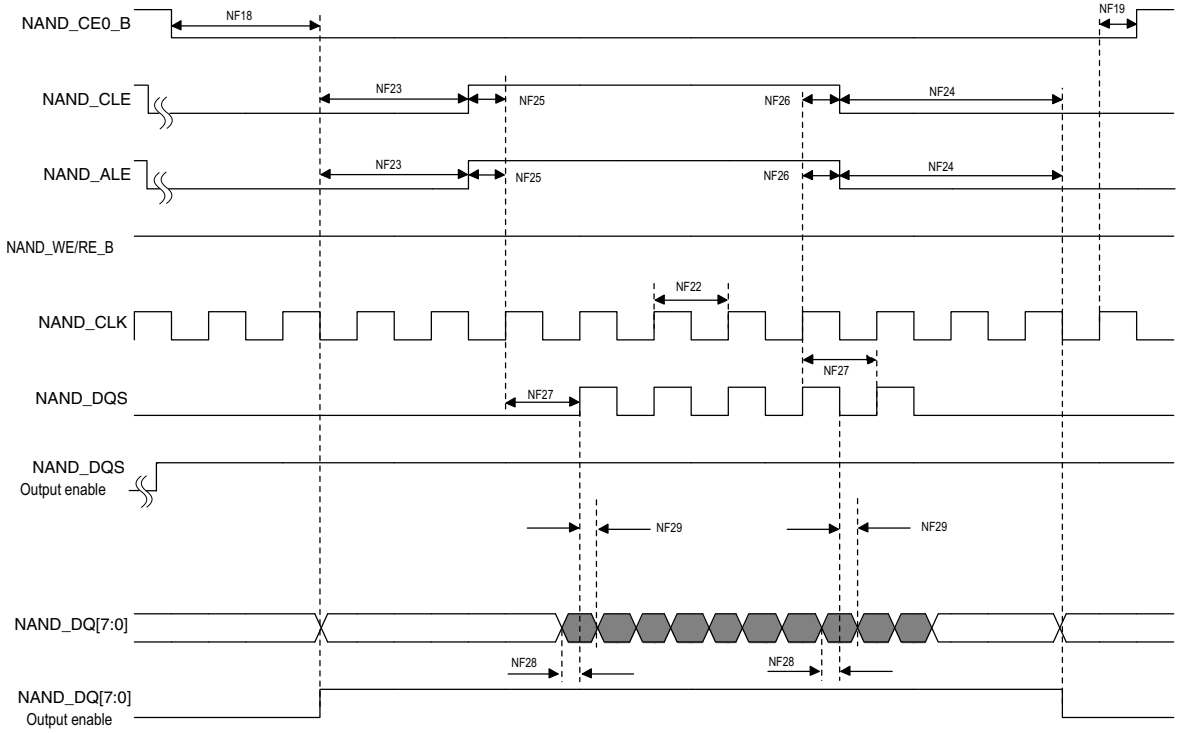


Figure 34. Source Synchronous mode data write timing diagram

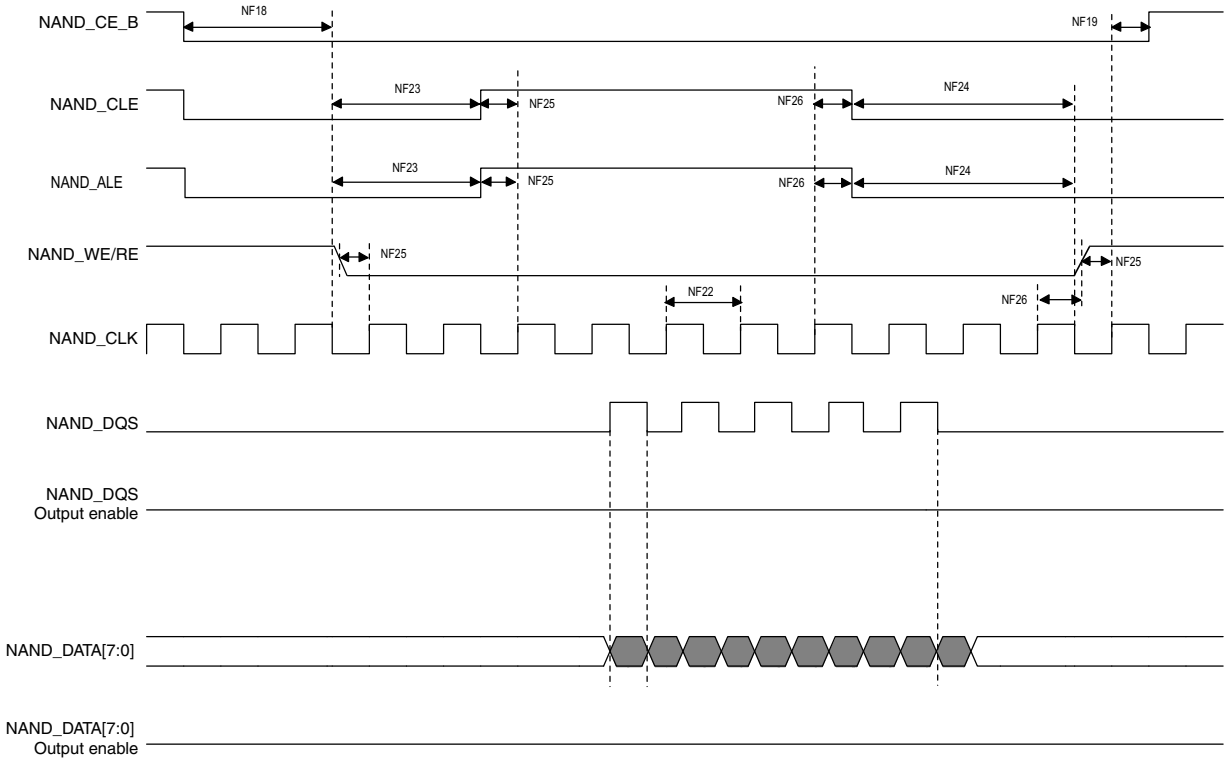


Figure 35. Source Synchronous mode data read timing diagram

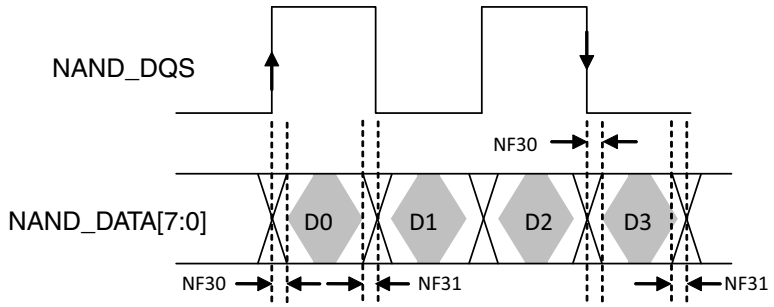


Figure 36. NAND_DQS/NAND_DQ read valid window

Table 51. Source Synchronous mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	NAND_CE0_B access time	tCE	CE_DELAY × T - 0.79 [see note[2]]		ns
NF19	NAND_CE0_B hold time	tCH	0.5 × tCK - 0.63 [see note[2]]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see note[2]]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see note[2]]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see note[2]]		ns
NF28	Data write setup	—	0.25 × tCK - 0.35		
NF29	Data write hold	—	0.25 × tCK - 0.85		
NF30	NAND_DQS/NAND_DQ read setup skew	—	—	2.06	
NF31	NAND_DQS/NAND_DQ read hold skew	—	—	1.95	

1 GPMI's Source Synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK(GPMI clock period) –0.075 ns (half of maximum p-p jitter).

For DDR Source Synchronous mode, Figure 36 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 8M Plus Applications Processor Reference Manual* [IMX8MPRM]). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.8.5.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

3.8.5.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 3.8.5.1, Asynchronous mode AC timing (ONFI 1.0 compatible) for details.

3.8.5.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See Section 3.8.5.4, Toggle mode AC Timing for details.

3.8.5.4 Toggle mode AC Timing

3.8.5.4.1 Command and address timing

NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See Section 3.8.5.1, Asynchronous mode AC timing (ONFI 1.0 compatible) for details.

3.8.5.4.2 Read and write timing

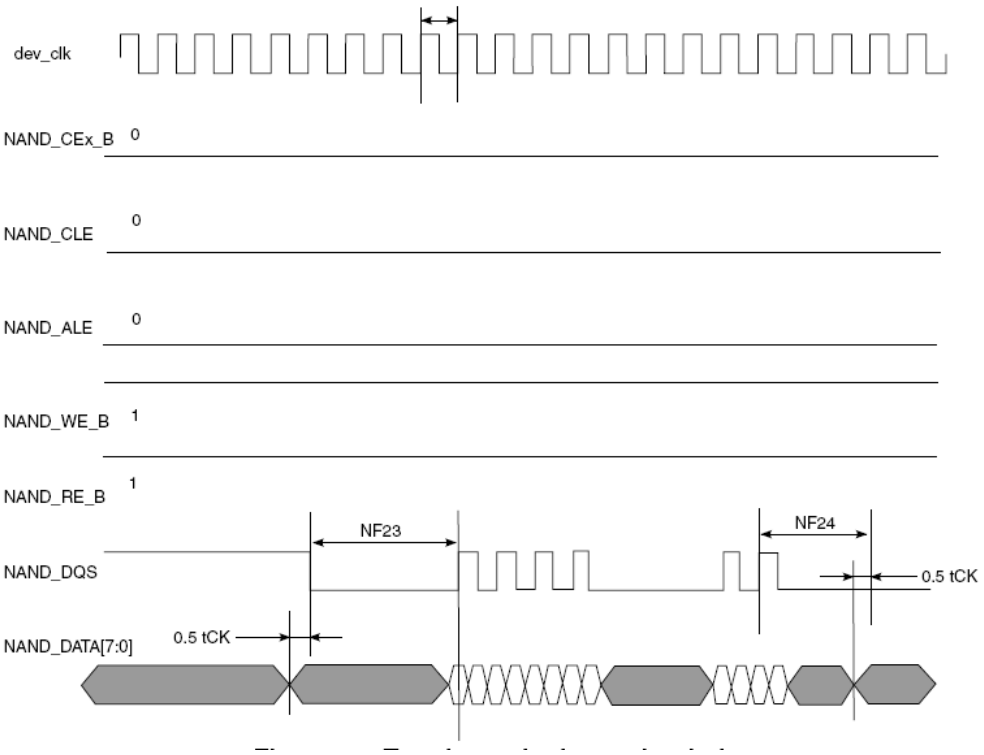


Figure 37. Toggle mode data write timing

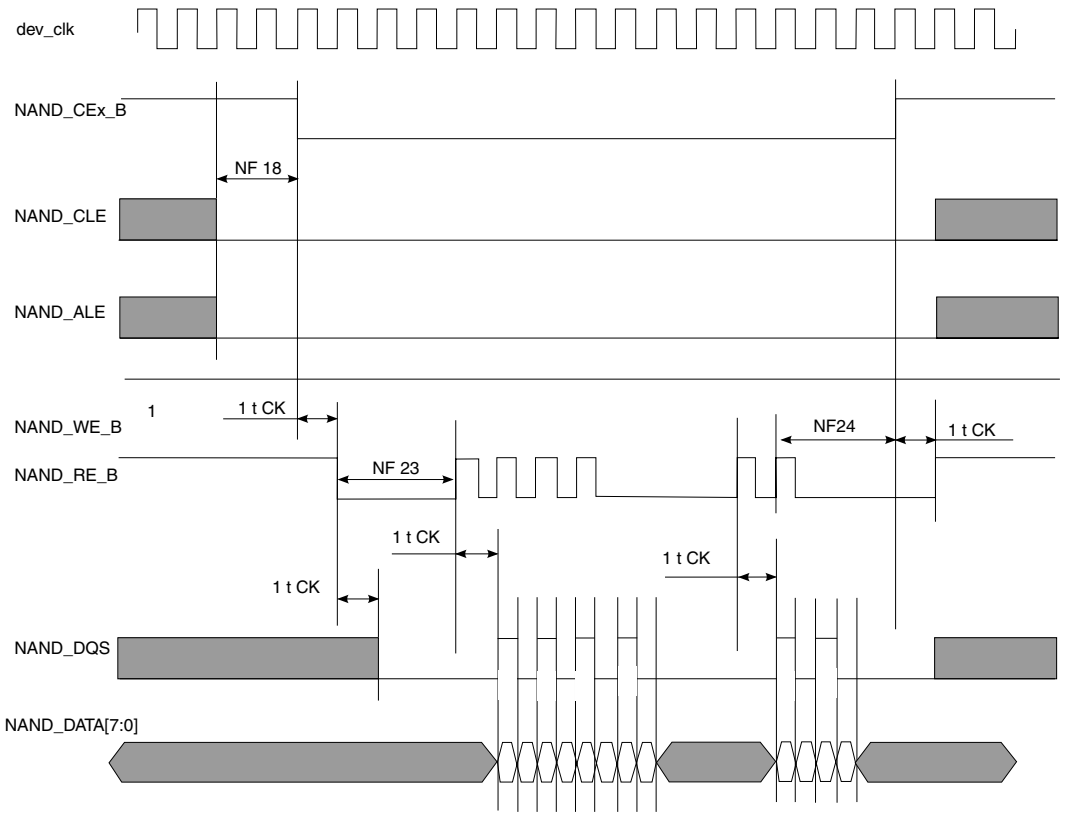


Figure 38. Toggle mode data read timing

Table 52. Toggle mode timing parameters

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[1,2]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes[,2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see note[2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see note[3,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see note[4,2]]	—	ns

Table 52. Toggle mode timing parameters (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF24	postamble delay	tPOST	POST_DELAY × T + 0.43 [see note[2]]	—	ns
NF28	Data write setup	tDS[5]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[5]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[6]	—	3.18	ns
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[6]	—	3.27	ns

1 AS minimum value can be 0, while DS/DH minimum value is 1.

2 T = tCK (GPMI clock period) - 0.075 ns (half of maximum p-p jitter).

3 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

4 PRE_DELAY + 1 ≥ (AS + DS)

5 Shown in Figure 37.

6 Shown in Figure 38.

For DDR Toggle mode, Figure 36 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI samples NAND_DATA[7:0] at both the rising and falling edges of a delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by the GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the *i.MX 8M Plus Applications Processor Reference Manual* [IMX8MPRM]). Generally, the typical delay value is equal to 0x7, which means a 1/4 clock cycle delay is expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

3.8.6 I²C bus characteristics

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. The I2C is designed to be compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).

3.8.7 CAN network AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has two CAN modules available. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

3.8.8 HDMI Tx module parameters

The HDMI 2.0a Tx interface (controller and PHY) is complaint with following specifications:

- *HDMI 2.0a Specification*
- *HDMI 1.4b Specification*

3.8.9 MIPI D-PHY parameters

MIPI D-PHY electrical specifications are compliance.

Typical values measured at AVDD = 1.8 V, AVSS = 0 V, T_J = 25°C; unless otherwise specified.

Table 53. Electrical characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage accuracy[1]	V_{OUT}	1.14	1.2	1.26	V	—
Driving current	I_{LOAD}	—	—	20	mA	—
AVDD current dissipation[2]	I_{OP_AVDD}	—	150	480	μA	EN = 1'b1
DVDD current dissipation[3]	I_{OP_DVDD}	—	0.05	7.3	μA	EN = 1'b1
AVDD power down current[2]	I_{PD_AVDD}	—	10	80	μA	EN = 1'b0
DVDD power down current[2]	I_{PD_DVDD}	—	0.05	7.3	μA	EN = 1'b0
Load capacitance	C_L	1	—	9.4	μF	—

1 This result is valid after output voltage trimming.

2 Typical values are measured at the typical supply voltage and at a junction temperature of 25°C. The maximum values are measured at the maximum supply voltage and at a junction temperature of 125°C.

3 This means the total effective capacitance value including parasitic capacitance.

Table 54 describes the electrical specifications.

Table 54. DC power supply, LP-RX, and skew calibration specifications (Sheet 1 of 2)

Category	Parameter	Description	Condition	Min	Typ	Max	Unit
Power	P_{OP}	Normal mode operating power	4 lane, 2.1 Gbps, TYP	—	54.12	—	mW
	P_{PD}	Power-down mode power	TYP	—	0.025	—	mW
LP-RX	VIH	Logic1 input voltage	—	880	—	—	mV
	VIL	Logic0 input voltage, not in ULPS state	—	—	—	550	mV

Table 54. DC power supply, LP-RX, and skew calibration specifications (continued) (Sheet 2 of 2)

Category	Parameter	Description	Condition	Min	Typ	Max	Unit
Skew calibration	$T_{skewcal}$ (Initial)	Timing that the transmitter drives the skew calibration pattern in the initial skew calibration mode	—	—	—	100	µs
			—	2^15	—	—	UI
	$T_{skewcal}$ (Periodic)	Timing that the transmitter drives the skew calibration pattern in the periodic skew calibration mode	—	—	—	10	µs
			—	2^13	—	—	UI

3.8.10 PCIe 3.0 PHY parameters

The PCIe interface is designed to be compatible with PCIe specification Gen3 x1 lane and supports the PCI Express 1.1/2.0/3.0 standards.

3.8.10.1 PCIe DC parameters

The DC parameters of PCIe are compliant with *PCI Express Base Specification, rev3.0*.

3.8.10.2 PCIE_RESREF reference resistor connection

The external resistor-referred current is generated by using 8.2 kΩ. 1% precision resistor, which is connected between the PCIE_RESREF pad and ground outside the chip.

3.8.11 Pulse width modulator (PWM) timing parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 39 depicts the timing of the PWM, and Table 55 lists the PWM timing parameters.

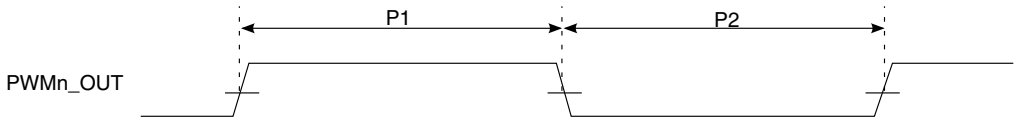


Figure 39. PWM timing

Table 55. PWM output timing parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	66 (ipg_clk)	MHz
P1	PWM output pulse width high	12	—	ns
P2	PWM output pulse width low	12	—	ns

3.8.12 FlexSPI timing parameters

Measurement is with a load of 35 pF on SCK and SIO pins and an input slew rate of 1 V/ns.

3.8.12.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these four internal sample clock sources.

3.8.12.1.1 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Table 56. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	66	MHz	—
F1	[D:] Setup time for incoming data	8.67	—	ns	[1]
F2	[D:] Hold time for incoming data	0	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

Table 57. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1, 0x2

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	133	MHz	—
F1	[D:] Setup time for incoming data	1.5	—	ns	[1]
F2	[D:] Hold time for incoming data	1	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

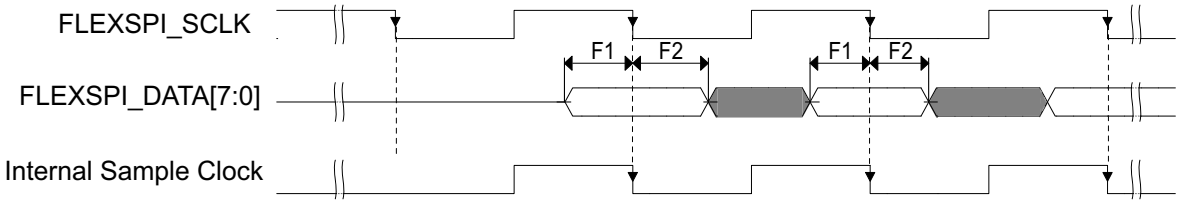


Figure 40. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

3.8.12.1.2 SDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

Table 58. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A1)

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation	—	166	MHz
F3	[D:] Time from SCK to data valid	—	—	ns
F4	[D:] Time from SCK to DQS	—	—	ns
—	[D:] Time delta between TSCKD and TSCKDQS	-2	2	ns

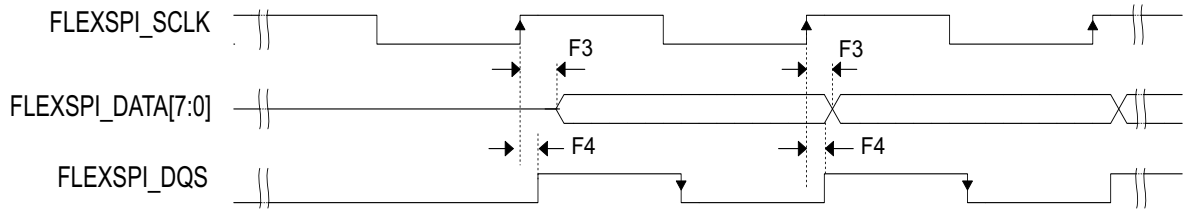


Figure 41. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 59. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A2)

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation	—	166	MHz
F5	[D:] Time from SCK to data valid	—	—	ns
F6	[D:] Time from SCK to DQS	—	—	ns
—	[D:] Time delta between TSCKD and TSCKDQS	-2	2	ns

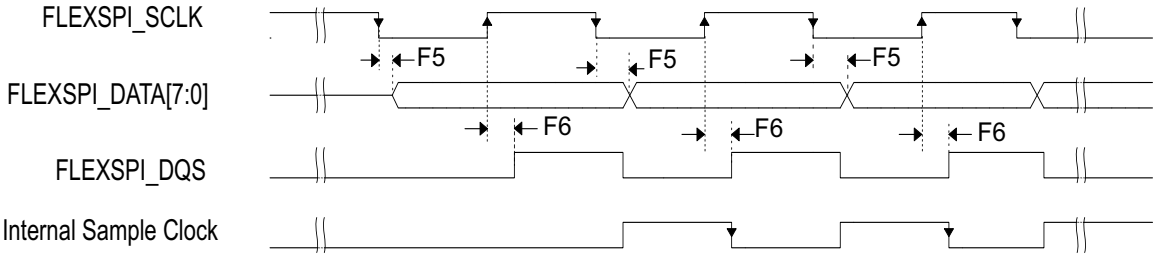


Figure 42. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case A2)

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half-cycle delayed DQS falling edge.

3.8.12.1.3 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

Table 60. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	33	MHz	—
F1	[D:] Setup time for incoming data	8.67	—	ns	[1]
F2	[D:] Hold time for incoming data	0	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

Table 61. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1, 0x2

Symbol	Parameter	Min.	Max.	Unit	Notes
—	[D:] Frequency of operation	—	66	MHz	—
F1	[D:] Setup time for incoming data	1.5	—	ns	[1]
F2	[D:] Hold time for incoming data	1	—	ns	—

[1] The setup specification here assumes the data learning feature is not used. If data learning is enabled, then TIS can be decreased by up to 2ns.

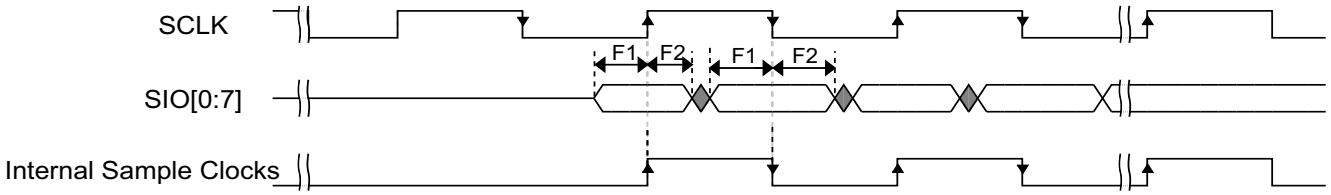


Figure 43. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0, 0x1, 0x2

3.8.12.1.4 DDR mode with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

Table 62. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Case 1)

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation	—	166	MHz
T_{SCKD}	[D:] Time from SCK to data valid	—	—	ns
T_{SCKDQS}	[D:] Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	[D:] Time delta between TSCKD and TSCKDQS	-0.6	0.6	ns

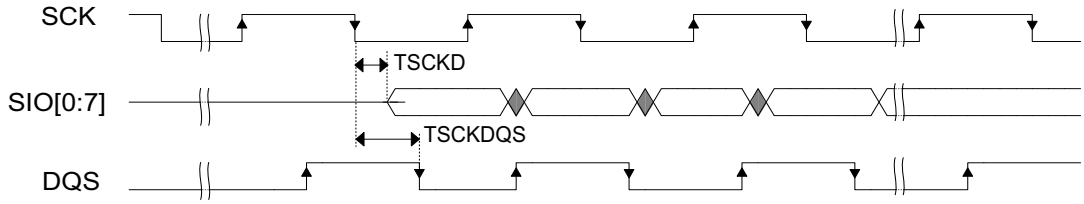


Figure 44. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3

3.8.12.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

3.8.12.2.1 SDR mode

Table 63. FlexSPI output timing in SDR mode

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation[1]	—	166	MHz
T_{CK}	[D:] SCK clock period	6.02	—	ns

Table 63. FlexSPI output timing in SDR mode (continued)

Symbol	Parameter	Min.	Max.	Unit
T_{DSO}	[D:] Output data setup time	2	—	ns
T_{DHO}	[D:] Output data hold time	2	—	ns
T_{CSS}	[D:] Chip select output setup time	3 x T_{CK} - 1	—	ns
T_{CSH}	[D:] Chip select output hold time	3 x T_{CK} - 1	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM) for more details.

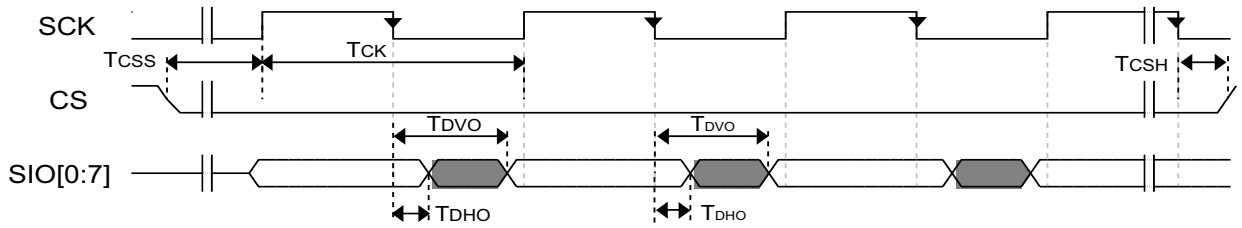


Figure 45. FlexSPI output timing in SDR mode

3.8.12.2.2 DDR mode

Table 64. FlexSPI output timing in DDR mode

Symbol	Parameter	Min.	Max.	Unit
—	[D:] Frequency of operation[1]	—	166	MHz
T_{CK}	[D:] SCK clock period	6.02	—	ns
T_{DSO}	[D:] Output data setup time	—	0.6	ns
T_{DHO}	[D:] Output data hold time	0.6	—	ns
T_{CSS}	[D:] Chip select output setup time	3 x T_{CK} - 1.075	—	ns
T_{CSH}	[D:] Chip select output hold time	3 x T_{CK} - 1.075	—	ns

1 The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used. See the FlexSPI SDR input timing specifications.

NOTE

T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register, the default values are shown above. See the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM) for more details.

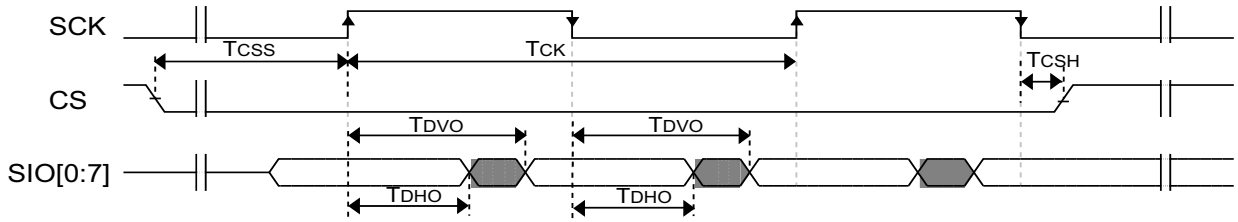


Figure 46. FlexSPI output timing in DDR mode

3.8.13 SAI/I2S switching specifications

This section provides the AC timings for the SAI in Master (clocks driven) and Slave (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and non inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 65. Master mode SAI timing (50 MHz)[1]

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	20	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	2	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	2	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

1 To achieve 50 MHz for BCLK operation, clock must be set in feedback mode.

Table 66. Master mode SAI timing (25 MHz)

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	2	ns

Table 66. Master mode SAI timing (25 MHz) (continued)

Num	Characteristic	Min	Max	Unit
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	2	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	12	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

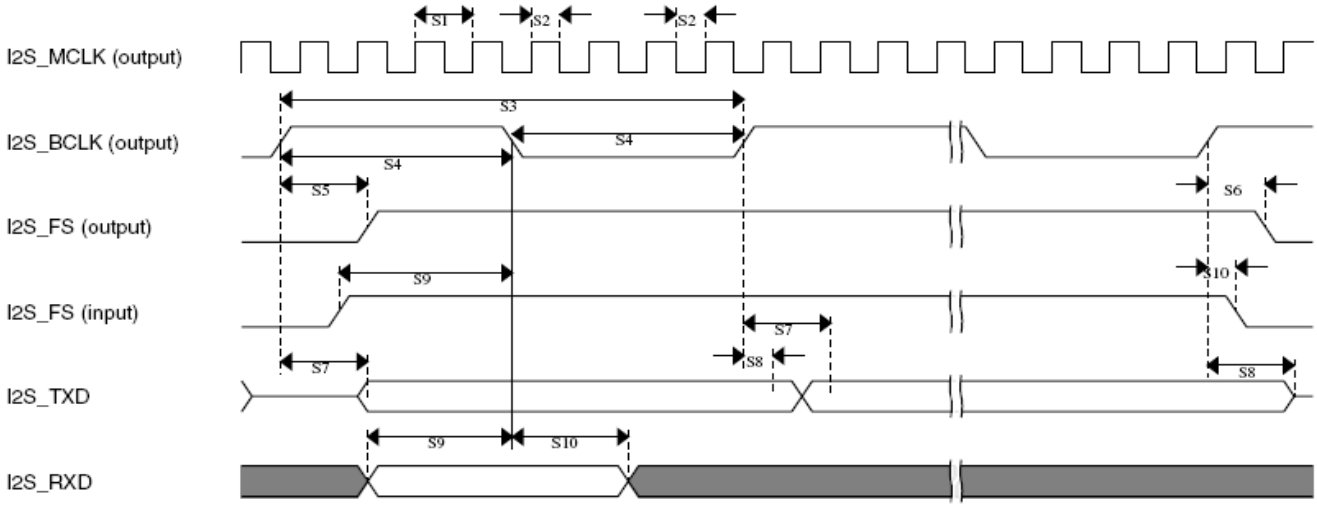


Figure 47. SAI timing—Master modes

Table 67. Slave mode SAI timing (50 MHz)[1]

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	20	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	2	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S17	SAI_RXD setup before SAI_BCLK	2	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

1 TX does not support 50 MHz operation in Slave mode.

Table 68. Slave mode SAI timing (25 MHz)

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period

Table 68. Slave mode SAI timing (25 MHz) (continued)

Num	Characteristic	Min	Max	Unit
S13	SAI_FS input setup before SAI_BCLK	12	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	7	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	12	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

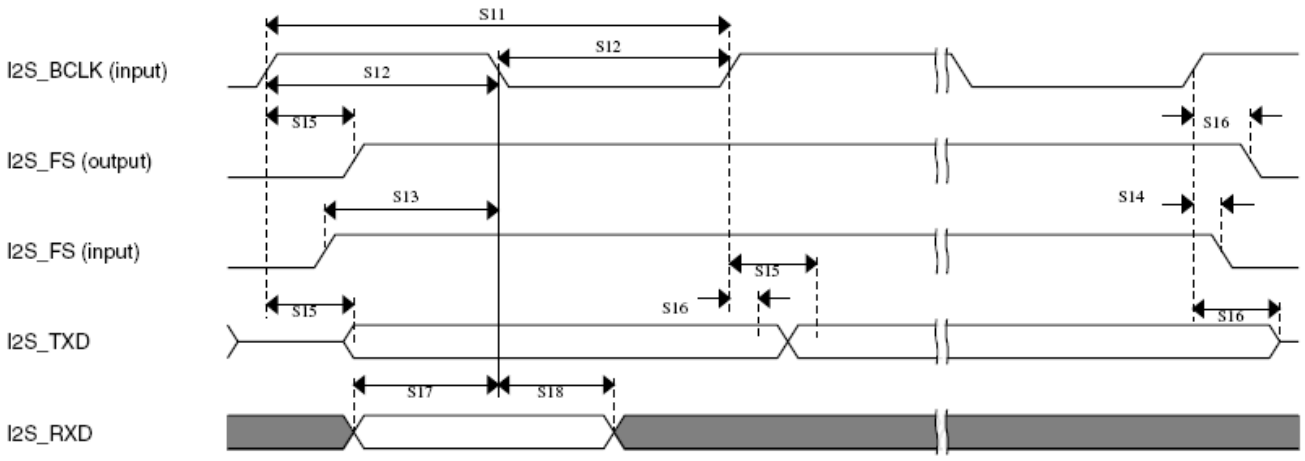


Figure 48. SAI Timing — Slave Modes

3.8.14 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 69, Figure 49, and Figure 50 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 69. SPDIF timing parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns

Table 69. SPDIF timing parameters (continued)

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

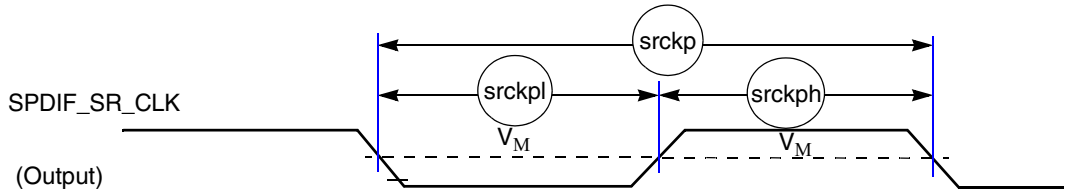


Figure 49. SPDIF_SR_CLK timing diagram

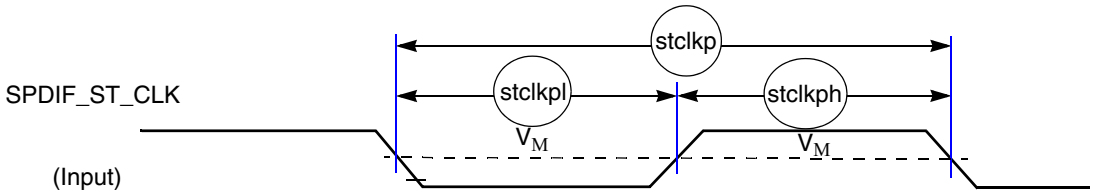


Figure 50. SPDIF_ST_CLK timing diagram

3.8.15 UART I/O configuration and timing parameters

3.8.15.1 UART RS-232 I/O configuration in different modes

The i.MX 8M Plus UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0—DCE mode). Table 70 shows the UART I/O configuration based on the enabled mode.

Table 70. UART I/O configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

3.8.15.2 UART RS-232 Serial mode timing

This section describes the electrical information of the UART module in the RS-232 mode.

3.8.15.2.1 UART transmitter

Figure 51 depicts the transmit timing of UART in the RS-232 Serial mode, with 8 data bit/1 stop bit format. Table 71 lists the UART RS-232 Serial mode transmit timing characteristics.

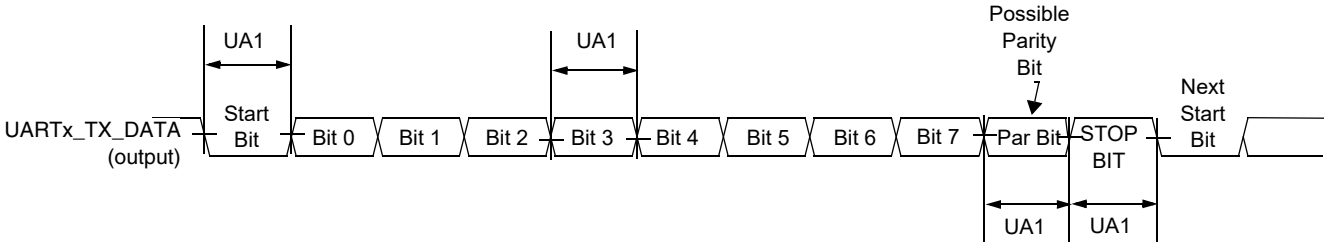


Figure 51. UART RS-232 Serial mode transmit timing diagram

Table 71. RS-232 Serial mode transmit timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] - T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

3.8.15.2.2 UART receiver

Figure 52 depicts the RS-232 Serial mode receive timing with 8 data bit/1 stop bit format. Table 72 lists Serial mode receive timing characteristics.

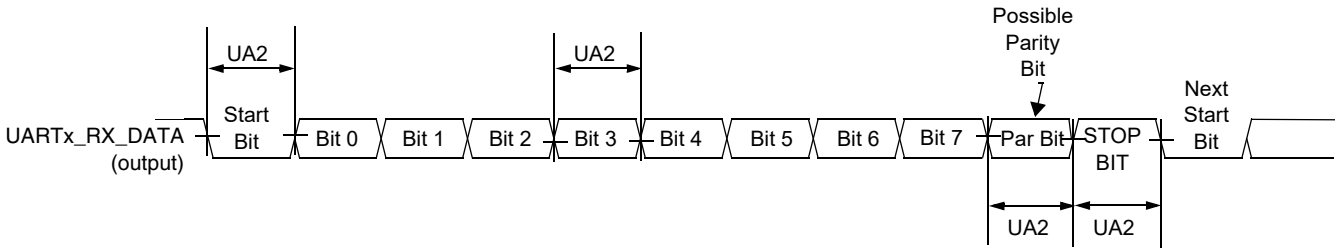


Figure 52. UART RS-232 Serial mode receive timing diagram

Table 72. RS-232 Serial mode receive timing parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

3.8.16 USB PHY parameters

The USB PHY parameters meet the electrical compliance requirements listed as following:

- *Universal Serial Bus Revision 3.0 Specification* (including ECNs and errata), *On-The-Go and Embedded Host Supplement to the USB 3.0 Specification* (including ECNS and Errata)
- *Universal Serial Bus Revision 2.0 Specification* (including ECNs and errata), *On-The-Go and Embedded Host Supplement to the Universal Serial Bus Revision 2.0 Specification* (including ECNs and errata)

3.8.16.1 Pad/Package/Board connections

The USBx_VBUS pin cannot directly connect to 5 V VBUS voltage on the USB2.0 link, each USBx_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor if connects to 5 V VBUS.

The USB 2.0 PHY uses USBx_TXRTUNE and an external resistor to calibrate the USBx_DP/DN 45 Ω source impedance. The external resistor value is 200 Ω 1% precision on each of USBx_TXRTUNE pad to ground.

3.8.16.2 USB PHY worst power consumption

Table 73 shows the USB 2.0 PHY worst power dissipation.

Table 73. USB 2.0 PHY worst power dissipation

Mode	VDD_USB_0P8		VDD_USB_3P3		VDD_USB_1P8		Total Power	
HS TX	8.286	mA	4.63	mA	23.409	mA	70.448	mW
FS TX	6.767		12.52		5.968		63.22	
LS TX	7.001		13.58		6.224		67.779	
Suspend	0.752		0.164		0.106		1.465	
Sleep	0.761		0.163		0.106		1.472	

4 Boot mode configuration

This section provides information on Boot mode configuration pins allocation and boot devices interfaces allocation.

4.1 Boot mode configuration pins

Table 74 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed Boot mode options configured by the Boot mode pins, see the "System Boot, Fusemap, and eFuse" chapter in the *i.MX 8M Plus Applications Processor Reference Manual* (IMX8MPRM).

Table 74. Fuses and associated pins used for boot

Interface	IP instance	Allocated pads during boot	Comment
BOOT_MODE0	Input	ccmsrcgpcmix.BOOT_MODE[0]	Boot mode selection
BOOT_MODE1	Input	ccmsrcgpcmix.BOOT_MODE[1]	
BOOT_MODE2	Input	ccmsrcgpcmix.BOOT_MODE[2]	
BOOT_MODE3	Input	ccmsrcgpcmix.BOOT_MODE[3]	

4.2 Boot device interface allocation

Table 75 lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 75. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	ECSPI1_SCLK, ECSPI1_MOSI, ECSPI1_MISO, ECSPI1_SS0	The chip-select pin used depends on the fuse "CS select (SPI only)".
SPI	ECSPI-2	ECSPI2_SCLK, ECSPI2_MOSI, ECSPI2_MISO, ECSPI2_SS0	The chip-select pin used depends on the fuse "CS select (SPI only)".
SPI	ECSPI-3	UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD	The chip-select pin used depends on the fuse "CS select (SPI only)".
NAND Flash	GPMI	NAND_ALE, NAND_CE0_B, NAND_CLE, NAND_DATA00,NAND_DATA01,NAND_DATA02, NAND_DATA03,NAND_DATA04,NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B, NAND_READY_B, NAND_WE_B, NAND_WP_B	8-bit, only CS0 is supported.

Table 75. Interface allocation during boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
SD/MMC	USDHC-1	GPIO1_IO03, GPIO1_IO06, GPIO1_IO07, SD1_RESET_B, SD1_CLK, SD1_CMD, SD1_STROBE, SD1_DATA0, SD1_DATA1, SD1_DATA2, SD1_DATA3, SD1_DATA4, SD1_DATA5, SD1_DATA6, SD1_DATA7	1, 4, or 8-bit
SD/MMC	USDHC-2	GPIO1_IO04, GPIO1_IO08, GPIO1_IO07, SD2_RESET_B, SD2_WP, SD2_CLK, SD2_CMD, SD2_DATA0, SD2_DATA1, SD2_DATA2, SD2_DATA3	1 or 4-bit
SD/MMC	USDHC-3	NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA02, NAND_DATA03, NAND_DATA04,NAND_DATA05,NAND_DATA06, NAND_DATA07,NAND_RE_B,NAND_READY_B, NAND_WE_B, NAND_WP_B	1, 4, or 8-bit
FlexSPI	FlexSPI	NAND_ALE, NAND_CE0_B, NAND_CE1_B, NAND_CE2_B, NAND_CE3_B, NAND_CLE, NAND_DATA00,NAND_DATA01,NAND_DATA02, NAND_DATA03,NAND_DATA04,NAND_DATA05, NAND_DATA06, NAND_DATA07, NAND_DQS, NAND_RE_B	For FlexSPI flash
USB	USB1, USB2	Dedicated USB pins	—

5 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 15 x 15 mm package information

5.1.1 15 x 15 mm, 0.5 mm pitch, ball matrix

Figure 53 shows the top, bottom, and side views of the 15 × 15 mm FCBGA package.

FC-PBGA-548 I/O
15 X 15 X 1.331 PKG, 0.5 PITCH, BARE DIE

SOT2047-1

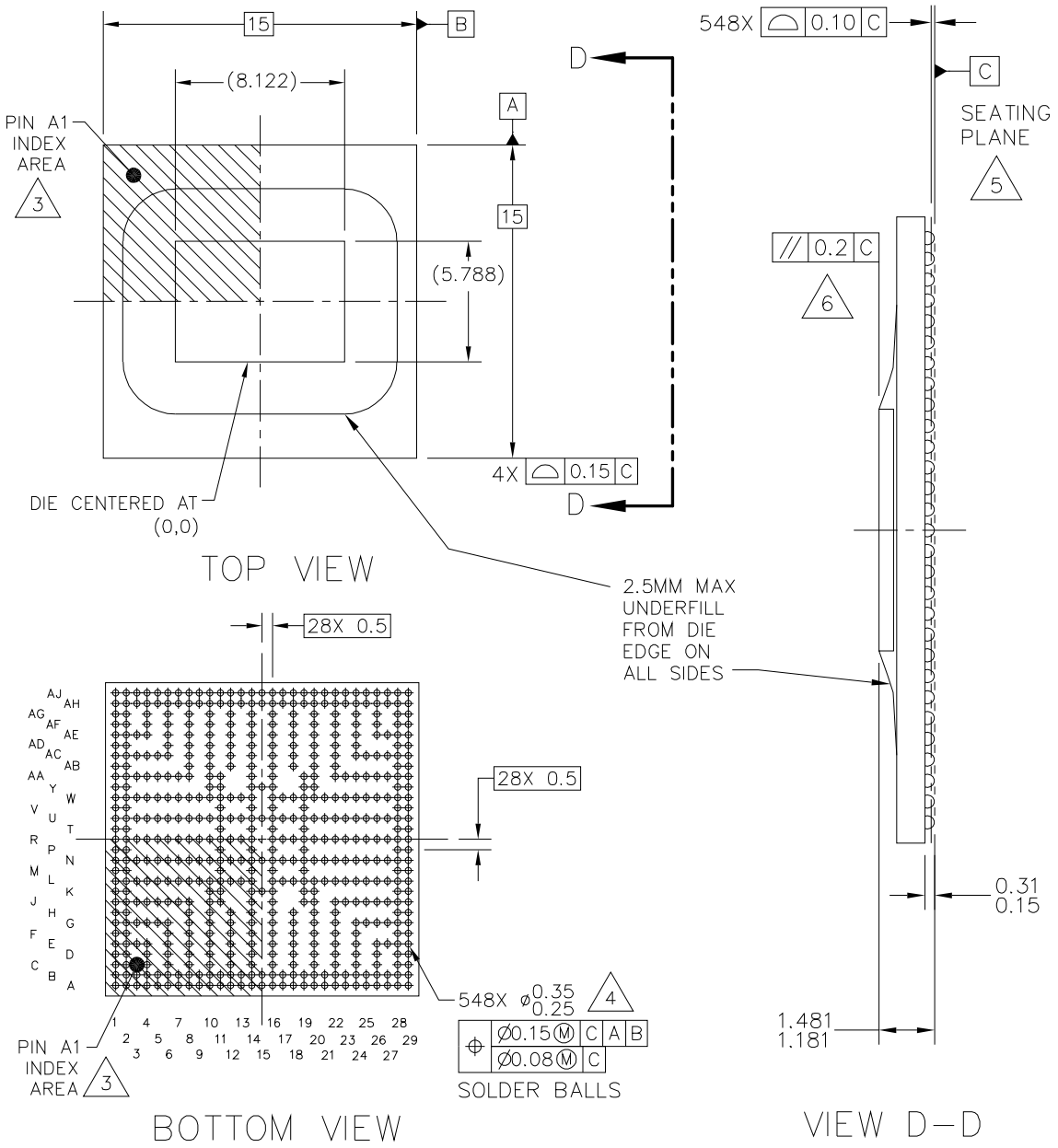


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Figure 53. 15 X 15 MM BGA, case x package top, bottom, and side views

5.1.2 15 x 15 mm supplies contact assignments and functional contact assignments

Table 76 shows supplies contact assignments for the 15 x 15 mm package.

Table 76. i.MX 8M Plus 15 x 15 mm supplies contact assignments

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_CLK	R22	Supply for CLK interface
NVCC_DRAM	J8, J10, L8, N8, R8, U8, W8, AA8, AA10	Supply for DRAM interface
NVCC_ECSPI_HDMI	AA14	Supply for ESCPI and HDMI interfaces
NVCC_ENET	AA24	Supply for ENET interface
NVCC_GPIO	J11	Supply for GPIO interface
NVCC_I2C_UART	Y10	Supply for I2C and UART interfaces
NVCC_JTAG	K11	Supply for JTAG interface
NVCC_NAND	U22	Supply for NAND interface
NVCC_SAI1_SAI5	Y11	Supply for SAI interface
NVCC_SAI2_SAI3_SPDIF	AA11	Supply for SAI and SPDIF interfaces
NVCC_SD1	U24	Supply for SDHC1 interface
NVCC_SD2	W24	Supply for SDHC2 interface
NVCC_SNVS_1P8	R24	Supply for SNVS interface
PVCC0_1P8	J16	Digital IO pre-drive
PVCC1_1P8	AA19	Digital IO pre-drive
PVCC2_1P8	AA16	Digital IO pre-drive
VDD_24M_XTAL_1P8	L22	Supply for XTAL
VDD_ANA0_1P8	J20	Supply for Analog logic
VDD_ANA1_0P8	R21	Supply for Analog logic
VDD_ANA1_1P8	N22	Supply for Analog logic
VDD_ANA2_1P8	Y20	Supply for Analog logic
VDD_ARM	T14, V16, W12, W13, W17, Y14, Y15, Y16, T16, U12, U13, U14, U15, U16, U17, V14	Supply for Arm Core
VDD_ARM_PLL_0P8	W21	Supply for ARM PLL
VDD_ARM_PLL_1P8	Y19	Supply for ARM PLL
VDD_AVPLL_1P8	W19	Supply for AV PLL
VDD_DRAM_PLL_0P8	R9	Supply for DRAM PLL
VDD_DRAM_PLL_1P8	R6	Supply for DRAM PLL
VDD_EARC_1P8	AA20	Supply for EARC interface

Table 76. i.MX 8M Plus 15 x 15 mm supplies contact assignments (continued)

VDD_HDMI_0P8	W22	Supply for HDMI interface
VDD_HDMI_1P8	AA22	Supply for HDMI interface
VDD_LVDS_1P8	J22	Supply for LVDS
VDD_MIPI_0P8	K16	Supply for MIPI PHY
VDD_MIPI_1P2_CAP	F20	Supply for MIPI PHY
VDD_MIPI_1P8	K20	Supply for MIPI PHY
VDD_PCI_0P8	K15	Supply for PCIe PHY
VDD_PCI_1P8	K19	Supply for PCIe PHY
VDD_SAI_PLL_0P8	U21	Supply for SAI PLL
VDD_SAI_PLL_1P8	W18	Supply for SAI PLL
VDD_SNVS_0P8_CAP	N26	Supply for SNVS logic
VDD_SOC	K10, L9, L10, L11, L12, L13, L17, L18, L19, L20, L21, M14, M16, N9, N10, N12, N13, N14, N15, N16, N17, N18, N20, N21, P14, P16, R10, R20, U9, U10, U20, W9, W10, W11, W20	Supply for SOC logic
VDD_USB_0P8	K14	Supply for USB PHY
VDD_USB_1P8	J19	Supply for USB PHY
VDD_USB_3P3	J14	Supply for USB PHY
VSS	A1, A29, C4, C6, C8, C10, C12, C14, C16, C18, C20, C22, C24, C26, E3, E27, G3, G6, G24, G27, H8, H10, H12, H14, H16, H18, H20, H22, J3, J7, J23, J27, L3, L7, L14, L16, L23, L27, M11, M19, N3, N7, N11, N19, N23, N27, P11, P19, R3, R7, R11, R12, R13, R14, R16, R17, R18, R19, R23, R27, T11, T19, U3, U7, U11, U18, U19, U23, U27, V11, V19, W3, W7, W14, W16, W23, W27, AA3, AA7, AA23, AA27, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AB22, AC3, AC6, AC24, AC27, AE3, AE27, AG4, AG6, AG8, AG10, AG12, AG14, AG16, AG18, AG20, AG22, AG24, AG26, AJ1, AJ29	—

Table 77 shows an alpha-sorted list of functional contact assignments for the 15 x 15 mm package.

Table 77. 15 x 15 mm functional contact assignments

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
BOOT_MODE0	G10	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[0]	Input with PD
BOOT_MODE1	F8	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[1]	Input with PD
BOOT_MODE2	G8	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[2]	Input with PD
BOOT_MODE3	G12	NVCC_JTAG	GPIO	ALT0	ccmsrcgpcmix.BOOT_MODE[3]	Input with PD
CLKIN1	K28	NVCC_CLK	GPIO	—	—	Input with PD
CLKIN2	L28	NVCC_CLK	GPIO	—	—	Input with PD
CLKOUT1	K29	NVCC_CLK	GPIO	—	—	Output low
CLKOUT2	L29	NVCC_CLK	GPIO	—	—	Output low
DRAM_AC00	J6	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC01	G5	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC02	N6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC03	J4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC04	M1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC05	M2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC06	G4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC07	J5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC08	L6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC09	L4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC10	E4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC11	D4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC12	N4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC13	N5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC14	L5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC15	R5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC16	N1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC17	N2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC19	P2	NVCC_DRAM	DDR	—	—	Input

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
DRAM_AC20	AA4	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC21	AA5	NVCC_DRAM	DDR	—	—	Output low
DRAM_AC22	AA6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC23	U4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC24	V2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC25	V1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC26	P1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC27	R4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC28	W4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC29	W5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC30	AE4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC31	AF4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC32	U5	NVCC_DRAM	DDR	—	—	Input
DRAM_AC33	U6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC34	U1	NVCC_DRAM	DDR	—	—	Input
DRAM_AC35	U2	NVCC_DRAM	DDR	—	—	Input
DRAM_AC36	W6	NVCC_DRAM	DDR	—	—	Input
DRAM_AC37	AC4	NVCC_DRAM	DDR	—	—	Input
DRAM_AC38	AC5	NVCC_DRAM	DDR	—	—	Input
DRAM_ALERT_N	T2	NVCC_DRAM	DDR	—	—	Input
DRAM_DM0	B2	NVCC_DRAM	DDR	—	—	Input
DRAM_DM1	H2	NVCC_DRAM	DDR	—	—	Input
DRAM_DM2	AB2	NVCC_DRAM	DDR	—	—	Input
DRAM_DM3	AH2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ00	B3	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ01	A2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ02	E1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ03	F2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ04	E2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ05	C1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ06	C2	NVCC_DRAM	DDR	—	—	Input

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
DRAM_DQ07	B1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ08	G1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ09	H1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ10	K1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ11	K2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ12	L2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ13	L1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ14	G2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ15	F1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ16	AC1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ17	AB1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ18	W2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ19	Y2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ20	Y1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ21	W1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ22	AC2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ23	AD1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ24	AH3	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ25	AJ2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ26	AE1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ27	AD2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ28	AE2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ29	AG1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ30	AG2	NVCC_DRAM	DDR	—	—	Input
DRAM_DQ31	AH1	NVCC_DRAM	DDR	—	—	Input
DRAM_DQS0_N	D1	NVCC_DRAM	DDRCLK	—	—	Input
DRAM_DQS0_P	D2	NVCC_DRAM	—	—	—	Input
DRAM_DQS1_N	J1	NVCC_DRAM	DDRCLK	—	—	Input
DRAM_DQS1_P	J2	NVCC_DRAM	—	—	—	Input
DRAM_DQS2_N	AA1	NVCC_DRAM	DDRCLK	—	—	Input
DRAM_DQS2_P	AA2	NVCC_DRAM	—	—	—	Input

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
DRAM_DQS3_N	AF1	NVCC_DRAM	DDRCLK	—	—	Input
DRAM_DQS3_P	AF2	NVCC_DRAM	—	—	—	Input
DRAM_RESET_N	T1	NVCC_DRAM	DDR	—	—	Output
DRAM_VREF	R2	NVCC_DRAM	DDR	—	—	—
DRAM_ZN	R1	NVCC_DRAM	DDR	—	—	Input
EARC_AUX	AH23	VDD_EARC_1P8	PHY	—	—	Input with PD
EARC_N_HPD	AH22	VDD_EARC_1P8	PHY	—	—	Output
EARC_P_UTIL	AJ23	VDD_EARC_1P8	PHY	—	—	Output
ECSPI1_MISO	AD20	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[8]	Input with PD
ECSPI1_MOSI	AC20	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[7]	Input with PD
ECSPI1_SCLK	AF20	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[6]	Input with PD
ECSPI1_SS0	AE20	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[9]	Input with PD
ECSPI2_MISO	AH20	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[12]	Input with PD
ECSPI2_MOSI	AJ21	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[11]	Input with PD
ECSPI2_SCLK	AH21	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[10]	Input with PD
ECSPI2_SS0	AJ22	NVCC_ECSPI_HDMI	GPIO	ALT5	gpio5.IO[13]	Input with PD
ENET_MDC	AH28	NVCC_ENET	GPIO	ALT5	gpio1.IO[16]	Input with PD
ENET_MDIO	AH29	NVCC_ENET	GPIO	ALT5	gpio1.IO[17]	Input with PD
ENET_RD0	AG29	NVCC_ENET	GPIO	ALT5	gpio1.IO[26]	Input with PD
ENET_RD1	AG28	NVCC_ENET	GPIO	ALT5	gpio1.IO[27]	Input with PD
ENET_RD2	AF29	NVCC_ENET	GPIO	ALT5	gpio1.IO[28]	Input with PD
ENET_RD3	AF28	NVCC_ENET	GPIO	ALT5	gpio1.IO[29]	Input with PD
ENET_RX_CTL	AE28	NVCC_ENET	GPIO	ALT5	gpio1.IO[24]	Input with PD
ENET_RXC	AE29	NVCC_ENET	GPIO	ALT5	gpio1.IO[25]	Input with PD
ENET_TD0	AC25	NVCC_ENET	GPIO	ALT5	gpio1.IO[21]	Input with PD
ENET_TD1	AE26	NVCC_ENET	GPIO	ALT5	gpio1.IO[20]	Input with PD
ENET_TD2	AF26	NVCC_ENET	GPIO	ALT5	gpio1.IO[19]	Input with PD
ENET_TD3	AD24	NVCC_ENET	GPIO	ALT5	gpio1.IO[18]	Input with PD
ENET_TX_CTL	AF24	NVCC_ENET	GPIO	ALT5	gpio1.IO[22]	Input with PD
ENET_TXC	AE24	NVCC_ENET	GPIO	ALT5	gpio1.IO[23]	Input with PD
GPIO1_IO00	A7	NVCC_GPIO	GPIO	ALT0	gpio1.IO[0]	Input with PD

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
GPIO1_IO01	E8	NVCC_GPIO	GPIO	ALT0	gpio1.IO[1]	Output low during reset, input with PD after reset
GPIO1_IO02	B6	NVCC_GPIO	GPIO	ALT0	gpio1.IO[2]	Input with PU
GPIO1_IO03	D6	NVCC_GPIO	GPIO	ALT0	gpio1.IO[3]	Input with PD
GPIO1_IO04	E6	NVCC_GPIO	GPIO	ALT0	gpio1.IO[4]	Input with PD
GPIO1_IO05	B4	NVCC_GPIO	GPIO	ALT0	gpio1.IO[5]	Output high during reset, input with PU after reset
GPIO1_IO06	A3	NVCC_GPIO	GPIO	ALT0	gpio1.IO[6]	Input with PD
GPIO1_IO07	F6	NVCC_GPIO	GPIO	ALT0	gpio1.IO[7]	Input with PD
GPIO1_IO08	A8	NVCC_GPIO	GPIO	ALT0	gpio1.IO[8]	Input with PD
GPIO1_IO09	B8	NVCC_GPIO	GPIO	ALT0	gpio1.IO[9]	Input with PD
GPIO1_IO10	B7	NVCC_GPIO	GPIO	ALT0	gpio1.IO[10]	Input with PD
GPIO1_IO11	D8	NVCC_GPIO	GPIO	ALT0	gpio1.IO[11]	Input with PD
GPIO1_IO12	A5	NVCC_GPIO	GPIO	ALT0	gpio1.IO[12]	Input with PD
GPIO1_IO13	A6	NVCC_GPIO	GPIO	ALT0	gpio1.IO[13]	Input with PD
GPIO1_IO14	A4	NVCC_GPIO	GPIO	ALT0	gpio1.IO[14]	Input with PD
GPIO1_IO15	B5	NVCC_GPIO	GPIO	ALT0	gpio1.IO[15]	Input with PD
HDMI_CEC	AD22	NVCC_ECSPI_HDMI	PHY	ALT5	gpio3.IO[28]	Input with PD
HDMI_DDC_SCL	AC22	NVCC_ECSPI_HDMI	PHY	ALT5	gpio3.IO[26]	Input with PD
HDMI_DDC_SDA	AF22	NVCC_ECSPI_HDMI	PHY	ALT5	gpio3.IO[27]	Input with PD
HDMI_HPD	AE22	NVCC_ECSPI_HDMI	PHY	ALT5	gpio3.IO[29]	Input with PD
HDMI_REXT	AJ28	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TX0_N	AJ25	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TX0_P	AH25	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TX1_N	AJ26	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TX1_P	AH26	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TX2_N	AJ27	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TX2_P	AH27	VDD_HDMI_1P8	PHY	—	—	—
HDMI_TXC_N	AJ24	VDD_HDMI_1P8	PHY	—	—	—

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
HDMI_TXC_P	AH24	VDD_HDMI_1P8	PHY	—	—	—
I2C1_SCL	AC8	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[14]	Input with PD
I2C1_SDA	AH7	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[15]	Input with PD
I2C2_SCL	AH6	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[16]	Input with PD
I2C2_SDA	AE8	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[17]	Input with PD
I2C3_SCL	AJ7	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[18]	Input with PD
I2C3_SDA	AJ6	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[19]	Input with PD
I2C4_SCL	AF8	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[20]	Input with PD
I2C4_SDA	AD8	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[21]	Input with PD
JTAG_MOD	G20	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.MOD	Input with PD
JTAG_TCK	G18	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TCK	Input with PU
JTAG_TDI	G16	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TDI	Input with PU
JTAG_TDO	F14	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TDO	Input with PU
JTAG_TMS	G14	NVCC_JTAG	GPIO	ALT0	cjtag_wrapper.TMS	Input with PU
LVDS0_CLK_N	G28	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_CLK_P	F29	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D0_N	E28	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D0_P	D29	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D1_N	F28	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D1_P	E29	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D2_N	H28	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D2_P	G29	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D3_N	J28	VDD_LVDS_1P8	PHY	—	—	—
LVDS0_D3_P	H29	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_CLK_N	B28	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_CLK_P	A28	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D0_N	B26	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D0_P	A26	VDD_LVDS_1P8	PHY	—	—	—

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
LVDS1_D1_N	B27	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D1_P	A27	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D2_N	C28	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D2_P	B29	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D3_N	D28	VDD_LVDS_1P8	PHY	—	—	—
LVDS1_D3_P	C29	VDD_LVDS_1P8	PHY	—	—	—
MIPI_CSI1_CLK_N	E22	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_CLK_P	D22	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D0_N	E18	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D0_P	D18	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D1_N	E20	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D1_P	D20	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D2_N	E24	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D2_P	D24	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D3_N	E26	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI1_D3_P	D26	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_CLK_N	B23	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_CLK_P	A23	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D0_N	B25	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D0_P	A25	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D1_N	B24	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D1_P	A24	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D2_N	B22	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D2_P	A22	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D3_N	B21	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_CSI2_D3_P	A21	VDD_MIPI_1P8	PHY	—	—	Input
MIPI_DSI1_CLK_N	B18	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_CLK_P	A18	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D0_N	B16	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D0_P	A16	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D1_N	B17	VDD_MIPI_1P8	PHY	—	—	Output low

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
MIPI_DSI1_D1_P	A17	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D2_N	B19	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D2_P	A19	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D3_N	B20	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_DSI1_D3_P	A20	VDD_MIPI_1P8	PHY	—	—	Output low
MIPI_VREG1_CAP	F18	VDD_MIPI_1P8	PHY	—	—	Output
MIPI_TEST_DNU	F24	VDD_MIPI_1P8	PHY	—	—	—
NAND_ALE	N25	NVCC_NAND	GPIO	ALT5	gpio3.IO[0]	Input with PD
NAND_CE0_B	L26	NVCC_NAND	GPIO	ALT5	gpio3.IO[1]	Input with PD
NAND_CE1_B	T29	NVCC_NAND	GPIO	ALT5	gpio3.IO[2]	Input with PD
NAND_CE2_B	P28	NVCC_NAND	GPIO	ALT5	gpio3.IO[3]	Input with PD
NAND_CE3_B	N28	NVCC_NAND	GPIO	ALT5	gpio3.IO[4]	Input with PD
NAND_CLE	M28	NVCC_NAND	GPIO	ALT5	gpio3.IO[5]	Input with PD
NAND_DATA00	R25	NVCC_NAND	GPIO	ALT5	gpio3.IO[6]	Input with PD
NAND_DATA01	L25	NVCC_NAND	GPIO	ALT5	gpio3.IO[7]	Input with PD
NAND_DATA02	L24	NVCC_NAND	GPIO	ALT5	gpio3.IO[8]	Input with PD
NAND_DATA03	N24	NVCC_NAND	GPIO	ALT5	gpio3.IO[9]	Input with PD
NAND_DATA04	P29	NVCC_NAND	GPIO	ALT5	gpio3.IO[10]	Input with PD
NAND_DATA05	N29	NVCC_NAND	GPIO	ALT5	gpio3.IO[11]	Input with PD
NAND_DATA06	M29	NVCC_NAND	GPIO	ALT5	gpio3.IO[12]	Input with PD
NAND_DATA07	R29	NVCC_NAND	GPIO	ALT5	gpio3.IO[13]	Input with PD
NAND_DQS	R26	NVCC_NAND	GPIO	ALT5	gpio3.IO[14]	Input with PD
NAND_RE_B	R28	NVCC_NAND	GPIO	ALT5	gpio3.IO[15]	Input with PD
NAND_READY_B	T28	NVCC_NAND	GPIO	ALT5	gpio3.IO[16]	Input with PD
NAND_WE_B	U28	NVCC_NAND	GPIO	ALT5	gpio3.IO[17]	Input with PD
NAND_WP_B	U29	NVCC_NAND	GPIO	ALT5	gpio3.IO[18]	Input with PD
ONOFF	G22	NVCC_SNVS	GPIO	ALT0	snvsmix.ONOFF	Input with PU
PCIE_REF_PAD_CLK_N	E16	VDD_PCI_1P8	PHY	—	—	High-Z
PCIE_REF_PAD_CLK_P	D16	VDD_PCI_1P8	PHY	—	—	High-Z
PCIE_RESREF	F16	VDD_PCI_1P8	PHY	—	—	High-Z
PCIE_RXN_N	B14	VDD_PCI_1P8	PHY	—	—	Input, High-Z

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
PCIE_RXN_P	A14	VDD_PCI_1P8	PHY	—	—	Input, High-Z
PCIE_TXN_N	B15	VDD_PCI_1P8	PHY	—	—	Output, High-Z
PCIE_TXN_P	A15	VDD_PCI_1P8	PHY	—	—	Output, High-Z
PMIC_ON_REQ	F22	NVCC_SNVS	GPIO	ALT0	snvsmix.PMIC_ON_REQ	Output high with PU
PMIC_STBY_REQ	J24	NVCC_SNVS	GPIO	ALT0	ccmsrcgpcmix.PMIC_STBY_REQ	Output low with PD
POR_B	J29	NVCC_SNVS	GPIO	ALT0	snvsmix.POR_B	Input with PU
RTC_XTALI	J25	NVCC_SNVS	ANALOG	ALT0	snvsmix.RTC	Input
RTC_XTALO	J26	NVCC_SNVS	ANALOG	—	—	Output, inverted of RTC_XTALI
SAI1_MCLK	AE12	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[20]	Input with PD
SAI1_RXC	AH8	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[1]	Input with PD
SAI1_RXD0	AC10	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[2]	Input with PD
SAI1_RXD1	AF10	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[3]	Input with PD
SAI1_RXD2	AH9	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[4]	Input with PD
SAI1_RXD3	AJ8	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[5]	Input with PD
SAI1_RXD4	AD10	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[6]	Input with PD
SAI1_RXD5	AE10	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[7]	Input with PD
SAI1_RXD6	AH10	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[8]	Input with PD
SAI1_RXD7	AH12	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[9]	Input with PD
SAI1_RXFS	AJ9	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[0]	Input with PD
SAI1_TXC	AJ12	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[11]	Input with PD
SAI1_TXD0	AJ11	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[12]	Input with PD
SAI1_TXD1	AJ10	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[13]	Input with PD
SAI1_TXD2	AH11	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[14]	Input with PD
SAI1_TXD3	AD12	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[15]	Input with PD
SAI1_TXD4	AH13	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[16]	Input with PD
SAI1_TXD5	AH14	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[17]	Input with PD
SAI1_TXD6	AC12	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[18]	Input with PD
SAI1_TXD7	AJ13	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[19]	Input with PD

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
SAI1_TXFS	AF12	NVCC_SAI1_SAI5	GPIO	ALT5	gpio4.IO[10]	Input with PD
SAI2_MCLK	AJ15	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[27]	Input with PD
SAI2_RXC	AJ16	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[22]	Input with PD
SAI2_RXD0	AJ14	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[23]	Input with PD
SAI2_RXFS	AH17	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[21]	Input with PD
SAI2_TXC	AH15	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[25]	Input with PD
SAI2_TXD0	AH16	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[26]	Input with PD
SAI2_TXFS	AJ17	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[24]	Input with PD
SAI3_MCLK	AJ20	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio5.IO[2]	Input with PD
SAI3_RXC	AJ18	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[29]	Input with PD
SAI3_RXD	AF18	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[30]	Input with PD
SAI3_RXFS	AJ19	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[28]	Input with PD
SAI3_TXC	AH19	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio5.IO[0]	Input with PD
SAI3_TXD	AH18	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio5.IO[1]	Input with PD
SAI3_TXFS	AC16	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio4.IO[31]	Input with PD
SAI5_MCLK	AF14	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[25]	Input with PD
SAI5_RXC	AD14	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[20]	Input with PD
SAI5_RXD0	AE16	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[21]	Input with PD
SAI5_RXD1	AD16	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[22]	Input with PD
SAI5_RXD2	AF16	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[23]	Input with PD
SAI5_RXD3	AE14	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[24]	Input with PD
SAI5_RXFS	AC14	NVCC_SAI1_SAI5	GPIO	ALT5	gpio3.IO[19]	Input with PD
SD1_CLK	W28	NVCC_SD1	GPIO	ALT5	gpio2.IO[0]	Input with PD
SD1_CMD	W29	NVCC_SD1	GPIO	ALT5	gpio2.IO[1]	Input with PD
SD1_DATA0	Y29	NVCC_SD1	GPIO	ALT5	gpio2.IO[2]	Input with PD
SD1_DATA1	Y28	NVCC_SD1	GPIO	ALT5	gpio2.IO[3]	Input with PD
SD1_DATA2	V29	NVCC_SD1	GPIO	ALT5	gpio2.IO[4]	Input with PD
SD1_DATA3	V28	NVCC_SD1	GPIO	ALT5	gpio2.IO[5]	Input with PD
SD1_DATA4	U26	NVCC_SD1	GPIO	ALT5	gpio2.IO[6]	Input with PD
SD1_DATA5	AA29	NVCC_SD1	GPIO	ALT5	gpio2.IO[7]	Input with PD
SD1_DATA6	AA28	NVCC_SD1	GPIO	ALT5	gpio2.IO[8]	Input with PD

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
SD1_DATA7	U25	NVCC_SD1	GPIO	ALT5	gpio2.IO[9]	Input with PD
SD1_RESET_B	W25	NVCC_SD1	GPIO	ALT5	gpio2.IO[10]	Input with PD
SD1_STROBE	W26	NVCC_SD1	GPIO	ALT5	gpio2.IO[11]	Input with PD
SD2_CD_B	AD29	NVCC_SD2	GPIO	ALT5	gpio2.IO[12]	Input with PD
SD2_CLK	AB29	NVCC_SD2	GPIO	ALT5	gpio2.IO[13]	Input with PD
SD2_CMD	AB28	NVCC_SD2	GPIO	ALT5	gpio2.IO[14]	Input with PD
SD2_DATA0	AC28	NVCC_SD2	GPIO	ALT5	gpio2.IO[15]	Input with PD
SD2_DATA1	AC29	NVCC_SD2	GPIO	ALT5	gpio2.IO[16]	Input with PD
SD2_DATA2	AA26	NVCC_SD2	GPIO	ALT5	gpio2.IO[17]	Input with PD
SD2_DATA3	AA25	NVCC_SD2	GPIO	ALT5	gpio2.IO[18]	Input with PD
SD2_RESET_B	AD28	NVCC_SD2	GPIO	ALT5	gpio2.IO[19]	Input with PD
SD2_WP	AC26	NVCC_SD2	GPIO	ALT5	gpio2.IO[20]	Input with PD
SPDIF_EXT_CLK	AC18	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio5.IO[5]	Input with PD
SPDIF_RX	AD18	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio5.IO[4]	Input with PD
SPDIF_TX	AE18	NVCC_SAI2_SAI3_SPDIF	GPIO	ALT5	gpio5.IO[3]	Input with PD
UART1_RXD	AD6	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[22]	Input with PD
UART1_TXD	AJ3	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[23]	Input with PD
UART2_RXD	AF6	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[24]	Input with PD
UART2_TXD	AH4	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[25]	Input with PD
UART3_RXD	AE6	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[26]	Input with PD
UART3_TXD	AJ4	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[27]	Input with PD
UART4_RXD	AJ5	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[28]	Input with PD
UART4_TXD	AH5	NVCC_I2C_UART	GPIO	ALT5	gpio5.IO[29]	Input with PD
USB1_D_N	E10	VDD_USB_3P3	PHY	—	—	Input
USB1_D_P	D10	VDD_USB_3P3	PHY	—	—	Input
USB1_DNU	B11	VDD_USB_3P3	PHY	—	—	—
USB1_RX_N	B9	VDD_USB_3P3	PHY	—	—	Input
USB1_RX_P	A9	VDD_USB_3P3	PHY	—	—	Input
USB1_TX_N	B10	VDD_USB_3P3	PHY	—	—	Output
USB1_TX_P	A10	VDD_USB_3P3	PHY	—	—	Output
USB1_TXRTUNE	F10	VDD_USB_3P3	PHY	—	—	Input

Table 77. 15 x 15 mm functional contact assignments (continued)

Ball Name	Ball	Power group	Ball type	Reset condition		
				Default	Default function	Input/ Output status
USB1_VBUS	A11	VDD_USB_3P3	PHY	—	—	Input
USB2_D_N	E14	VDD_USB_3P3	PHY	—	—	Input
USB2_D_P	D14	VDD_USB_3P3	PHY	—	—	Input
USB2_DNU	E12	VDD_USB_3P3	PHY	—	—	—
USB2_RX_N	B12	VDD_USB_3P3	PHY	—	—	Input
USB2_RX_P	A12	VDD_USB_3P3	PHY	—	—	Input
USB2_TX_N	B13	VDD_USB_3P3	PHY	—	—	Output
USB2_TX_P	A13	VDD_USB_3P3	PHY	—	—	Output
USB2_TXRTUNE	F12	VDD_USB_3P3	PHY	—	—	—
USB2_VBUS	D12	VDD_USB_3P3	PHY	—	—	Input
XTALI_24M	G25	VDD_24M_XTAL_1P8	ANALOG	—	—	Input
XTALO_24M	G26	VDD_24M_XTAL_1P8	ANALOG	—	—	Output

5.1.3 i.MX 8M Plus 15 x 15 mm 0.5 mm pitch ball map

Table 78 shows the i.MX 8M Plus 15 x 15 mm 0.5 mm pitch ball map.

Table 78. 15 x 15 mm, 0.5 mm pitch ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	VSS	DRAM_DQ01	GPIO1_IO06	GPIO1_IO14	GPIO1_IO12	GPIO1_IO13	GPIO1_IO00	GPIO1_IO08	USB1_RX_P	USB1_TX_P	USB1_VBUS	USB2_RX_P	USB2_TX_P	PCIE_RXN_P	PCIE_TXN_P	MIPI_DSI1_D0_P	MIPI_DSI1_D1_P	MIPI_DSI1_CLK_P	MIPI_DSI1_D2_P	MIPI_DSI1_D3_P	MIPI_CSI2_D3_P	MIPI_CSI2_D2_P	MIPI_CSI2_CLK_P	MIPI_CSI2_D1_P	MIPI_CSI2_D0_P	LVDS1_D0_P	LVDS1_D1_P	LVDS1_CLK_P	VSS	A
B	DRAM_DQ07	DRAM_DM0	DRAM_DQ00	GPIO1_IO05	GPIO1_IO15	GPIO1_IO02	GPIO1_IO10	GPIO1_IO09	USB1_RX_N	USB1_TX_N	USB1_DNU[1]	USB2_RX_N	USB2_TX_N	PCIE_RXN_N	PCIE_TXN_N	MIPI_DSI1_D0_N	MIPI_DSI1_D1_N	MIPI_DSI1_CLK_N	MIPI_DSI1_D2_N	MIPI_DSI1_D3_N	MIPI_CSI2_D3_N	MIPI_CSI2_D2_N	MIPI_CSI2_CLK_N	MIPI_CSI2_D1_N	MIPI_CSI2_D0_N	LVDS1_D0_N	LVDS1_D1_N	LVDS1_CLK_N	LVDS1_D2_P	B
C	DRAM_DQ05	DRAM_DQ06		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		LVDS1_D2_N	LVDS1_D3_P	C

Table 78. 15 x 15 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
D	DRAM_DQS0_N	DRAM_DQS0_P		DRAM_AC11		GPIO1_IO03		GPIO1_IO11		USB1_D_P		USB2_VBUS		USB2_D_P		PCIE_REF_PAD_CLK_P		MIPI_CSI1_D0_P		MIPI_CSI1_D1_P		MIPI_CSI1_CLK_P		MIPI_CSI1_D2_P		MIPI_CSI1_D3_P		LVDS1_D3_N	LVDS0_D0_P	D
E	DRAM_DQ02	DRAM_DQ04	VSS	DRAM_AC10		GPIO1_IO04		GPIO1_IO01		USB1_D_N		USB2_DNU[2]		USB2_D_N		PCIE_REF_PAD_CLK_N		MIPI_CSI1_D0_N		MIPI_CSI1_D1_N		MIPI_CSI1_CLK_N		MIPI_CSI1_D2_N		MIPI_CSI1_D3_N	VSS	LVDS0_D0_N	LVDS0_D1_P	E
F	DRAM_DQ15	DRAM_DQ03				GPIO1_IO07		BOOT_MODE1		USB1_TXRTUNE		USB2_TXRTUNE		JTAG_TDO		PCIE_RESREF		MIPI_VREG1_CAP		VDD_MIPI_1P2_CAP		PMIC_ON_REQ		MIPI_TEST_DNU[3]				LVDS0_D1_N	LVDS0_CLK_P	F
G	DRAM_DQ08	DRAM_DQ14	VSS	DRAM_AC06	DRAM_AC01	VSS		BOOT_MODE2		BOOT_MODE0		BOOT_MODE3		JTAG_TMS		JTAG_TDI		JTAG_TCK		JTAG_MOD		ONOFF		VSS	XTALI_24M	XTALO_24M	VSS	LVDS0_CLK_N	LVDS0_D2_P	G
H	DRAM_DQ09	DRAM_DM1						VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS						LVDS0_D2_N	LVDS0_D3_P	H
J	DRAM_DQS1_N	DRAM_DQS1_P	VSS	DRAM_AC03	DRAM_AC07	DRAM_AC00	VSS	NVCC_DRAM		NVCC_DRAM	NVCC_GPIO			VDD_USB_3P3		PVCC0_1P8			VDD_USB_1P8	VDD_ANA0_1P8		VDD_LVDS_1P8	VSS	PMIC_STBY_REQ	RTC_XTALI	RTC_XTALO	VSS	LVDS0_D3_N	POR_B	J
K	DRAM_DQ10	DRAM_DQ11								VDD_SOC	NVCC_JTAG			VDD_USB_0P8	VDD_PCI_0P8	VDD_MIPI_0P8			VDD_PCI_1P8	VDD_MIPI_1P8								CLKIN1	CLKOUT1	K

Table 78. 15 x 15 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
L	DRAM_DQ13	DRAM_DQ12	VSS	DRAM_AC09	DRAM_AC14	DRAM_AC08	VSS	NVCC_DRAM	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VSS		VSS	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_24M_XTAL_1P8	VSS	NAND_DATA02	NAND_DATA01	NAND_CE0_B	VSS	CLKIN2	CLKOUT2	L
M	DRAM_AC04	DRAM_AC05									VSS			VDD_SOC		VDD_SOC			VSS									NAND_CLE	NAND_DATA06	M
N	DRAM_AC16	DRAM_AC17	VSS	DRAM_AC12	DRAM_AC13	DRAM_AC02	VSS	NVCC_DRAM	VDD_SOC	VDD_SOC	VSS	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VSS	VDD_SOC	VDD_SOC	VDD_ANA1_1P8	VSS	NAND_DATA03	NAND_ALE	VDD_SNVS_0P8_CAP	VSS	NAND_CE3_B	NAND_DATA05	N
P	DRAM_AC26	DRAM_AC19									VSS			VDD_SOC		VDD_SOC			VSS									NAND_CE2_B	NAND_DATA04	P
R	DRAM_ZN	DRAM_VREF	VSS	DRAM_AC27	DRAM_AC15	VDD_DRAM_PLL_1P8	VSS	NVCC_DRAM	VDD_DRAM_PLL_0P8	VDD_SOC	VSS	VSS	VSS	VSS		VSS	VSS	VSS	VSS	VSS	VDD_SOC	VDD_ANA1_0P8	NVCC_CLK	VSS	NVCC_SNVS_1P8	NAND_DATA00	NAND_DQS	VSS	NAND_RE_B	NAND_DATA07	R
T	DRAM_RESET_N	DRAM_ALERT_N									VSS			VDD_ARM		VDD_ARM			VSS									NAND_READY_B	NAND_CE1_B	T

Table 78. 15 x 15 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AC	DRAM_DQ16	DRAM_DQ22	VSS	DRAM_AC37	DRAM_AC38	VSS		I2C1_SCL		SAI1_RXD0		SAI1_TXD6		SAI5_RXFS		SAI3_TXFS		SPDIF_EXT_CLK		ECSPI1_MOSI		HDMI_DDC_SCL		VSS	ENET_TD0	SD2_WP	VSS	SD2_DATA0	SD2_DATA1	**AC**
AB	DRAM_DQ17	DRAM_DM2	VSS					VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS						SD2_CMD	SD2_CLK	**AB**
AA	DRAM_DQS2_N	DRAM_DQS2_P	VSS	DRAM_AC20	DRAM_AC21	DRAM_AC22	VSS	NVCC_DRAM		NVCC_DRAM	NVCC_SAI2_SAI3_SPDIF			NVCC_ECSPI_HDMI		PVCC2_1P8			PVCC1_1P8	VDD_EARC_1P8		VDD_HDMI_1P8	VSS	NVCC_ENET	SD2_DATA3	SD2_DATA2	VSS	SD1_DATA6	SD1_DATA5	**AA**
Y	DRAM_DQ20	DRAM_DQ19								NVCC_I2C_UART	NVCC_SAI1_SAI5			VDD_ARM	VDD_ARM	VDD_ARM			VDD_ARM_PLL_1P8	VDD_ANA2_1P8								SD1_DATA1	SD1_DATA0	**Y**
W	DRAM_DQ21	DRAM_DQ18	VSS	DRAM_AC28	DRAM_AC29	DRAM_AC36	VSS	NVCC_DRAM	VDD_SOC	VDD_SOC	VDD_SOC	VDD_ARM	VDD_ARM	VSS		VSS	VDD_ARM	VDD_SAI_PLL_1P8	VDD_AVPLL_1P8	VDD_SOC	VDD_ARM_PLL_0P8	VDD_HDMI_0P8	VSS	NVCC_SD2	SD1_RESET_B	SD1_STROBE	VSS	SD1_CLK	SD1_CMD	**W**
V	DRAM_AC25	DRAM_AC24									VSS			VDD_ARM		VDD_ARM			VSS										SD1_DATA3	SD1_DATA2	**V**
U	DRAM_AC34	DRAM_AC35	VSS	DRAM_AC23	DRAM_AC32	DRAM_AC33	VSS	NVCC_DRAM	VDD_SOC	VDD_SOC	VSS	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VDD_ARM	VSS	VSS	VDD_SOC	VDD_SAI_PLL_0P8	NVCC_NAND	VSS	NVCC_SD1	SD1_DATA7	SD1_DATA4	VSS	NAND_WE_B	NAND_WP_B	**U**

Table 78. 15 x 15 mm, 0.5 mm pitch ball map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AD	DRAM_DQ23	DRAM_DQ27				UART1_RXD		I2C4_SDA		SAI1_RXD4		SAI1_TXD3		SAI5_RXC		SAI5_RXD1		SPDIF_RX		ECSPI1_MISO		HDMI_CEC		ENET_TD3				SD2_RESET_B	SD2_CD_B	**AD**
AE	DRAM_DQ26	DRAM_DQ28	VSS	DRAM_AC30		UART3_RXD		I2C2_SDA		SAI1_RXD5		SAI1_MCLK		SAI5_RXD3		SAI5_RXD0		SPDIF_TX		ECSPI1_SS0		HDMI_HPD		ENET_TXC		ENET_TD1	VSS	ENET_RX_CTL	ENET_RXC	**AE**
AF	DRAM_DQS3_N	DRAM_DQS3_P		DRAM_AC31		UART2_RXD		I2C4_SCL		SAI1_RXD1		SAI1_TXFS		SAI5_MCLK		SAI5_RXD2		SAI3_RXD		ECSPI1_SCLK		HDMI_DDC_SDA		ENET_TX_CTL		ENET_TD2		ENET_RD3	ENET_RD2	**AF**
AG	DRAM_DQ29	DRAM_DQ30		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS		ENET_RD1	ENET_RD0	**AG**
AH	DRAM_DQ31	DRAM_DM3	DRAM_DQ24	UART2_TXD	UART4_TXD	I2C2_SCL	I2C1_SDA	SAI1_RXC	SAI1_RXD2	SAI1_RXD6	SAI1_TXD2	SAI1_RXD7	SAI1_TXD4	SAI1_TXD5	SAI2_TXC	SAI2_TXD0	SAI2_RXFS	SAI3_TXD	SAI3_TXC	ECSPI2_MISO	ECSPI2_SCLK	EARC_N_HPD	EARC_AUX	HDMI_TXC_P	HDMI_TX0_P	HDMI_TX1_P	HDMI_TX2_P	ENET_MDC	ENET_MDIO	**AH**
AJ	VSS	DRAM_DQ25	UART1_TXD	UART3_TXD	UART4_RXD	I2C3_SDA	I2C3_SCL	SAI1_RXD3	SAI1_RXFS	SAI1_TXD1	SAI1_TXD0	SAI1_TXC	SAI1_TXD7	SAI2_RXD0	SAI2_MCLK	SAI2_RXC	SAI2_TXFS	SAI3_RXC	SAI3_RXFS	SAI3_MCLK	ECSPI2_MOSI	ECSPI2_SS0	EARC_P_UTIL	HDMI_TXC_N	HDMI_TX0_N	HDMI_TX1_N	HDMI_TX2_N	HDMI_REXT	VSS	**A1**

1 Do not use.

2 Do not use.

3 Do not use, NXP internal test only.

5.2 DDR pin function list

Table 79 shows the DDR pin function list.

Table 79. DDR pin function list

Ball name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A

Table 79. DDR pin function list (continued)

Ball name	LPDDR4	DDR4
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ08_A	DQU0_A
DRAM_DQ09	DQ09_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B

Table 79. DDR pin function list (continued)

Ball name	LPDDR4	DDR4
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ08_B	DQU0_B
DRAM_DQ25	DQ09_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	—	ACT_n
DRAM_AC07	—	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	—	A4
DRAM_AC15	—	A3
DRAM_AC16	—	CK_t_A
DRAM_AC17	—	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B

Table 79. DDR pin function list (continued)

Ball name	LPDDR4	DDR4
DRAM_AC22	CS1_B	—
DRAM_AC23	CS0_B	—
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	—	BA1
DRAM_AC27	—	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34	—	WE_n / A14
DRAM_AC35	—	RAS_n / A16
DRAM_AC36	—	ODT0
DRAM_AC37	—	ODT1
DRAM_AC38	—	CS1_n
DRAM_ZN_SENSE	ZQ	ZQ
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

6 Revision history

Table 80 provides a revision history for this data sheet.,

Table 80. Revision history

Rev.number	Date	Substantive change(s)
Rev. 0	03/2021	• Initial version

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