MLX75411, MLX75412

Avocet HDR Image Sensors Datasheet

Features and Benefits

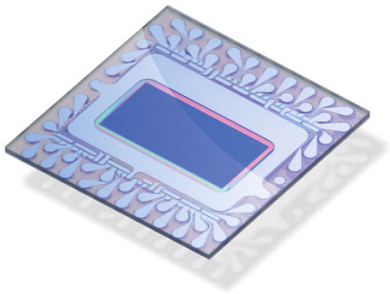
- 1024 x 512 pixels CMOS image sensor
- 154dB Extended HDR
- Low noise, low power rolling shutter
- 1/3" Optical format for 1024x512
- 1/4" Optical format with VGA subwindow
- Monochrome, RCCC, Standard Bayer (RGBG) or special Bayer (RGBi)
- Parallel data output
  8/10/12 bits + CLK/HSYNC/VSYNC
- Operating Temperature Range:
  -40C to +85°C full performance
  -40C to +115°C reduced performance
- Storage Temperature Range:
  -40°C to +125°C
- Automotive Qualified AEC-Q100

Application Examples

- Advanced Driver Assistance Systems (ADAS)
  - Lane departure warning (LDW)
  - Forward collision warning (FCW)
  - Automatic high-beam assist
  - Pedestrian Detection for Autonomous Emergency Braking (AEB)
- Cameras on trucks, trains, busses, emergency vehicles, agricultural vehicles, autonomous vehicles, heavy off-road vehicles
- Night vision cameras
- HDR surveillance cameras
- Traffic monitoring cameras
- Fleet Safety/ Black-box cameras

Additionally for MLX75412

- On-chip Autobrite® auto-exposure (AE) and auto-HDR. This high performing function automatically sets the best exposure and HDR setting on a frame by frame basis.
- On-chip Autoview™ histogram remapping. This function optimizes 8 bit performance, for display-based applications for example.



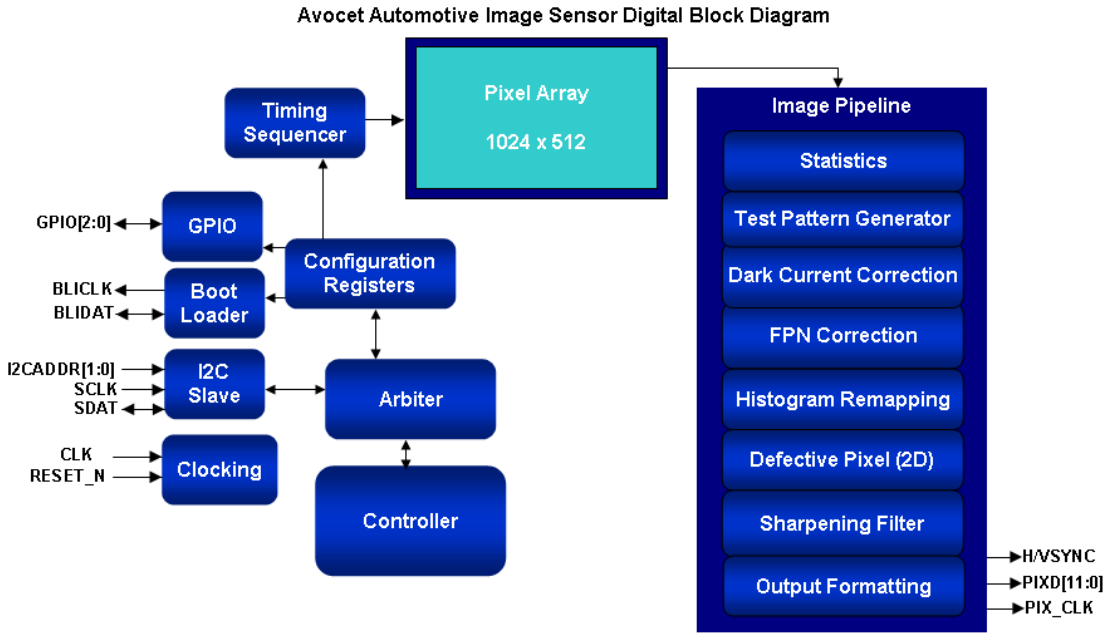
Ordering Information

Ordering code: Part No. - Temperature Code & Package Code - Option code - Packaging code

Part No. :	MLX75411 or MLX75412
Temperature Code:	V (-40°C to 115 °C)
Package Code:	TF (glass-BGA) or UC (wafer)
Option Code:	MAA-000 (monochrome version) or RAA-000 (RCCC version) or GAA-000 (RGBG version) or IAA-000 (RGBi version)
Packaging Code:	TR (for Glass-BGA parts) or WB (for wafers)

Example: MLX75412 – VTF-MAA-000-TR

1 Functional Diagram



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2 General Description

The Avocet image sensor integrates a high-sensitivity array, a feature-rich digital processor for monochrome images and camera control functions into a single chip.

In a monochrome system, image processing is performed on the Avocet as a single chip solution.

In a color system Avocet acts as a slave in a system controlled by a separate Image Signal Processor chip through one of the external interfaces delivering raw single images or video-like streams of color Bayer-patterned images. The sensor captures the images at the required speed, exposure, and gain, and the external device is responsible for all further image processing such as color demosaicing and white balance.

Table of Contents

3 Glossary of Terms.

HDR	High Dynamic Range
FOV	Field of View
CRA	Chief Ray Angle
NIR	Near Infrared Light

4 Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Analog supply voltage	V_{dda}	3.3 ± 5%	V
I/O supply voltage	V_{ddio}	3.3 ± 5%	V
Digital supply voltage	V_{ddd}	1.8 ± 5%	V
Storage Temperature	T_{stg}	-40 to +125	°C
Operational Temperature	T_{opl}	-40 to +115	°C

Table 1: Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5 Pin Definitions and Descriptions

Pin №	Name	Type	Function
6, 7, 8, 12, 11, 10, 9, 2, 3, 4, 47, 46	PIXD[11:0]	OUTPUT	Parallel pixel data output bit 11 (MSB) to 0 (LSB)
29	HSYNC	OUTPUT	Line valid. Asserted high when PIXDAT data is valid
15	VSYNC	OUTPUT	Frame valid. Asserted high when PIXDAT data is valid
52	PIXCLK	OUTPUT	Pixel clock out.
26	SDAT	I/O	2-wire slave serial data interface.
25	SCLK	INPUT	2-wire slave serial clock interface.
28	BLIDAT	I/O	2-wire serial boot loader interface data.
27	BLICLK	OUTPUT	2-wire serial boot loader interface clock.
48	ADDR0	INPUT	2-wire slave serial interface address bit select [0]
49	ADDR1	INPUT	2-wire slave serial interface address bit select [1]
34	XTALIN	INPUT	System clock input.
42	RESET_N	INPUT	Active low image sensor reset.
1, 18, 20, 36	VDDA	SUPPLY	Analog power supply 3.3V
5, 32, 38, 54	GNDA	SUPPLY	Analog Power supply ground
17, 37, 55	VDDD	SUPPLY	Digital power supply 1.8V
16, 39, 53	GNDD	SUPPLY	Digital Power supply ground
13, 40, 51	VDDIO	SUPPLY	I/O pad power supply 3.3V
14, 41, 50	GNDIO	SUPPLY	I/O Power supply ground

30	VREFM	REF	Analog reference voltage
31	VREFP	REF	Analog reference voltage
19	VCM	REF	Analog reference voltage
24	GPIO	INPUT	Connect to GND
23	GPIO2	INPUT	Connect to GND
22	GPIO3	INPUT	Connect to GND
45	RSVD_1	INPUT	Connect to GND
44	RSVD_2	INPUT	Connect to GND
43	RSVD_3	INPUT	Connect to GND
21	RSVD_4	I/O	Connect to GND
33	RSVD_5	INPUT	Connect to VDD
35	RSVD_6	OUTPUT	Leave unconnected
	NC	N/C	No connection

Table 2: Pin definitions and descriptions

6 General Electrical Specifications

DC Operating Parameters T_A = 25°C, V_{DDIO} = 3.3V ± 5%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH}		2.4	-	VDDIO + 0.3	V
Input low voltage	V_{IL}		-0.3	-	0.8	V
Input leakage current	I_{IN}	No pull-up resistor; Vin =	-2	-	2	uA
Output high voltage	V_{OH}	I_{OH} = -4.0mA	V_{DDIO} – 0.4	-	-	V
Output low voltage	V_{OL}	I_{OL} = 4.0mA	-	-	0.4	V
Output high current	I_{OH}	V_{OH} = VDDIO -0.7	-7	-	-	mA
Output low current	I_{OL}	V_{OL} = 0.7	-	-	7	mA
Analog supply voltage	VDDA	Default settings	3.135	3.3	3.465	V
Analog supply current	I_{DDA}	Default settings;	-	40	60	mA
I/O supply voltage	VDDIO	Default settings	3.135	3.3	3.465	V
I/O supply current	I_{DDIO}	Default settings;	-	9	15	mA
Digital supply voltage	VDDD	Default settings	1.71	1.8	1.89	V
Digital supply current	I_{DDD}	Default settings;	-	30	55	mA

Table 3: Electrical Specifications: DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input system clock frequency	XTALIN		20	27	54	MHz
Clock duty cycle			45	50	55	%
Input clock rise time	t_{RCLK}		0.5	2	3	ns
Input clock fall time	t_{FCLK}		0.5	2	3	ns
XTALIN to PIXCLK propagation delay	t_{PDXP}	C_{LOAD} = 10pF	1.6	2.6	3.5	ns
PIXCLK to valid DOUT[11:0] propagation	t_{PDPD}	C_{LOAD} = 10pF	2.5	3.8	5	ns
Data setup time	t_{SUD}		-1	-0.5	-0.1	ns
Data hold time	t_{HD}		0	0.25	0.5	ns
PIXCLK to HSYNC propagation delay	t_{PDPH}	C_{LOAD} = 10pF	1.2	2.4	3.5	ns
PIXCLK to VSYNC propagation delay	t_{PDPV}	C_{LOAD} = 10pF	1.2	2.4	3.5	ns

Table 4: Electrical Specifications: AC Electrical Characteristics (Non-inverted PIXCLK, default)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input system clock frequency	XTALIN		20	27	54	MHz
Clock duty cycle			45	50	55	%
Input clock rise time	t_{RCLK}		0.5	2	3	ns
Input clock fall time	t_{FCLK}		0.5	2	3	ns
XTALIN to PIXCLK propagation delay	t_{PDXP}	C_{LOAD} = 10pF	10.8	11.8	12.8	ns
PIXCLK to valid DOUT[11:0] propagation	t_{PDPD}	C_{LOAD} = 10pF	-4.5	-6	-6.5	ns
Data setup time	t_{SUD}		4.5	6	6.5	ns
Data hold time	t_{HD}		8	8.5	9	ns
PIXCLK to HSYNC propagation delay	t_{PDPH}	C_{LOAD} = 10pF	-6	-6.5	-7	ns
PIXCLK to VSYNC propagation delay	t_{PDPV}	C_{LOAD} = 10pF	-6	-6.5	-7	ns

Table 5: Electrical Specifications: AC Electrical Characteristics (Inverted PIXCLK, with 18ns clock period)

7 Sensor Specific Specifications

DC Operating Parameters T_A = 25°C, V_{DDIO} = 3.3V ± 5%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Sensitivity	SNR10	@535nm		25		nW/cm^2
Responsivity		@535nm		2.28		e-/DN12
Dark Leakage		T=65 °C		1008		DN12/sec
Number of barriers					6	
Dynamic Range					154	dB
Chief ray angle the sensor has been optimized for.	CRA			10		degrees

Table 6: Specifications: Optical Characteristics

8 Device Overview

8.1 Avocet Sensor Overview

The Avocet image sensor integrates a high-sensitivity array, a feature-rich digital processor for monochrome images and camera control functions into a single chip.

Specification	Avocet	Comments
Active Resolution	1024 x 512	Wider horizontal resolution for next generation ADAS
Optical format	~1/3“(6.45mm)	Center 1/4“ can be used for VGA resolution
Pixel size	5.6µ square	Optimized for sensitivity at 1024x512 resolution
Max frame rate	60fps	At full resolution
Input clock range	20 – 54 MHz	Options for clocking: Crystal input, Oscillator
Exposure time range @ 60fps	12.5µs – 16.7 ms	At 54MHz and 60fps, at full resolution and speed. Minimum barrier time 1.22us.
Control interface	2 Wire Boot Loader Interface	Used to load register settings on recovery from a reset. Must be accessible (for programming of serial PROM) via other control interfaces.
	2 Wire Serial Slave	2-Wire, low speed, serial control interface used for short distances. Supports broadcast writes for writing to multiple imagers.

Video interface	LVTTL	12-bit Monochrome or Raw Color. Pixel clock, vsync and hsync compatible with DSPs. (i.e. TI DaVinci or ADI Blackfin)
Signal processing	Defect pixel interpolation FPN correction Histogram Optimization Dark Current correction Sharpening	Sensor provides on-chip processing required for vision applications or monochrome display applications. (Color processing is not included in on-chip functions.)
Scanning modes	Progressive	Required to support machine vision applications
	Subsample	2x and 4x vertical subsampling
	Subwindow	Single rectangular region. The starting point of the x- and y-address is programmable, as well as the window size.
Sensitivity	SNR10	25nW/cm2 @ 25degC @ 535nm
Responsivity	2.28 e-/DN12	In dark at 25°C 535nm
Dark leakage	1008 DN12/sec	At 65°C

Table 4 - Avocet image sensor highlights

8.2 Sensor Architecture

In a monochrome system, image processing is performed on the Avocet as a single chip solution.

In a color system Avocet acts as a slave in a system controlled by a separate Image Signal Processor chip through one of the external interfaces delivering raw single images or video-like streams of color Bayer-patterned images. The sensor captures the images at the required speed, exposure, and gain, and the external device is responsible for all further image processing such as color demosaicing and white balance.

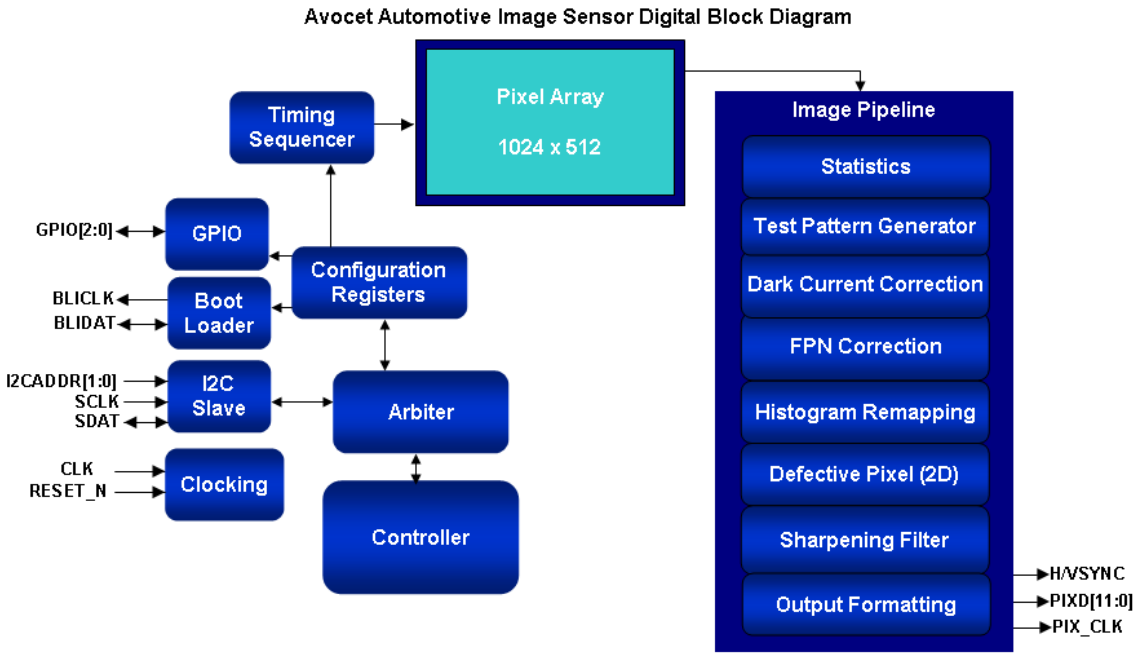


Figure 1 – Avocet Architecture Block Diagram

8.3 Pixel Array Description & Operation

The pixel array is composed from 5.6um square sensing elements. The image sensor operates using an electronic rolling shutter. This maximizes the amount of integration time available by overlapping the readout with the “reset” of a pixel to begin integration.

Avocet operates in an adaptable, programmable Extended High Dynamic Range (HDR) mode maximizing sensitivity while providing uncompromising dynamic range.

The response curve is stretched towards the NIR region, featuring high sensitivity up to 850nm.

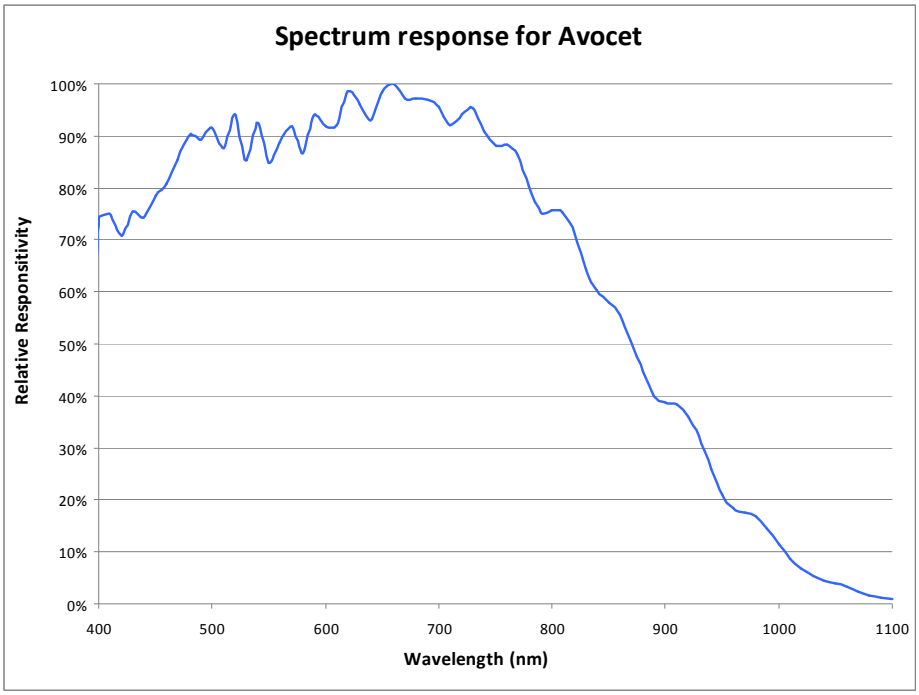


Figure 2 – Avocet spectral response: relative responsitivity

8.4 Avocet Extended High Dynamic Range Principle

To capture up to 154dB of dynamic range in a single frame, the Avocet features a piecewise linear response curve with up to 6 dynamically settable kneepoints.

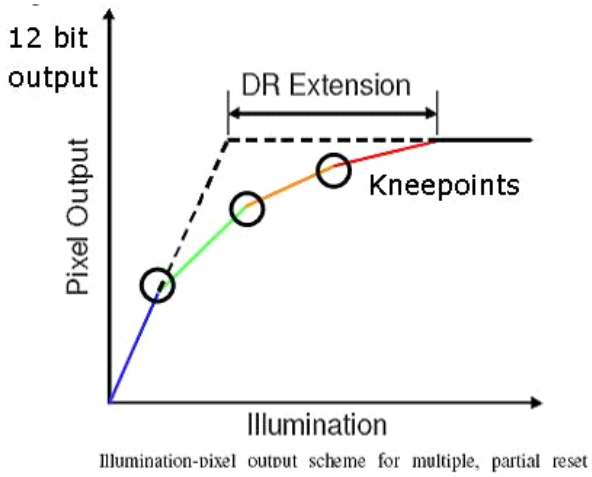


Figure 3 – Avocet HDR Piecewise Linear Response Curve

Every single kneepoint can be manually controlled by the user. With Autobrite, these kneepoints are semi-automatically or fully automatically set by the on-chip control function. The goal of this function is to maximize picture detail content on a frame-by-frame basis and adapt automatically and swiftly to possibly rapid changing light conditions.

Kneepoints are obtained by using the variable height/multiple reset method. Within the time period of the exposure time, all pixels are partially reset for extending dynamic range.

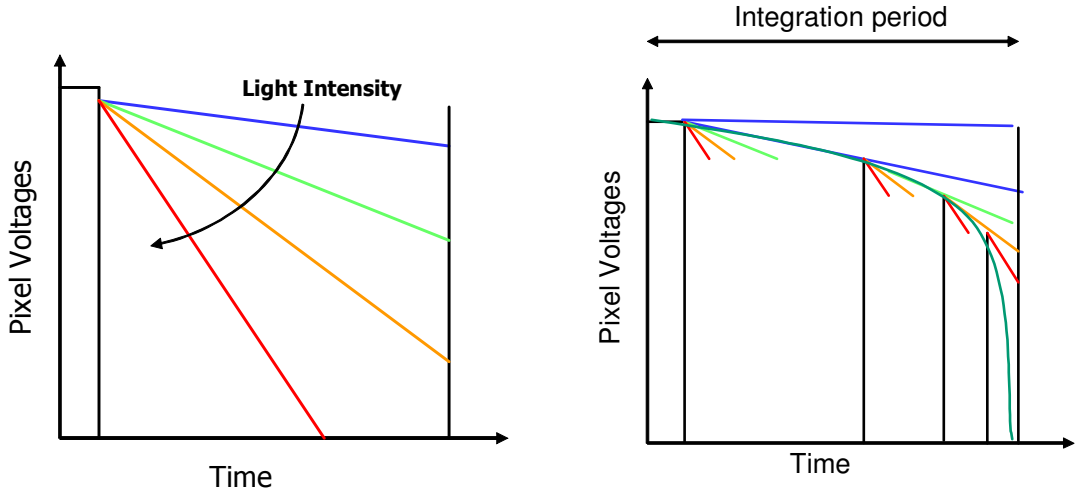


Figure 4 – Kneepoints correspond to voltage barriers for partial reset in the exposure window

So, every kneepoint corresponds to a voltage barrier in the pixel reset mechanism. Every voltage barrier features a barrier height and a barrier position within the time period of the exposure time. In manual mode, the user will set the height and position of up to 6 voltage barriers. In automatic mode, the Autobrite control function does this automatically and dynamically.

With the variable height/multiple reset method, no additional frame buffers or post processing is required. Based on research conducted at the Massachusetts Institute of Technology, Autobrite controls the pixel through Melexis proprietary variable height/multiple reset method. In automatic mode, a complete feedback loop simultaneously controls the integration time and dynamic range expansion for total adaptability and programmability.

8.5 On-chip Algoritms

The image processing algorithms for Avocet are described in this section. Each algorithm is individually controlled with an enable/disable. All of the algorithms also have individual control bits that allow tuning and control of the behavior of the individual algorithms. The Spatial Filtering algorithms are not color aware, and should be disabled if color filters are present.

Algorithm	Description
Autobrite® semi automatic	User only has to set two registers to fully control the sensitivity and response curve
Autobrite® full automatic	An Automatic Exposure (AE) controller that regulates the dynamic range compression and integration time of high-dynamic-range pixels.
Column FPN removal	Uses electrical black from DAC's to compensate for ADC and column circuitry offset mismatches.
Dark Current subtraction	Performed using optical black (dark row) averages.
Spatial Filtering	Done within a single 3x3 kernel
Image Statistics	Feeds image information to apply to the next frame for Autobrite, spatial filtering, and Melexis' histogram optimization
Autoview™	Performs automatic histogram equalization, or gamma correction, or a user-

	programmable transfer function
Context switching	The imager will toggle each frame between two configurations. For cases where the output stream is used by several applications.
Stereo support	To synchronize the output stream of two imagers

Table 5 - On Chip Algorithms

8.5.1 Autobrite Automatic HDR Function (MLX75412 Only)

8.5.1.1 Autobrite® Automatic Mode Feedback Loop

Achieving High Dynamic range through an image sensor with linear response at low illumination and non-linear response at high illumination solves only part of the problem. To complete the solution, the automotive camera must be able to decide which response curve to use. Furthermore, system designers must be able to override the automated decision to customize the response for specific applications. Autobrite uniquely meets these criteria with its key features: adaptability and programmability. Autobrite includes a mechanism to dynamically adjust both the response curve and the total integration time based on the scene being observed. Essentially, the dynamic range is expanded in real time by changing the timing and height of the reset signal. The control mechanism can be configured to automatically adapt to each environment or programmed for a specific application, thereby providing performance that is unmatched by other approaches for achieving High Dynamic range. “Figure 5 – Autobrite® feedback and control mechanism” illustrates the Autobrite control mechanism.

The control loop starts with the image sensor capturing an image. Registers acquire statistics of the scene such as number of pixels that exceed a threshold. A proprietary control mechanism, which can be tailored to a specific application, uses the statistics to select the optimum response curve and integration time. A multiplexing device inputs the signals and allows either the calculated values or user-supplied values to be fed to the voltage and timing control, which generates the barrier voltage(s) for the image sensor. Simultaneously calculating both the integration time and the required dynamic range expansion allows the image sensor to settle on optimal settings very quickly. This fast response time is critical in applications where dramatic changes in the lighting conditions occur quickly, such as the appearance of headlights from other vehicles. Another advantage of this approach is that the collection of the statistics and the control algorithms can be tailored to a specific application. Users can program Autobrite to meet specific requirements of their application.

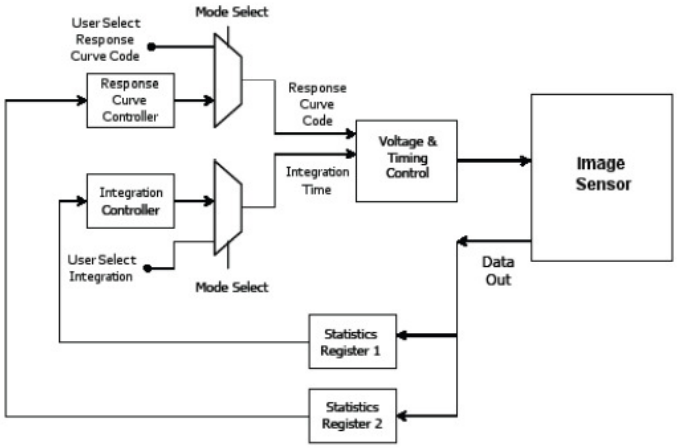


Figure 5 – Autobrite® feedback and control mechanism

For example, system engineers can program Autobrite to:

- Select a specific region of interest within the image frame that Autobrite will use to optimize the integration time and response curve.
- Select a specific integration time and response curve, overriding the automated adjustment.
- Select a maximum integration time or response curve that the automated adjustment is not to exceed.
- Adjust the speed of adaptability to respond more quickly or slowly to lighting changes.
- Manually adjust the height and timing of the barrier voltages.

8.5.1.2 Autobrite® Advantages

Figure 6 provides a side-by-side comparison of images captured with and without Autobrite. In the image on the left, the intra-scene dynamic range clearly exceeds the dynamic range of the camera, resulting in lost details in both the light and dark regions. In the image on the right, Autobrite enables the same scene to be captured with complete visual details even in the extremes of brightness and darkness.

Figure 6 – Images captured without (left) and with (right) Autobrite

8.5.2 Autoview™ Histogram Optimization (MLX75412 Only)

Avocet includes a histogram remapping function that maps from 12 bit pixels to 8 or 10 bit pixels to facilitate data processing and transfer in systems that do not implement the full 12 bit pixels. The algorithm emphasizes areas in the histogram that contain most of the information while compressing areas with limited information.

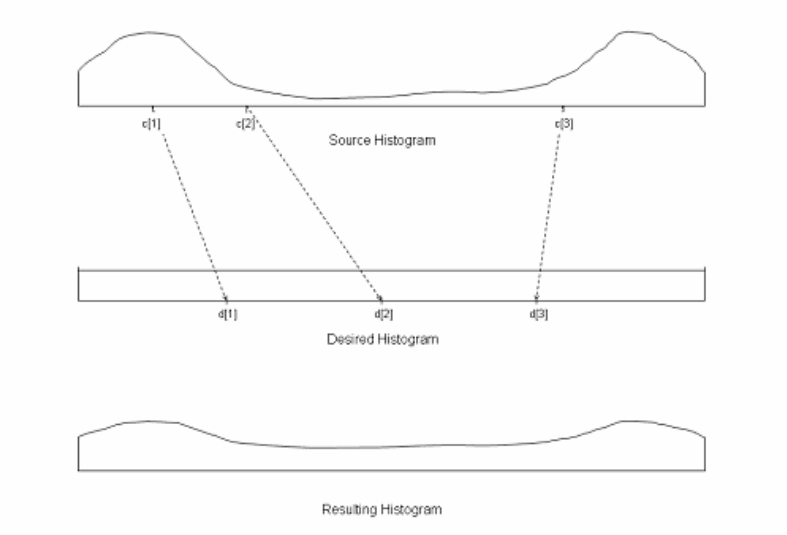


Figure 7 Autoview Histogram Remapping Principle

This is particularly useful in scenes that naturally have a somewhat sparse histogram. An automotive night scene is an example where most of the information is lumped into three luminance bands: headlights and taillights which are very bright; traffic signs that are of medium intensity; and pavement which is relatively dark. By emphasizing the regions containing the most information, 12 bits can be reduced to 8 with a minimum loss of information.

The on-chip hardware is capable of remapping 8 individual segments of the histogram to new areas. Both the offset and the gain of the remapping are controllable through register settings. The automatic algorithm uses the image statistics to calculate remapping constants to provide a good mapping when reducing the number of bits of the pixels.

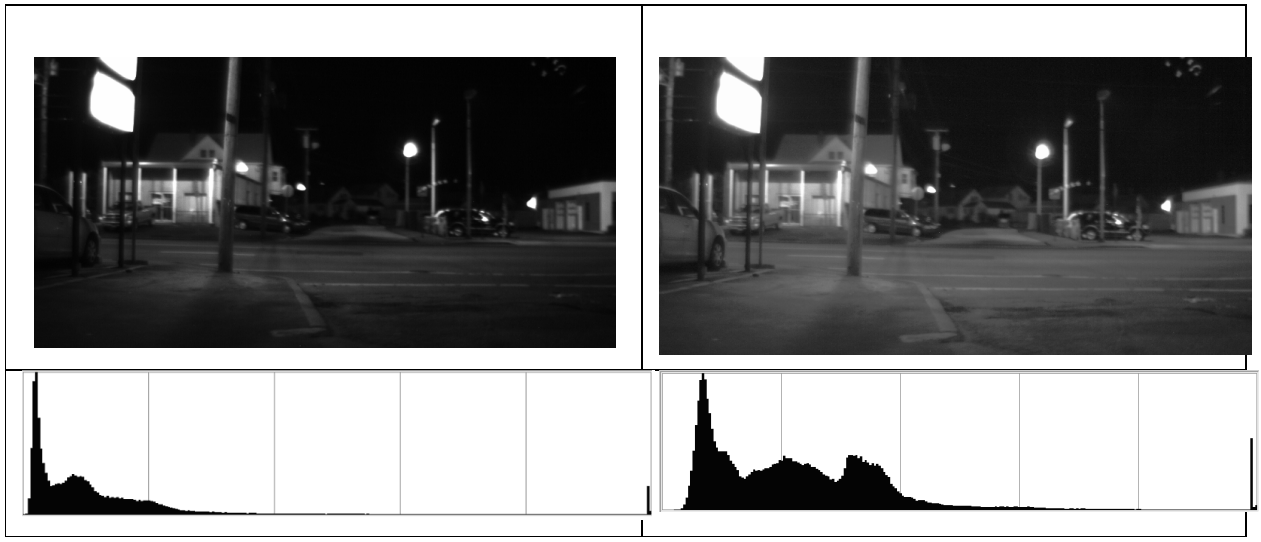


Figure 8: Autoview ON and OFF – Picture and Histogram Example

8.5.3 Spatial Filtering: Sharpening

Sharpening is meant to enhance the contrast differences between adjacent pixels. This has the visual effect of "sharpening" the focus of an image. Below is an example of an image.

Figure 9 – Sharpening Filter (Unsharpened image)

Figure 10 – Sharpening Filter (Sharpened image)

Note: The on-chip sharpening algorithm is not color aware, and should be disabled if color filters are present.

8.6 Interfaces

Avocet has four main interfaces: pixel data output, two wire serial slave, two wire serial master, and GPIO. We refer to table Table 2, page 5 for the complete list of pin descriptions.

NOTES:

1. PIXDAT data is valid on rising edge of pixel clock by default. Pixel clock can be inverted via register write to bit [6] of the output_option_enables register (0x8205).
2. A 2k pullup resistor is required for the boot load interface wires. A minimum128k EEPROM such as Microchips 24LC128 is also required.
3. With default power-up frame dimensions, 27MHz provides 30fps full resolution 1024x512 operation, and 54MHz provides 60fps full resolution 1024x512 operation. Frequency range is up to 54MHz.
4. Avocet has an internal POR (Power On Reset) circuit. Either a reset controller device or an RC filter can be used to adjust the RC ramp time of the reset_n signal as desired.

8.6.1 Pixel data output interface

The image data from Avocet is sent via a pixel interface. The interface is designed to be compatible with standard interfaces to DSP's (TI DaVinci and ADI Blackfin) for image data transfer.

Data is transferred as frames (images), one line at a time from the top of the image to the bottom of the image. Each line is transferred in contiguous data bursts from the left of each line to the right.

The interface consists of the following pins:

- PIXD[11:0] – 12/10/8 bit pixel data interface. In the 10 and 8 bit modes, the lower order bits are not used and are held to zeros.
- HSYNC – This signal indicates horizontal sync or data valid. It can be configured as active high or active low by changing on-chip configuration registers.
- VSYNC – This signal indicates vertical sync. It can be configured as active high or active low by changing on-chip configuration registers.
- PIXCLK – This is the output clock that should be used to clock in HSYNC, VSYNC, and PIXD[11:0] on the receiving end. By default, the output registers are clocked on the rising edge of this clock. This can be changed so that the negative edge corresponds to the data changing by an on-chip configuration register.

8.6.1.1 12/10/8 bit digital video mode (default)

When configured in digital video mode, the chip outputs pixel data on the PIXD bus and signals start of line and frame with HSYNC and VSYNC.

The chip will output one pixel per clock at the input clock rate; with data changing on the rising edge of PIXCLK by default (can be changed to negative edge if desired).

HSYNC will be asserted for every valid pixel of a line (1024 by default), and de-asserted during h-blank and v-blank intervals. By default, h-blank will be for 298 clocks between valid lines.

VSYNC will be asserted for every valid line, and will rise coincident with the rise of the first HSYNC of the frame. It will drop coincident with the fall of the last HSYNC of the frame. By default, Vsync is low for 168 rowtimes.

The digital video timing is as follows:

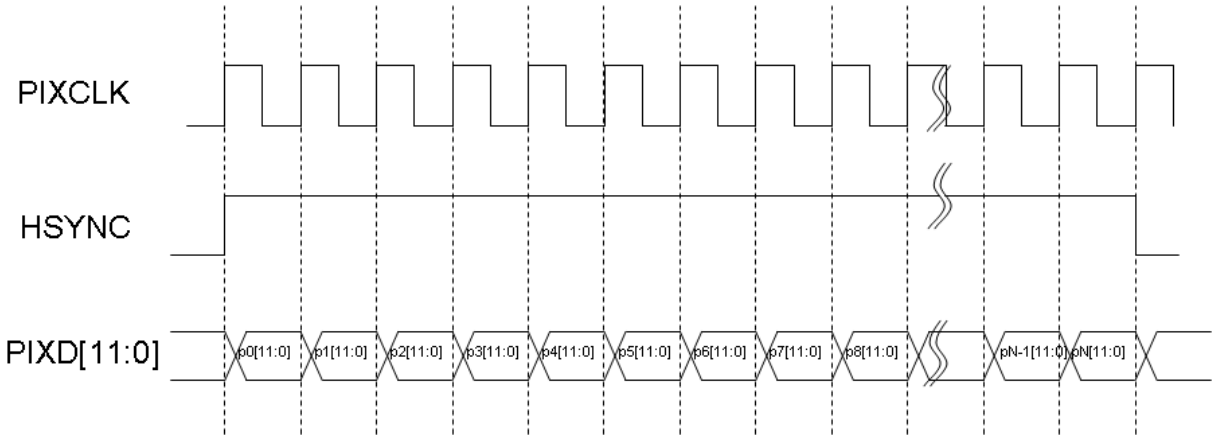


Figure 11 – Digital Video Interface Line Timing

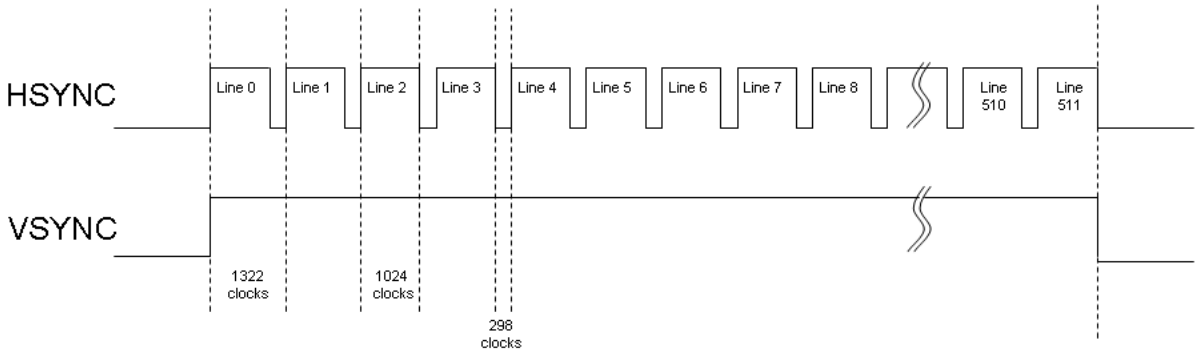


Figure 12 – Digital Video Interface Frame Timing

8.6.2 Two Wire Serial Slave Interface

Avocet provides an interface to all configuration and control of the imager sensor and image processing functions. This two wire interface is comprised of a single clock line and a single data line. A serial protocol is used to address the chip and to read and write data.

8.6.3 Two Wire Boot Loader Interface

Avocet is capable of using an external PROM to control the behavior of the device after power up and to augment the internal processing. It does this through a 2 wire interface that uses the same protocol as the two wire serial slave interface. The only supported use of this interface is for the connection of the external PROM to control the power up behavior. Note: These pins should not be physically connected to the slave interface pins.

8.7 Device power up behavior and initialization

Avocet has an internal power-on reset circuit that will reset the chip after power has reached acceptable levels. After power-on, the user may optionally download a set of application specific register values. These values configure the internal circuitry (analog bias levels, register settings ...) for optimal application specific performance. This initialization may be accomplished using a standard serial PROM or over the 2 wire interface from a host controller.

From a high level, the power up sequence is as follows:

1. Power is applied to the chip.
2. A clock is applied to the chip. The default programming expects a 27MHz clock, which will give 30FPS video on the output interface.
3. The on-chip power-on-reset logic holds the chip in reset until the power is stable.
4. All on-chip registers are reset to the default states.
5. If the reset pin level is low (0V), the chip will be held in reset and the boot sequence is held at this step. If the reset pin level is high (3.3V), the chip comes out of reset with all the power on values and proceeds to the next step in the sequence.
6. The firmware boot sequence takes over. The boot sequence comprises:
    a. Query the 2 wire serial master interface to see if a valid PROM is located at device address 0xA0.
    b. If a valid PROM is present, load the contents of the PROM into the chip. If no valid PROM is present, continue with the boot sequence. The contents of the PROM can be used to change the default behavior of the device. See section 8.6.3 for more information about the use of the boot loader interface and the PROM.
    c. Enable the image capture and enable the output to begin transmission of video.
    d. Complete the firmware boot by setting register 0x8500 to 0x00, which indicates the boot process is complete. (Until the boot process is complete, 0x8500 will read as non-zero.)
7. At this point, the user can change the device operation by using the 2 wire serial slave interface to set the chip control registers.

9 55-pin Glass-BGA package information

The following sections detail the information about the pinout and physical dimensions of Avocet in the 55-pin GBGA package. Please refer to the “Printed Circuit Board (PCB) Layout” for information concerning use of Avocet on a circuit board.

9.1 GBGA55 Mechanical Drawings

The following sections contain mechanical drawings and dimensional information for the GBGA55 package.

9.1.1 Package mechanical drawings

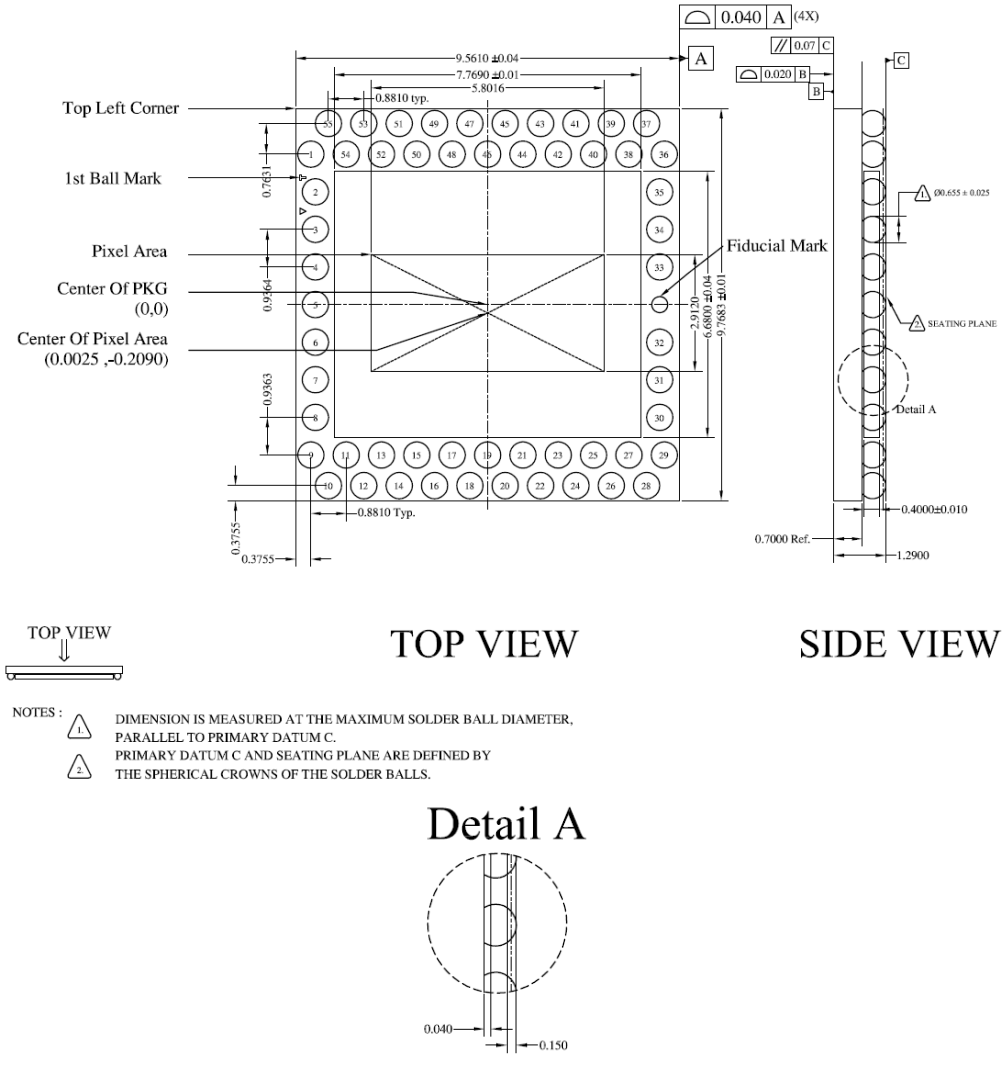
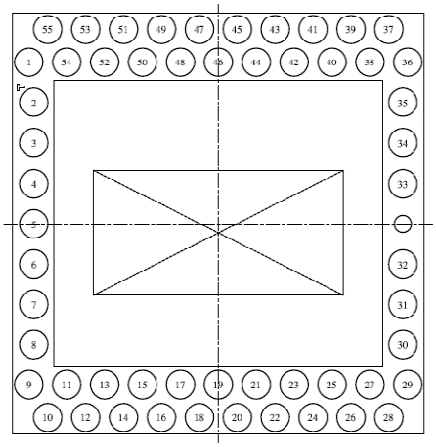


Figure 13 – 55-pin GBGA package mechanical drawings

9.1.2 Package ball coordinates



TOP VIEW

BALL PAD#	BALL COORDINATE	BALL PAD#	BALL COORDINATE
1	(-4.4050 , 3.7455)	29	(4.4050 , -3.7455)
2	(-4.2877 , 2.8092)	30	(4.2877 , -2.8092)
3	(-4.2877 , 1.8728)	31	(4.2877 , -1.8728)
4	(-4.2877 , 0.9364)	32	(4.2877 , -0.9364)
5	(-4.2877 , 0.0000)	33	(4.2877 , 0.9364)
6	(-4.2877 , -0.9364)	34	(4.2877 , 1.8728)
7	(-4.2877 , -1.8728)	35	(4.2877 , 2.8092)
8	(-4.2877 , -2.8092)	36	(4.4050 , 3.7455)
9	(-4.4050 , -3.7455)	37	(3.9645 , 4.5086)
10	(-3.9645 , -4.5086)	38	(3.5240 , 3.7455)
11	(-3.5240 , -3.7455)	39	(3.0835 , 4.5086)
12	(-3.0835 , -4.5086)	40	(2.6430 , 3.7455)
13	(-2.6430 , -3.7455)	41	(2.2025 , 4.5086)
14	(-2.2025 , -4.5086)	42	(1.7620 , 3.7455)
15	(-1.7620 , -3.7455)	43	(1.3215 , 4.5086)
16	(-1.3215 , -4.5086)	44	(0.8810 , 3.7455)
17	(-0.8810 , -3.7455)	45	(0.4405 , 4.5086)
18	(-0.4405 , -4.5086)	46	(0.0000 , 3.7455)
19	(0.0000 , -3.7455)	47	(-0.4405 , 4.5086)
20	(0.4405 , -4.5086)	48	(-0.8810 , 3.7455)
21	(0.8810 , -3.7455)	49	(-1.3215 , 4.5086)
22	(1.3215 , -4.5086)	50	(-1.7620 , 3.7455)
23	(1.7620 , -3.7455)	51	(-2.2025 , 4.5086)
24	(2.2025 , -4.5086)	52	(-2.6430 , 3.7455)
25	(2.6430 , -3.7455)	53	(-3.0835 , 4.5086)
26	(3.0835 , -4.5086)	54	(-3.5240 , 3.7455)
27	(3.5240 , -3.7455)	55	(-3.9645 , 4.5086)
28	(3.9645 , -4.5086)		

Figure 14 – 55-pin GBGA package ball coordinate table

Remark: Pixel (0,0), which is the first pixel in the output stream, is located in the bottom left corner of Figure 14.

The recommended PCB ball land size for the GBGA-package: 610µm.

9.2 Solder recommendations

9.2.1 Recommended Solder materials & procedure

Recommended sequence for soldering:

1. Stencil printing
2. GBGA placement
3. Reflow soldering (no manual soldering)

The recommended stencil mask thickness is 120µm and it has a 610µm ball land.

Recommended solder paste: Lead-free no-clean solder paste.

Remark: In case underfill is used, contact Melexis for material compatibility.

9.2.2 Solder profile

The table and graph below shows the recommended reflow soldering temperature profile for the Glass-BGA package.

Step	Details
Preheat	90s (± 10s) @ 150-200°C
Ramp up	1°C/s
Peak temperature	240°C (± 5°C)
Peak time	60s (± 5s) above 220°C

Table 6 – Reflow profile

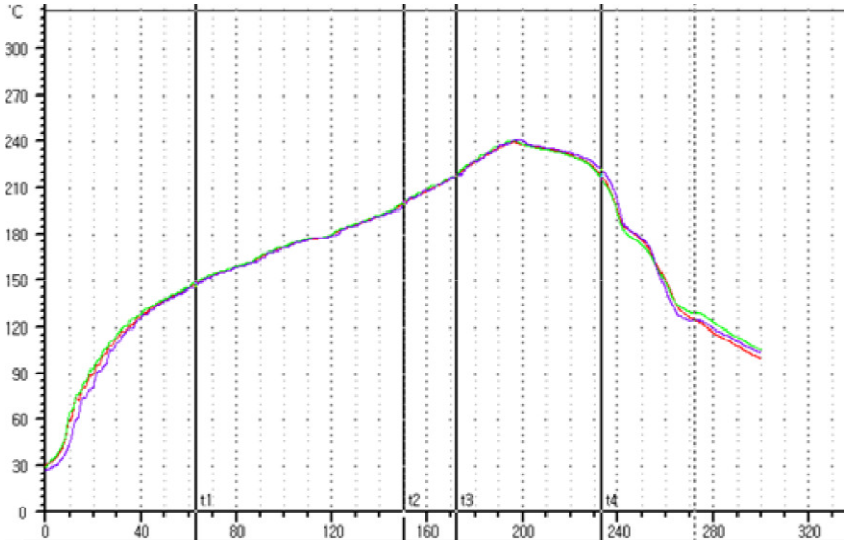


Figure 15 – Recommended temperature profile

10 Board design guidelines

The following sub-sections provide a set of electrical recommendations for the Avocet image sensor. The intention of these recommendations is to provide an experienced board designer with some guidance to aide in adding an Avocet image sensor to their board design. The use of a multi-layer PCB with solid ground and power plane pairs is recommended. It is left to the designer to follow sound signal integrity practices when designing the PCB (stack-up, signal routing, etc.).

The Avocet is a highly integrated mixed signal device consisting of both high precision analog and digital circuitry. It has been designed to minimize interference effects from digital circuitry on signal integrity of the analog circuitry. To guarantee maximum performance, these same design and layout techniques should be carried forward to the system-level design of the PCB.

Mixed signal device layout techniques should be used to optimize for lowest noise on the power supply and ground planes. Strong digital signal aggressors (such as clock and PIXDAT pins) should be shielded and/or routed away from analog signals (such as the VREFP/VREFM pins). Remain mindful of the entire current loop/path and maintaining good isolation between the digital and analog signal current paths.

10.1 Recommendations

10.1.1 Unused Pins

Unused digital input pins should be tied directly to GNDIO on the PCB.

As described earlier, Avocet has 2 primary output modes of operation: 1) **Parallel Digital Output Mode** and 2) **Framed Packetized Digital Output Mode**.

In **Parallel Digital Output Mode**, configuration options allow for 12bit, 10bit, or 8bit pixel data to be output. When 10bit pixel data output has been selected, pixel data is output on the upper 10 bits (PIXDAT[11:2]) and the lower 2 bits (PIXDAT[1:0]) are internally driven low and can therefore be left unconnected (floating) on the PCB. When 8bit pixel data output has been selected, pixel data is output on the upper 8 bits (PIXDAT[11:4]) and the lower 4 bits (PIXDAT[3:0]) are internally driven low and can therefore be left unconnected (floating) on the PCB.

In **Framed Packetized Digital Output Mode** the HSYNC and VSYNC outputs are unused and internally driven low. These two pins should be left unconnected (floating) on the PCB.

10.1.2 External Loop Filter

The external loop filter capacitors connected to the VREFP, VREFM, and VCM pins should be placed as close as possible to the pins (vias on the backside under the CBGA, or topside close to the bond-pads if using the COB package). Avoid adding unnecessary vias for these components as it will increase series inductance and reduce their effectiveness.

10.1.3 Series Termination Resistors

The use of series termination resistors on the parallel video output bus signals may be required depending on the specific system requirements (i.e. driving distance, drive strength, edge rate, etc.).

10.1.4 Power Supplies

Avocet requires two voltages: 3.3V for the VDDA (analog) and VDDIO (I/O) supplies, and 1.8V for VDDD (digital) supply.

Power Net	Voltage
VDDA (analog)	3.3V
VDDIO (I/O)	3.3V
VDDD (digital)	1.8V

Table 7 - Avocet Power Domains and Voltages

It is recommended that a separate regulated supply be provided for each power domain (VDDA, VDDIO, and VDDD). For optimal performance linear regulators with high power supply rejection ratios (PSRR) should be used in place of switch-mode regulators. If switch-mode regulators are used, careful design consideration should be given to the quality of the output voltage and the amount of voltage ripple and noise. Low voltage ripple and noise is especially important to the VDDA power domain. Each individual power supply should make a single-point connection to the system power supply through a series filtering ferrite bead.

10.1.5 Grounds

Avocet has three separate power domains: VDDA/GNDA (analog), VDDD/GNDD (digital), and VDDIO/GNDIO (I/O). Without proper decoupling and isolation, unwanted noise can couple from the digital or I/O domains and interfere with analog circuitry. This noise will manifest as unwanted artifacts in the final video image. For most applications it is sufficient to use a common ground for GNDA, GNDIO, and GNDDD.

For applications requiring the highest quality and performance, splitting the analog and digital power domains may provide greater isolation for the analog circuits. In this configuration, analog power should be referenced to analog ground and digital & I/O power to digital ground (i.e. VDDA references to GNDA, and VDDD and VDDIO referenced to GNDD). GNDD and GNDIO pins of the image sensor can both be connected to a common digital ground (DGND). **When splitting the analog ground (GNDA) from the digital and I/O grounds (DGND) a single point connection must be made between GNDA and DGND**. This along with proper signal routing will ensure current return paths between the analog and digital circuits remain isolated to their respective power domains. Additionally, VREFP, VREFM, and VCM pins should be referenced to GNDA. Table 8 below provides a summary for the split ground plane configuration.

Power Net	PCB GND Net
VDDA (analog)	**GNDA**
VREFP	**GNDA**
VREFM	**GNDA**
VCM	**GNDA**
VDDD (digital)	**DGND**
VDDIO (I/O)	**DGND**

Table 8 - Avocet Special configuration of power domains referenced to split grounds

10.1.6 Power Supply Decoupling

It is recommended that each power supply domain be decoupled with a 100nF ceramic capacitor at a minimum. Each of the power domains, VDDA, VDDIO, and VDDD should be individually decoupled to ground. Choose smallest packages for a given capacitance to lower package inductance. Place all decoupling capacitors close to the pins they are decoupling giving priority from smallest to largest to minimize the series and lead inductance. The addition of a 1uF moderate ESR Tantalum decoupling capacitor to the VDDA pins will help to spread the low freq impedance and add a little damping to the high-Q ceramic capacitors.

When using the split ground plane approach, decoupling capacitors must make connections between proper power and ground pairs (i.e. between VDDA and GNDA or VDDD/VDDIO and DGND).

10.1.7 Power Supply Sequencing

Avocet has a robust Power On Reset (POR) circuit. No specific combination of power supply sequencing is required. The only requirement is that all power supplies settle to their nominal voltage within 500ms.

10.1.8 Digital Signal Interconnect

The digital signal traces should be isolated as much as possible from the analog power pins and VREFP, VREFM, and VCM loop filter pins. Digital signal traces should not be routed over the VDDA or GNDA planes. Any pull-up resistors should be connected to the VDDIO power supply.

10.1.9 Analog Signal Interconnect

The analog traces for the analog power decoupling and loop filter (VREFP, VREFM, VCM), should be routed over VDDA and GNDA planes. Keep as much space as possible between the analog and digital traces to avoid capacitive coupling from nearby digital traces.

10.1.10 Slave I2C interface and Master Boot Loader Interface

These signals must meet fast I2C spec for timing. These pins should not be connected together to form a single bus.

10.2 Typical Application Circuit

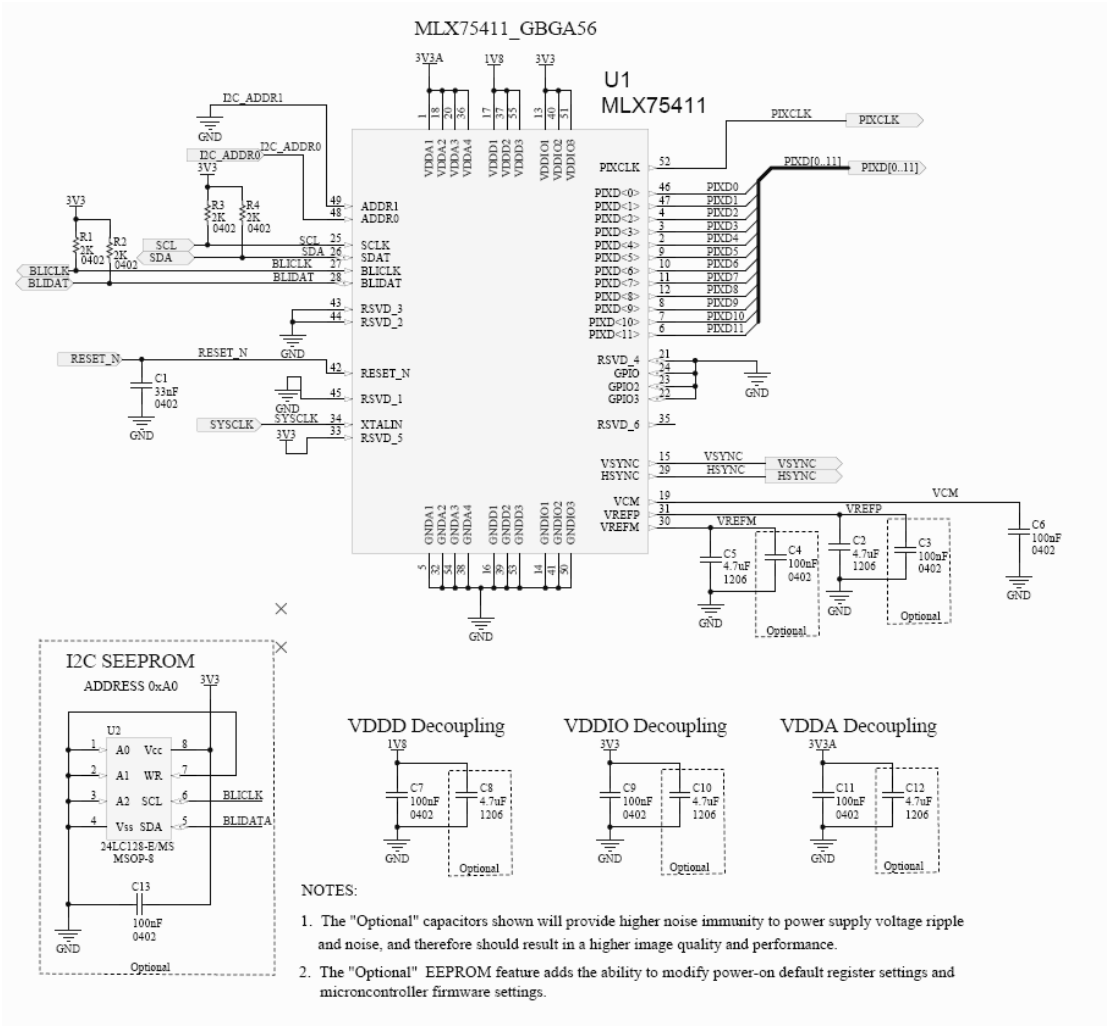


Figure 16 – Avocet typical circuit connection

11 Appendix A: Control protocol

The Avocet imager includes two serial control interfaces. The slave interface allows the application processor to control the imager using only two signals. The same interface is available as a master interface that the imager can use to store configuration settings that are loaded on reset. This section is intended to describe both interfaces – the only difference being whether Avocet or the controlling device is the master. The serial bus interface is a simple bi-directional communication that is in wide use throughout the industry. The serial bus operates at speeds of up to 400,000 bits per second. The interface is a multi-drop protocol which allows multiple devices to be connected to a single pair of wires. The two interface signals are called SCLK and SDAT. SCLK provides a clock for asserting and sampling the SDAT signal. SCLK is unidirectional from the bus master to the Avocet image sensor. SDAT is the data bus and is bi-directional. Data is always transmitted with the Most-Significant-Bit (MSB) first. Eight bits of data are always transferred and are followed by a single ACKnowledge bit. Data transfer on the Serial Bus Interface is initiated with a START condition. The START condition is indicated when the SDAT signal goes low while SCLK remains high. The START condition may be initiated at anytime during a transfer and the imager will restart the transfer to begin accepting the DEVICE ADDRESS which must immediately follow the START. The SDAT line must only transition when SCLK is low when data is being transferred. If SDAT transitions while SCLK is high, then it will be interpreted as either a START or a STOP condition. Sufficient timing margins must be provided around the rising and falling edges of SCLK to insure that a START or STOP condition is not mistakenly recognized.

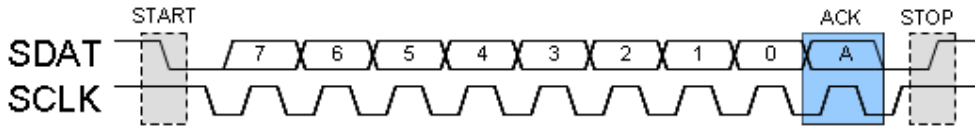


Figure 17 – Avocet 2 Wire Serial Interface General

The DEVICE ADDRESS is a sequence of 7 bits, a READ/WRITE bit and an ACKnowledge bit. Data is always transmitted MSB first and LSB last as shown in the figure above. The DEVICE ADDRESS is 7 bits long. The ADDR[1:0] pins allow up to four Avocet image sensors to be connected to the same Serial Bus Interface.

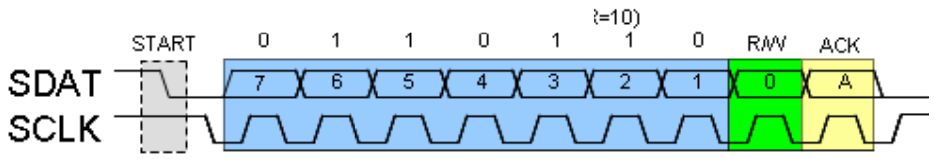


Figure 18 – Avocet 2 Wire Serial Interface Device Address

The table below lists the mapping of the ADDR bits to the DEVICE ADDRESS. The Avocet will respond to a DEVICE ADDRESS of all zeroes as a broadcast command to all cameras. This feature allows several cameras to be updated simultaneously.

ADDR [1:0]	DEVICE ADDR	Comment
00	0101_100	
01	0101_101	
10	0110_110	
11	RESERVED	Do not use

Table 9 - Avocet 2 wire serial interface address selection

Note that the microcontroller can write to a register to alter the device address to be any value. This allows the DEVICE ADDRESS of a camera to be stored in the EEPROM and be programmed after the camera is sealed and installed in its final location. The LSB of the first byte after a START is the READ/WRITE bit where a high (1) indicates that a READ cycle will follow and a low (0) indicates that a write cycle will follow. After the READ/WRITE bit, the Avocet Image Sensor will assert SDAT low shortly after SCLK goes low to acknowledge that the DEVICE ADDRESS has been recognized and is ready to process the command that will follow. If a read transaction has been requested (READ/WRITE is high), then the imager will begin driving SDAT with the register data at the current address. If a write transaction has been requested then the bus master should send the two REG ADDRESS bytes. The REG ADDRESS bytes specify which register in the imager is to be accessed. The next byte of data is the write data. Additional bytes of data can be written and the ADDRESS will be automatically incremented to the next register. Upon completion of all data being transferred, the master should issue a STOP command to place the SBI in an idle state. A STOP command is initiated by first driving SDAT low and SCLK high, then bringing SDAT high while SCLK remains high.

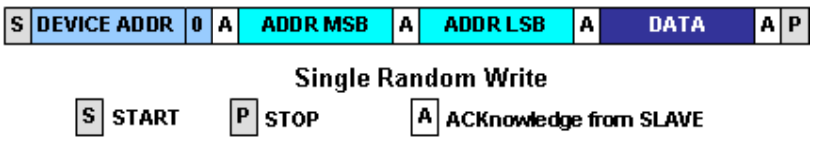


Figure 19 – Avocet 2 Wire Serial Interface Single Random Write

A WRITE cycle to any register is accomplished by sending a START followed by a 7 bit DEVICE ADDRESS, one bit of zero (the read/write indicator) and an ACK bit. Then the 16-bit register address must be sent in two bytes, each with an ACK bit from the slave. Finally the 8-bits of data are sent and the slave will respond with a final ACK bit. The master can then either issue a STOP command or write to the next sequential address by sending additional data bytes.

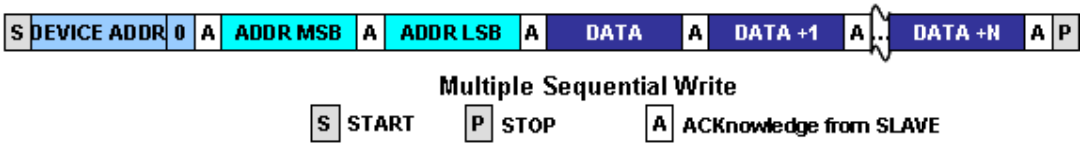


Figure 20 – Avocet 2 Wire Serial Interface Multiple Write

Multiple registers can be written in a single stream of data which reduces the time required to update registers. In the case shown here, DATA would be written to the address given in ADDR. DATA+1 would be written to ADDR+1 and so on with each byte of data being written to the next higher register address.

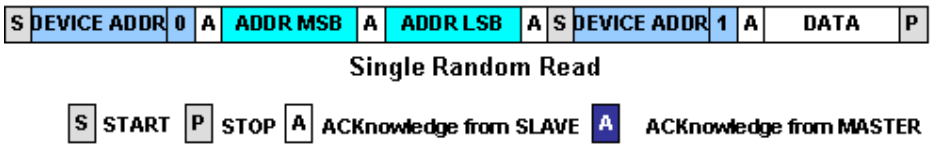


Figure 21 – Avocet 2 Wire Serial Interface Single Random Read

A single random read cycle requires that a dummy write cycle be done first so that the register address can be set. The first DEVICE ADDR is followed with a 0 bit which indicates that this is a write cycle. The register address follows but instead of sending the data to write, a new START condition is sent which restarts the SBI state machine but the REG ADDR remains initialized. The DEVICE ADDR must be sent again but this time is followed with a 1 bit indicating that this is a read cycle. The slave responds with the ACK bit and then drives the 8 data bits of the register which has been read. After the eight data bits, the slave does NOT assert the ACK bit. Instead, it tristates the SDAT signal so that the master can either ACK, or assert the STOP condition.

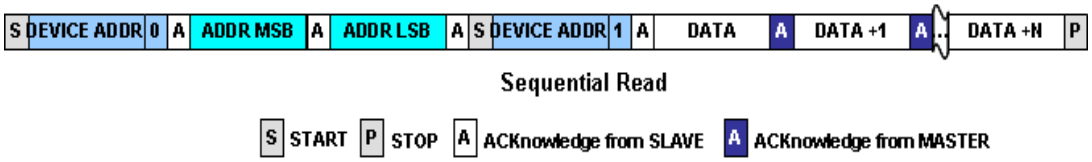


Figure 22 – Avocet 2 Wire Serial Interface Multiple Sequential Read

Multiple sequential registers can be read without having to resend the DEVICE ADDR and register addresses. To read multiple registers, simply continue to issue more SCLKs and the imager will increment to the next higher register address. After each byte that is transferred, the master must issue an ACK by driving SDAT low if it wishes to continue to read more data. The last byte that is read should not ACK which allows the master to drive SDAT low before releasing SCLK and then release SDAT to cause a STOP condition to be recognized. Alternatively, if the master does not drive SDAT low during the ACK bit, the imager will release the SDAT line and the state machine will return to its idle state waiting for the next START condition.

The register ADDR is always retained at the current address as long as power is applied to the chip. A register read at the current address can be initiated at any time without having to send

the register ADDR first if the desired register is already being addressed. Note that the register address is incremented on the rising edge of SCLK at the start of the ACK bit.

12 Appendix B: Use of the 2 wire boot loader interface

The 2 wire serial master interface is designed to all the connection of an external PROM. The purpose of this PROM is to store configuration information that is read at boot time to alter the default behavior of the device. The PROM can contain control register settings as well as supplemental controller.

PROM part specification

The serial PROM should be selected to be compatible with the following part:

24LC128-X/XX - Microchip 24LC128 128K-BIT I2C SERIAL EEPROM

PROM connections

The PROM should be connected as follows:

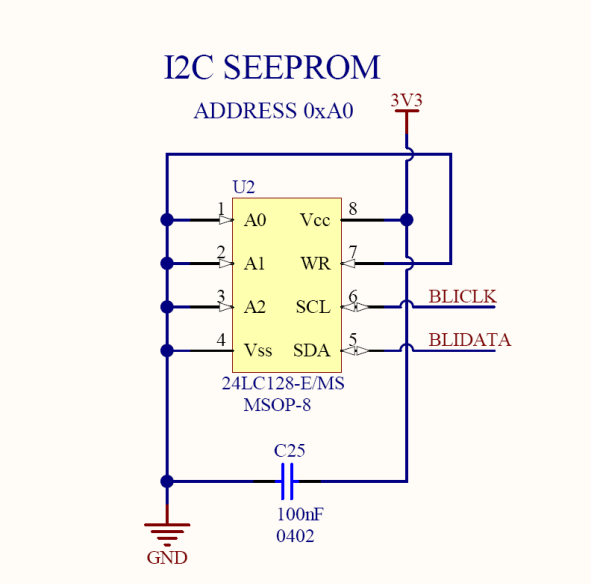


Figure 23 – Example boot loader interface PROM connection

- BLICLK should be connected to MCLK on Avocet.
- BLIDATA should be connected to MDAT on Avocet.

13 Appendix C: Control Registers

Commonly used Avocet functions can be controlled through a basic subset of the total available control registers. All control registers are accessed through the 2-wire slave interface. Below is a list of the registers used to control the basic functions of the imager.

13.1 Common Tasks

The sections below list many of the common tasks and how to accomplish them.

13.1.1 How to determine the revision of the hardware and the firmware

The hardware, firmware, and patch versions should be read when determining the version of the device. All the version numbers are used as incrementing version numbers. (Higher values indicate more recent versions.)

The hardware revision can be determined by reading the following registers:

- Read registers 0x8000 and 0x8001 to get the model ID. For Avocet, this will read as 0x41 and 0x00, respectively.
- Read register 0x8002 to get the silicon revision. For the current version of Avocet, this will read 0x01.

The firmware ROM revision can be determined by reading the following registers:

- Read 0x853C to get the firmware major revision number.
- Read 0x853D to get the firmware minor revision number.
- Read 0x853E to get the firmware minor-minor revision number.
- Read 0x853F to get the firmware build number.

The firmware patch revision can be determined by reading the following registers:

- Read 0x8504, bit [5] to make sure EEPROM load was successful. It reads 1 in case of successful load. If the load was not successful, the firmware version is not valid.
- Read 0x857C to get the patch major revision number.
- Read 0x85D to get the patch minor revision number.
- Read 0x857E to get the patch minor-minor revision number.
- Read 0x857F to get the patch build number.

If the patch number reads as 0x00000000, then no patch has been applied.

13.1.2 How to disable/enable image processing functions

Image processing functions are disabled through a set of hardware registers. By default, all the image processing functions are enabled at power on. Register 0x8102 controls all the hardware functions. It is used as follows:

- Histogram remapping: To disable histogram remapping, write register 0x8102, bit [6] to a 0. A separate control is provided to enable/disable the AutoView algorithm by using register 0x8502, bit [7] to control the firmware. When disabling histogram remapping permanently, this bit should be written to a 0 as well to reduce the amount of processing that the chip performs. To enable, write register 0x8102, bit [6] to a 1. (And write bit [7] of register 0x8502 to a 1 if it was disabled.)
- Sharpening filter: To disable the sharpening filter, write register 0x8102, bit [5] to a 0. To enable, write this bit to a 1. When enabled, the filter strength can be controlled via register 0x9058.
- Defective pixel correction: To disable the defective pixel correction algorithm, write register 0x8102, bit [4] to a 0. To enable, write this bit to a 1. When enabled, the algorithm can be controlled by using register 0x9050.
- Fixed pattern noise correction: To disable fixed pattern noise correction, write registers 0x8102, bit [2] to a 0. To enable, write this bit to a 1.
- Dark current correction: To disable dark current correction, write register 0x8102, bit [1:0] with '00'. Bit 0 controls the offset correction portion, and bit 1 controls the gain correction. To enable, write these bits to '11'.

Some notes concerning the operation of register 0x8102:

1. When writing register 0x8102, all bits should be written with appropriate values. This should be done by setting all bits explicitly or using a read/modify/write to preserve the register contents of the bits not being modified.
2. When writing register 0x8102, bit [3] should always be set to a 1. Bit 3 controls a hardware function that orders the pixels in scan line order. Pixels will not be in scan line order, and other image processing functions will not operate properly if this bit is disabled.

Whenever dark current gain correction is enabled, dark current offset correction should also be enabled.

13.1.3 How to control Autobrite autoexposure and dynamic range

There are several parameters that allow control of the Autobrite algorithm (automatic mode). The parameters control the settling point of the exposure time and the compression curve.

- Wait until register 0x8500 reads 0x00.
- Ensure register 0x8502, bits [6:4] are set. (They are set by default.)
- Use registers 0x852C-0x852F to set the maximum allowed pixels in the upper part of the histogram. This parameter will affect the amount of compression applied to the image. If the number of pixels in the upper part of the histogram is greater than this number, the compression will be increased. Smaller numbers will tend to cause greater compression.
- Use registers 0x8530-0x8531 to set the minimum number of pixels in the lower portion of the histogram and 0x8532-0x8533 to set the maximum. This area of the histogram is defined as all values below $1/16^{th}$ of a full scale output (255 for a 12b output). These parameters affect the exposure time: If the amount of pixels in the bottom part of the histogram is larger than this number, the exposure time will be increased.
- Write register 0x8500 with 0x03.

Registers 0x9302-0x9393 set the start of the upper bin (for automatic compression control).

13.1.4 How to control Autoview histogram remapping

There are several parameters that allow control of the Autoview algorithm. The parameters control the settling point of the remapping gain and offset constants.

- Wait until register 0x8500 reads 0x00.
- Ensure register 0x8102, bits [6] is set to '1'. (It is set by default.)
- Ensure register 0x8502, bits [7] is set to '1'. (It is set by default.)
- Use register 0x8522 to set the strength parameter to the remapping algorithm. Lower strength values will cause less change to the histogram.
- Write register 0x8500 with 0x03.

13.1.5 How to disable the automatic exposure control (Autobrite)

Automatic calculation of the exposure and barriers is performed by the firmware. These calculations can be disabled individually.

- Wait until register 0x8500 reads 0x00.
- Automatic exposure control: To disable automatic exposure control, write register 0x8502, bit [5] to a 0. To enable, write this bit to a 1.

- Automatic barrier control: To disable automatic barrier control, write register 0x8502, bit [4] to a 0. To enable, write this bit to a 1.
- Write register 0x8500 with 0x03.

13.1.6 How to set a specific frame rate

The frame rate of the chip is a function of the clock provided to the chip, and its programming. To simplify the control of frame rate, firmware is used to assist in the calculations.

- Wait until register 0x8500 reads 0x00.
- In register 0x8503, write bit [0] to 1. (It is disabled by default.)
- Write the number of clocks per second into registers 0x8518-0x851B. By default, these registers contain a value consistent with 27MHz (27,000,000 = 0x019BFCC0).
- Write the desired value of frames per second into registers 0x851C-0x851D. This value is a 16 bit number indicating the frame rate. By default, it contains 0x001E (indicating 30 frames per second).
- Write register 0x8500 with 0x03.

The chip will be programmed to provide the closest possible value to the frame rate requested. The value will be accurate to within 1 line time (if possible). If greater accuracy is required, please contact Melexis.

Remark: There is a lower and upper limitation for which framerates can be achieved for a given clock frequency and resolution:

$$\frac{Fclk}{1322 \cdot (nr\_active\_rows + 3583)} \leq FPS \leq \frac{Fclk}{1322 \cdot (nr\_active\_rows + 40)}$$

In this formula, nr_active_rows is the amount of rows set in the subwindow (512 by default). For a clock frequency of 27MHz, this corresponds to framerates between 5 and 36 FPS.

13.1.7 How to set up sub-windowing

The control of the subwindowing function of the chip is simplified through the use of firmware.

- Wait until register 0x8500 reads 0x00.
- Ensure register 0x8503, bit [0] is set to 1. (It is disabled by default.)
- Write the desired X size (in pixels) into registers 0x8508-0x8509. These registers are used as a 2-byte value. The values are limited from 1 to 1024.
- Write the desired Y size (in rows) into registers 0x850A-0x850B. These registers are used as a 2-byte value. The values are limited from 1 to 512.

- Write the desired X starting position (in pixels) into registers 0x850C-0x850D. These registers are used as a 2-byte value. The values are limited from 0-1023 (with 0 being the left of the frame).
- Write the desired Y starting position (in rows) into registers 0x850E-0x850F. These registers are used as a 2-byte value. The values are limited from 0 to 511, and bits [2:0] of the value used must be '000'. (0 being the top of the frame)
- Write register 0x8500 with 0x03.

Remark: When using subwindowing, size and position in the vertical dimension must be multiples of 8.

13.1.8 How to control statistics collection (and Autobrite to expose) based on a sub-region of the image

To control Autobrite to only used statistics from a sub-region of the image:

- Wait until register 0x8500 reads 0x00.
- Ensure register 0x8502, bits [6:4] are set to '111'.
- Ensure register 0x8503, bit [3] is set to 1.
- Write the desired X size (in pixels) into registers 0x8510-0x8511. These registers are used as a 2-byte value. The values are limited from 1 to 1024.
- Write the desired Y size (in rows) into registers 0x8512-0x8513. These registers are used as a 2-byte value. The values are limited from 1 to 512.
- Write the desired X starting position (in pixels) into registers 0x8514-0x8515. These registers are used as a 2-byte value. The values are limited from 0-1023 (with 0 being the left of the frame).
- Write the desired Y starting position (in rows) into registers 0x8516-0x8517. These registers are used as a 2-byte value. The values are limited from 0 to 511, and bits [2:0] of the value used must be '000'. The y position is referenced from the top of the frame (0 being the top row).
- Write register 0x8500 with 0x03.

Notes concerning the use of the sub-region feature of Autobrite:

The region of interest should be contained within the viewable frame. (Only a concern if sub-windowing is also used.)

The parameters to the Autobrite algorithm should be adjusted to account for the smaller number of pixels in the sub-region.

13.1.9 How to output a test pattern

The imager can be set to output a test pattern. This test pattern can be generated before the internal digital pipeline or after the pipeline.

To output a test pattern generated after the digital pipeline:

- Write 0x0E to 0x8600

To output a test pattern generated before the digital pipeline:

- All dark columns and rows are to be enabled to make sure the pipeline handles the pattern correctly. To do this, write 0xFF to registers 0x902A, 0x902B, 0x902C, 0x902D.
- Write 0x0D to 0x8600

13.2 Register reference – register list

Following the register list table is a description of the use of each of these registers.

The hardware sync field indicates which of the registers have the ability to be synced cleanly to frame boundaries by the hardware. For the use of the hardware sync mechanism, please refer to the definition of Software Reset / Sync Register (0x8101) in section 13.3.1.5 on page 42.

Register Address	Register Name	Length	Reset Value	Hardware Synced	Description
0X8000	model_id	16b	0X4100		Model ID
0x8002	silicon_revision	8b	0X01		Silicon Revision
0x8004	frame_number	16b	0X0000		Frame Count
0x8100	mode_select	8b	0X03		Mode select
0x8101	sync_register	8b	0X00		Software reset and hardware sync
0x8102	feature_enable_1	8b	0X7F	X	Enables for imager hardware functions.
0x8200	frame_length_lines	16b	0X0200		Frame length in lines
0x8202	row_length_pixels	16b	0X0400		Line length in pixels
0x8205	output_options	8b	0x40		Sets options for output interface
0x8500	fw_csr_sync	8b	0x00		Synchronization control for firmware registers
0x8502	fw_feature_enable_1	8b	0XF0		Enable bits for firmware features
0x8503	fw_feature_enable_2	8b	0X00		Enable bits for firmware features
0x8504	fw_status	8b			Firmware status register
0x8505	fw_subsample	8b	0X00		Vertical subsampling control
0x8506	fw_img_average	16b			Average pixel value
0x8508	fw_subwindow_x_size	16b	0X0400		X-size for subwindow

0x850A	fw_subwindow_y_size	16b	0x0200		Y-size for subwindow
0x850C	fw_subwindow_x_pos	16b	0X0000		X-position for subwindow
0x850E	fw_subwindow_y_pos	16b	0x0000		Y-position for subwindow
0x8510	fw_roi_x_size	16b	0X0400		X-size for Region of Interest
0x8512	Fw_roi_y_size	16b	0x0200		Y-size for Region of Interest
0x8514	Fw_roi_x_pos	16b	0X0000		X-position for Region of Interest
0x8516	fw_roi_y_pos	16b	0X0000		Y-position for Region of Interest
0x8518	fw_clocks_per_second	32b	0X019BFCC0		Clock frequency for frame rate setting
0x851C	fw_frames_per_second	16b	0X001E		Frame rate
0x8520	fw_clocks_per_row	16b	0x052A		Number of clock cycles in one rowtime
0x8522	fw_hr_remap_strength	8b	0X03		Histogram remapping strength
0x8524	fw_mss_time_h	8b	0x01		Top byte for stereo synchronization register
0x8526	fw_wdr_tint	16b			Autobrite exposure time in rowtimes
0x8528	fw_wdr_last_barrier_time	32b			Autobrite position of last barrier
0x852C	fw_wdr_desired_num_pix_upper_bin	32b	0X000005DC		Input for automatic compression control
0x8530	fw_wdr_desired_min_num_pix_lower_bin	16b	0x0200		Input for automatic exposure control
0x8532	fw_wdr_desired_max_num_pix_lower_bin	16b	0x1c00		Input for automatic exposure control
0x8534	fw_min_allowed-tint	16b	0X0002		Lower limit for automatic exposure algorithm
0x8538	fw_mss_time_l	16b	0x0000		Lower bytes for stereo synchronization register
0x853C	fw_rom_version	32b	0x02000089		Rom version code
0x8550	fw_context_0_exposure_time	16b	0x0000		Exposure time for context 0
0x8552	fw_context_0_last_barrier_time	32b	0xC0000000		Last barrier time of context 0
0x8556	fw_context_0_hw_features	8b	0x00		Hardware feature enable for context 0
0x8557	fw_context_0_sharpening	8b	0x1E		Sharpening setting for context 0
0x8558	fw_context_1_exposure_time	16b	0x0000		Exposure time for context 1
0x855A	fw_context_1_last_barrier_time	32b	0x00000000		Last barrier time of context 1
0x855E	fw_context_1_hw_features	8b	0x00		Hardware feature enable for context 1
0x855F	fw_context_1_sharpening	8b	0x00		Sharpening setting for context 1
0x857C	fw_patch_version	32b			FW revision nr
0x8600	test_pattern_mode	8b	0X0C	X	Test pattern mode
0x902E	dark_current_average	16b			Dark Current Average
0x9050	defect_pixel_control	8b	0X00		Enables for defect pixel correction functions
0x9058	sharpening_filter_control	8b	0X02		Enables for sharpening filter functions.
0x9302	Upper_bin_pixel_start	16b	0x0F3C		Sets top bin start for Autobrite

Table 10 - Basic control register list

13.3 Register reference – Register descriptions

13.3.1 Hardware registers

13.3.1.1 Model ID (0x8000-0x8001)

0x8000 Model ID (high byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1
MODEL_ID_H							

0x8001 Model ID (low byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
MODEL_ID_L							

These 2 registers indicate the model number for the chip. For Avocet, this will read 0x4100.

13.3.1.2 Silicon Revision (0x8002)

0x8002 Silicon Revision

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
Silicon_revision							

This register indicates the silicon revision for the chip. For the current version of Avocet, this will read 0x01.

13.3.1.3 Frame number (0x8004-0x8005)

0x8004 Frame Number (high byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
FRAME_NUMBER_H							

0x8005 Frame Number (low byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
FRAME_NUMBER_L							

These 2 registers indicate the current frame number. This read-only 2-byte register will increment for each frame read off the image array.

13.3.1.4 Mode Select (0x8100)

0x8100 Mode Select

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
Unused	10-bit mode enable	8-bit mode enable	Interlaced mode enable	Reserved	Framed output enable	Chip output enable	Imager enable

This register allows the user to control the major modes of the chip.

- Bits [6] and [5] control the output bit depth. Only 1 bit should be set at a time. If neither bit is set, the chip will output 12-bit pixels.
- Bit [4] controls the interlacing function of the chip. If this bit is set, the chip will output even lines on even frames and odd lines on odd frames.
- Bit [3] is a reserved bit and should be written with ‘0’.
- Bit [2] controls the framed output mode. This bit enables a framed or packetized mode of data transmission. In this mode, all the data lines and frames are sent as data packets. This mode is meant to be connected to a serializer to allow data transmission on a pair of wires. In this mode, the HSYNC and VSYNC lines are disabled. This mode should only be used in 12-bit default mode. For more information on the Framed Output Mode, please see Appendix F.

- Bit [1] controls the chip output enables. This is independent of the imager gathering data. The outputs can be disabled, and the imager will still collect data and statistics but will not send the data to the outputs. When the outputs are disabled PIXD, HSYNC, VSYNC, and PIXCLK will all be held at 0. Normally, this bit powers up to 0 and is turned on by default by the firmware.
- Bit [0] controls if the image array is collecting data. If this bit is turned off, no image data will be gathered and no statistics will be collected. When this bit is re-enabled, the first frame sent out of the chip will have an undetermined exposure and all following frames will be exposed according to the chip settings. Normally, this bit powers up to 0 and is by default turned on by the firmware.

13.3.1.5 Software Reset / Sync Register (0x8101)

0x8101 Software Reset / Sync Register

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
SOFTWARE_RESET				Unused	Unused	Sync mechanism active	Sync

This register has two main functions:

- The bits [7:4] function as a software reset. When the value ‘1010’ is written to these bits, the chip will perform a software reset. If any other value is written to these bits, nothing will happen. These bits will always read as ‘0000’.
- Bit [1] activates the sync mechanism, and bit [0] causes the chip to perform the sync. This mechanism is to allow several values to be updated and all be applied to the chip simultaneously. The way to use the sync mechanism is to follow the sequence:
    1. Write a value of 0x02 to this register.
    2. Write any number of other registers, with any delay. While this register contains a value of 0x02, none of the other writes will take effect.
    3. Once all writes have been completed, write a value of 0x03 to this register.
    4. The values written in step 2 will all take effect on the next possible frame boundary.

Note: Not all chip registers are part of the sync mechanism. Any register that is part of the mechanism will be marked as a “Sync’d” register in the register lists.

13.3.1.6 Hardware feature Enables (0x8102)

0x8102 Hardware feature enables

Bit Definition							
7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	1
Unused	Histogram Remapping Enable	Sharpening Filter Enable	Defective Pixel Correction Enable	Reorder Buffer Enable	FPN Offset Correction Enable	Dark Current Gain Correction Enable	Dark Current Offset Correction Enable

This register controls the major hardware-based image processing and noise correction functions of the chip. For all these functions, a '1' in the associated bit means the feature is enabled and a '0' indicates that the feature is disabled.

- Bit [6] controls the histogram remapping function. When enabled, the hardware will remap the histogram by using the gain and offset values in registers 0x9060 to 0x917F. This bit only controls the use of the hardware remapping facilities. A separate control is provided to enable/disable the AutoView algorithm by using register 0x8502 to control the firmware.
- Bit [5] enables the hardware sharpening filter. The filter strength can be controlled via register 0x9058.
- Bit [4] enables the hardware defective pixel correction algorithm. The algorithm can be controlled by using register 0x9050.
- Bit [3] controls the reorder buffer. This bit should always be set to '1' for proper chip operation.
- Bit [2] enables the fixed pattern noise (FPN) hardware correction algorithm. The algorithm can be controlled via the advanced register settings at 0x9030 – 0x9042.
- Bit [1] enables the dark current gain correction. This should always be enabled along with the dark current gain correction for proper chip operation. Further control of the dark current correction algorithm is available through the use of advanced register settings at 0x9020-0x902D. The dark current average can be read from registers 0x902E-0x902F.
- Bit [0] enables the dark current offset correction. This can be enabled independently from the dark current gain correction. Further control of the dark current correction algorithm is available through the use of advanced register settings at 0x9020-0x902D. The dark current average can be read from registers 0x902E-0x902F.

13.3.1.7 Frame length in lines (0x8200-0x8201)

0x8200 Frame Length in Lines (high byte)

Bit Definition

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
FRAME_LENGTH_LINES_H							

0x8201 Frame Length in Lines (low byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
FRAME_LENGTH_LINES_L							

These 2 read-only registers indicate the number of active lines in each frame. This total excludes the vblank rows.

13.3.1.8 Row length in pixels (0x8202-0x8203)

0x8202 Row Length in Pixels (high byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
ROW_LENGTH_PIXELS_H							

0x8203 Row Length in Pixels (low byte)

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROW_LENGTH_PIXELS_L							

These 2 read-only registers indicate the number of active pixels in each row. This total excludes the hblank pixels.

13.3.1.9 Output option enables (0x8205)

0x8205 Output_options

Bit Definition							
7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0
Enable_digital_	Pixel_xlk_	Vsync_	Hsync_	Select output pixels.			

This register is used to control the output frame and select which type of pixels are included. The bits are defined as follows:

[7] - Enable_digital_y_subwindowing

[6] - Pixel_clk_polarity: 1=inverted, 0 = default

[5] - Vsync_clk_polarity: 1=inverted, 0 = default

[4] - Hsync_clk_polarity: 1=inverted, 0 = default

[3:0] –

1111 – Active pixels +Embedded rows + FPN data + dark pixels + interpolation pixels

0111 – Active pixels + FPN data + dark pixels + interpolation pixels

0111 – Active pixels + FPN data + dark pixels + interpolation pixels

0011 – Active pixels + dark pixels + interpolation pixels

0001 – Active pixels + interpolation pixels

0000 – Active pixels

13.3.1.10 Test pattern mode (0x8600)

0x8600 test_pattern_mode

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0
Reserved	Reserved	Color test pattern select		Monochrome / color test pattern select	Reserved	Enable post processing pipeline test pattern	Enable pre processing pipeline test pattern

This register is used to enable and select the test pattern function. The bits are defined as follows:

[7] - Reserved

[6] - Reserved

[5:4] - if color, indicates which RGB bayer pattern

00 - 1st pixel is R (Red)

01 - 1st pixel is B (Blue)

10 - 1st pixel is Gr (Green in red row)

11 - 1st pixel is Gb (Green in blue row)

[3] - selects a black and white/color test pattern

1 = black and white, 0 = color

[2] - Reserved

[1] - enable post processing (end of pipeline) test pattern generator

[0] - enable pre-processing (start of pipeline) test pattern generator

See 13.1.9 on how to output a test pattern.

13.3.1.11 Dark current average (0x902E-0x902F)

0x902E dark_current_average_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved				Dark_current_average [11:8]			

0x902F dark_current_average_lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Dark_current_average [7:0]							

These two registers are a read only register that can be used to read the dark current average used by the hardware correction.

13.3.1.12 Defective pixel control (0x9050)

0x9050 defect_pixel_control

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved							Defect pixel correction scale

This register is used to control the defective pixel function. The bits are defined as follows:

[7:2] - Reserved

[1:0] - Defect Pixel Correction Scale

00 - Scale = 0

01 - Scale = 1/4

10 - Scale = 1/2

11 - Scale = 1

Note, this register takes effect cleanly on a frame boundary even though it is not controlled by the hardware synchronization mechanism.

The scale indicates how far the pixel is allowed to differ from its neighbors before it is considered a defect. Larger values are more lenient, and will force less correction. The scale is used as follows:

- Find the maximum and minimum valued neighbors (max_meighbor, min_neighbor).
- Calculate the range = max_meighbor - min_neighbor
- Calculate the allowed_variance = scale * range
- Calculate the max_allowed = max_neighbor + allowed_variance.
- Calculate the min_allowed = min_neighbor - allowed_variance.
- If the current value is greater than max_allowed, set it to max_allowed. If the current value is less than the min_allowed, set it to min_allowed.

13.3.1.13 Sharpening filter control (0x9058)

0x9058 sharpening_filter_control

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
Reserved						Sharpening Filter Strength	

This register is used to enable and select the strength of the sharpening filter. The bits are defined as follows:

[7:2] - Reserved

[1:0] - Sharpening Filter Strength

00 - Strength = 0 (equivalent to no sharpening)

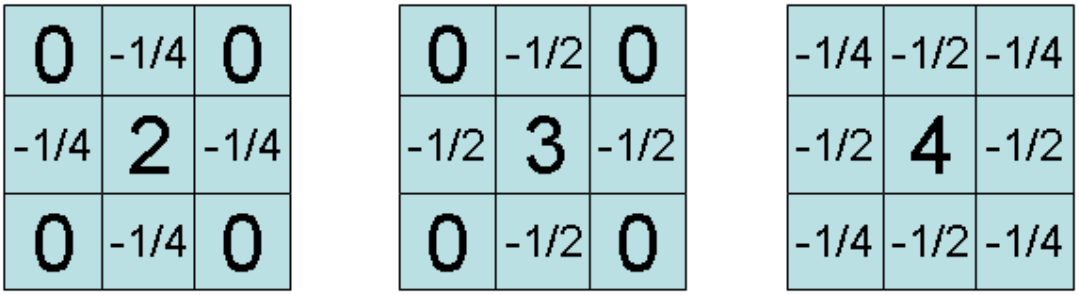
01 - Strength = 1 (light sharpening)

10 - Strength = 2 (medium sharpening)

11 - Strength = 3 (heavy sharpening)

Note: This register takes effect cleanly on a frame boundary even though it is not controlled by the hardware synchronization mechanism.

The matrix coefficients for setting 01 (left), 10 (middle) and 11 (right):



13.3.2 Firmware registers

Many of the other features of the chip are controlled indirectly by interacting with the on-chip firmware. The firmware registers exist from address 0x8500 to 0x857F. Not all of these registers are currently used. The most important registers are detailed below:

13.3.2.1 Firmware Sync (0x8500)

0x8500 fw_csr_sync

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
fw_csr_sync							

This register controls the syncing of the firmware registers in much the same way that the hardware sync is controlled by register 0x8101. The difference is that the firmware sync mechanism is always active. The firmware registers should be updated as follows:

- Wait until this register reads 0x00.
- Write the firmware registers with new values. A firmware register that uses the sync mechanism is a register whose name begins with “fw_” and is marked as “Sync’d” in the register tables.
- Once all writes have been completed, write a value of 0x03 to this register.
- The values written in step 1 will all take effect on the next possible frame boundary.

13.3.2.2 Firmware feature enable 1 (0x8502)

0x8502 fw_feature_enable_1

Bit Definition							
7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	0
AutoView Enable	Barrier Update Enable	Auto Tint Enable	Auto Dynamic Range Enable	Context Switch Enable	Stereo Active	Stereo master Enable	Stereo Slave Enable

This register is used to control the firmware features. The bits act as enables for various imager functions:

[7] – Enable Histogram Remapping algorithm. Setting this bit to '1' tells the firmware to calculate new remapping constants based upon the image statistics. Setting this bit to '0' will cause the firmware to leave the remapping constants in their current state. Note: This does not disable the remapping of the histogram, just the calculation of new remapping constants. To disable the remapping, use register 0x8102.

[6] – Enable barrier updates. Setting this bit to '1' allows the firmware to update the barrier registers. It should be set to '1' for both automatic and semi-automatic mode.

[5] – Enable automatic exposure time control. Setting this bit to '1' will cause the firmware to calculate a new exposure time based on the image statistics. Setting this bit to '0' will disable the automatic update and leave the exposure time at its current setting.

[4] – Enable automatic dynamic range control. Setting this bit to '1' will cause the firmware to calculate a new compression curve based on the image statistics. Setting this bit to '0' will disable the automatic update and leave the compression curve at its current setting.

[3] – Enable context switching.

[2] – Stereo Active. Flag to host, indicates stereo mode is active.

[1] – Enable Stereo Master

[0] – Enable Stereo Slave

13.3.2.3 Firmware feature enable 2 (0x8503)

0x8503 fw_feature_enable_2

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved	Reserved	Reserved	Reserved	ROI control	Reserved	Reserved	Frame Control

This register is used to control the firmware features. The bits act as enables for various imager functions:

[7] – Reserved

[6] – Reserved

[5] – Reserved

[4] – Reserved

[3] – Enable region of interest (ROI) control. Setting this bit to '1' allows the firmware to update the sensor configuration related to the ROI. This allows simple setting of the ROI based on region position and size. The ROI is controlled by using registers 0x8510 to 0x8510.

[2] - Reserved

[1] - Reserved

[0] – Enable firmware frame control. Setting this bit to '1' allows the firmware to update the sensor configuration to control the frame rate and sub-windowing features through the simple firmware interface. The frame rate is controlled using registers 0x8518 to 0x8521.

13.3.2.4 Firmware status (0x8504)

0x8504 fw_status

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved	Reserved	PROM Load Pass	Prom Present	Reserved	reserved	Maximum Vblank violated	Minimum Vblank violated

This register is used to obtain status information from the firmware. These bits will be set on various error conditions after trying to set the frame dimensions through the firmware. The bits are defined as follows:

[7] – Reserved

[6] – Reserved

[5] – This bit can be read to determine if the external PROM was loaded without errors

[4] – This bit can be read to determine if an external PROM was detected

[3] – Reserved

[2] – Reserved

[1] – This bit can be read to determine if num_vblank_rows > max_num_vblank_rows

[0] – This bit can be read to determine if num_vblank_rows < 7

13.3.2.5 Firmware subsampling control (0x8505)

0x8505 fw_subsample

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved				Vertical subsampling factor			

This register is used to control the sub-sampling of the chip. The bits are defined as follows:

[7:4] – Reserved
[3:0] - Vertical factor
0x0100 = subsample by 2
0x1000 = subsample by 4

13.3.2.6 Firmware image average (0x8506-0x8507)

0x8506 fw_img_average_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved				Image_average[11:8]			

0x8507 fw_img_average_lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Image_average[7:0]							

These two register contain the read-only image average (12 bit value). This information is updated once per frame.

13.3.2.7 Firmware subwindow frame X-size (0x8508-0x8509)

0x8508 fw_subwindow_x_size_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
Reserved					Subwindow x_size [10:8]		

0x8509 fw_subwindow_x_size _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Subwindow x_size [7:0]							

These two registers are used to control the x-size of the subwindow. See section 13.1.7 – “How to set up sub-windowing” on page 36 for details on how to set up a subwindow.

13.3.2.8 Firmware subwindow frame Y-size (0x850A-0x850B)

0x850A fw_subwindow_y_size_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
Reserved					Subwindow y_size [10:8]		

0x850B fw_subwindow_y_size _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Subwindow y_size [7:0]							

These two registers are used to control the y-size of the subwindow. See section 13.1.7 – “How to set up sub-windowing” on page 36 for details on how to set up a subwindow. Also note the remark in this paragraph on the limitation in the vertical dimension.

13.3.2.9 Firmware subwindow frame X-position (0x850C-0x850D)

0x850C fw_subwindow_x_position_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved					Subwindow x_position [10:8]		

0x850D fw_subwindow_x_position _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Subwindow x_position [7:0]							

These two registers are used to control the x-position of the subwindow. See section 13.1.7 – “How to set up sub-windowing” on page 36 for details on how to set up a subwindow.

Note: Subwindow reference is the top-left corner of the frame.

13.3.2.10 Firmware subwindow frame Y-position (0x850E-0x850F)

0x850E fw_subwindow_y_position_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved					Subwindow y_position [10:8]		

0x850F fw_subwindow_y_position _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Subwindow y_position [7:0]							

These two registers are used to control the y-position of the subwindow. See section 13.1.7 – “How to set up sub-windowing” on page 36 for details on how to set up a subwindow. Also note the remark in this paragraph on the limitation in the vertical dimension.

Note: Subwindow reference is the top-left corner of the frame.

13.3.2.11 Firmware region of interest (ROI) X-size (0x8510-0x8511)

0x8510 fw_roi_x_size_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0
Reserved					ROI x_size [10:8]		

0x8511 fw_roi_x_size _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROI x_size [7:0]							

These two registers are used to control the x-size of the region of interest. See section 13.1.8 – “How to control statistics collection (and Autobrite to expose) based on a sub-region of the image” on page 37 for details on how to set up a region of interest.

13.3.2.12 Firmware region of interest (ROI) Y-size (0x8512-0x8513)

0x8512 fw_roi_y_size_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
Reserved					ROI y_size [10:8]		

0x8513 fw_roi_y_size _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROI y_size [7:0]							

These two registers are used to control the y-size of the region of interest. See section 13.1.8 – “How to control statistics collection (and Autobrite to expose) based on a sub-region of the image” on page 37 for details on how to set up a region of interest.

13.3.2.13 Firmware region of interest (ROI) X-position (0x8514-0x8515)

0x8514 fw_roi_x_position_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved					ROI x_position [10:8]		

0x8515 fw_roi_x_position _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROI x_position [7:0]							

These two registers are used to control the x-position of the statistic region of interest. See section 13.1.8 – “How to control statistics collection (and Autobrite to expose) based on a sub-region of the image” on page 37 for details on how to set up a region of interest.

Note: ROI reference is top-left of a frame.

13.3.2.14 Firmware region of interest (ROI) Y-position (0x8516-0x8517)

0x8516 fw_roi_y_position_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Reserved					ROI y_position [10:8]		

0x8517 fw_roi_y_position _lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROI y_position [7:0]							

These two registers are used to control the y-position of the statistic region of interest. See section 13.1.8 – “How to control statistics collection (and Autobrite to expose) based on a sub-region of the image” on page 37 for details on how to set up a region of interest.

Note: ROI reference is top-left of a frame.

13.3.2.15 Firmware frame rate control – clocks per second (0x8518-0x851B)

0x8518 fw_clocks_per_second_hi_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
Clocks_per_second [31:24]							

0x8519 fw_clocks_per_second_hi

Bit Definition							
7	6	5	4	3	2	1	0
1	0	0	1	1	0	1	1
Clocks_per_second [23:16]							

0x851A fw_clocks_per_second_m

Bit Definition							
7	6	5	4	3	2	1	0
1	1	1	1	1	1	0	0
Clocks_per_second [15:8]							

0x851B fw_clocks_per_second_lo

Bit Definition							
7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0
Clocks_per_second [7:0]							

These four registers are used to set the clock rate input of the chip in clocks per second. This is used in the calculations for setting the frame rate. By default, it is set for 27MHz (27,000,000 = 0x019BFCC0). See section 13.1.6 – “How to set a specific frame rate” on page 36 for details on how to set a specific frame rate.

13.3.2.16 Firmware frame rate control – frames per second (0x851C-0x851D)

0x851C fw_frames_per_second_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
frames_per_second [15:8]							

0x851D fw_frames_per_second_lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	1	1	1	1	0
frames_per_second [7:0]							

These two registers are used to set the frame rate of the chip. By default, the registers are set for 30 FPS. See section 13.1.6 – “How to set a specific frame rate” on page 36 for details on how to set a specific frame rate.

13.3.2.17 Firmware histogram remapping control – strength (0x8522)

0x8522 fw_hr_remap_strength

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1
Histogram_remap_strength [7:0]							

This register is used to set the strength factor for the histogram remapping function. See section 13.1.4 – “How to control Autoview histogram remapping” on page 35 for details on how to control the histogram remapping algorithm.

13.3.2.18 Firmware Autobrite control - number of upper bin pixels (0x852C-0x852F)

0x852C fw_wdr_desired_num_pix_upper_bin_hh

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Wdr_desired_num_pix_upper_bin [31:24]							

0x852D _wdr_desired_num_pix_upper_bin_h

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Wdr_desired_num_pix_upper_bin [23:16]							

0x852E _wdr_desired_num_pix_upper_bin_l

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
Wdr_desired_num_pix_upper_bin [15:8]							

0x852F _wdr_desired_num_pix_upper_bin_ll

Bit Definition							
7	6	5	4	3	2	1	0
1	1	0	1	1	1	0	0
Wdr_desired_num_pix_upper_bin [7:0]							

These four registers are used to set the desired amount of pixels whose values are in the upper bin range. This is used as an input for the firmware to automatically control the compression curve. See section 13.1.3 – “How to control Autobrite autoexposure and dynamic range” on page 35 for details on how to control Autobrite.

13.3.2.19 Firmware Autobrite control – desired minimum lower bin pixels (0x8530-0x8531)

0x8530 fw_wdr_des_min_num_pix_upper_bin_h

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Wdr_desired_min_num_pix_lower_bin [15:8]							

0x8531 fw_wdr_des_min_num_pix_upper_bin_l

Bit Definition							
7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	0
Wdr_desired_min_num_pix_lower_bin [7:0]							

This word is used to set the minimum desired amount of pixels whose values are in the lower bin range. This is used as an input for the firmware to automatically control the exposure time. See section 13.1.3 – “How to control Autobrite autoexposure and dynamic range” on page 35 for details on how to control Autobrite.

13.3.2.20 Firmware Autobrite control – desired maximum lower bin pixels (0x8530-0x8531)

0x8532 fw_wdr_des_max_num_pix_upper_bin_h

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0
Wdr_desired_max_num_pix_lower_bin [15:8]							

0x8533 fw_wdr_des_max_num_pix_upper_bin_l

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Wdr_desired_max_num_pix_lower_bin [7:0]							

This word is used to set the maximum desired amount of pixels whose values are in the lower bin range. This is used as an input for the firmware to automatically control the exposure time. See section 13.1.3 – “How to control Autobrite autoexposure and dynamic range” on page 35 for details on how to control Autobrite.

13.3.2.21 Upper bin pixel start (0x9302-0x9303)

0x9302 Upper bin pixel start_h

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1
				Upper bin start[11:8]			

0x9303 Upper bin pixel start_l

Bit Definition							
7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0
Upper bin start [7:0]							

This 12b word sets the lower limit for the top bin. All pixels with ADC values larger than this word will be counted as upper bin values for the automatic High Dynamic range control in Autobrite.

See also 13.1.3 – “How to control Autobrite autoexposure and dynamic range” on page 35 for details how to control Autobrite.

13.3.2.22 Firmware Autobrite control – minimum exposure time (0x8534-0x8535)

0x8534 fw_wdr_min_tint_hi

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
Wdr_min_tint [15:8]							

0x8535 fw_wdr_min_tint_lo

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
Wdr_min_tint [7:0]							

These two registers are used to set the minimum exposure time for the Autobrite algorithm. The value is expressed in row times. See section 13.1.3 – “How to control Autobrite autoexposure and dynamic range” on page 35 for details on how to control Autobrite.

13.3.2.23 Firmware ROM version number (0x853C-0x853F)

0x853C fw_version_number_major

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
ROM_version[31:24]							

0x853D fw_version_number_minor

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROM_version [23:16]							

0x853E fw_version_number_minor_minor

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
ROM_version [15:8]							

0x853F fw_version_number_build

Bit Definition							
7	6	5	4	3	2	1	0
1	0	0	0	1	0	0	1
ROM_version [7:0]							

These four registers are used to indicate the version number of the ROM. By default, the registers are set to 0x02000089. See section 13.1.1 – “How to determine the revision of the hardware and the firmware” on page 33 for details on how to determine the version number.

13.3.2.24 Firmware patch version number (0x857C-0x857F)

0x857C fw_patch_version_number_major

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
patch_version[31:24]							

0x857D fw_patch_version_number_minor

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
patch_version [23:16]							

0x857E fw_patch_version_number_minor_minor

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
patch_version [15:8]							

0x857F fw_patch_version_number_build

Bit Definition							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
patch_version [7:0]							

These four registers are used to indicate the version number of the firmware patch (if any). By default, the registers are set to 0x00000000, which indicates no patch. See section 13.1.1 – “How to determine the revision of the hardware and the firmware” on page 33 for details on how to determine the version number.

14 Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.asp

15 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

16 Disclaimer

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Or for additional information contact Melexis Direct:

Europe, Africa, Asia:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

America:
Phone: +1 248 306 5400
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