iW-RainboW-G15D
Qseven Generic Carrier Board
Hardware User Guide

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1   INTRODUCTION

1.1   Purpose

This document is the Hardware Reference Manual for the Qseven Generic Carrier Board. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Manual includes system setup, debugging and provides detailed information on the overall design and usage of the Qseven Generic Carrier Board from a Hardware Systems perspective.

1.2   Qseven Overview

The Qseven concept is an off-the-shelf, multi-vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven modules have a standardized form factor of 70mm x 70mm and have specified pinouts based on the high speed MXM system connector that has a standardized pinout regardless of the vendor.

The Qseven module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network and multiple USB ports. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven module. This MXM connector is a well-known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

iWave's Qseven Generic carrier board is also incorporated with additional two 80pin expansion connectors which can be used to connect iWave's Qseven CPU modules. These Expansion connectors bring the additional interfaces to carrier boards which are not supported by Qseven Edge connector.

1.3   List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Description
AC'97	Audio Codec '97
ARM	Advanced RISC Machine
BPP	Bits Per Pixel
CAN	Controller Area Network
CSI	Camera Sensor Interface
EEPROM	Electrically Erasable Programmable Read Only Memory
GBE	Gigabit Ethernet
GPIO	General Purpose Input Output

HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
I/O	Input/Output
JTAG	Joint Test Action Group
KB	Kilo Byte
LCD	Liquid Crystal Display
LDO	Low Drop-Out
LED	Light Emitting Diode
LVDS	Low-Voltage Differential Signalling
MB	Mega Byte
Mbps	Mega Bits per sec
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
MMC	Multi Media Card
OTG	On the Go
PCB	Printed Circuit board
PCI	Peripheral Controller Interconnect
PWM	Pulse Width Modulation
RGB	Red Green Blue
RJ45	Registered Jack 45
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TMDS	Transition-Minimized Differential Signalling
UART	Universal Asynchronous Receiver Transmitters
USB	Universal Serial bus
Wi-Fi	Wireless Fidelity

1.4   Reference

- Qseven Specification Revision 2.0

- Qseven® Design Guide

2   Qseven GENERIC CARRIER BOARD DESIGN

This section is designed to provide detailed information about the electrical design and practical considerations that went into the Qseven Generic Carrier Board. This section is organized to discuss each block in the following high level block diagram, as shown below.

2.1   Qseven Generic Carrier Board Block Diagram
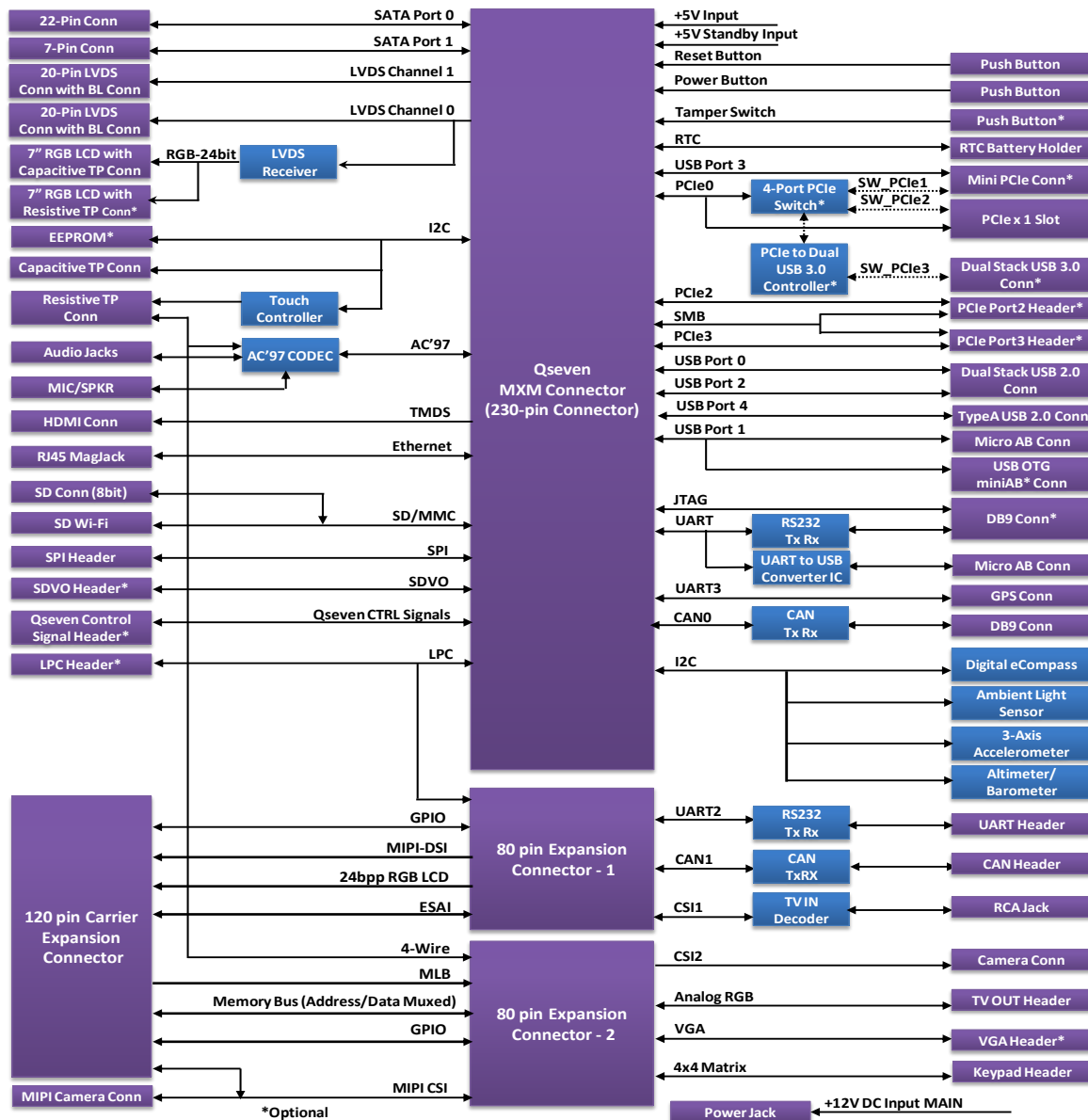
Figure 1: Qseven Generic Carrier Board Block Diagram

2.2 Qseven Generic Carrier Board Features

Qseven Generic Carrier Board supports the following features to validate Qseven Edge Connector Interfaces and iWave's Qseven CPU Module specific Expansion Connector interfaces.

Qseven Edge Connector Features

Serial Interface Features

- Debug UART console through USB Micro AB Connector

- UART0 header for iWave GPS

Communication Features

- 10/100/1000 Mbps Ethernet through RJ45MagJack

- SDIO Ports

  ❖ SD/MMC Connector[1]

  ❖ On board Taiyo Yuden SDIO Wi-Fi module "WYSAAVDX7"[1]

- USB Ports

  ❖ USB 2.0 Host x 2 Ports through Type-A Stacked Connector

  ❖ USB 2.0 OTG Port through Mini AB Connector

  ❖ USB 2.0 Host Port4 through Type A Connector

  ❖ Mini PCIe connector with USB 2.0 Host Interface[2]

- CAN port1 through DB9 Connector

High Speed Interface Features

- SATA

  ❖ 22pin Serial ATA Connector for SATA port0

  ❖ 7pin Serial ATA Connector for SATA port1

- PCI Express

  ❖ PCIe x1 Connector from Qseven MXM Connector

  ❖ PCIe Port 2 - SMD Pad Header

  ❖ PCIe Port 3 - SMD Pad Header

  ❖ 4-port PCIe Switch[4] through PCIe Port0 (Optional)

    ▪ Mini PCIe Connector through PCIe Switch Port1[2,4]

▪ PCIe to USB 3.0 Hub controller through PCIe Switch Port3 for USB 3.0 Host x 2[4]

Audio/Video Features

- AC'97 Audio Codec with 3.5mm Audio IN/OUT jack

- LVDS Display Interface

  ❖ 20pin LVDS0 connector with backlight connector[3]

  ❖ 7" RGB Resistive Touch LCD[3]

  ❖ 7" RGB Capacitive Touch LCD[3]

  ❖ 20pin LVDS1 connector with backlight connector

- HDMI port

Additional Features

- 10-Pin JTAG Connector

- RTC Coin cell Holder

- Control Buttons

  ❖ Power On/Off Button

  ❖ Reset Button

  ❖ Tamper Switch (Optional)

- EEPROM (Optional)

- Sensors

  ❖ Ambient Light Sensor

  ❖ Digital eCompass

  ❖ 3-Axis accelerometer

  ❖ Altimeter/Barometer

- Add-on Headers

  ❖ SPI Header

  ❖ LPC Header

  ❖ SDVO Header

  ❖ Qseven control signal Header

Note:
1. *Either 8-bit MMC/SDIO or Wi-Fi Module only can be used at a time.*
2. *Mini PCIe connector supports both USB interface and PCIe interface.*
3. *Either LVDS0 connector or 7" RGB resistive LCD or 7" RGB capacitive LCD can be used at a time.*
4. *By default 4-Port PCIe switch and USB 3.0 controller are not populated.*

iWave's Qseven CPU Module specific Expansion Connector Features

- UART2 Header
- CAN port2 connector
- TV-In Composite Video through RCA Jack
- 8bit CMOS Camera Connector
- MIPI Camera Connector
- 4X4 Keypad Header
- TV Out Composite Video Header
- VGA Interface Header
- 120-pin Carrier Board Expansion Connector

General Specification

- Power Supply   : 12V, 2A Power Input Jack
- LED Indicators
    - ❖ Power Indicator Red LEDs
    - ❖ Reset Indicator Red LED
- Temperature   **:** 0°C to +60°C
- Form Factor   : 120mm X 120mm Nano ITX

2.3   Qseven MXM Connector

The Qseven module utilizes a 230-pin board-edge connector that is also used for PCI Express capable notebook graphics cards following the MXM specification. Therefore this connector type is also known as MXM connector. The MXM connector (J12) is a robust, low-cost edge connector that is capable of handling high-speed serialized signals.
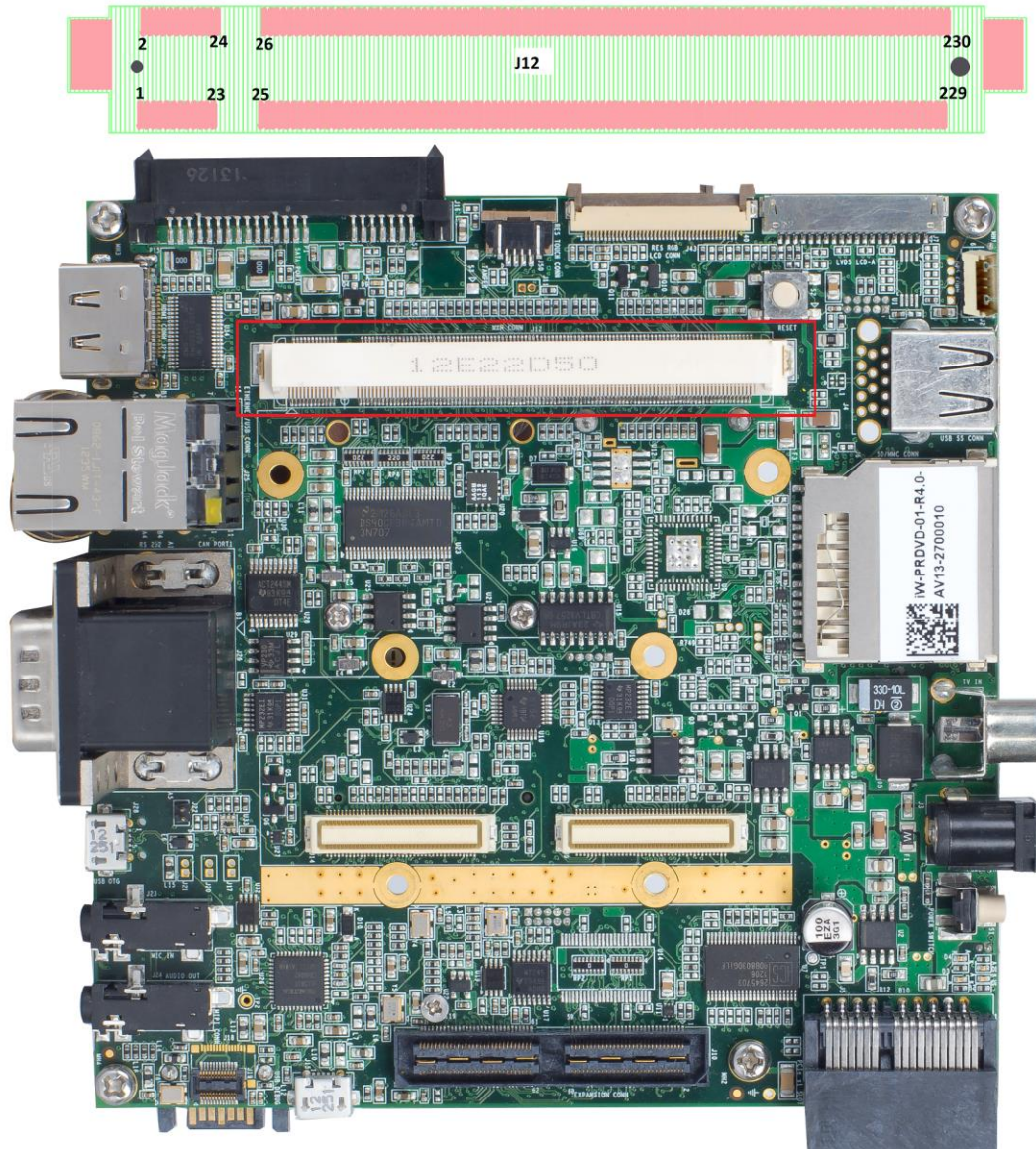
Figure 2: Qseven MXM Connector

Table 2: Qseven MXM Connector Pin Out

Pin No.	Edge Connector Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND1	Power	0V	Ground.
2	GND2	Power	0V	Ground.
3	GBE_MDI3-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 3 negative.
4	GBE_MDI2-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 2 negative.
5	GBE_MDI3+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 3 positive.
6	GBE_MDI2+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 2 positive.
7	GBE_LINK100#	Input	3.3V CMOS	100Mbps Ethernet Link status LED.
8	GBE_LINK1000#	Input	3.3V CMOS	Gigabit Ethernet Link status LED.
9	GBE_MDI1-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 1 negative.
10	GBE_MDI0-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 0 negative.
11	GBE_MDI1+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 1 positive.
12	GBE_MDI0+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 0 positive.
13	GBE_LINK#	Input	3.3V CMOS	Gigabit Ethernet Link status LED.
14	GBE_ACT#	Input	3.3V CMOS	Gigabit Ethernet Activity status LED.
15	GBE_CTREF	Power In	3.3V	Reference voltage for Ethernet magnetic centre tap.
16	SUS_S5#	Input	3.3V CMOS	Soft Off State. Default NC.
17	WAKE#	Output	3.3V CMOS	External system wake event. Default NC. Connected to 8th Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
18	SUS_S3#	Input	3.3V CMOS	Suspend to RAM. Default NC.

19	SUS_STAT#	Input	3.3V CMOS	Suspend Status. Default NC. Connected to 3rd Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
20	PWRBTN#	Output	3.3V CMOS/ 10K Pull-up	Power button. Connected to push button S1.
21	SLP_BTN#	Output	3.3V CMOS	Sleep button. Default NC. Connected to 5th Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
22	LID_BTN#	Output	3.3V CMOS	LID Button. Default NC. Connected to 6th Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
23	GND3	Power	0V	Ground.
24	GND4	Power	0V	Ground.
25	GND5	Power	0V	Ground.
26	PWGIN	Output	5V CMOS/ 10K Pull-up	Power good input.
27	BATLOW#	Output	3.3V CMOS	Battery low indication. Default NC. Connected to 9th Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
28	RSTBTN#	Output	3.3V CMOS	Active low Reset button. Connected to push button S2.
29	SATA0_TX+	Input	Differential	SATA0 Transmit Input differential positive.
30	SATA1_TX+	Input	Differential	SATA1 Transmit Input differential positive.
31	SATA0_TX-	Input	Differential	SATA0 Transmit Input differential negative.

32	SATA1_TX-	Input	Differential	SATA1 Transmit Input differential negative.
33	SATA_ACT#	Input	3.3V CMOS	SATA command Activity line.
34	GND6	Power	0V	Ground.
35	SATA0_RX+	Output	Differential	SATA0 Receive Output differential positive.
36	SATA1_RX+	Output	Differential	SATA1 Receive Output differential positive.
37	SATA0_RX-	Output	Differential	SATA0 Receive Output differential negative.
38	SATA1_RX-	Output	Differential	SATA1 Receive Output differential negative.
39	GND7	Power	0V	Ground.
40	GND8	Power	0V	Ground.
41	BIOS_DISABLE#/ BOOT_ALT#	Output	3.3V CMOS	Default NC. Connected to 10th Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
42	SDIO_CLK#	Input	3.3V CMOS	SD/MMC card clock.
43	SDIO_CD#	Output	3.3V CMOS	SD/MMC card Detect pin.
44	SDIO_LED	Input	3.3V CMOS	SD/MMC card indication LED.
45	SDIO_CMD	Input/Output	3.3V CMOS	SD/MMC card Command line.
46	SDIO_WP	Output	3.3V CMOS	SD/MMC card Write Protect pin.
47	SDIO_PWR#	Input	3.3V CMOS	SD/MMC card Power Enable pin.
48	SDIO_DAT1	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit1).
49	SDIO_DAT0	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit0).
50	SDIO_DAT3	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit3).
51	SDIO_DAT2	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit2).
52	SDIO_DAT5	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit5).
53	SDIO_DAT4	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit4).
54	SDIO_DAT7	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit7).
55	SDIO_DAT6	Input/Output	3.3V CMOS	SD/MMC card Data Line (Bit6).
56	RSVD1	NC	NC	Default NC. Connected to 1st Pin of Qseven Control Signal Header (J53) through resistor and default not populated.

57	GND9	Power	0V	Ground.
58	GND10	Power	0V	Ground.
59	HDA_SYNC/ I2S_WS	Input	3.3V CMOS	Audio Transmit frame synchronization line.
60	SMB_CLK/ GP1_I2C_CLK	Input	3.3V CMOS	System Management Bus Clock.
61	HDA_RST#/ I2S_RST#	Input	3.3V CMOS	Audio reset.
62	SMB_DAT/ GP1_I2C_DAT	Input/Output	3.3V CMOS	System Management Bus Data.
63	HDA_BITCLK/ I2S_CLK	Input	3.3V CMOS	Audio Transmit Clock line.
64	SMB_ALERT#	Output	3.3V CMOS	System Management Bus Alert input. Default NC. Connected to 3rd Pin of SDVO Header (J47) through resistor and default not populated.
65	HDA_SDI/ I2S_SDI	Output	3.3V CMOS	Audio Transmit data line.
66	GP0_I2C_CLK	Input	3.3V CMOS/ 4.7K Pull-up	I2C Clock signal.
67	HDA_SDO/ I2S_SDO	Input	3.3V CMOS	Audio Receive data line.
68	GP0_I2C_DAT	Input/Output	3.3V CMOS/ 4.7K Pull-up	I2C Data signal.
69	THRM#	Output	3.3V CMOS	Thermal Alarm active low signal. Connected to 11th Pin of Qseven Control Signal Header (J53).
70	WDTRIG#	Output	3.3V CMOS	Watchdog trigger signal. Default NC. Connected to 2nd Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
71	THRMTRIP#	Input	3.3V CMOS	Thermal Trip indicates an overheating condition of the Processor. Connected to 12th Pin of Qseven Control Signal Header (J53).

72	WDOUT	Input	3.3V CMOS	Watchdog event indicator input. Default NC. Connected to 4th Pin of Qseven Control Signal Header (J53) through resistor and default not populated.
73	GND11	Power	0V	Ground.
74	GND12	Power	0V	Ground.
75	USB_P7-/ USB_SSTX0-	Input/Output	Differential	USB Host Port7 Data negative.
76	USB_P6-/ USB_SSRX0-	Input/Output	Differential	USB Host Port6 Data negative.
77	USB_P7+/ USB_SSTX0+	Input/Output	Differential	USB Host Port7 Data positive.
78	USB_P6+/ USB_SSRX0+	Input/Output	Differential	USB Host Port6 Data positive.
79	USB_6_7_OC#	Output	3.3V CMOS	Over current sense for USB ports 6 & 7. Connected to 114th Pin of Carrier board Expansion connector (J10).
80	USB_4_5_OC#	Output	3.3V CMOS	Over current sense for USB port 4 & 5.
81	USB_P5-/ USB_SSTX1-	Input/Output	Differential	USB Host Port5 Data Negative.
82	USB_P4-/ USB_SSRX1-	Input/Output	Differential	USB Host Port4 Data negative.
83	USB_P5+/ USB_SSTX1+	Input/Output	Differential	USB Host Port5 Data Positive.
84	USB_P4+/ USB_SSRX1+	Input/Output	Differential	USB Host Port4 Data Positive.
85	USB_2_3_OC#	Output	3.3V CMOS	Over current sense for USB port 2 & 3.
86	USB_0_1_OC#	Output	3.3V CMOS	Over current sense for USB port 0 & 1.
87	USB_P3-	Input/Output	Differential	USB Host Port3 Data negative.
88	USB_P2-	Input/Output	Differential	USB Host Port2 Data negative.
89	USB_P3+	Input/Output	Differential	USB Host Port3 Data Positive.
90	USB_P2+	Input/Output	Differential	USB Host Port2 Data Positive.
91	USB_CC	Output	3.3V CMOS	USB client connect.
92	USB_ID	Output	3.3V CMOS	USB OTG ID to identify Host & device.
93	USB_P1-	Input/Output	Differential	USB OTG Data negative.

94	USB_P0-	Input/Output	Differential	USB Host Port0 Data negative.
95	USB_P1+	Input/Output	Differential	USB OTG Data Positive.
96	USB_P0+	Input/Output	Differential	USB Host Port0 Data Positive.
97	GND13	Power	0V	Ground.
98	GND14	Power	0V	Ground.
99	eDP0_TX0+/ LVDS_A0+	Input	LVDS	LVDS primary channel differential pair0 positive.
100	eDP1_TX0+/ LVDS_B0+	Input	LVDS	LVDS secondary channel differential pair0 positive.
101	eDP0_TX0-/ LVDS_A0-	Input	LVDS	LVDS primary channel differential pair0 negative.
102	eDP1_TX0-/ LVDS_B0-	Input	LVDS	LVDS secondary channel differential pair0 negative.
103	eDP0_TX1+/ LVDS_A1+	Input	LVDS	LVDS primary channel differential pair1 positive.
104	eDP1_TX1+/ LVDS_B1+	Input	LVDS	LVDS secondary channel differential pair1 positive.
105	eDP0_TX1-/ LVDS_A1-	Input	LVDS	LVDS primary channel differential pair1 negative.
106	eDP1_TX1-/ LVDS_B1-	Input	LVDS	LVDS secondary channel differential pair1 negative.
107	eDP0_TX2+/ LVDS_A2+	Input	LVDS	LVDS primary channel differential pair2 positive.
108	eDP1_TX2+/ LVDS_B2+	Input	LVDS	LVDS secondary channel differential pair2 positive.
109	eDP0_TX2-/ LVDS_A2-	Input	LVDS	LVDS primary channel differential pair2 negative.
110	eDP1_TX2-/ LVDS_B2-	Input	LVDS	LVDS secondary channel differential pair2 negative.
111	LVDS_PPEN	Input	3.3V CMOS	LVDS LCD panel power enable control.
112	LVDS_BLEN	Input	3.3V CMOS	LVDS LCD panel Backlight enable control.
113	eDP0_TX3+/ LVDS_A3+	Input	LVDS	LVDS primary channel differential pair3 positive.
114	eDP1_TX3+/ LVDS_B3+	Input	LVDS	LVDS secondary channel differential pair3 positive.

115	eDP0_TX3-/ LVDS_A3-	Input	LVDS	LVDS primary channel differential pair3 negative.
116	eDP1_TX3-/ LVDS_B3-	Input	LVDS	LVDS secondary channel differential pair3 negative.
117	GND15	Power	0V	Ground.
118	GND16	Power	0V	Ground.
119	eDP0_AUX+/ LVDS_A_CLK+	Input	LVDS	LVDS primary channel differential clock positive.
120	eDP1_AUX+/ LVDS_B_CLK+	Input	LVDS	LVDS secondary channel differential clock positive.
121	eDP0_AUX-/ LVDS_A_CLK-	Input	LVDS	LVDS primary channel differential clock negative.
122	eDP1_AUX-/ LVDS_B_CLK-	Input	LVDS	LVDS secondary channel differential clock negative.
123	LVDS_BLT_CTRL/ GP_PWM_OUT0	Input	3.3V CMOS	LVDS LCD Panel backlight brightness control.
124	GP_1-Wire_Bus	Input/Output	3.3V CMOS	HDMI CEC bus.
125	GP2_I2C_DAT/ LVDS_DID_DAT	Input/Output	3.3V CMOS/ 4.7K Pull-up	Display ID DDC data line used for LVDS flat panel detection.
126	eDP0_HPD#/ LVDS_BLC_DAT	Input/Output	3.3V CMOS/ 4.7K Pull-up	Control data signal for external SSC clock chip.
127	GP2_I2C_CLK/ LVDS_DID_CLK	Input	3.3V CMOS/ 4.7K Pull-up	Display ID DDC clock line used for LVDS flat panel detection.
128	eDP1_HPD#/ LVDS_BLC_CLK	Input	3.3V CMOS/ 4.7K Pull-up	Control clock signal for external SSC clock chip.
129	CAN0_TX	Input	3.3V CMOS	CAN channel one TX line.
130	CAN0_RX	Output	3.3V CMOS	CAN channel one RX line
131	DP_LANE3+/ TMDS_CLK+	Input	TMDS	HDMI differential clock positive.
132	RSVD2 (Differential Pair)	NC	NC	Default NC. Connected to 2nd Pin of SDVO Header (J47) through resistor and default not populated.
133	DP_LANE3-/ TMDS_CLK-	Input	TMDS	HDMI differential clock negative

134	RSVD3 (Differential Pair)	NC	NC	Default NC. Connected to 4th Pin of SDVO Header (J47) through resistor and default not populated.
135	GND17	Power	0V	Ground.
136	GND18	Power	0V	Ground.
137	DP_LANE1+/ TMDS_LANE1+	Input	TMDS	HDMI differential data1 positive.
138	DP_AUX+	Input/Output	TMDS	HDMI differential device control data positive. Default NC. Connected to 6th Pin of SDVO Header (J47) through resistor and default not populated.
139	DP_LANE1-/ TMDS_LANE1-	Input	TMDS	HDMI differential data1 negative.
140	DP_AUX-	Input/Output	TMDS	HDMI differential device control data negative. Default NC. Connected to 8th Pin of SDVO Header (J47) through resistor and default not populated.
141	GND19	Power	0V	Ground.
142	GND20	Power	0V	Ground.
143	DP_LANE2+/ TMDS_LANE0+	Input	TMDS	HDMI differential data0 positive.
144	RSVD4 (Differential Pair)	Input	TMDS	Default NC. Connected to 10th Pin of SDVO Header (J47) through resistor and default not populated.
145	DP_LANE2-/ TMDS_LANE0-	Input	TMDS	HDMI differential data0 negative.
146	RSVD5 (Differential Pair)	NC	NC	Default NC. Connected to 12th Pin of SDVO Header (J47) through resistor and default not populated.

147	GND21	Power	0V	Ground.
148	GND22	Power	0V	Ground.
149	DP_LANE0+/ TMDS_LANE2+	Input	TMDS	HDMI differential data2 positive.
150	HDMI_CTRL_DAT	Input/Output	3.3V CMOS	I2C2 Data signal.
151	DP_LANE0-/ TMDS_LANE2-	Input	TMDS	HDMI differential data2 negative.
152	HDMI_CTRL_CLK	Input	3.3V CMOS/ 4.7K Pull-up	I2C2 Clock signal.
153	DP_HDMI_HPD#	Output	3.3V CMOS	HDMI Hot Plug Detect.
154	RSVD6	NC	NC	Default NC. Connected to 9th Pin of SDVO Header (J47) through resistor and default not populated.
155	PCIE_CLK_REF+	Input	Differential	PCIe differential reference clock positive.
156	PCIE_WAKE#	Output	3.3V CMOS	PCIe interface wake up signal.
157	PCIE_CLK_REF-	Input	Differential	PCIe differential reference clock negative.
158	PCIE_RST#	Input	3.3V CMOS	PCIe Reset.
159	GND23	Power	0V	Ground.
160	GND24	Power	0V	Ground.
161	PCIE3_TX+	Input	Differential	PCIe3 differential transmit line positive.
162	PCIE3_RX+	Output	Differential	PCIe3 differential receive line positive.
163	PCIE3_TX-	Input	Differential	PCIe3 differential transmit line negative.
164	PCIE3_RX-	Output	Differential	PCIe3 differential receive line negative.
165	GND25	Power	0V	Ground.
166	GND26	Power	0V	Ground.
167	PCIE2_TX+	Input	Differential	PCIe2 differential transmit line positive.
168	PCIE2_RX+	Output	Differential	PCIe2 differential receive line positive.
169	PCIE2_TX-	Input	Differential	PCIe2 differential transmit line negative.
170	PCIE2_RX-	Output	Differential	PCIe2 differential receive line negative.
171	UART0_TX	Input	3.3V CMOS	UART3 Transmit signal.
172	UART0_RTS#	Input	3.3V CMOS	UART3 RTS signal.
173	PCIE1_TX+	Input	Differential	PCIe1 differential transmit line positive.
174	PCIE1_RX+	Output	Differential	PCIe1 differential receive line positive.

175	PCIE1_TX-	Input	Differential	PCIe1 differential transmit line negative.
176	PCIE1_RX-	Output	Differential	PCIe1 differential receive line negative.
177	UART0_RX	Output	3.3V CMOS	UART3 Receive signal.
178	UART0_CTS#	Output	3.3V CMOS	UART3 CTS signal.
179	PCIE0_TX+	Input	Differential	PCIe0 differential transmit line positive.
180	PCIE0_RX+	Output	Differential	PCIe0 differential receive line positive.
181	PCIE0_TX-	Input	Differential	PCIe0 differential transmit line negative.
182	PCIE0_RX-	Output	Differential	PCIe0 differential receive line negative.
183	GND27	Power	0V	Ground.
184	GND28	Power	0V	Ground
185	LPC_AD0/GPIO0	Input/Output	3.3V CMOS	GPIO. Connected to Touch Controller interrupt and to 5th Pin of LPC Header (J34).
186	LPC_AD1/GPIO1	Input/Output	3.3V CMOS	GPIO. Connected to Digital eCompass interrupt & 6th Pin of LPC Header (J34).
187	LPC_AD2/GPIO2	Input/Output	3.3V CMOS	GPIO. Connected to 3-Axis Accelerometer interrupt & 7th Pin of LPC Header (J34).
188	LPC_AD3/GPIO3	Input/Output	3.3V CMOS	GPIO. Connected to Ambient Light Sensor interrupt & 8th Pin of LPC Header (J34).
189	LPC_CLK/GPIO4	Input/Output	3.3V CMOS	GPIO. Connected to Altimeter/ Barometer interrupt & 9th Pin of LPC Header (J34).
190	LPC_FRAME#/ GPIO5	Input/Output	3.3V CMOS	GPIO. Connected to SATA and to 10th Pin of LPC Header (J34).
191	SERIRQ/GPIO6	Input/Output	3.3V CMOS	GPIO Connected to MIPI power down signal and to 11th Pin of LPC Header (J34).
192	LPC_LDRQ#/ GPIO7	Input/Output	3.3V CMOS	GPIO. Connected to USB power switch and to 12th Pin of LPC Header (J34).
193	VCC_RTC	Power	3V	RTC battery voltage input.

194	SPKR/ GP_PWM_OUT2	Input	3.3V CMOS	PWM used to control the LVDS LCD Backlight.
195	FAN_TACHOIN/ GP_TIMER_IN	Output	3.3V CMOS	Fan tachometer input. Default NC. Connected to 5th Pin of SDVO Header (J47) through resistor and default not populated.
196	FAN_PWMOUT/ GP_PWM_OUT1	Input	3.3V CMOS	Fan PWM input. Default NC. Connected to 7th Pin of SDVO Header (J47) through resistor and default not populated.
197	GND29	Power	0V	Ground.
198	GND30	Power	0V	Ground.
199	SPI_MOSI	Input/Output	3.3V CMOS	SPI Master Out Slave In. Connected to 4th Pin of SPI Header (J29).
200	SPI_CS0#	Input	3.3V CMOS	SPI chip select 0. Connected to 1st Pin of SPI Header (J29).
201	SPI_MISO	Input/Output	3.3V CMOS	SPI Master In Slave Out. Connected to 2nd Pin of SPI Header (J29).
202	SPI_CS1#	Input	3.3V CMOS	SPI chip select 1. Connected to 7th Pin of SPI Header (J29).
203	SPI_SCK	Input	3.3V CMOS	SPI clock input. Connected to 5th Pin of SPI Header (J29).
204	MFG_NC4	Output	3.3V CMOS	JTAG Reset Output.
205	VCC_5V_SB1	Power	5V	Standby Power Supply.
206	VCC_5V_SB2	Power	5V	Standby Power Supply.
207	MFG_NC0	Output	3.3V CMOS	JTAG Test Clock.
208	MFG_NC2	Output	3.3V CMOS	Debug UART RX data line UART2_RXD (EIM_D27).
209	MFG_NC1	Input	3.3V CMOS	Debug UART TX data line. UART2_TXD (EIM_D26).
210	MFG_NC3	Output	3.3V CMOS	JTAG Test Mode Select.
211	VCC1	Power	5V	Input Supply Voltage.
212	VCC2	Power	5V	Input Supply Voltage.

213	VCC3	Power	5V	Input Supply Voltage.
214	VCC4	Power	5V	Input Supply Voltage.
215	VCC5	Power	5V	Input Supply Voltage.
216	VCC6	Power	5V	Input Supply Voltage.
217	VCC7	Power	5V	Input Supply Voltage.
218	VCC8	Power	5V	Input Supply Voltage.
219	VCC9	Power	5V	Input Supply Voltage.
220	VCC10	Power	5V	Input Supply Voltage.
221	VCC11	Power	5V	Input Supply Voltage.
222	VCC12	Power	5V	Input Supply Voltage.
223	VCC13	Power	5V	Input Supply Voltage.
224	VCC14	Power	5V	Input Supply Voltage.
225	VCC15	Power	5V	Input Supply Voltage.
226	VCC16	Power	5V	Input Supply Voltage.
227	VCC17	Power	5V	Input Supply Voltage.
228	VCC18	Power	5V	Input Supply Voltage.
229	VCC19	Power	5V	Input Supply Voltage.
230	VCC20	Power	5V	Input Supply Voltage.

2.4   Serial Interface Features

2.4.1 Debug UART console

Debug UART signals from Qseven MXM connector is connected to UART to USB conversion and to USB Micro AB Connector (J15). This Micro USB Connector can be used for Debug purpose. This is not the full functional UART and supports only TX and RX signals.
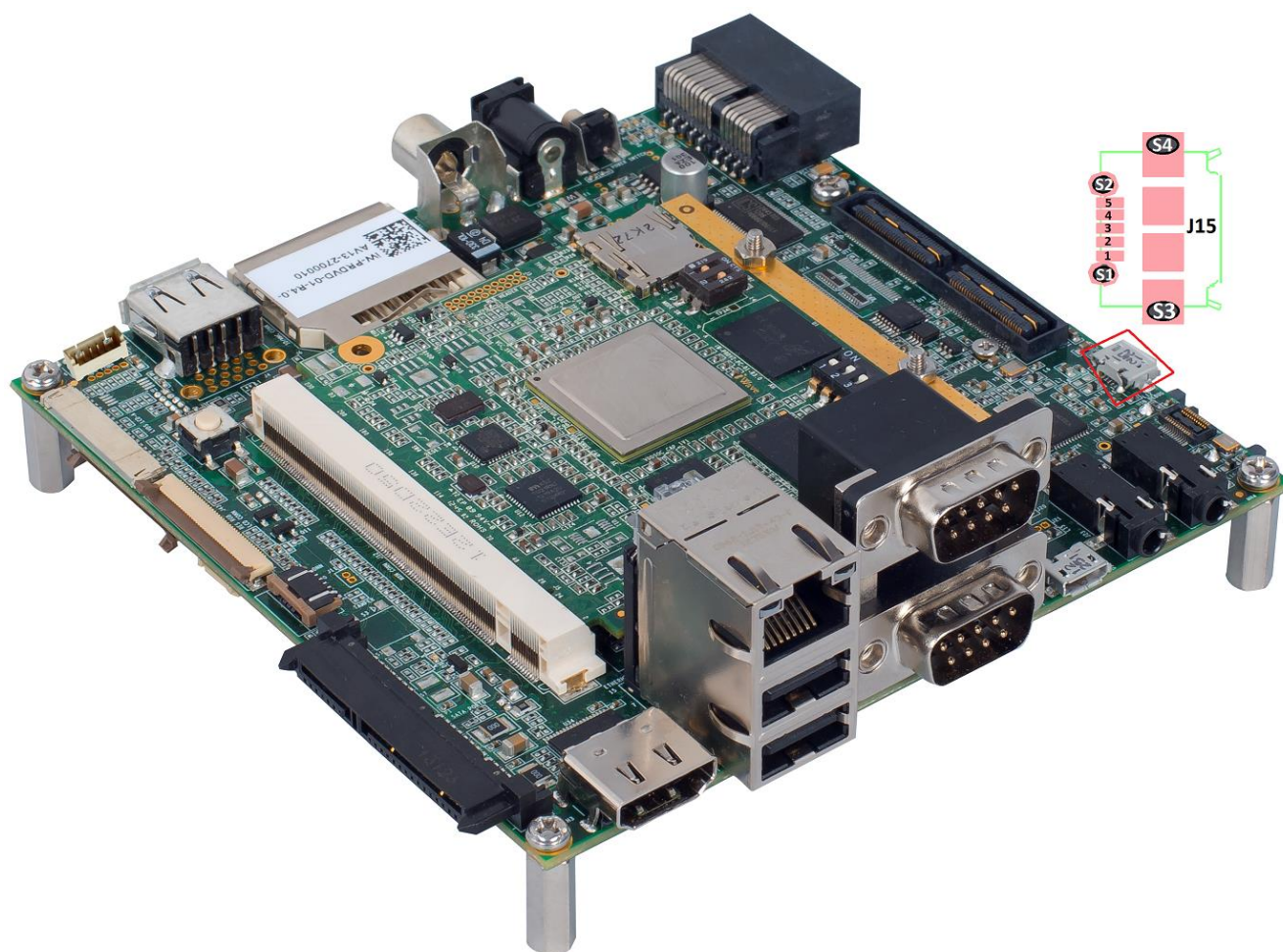
Figure 3: Debug UART Connector

Table 3: Debug UART Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	DBUG_VBUS	Power	5V	Debug USB, 5V Power.
2	DBUG_USB_DM	Input/Outpu	Differential	Debug USB, Data negative.
3	DBUG_USB_DP	Input/Outpu	Differential	Debug USB, Data positive.
4	NC	NC	NC	NC.
5	GND	Power	0V	Ground.
S1,S2, S3,S4	DSUB_SHLD_GND	Power	0V	Shield Ground.

Note: Refer "APPENDIX IV" for connecting Debug UART USB Cable Procedure

2.4.2 UART0 header for iWave GPS

Qseven Generic Carrier Board supports on board UART0 header (J2) through UART0 interface of Qseven MXM connector. This header can be used to connect iWave's GPS module and physically located on the top of the board as shown below.

Number of Pins: 6
Connector Part number: 10114829-10106LF
Mating Connector: 10114826-00006LF from FCI
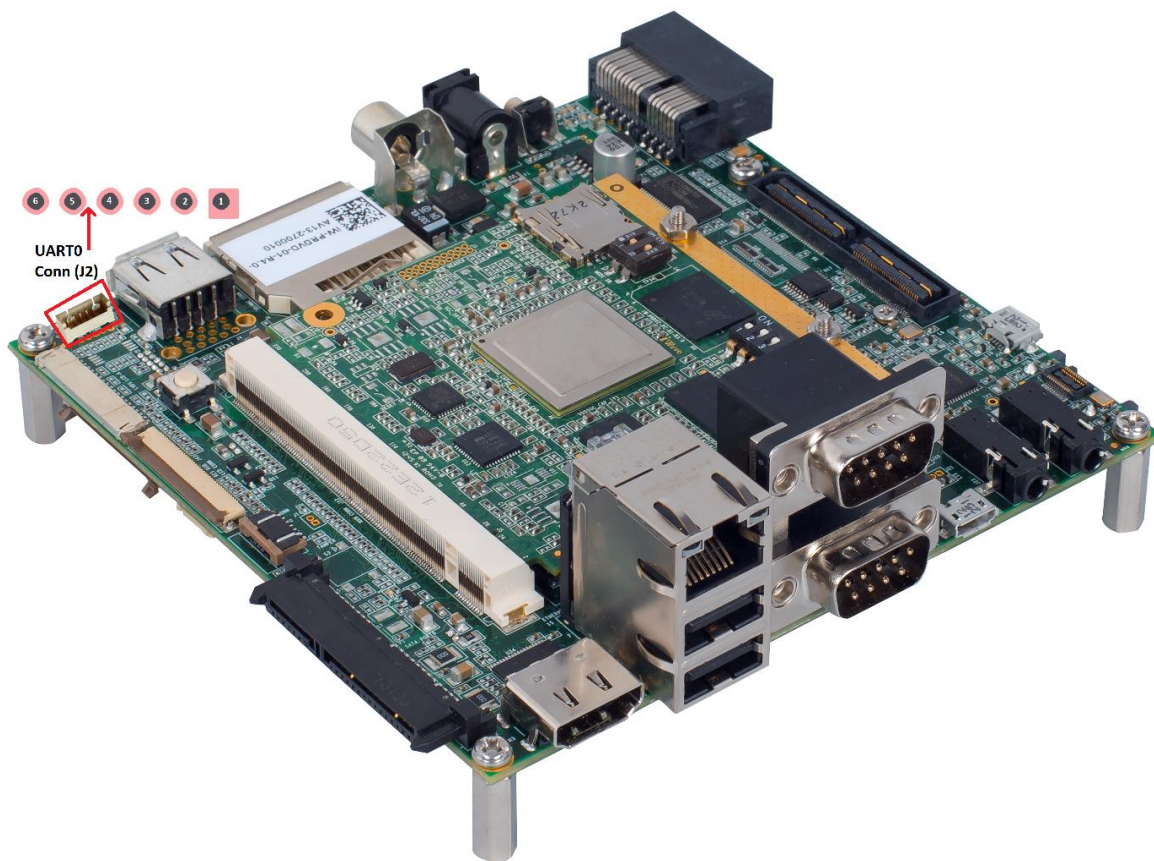
Figure 4: UART0 header

Table 4: UART0 header Pin Outs

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	V_BCKUP	Power	3V	RTC battery voltage Input from RTC battery.
2	3.3V_MAIN	Power	3.3V	Input voltage.
3	GND	Power	0V	Ground.
4	UART_RXD	Input	3.3V CMOS	UART receive signal. Connected to 177th Pin of Qseven MXM Connector.
5	UART_TXD	Output	3.3V CMOS	UART transmit signal. Connected from 171st Pin of Qseven MXM Connector.
6	NC	NC	NC	NC.

2.5   Communication Features

2.5.1 Gigabit Ethernet

Gigabit Ethernet signals from Qseven MXM connector are connected to RJ45 MagJack (J25A-Top), with LED indicators. RJ45 MagJack will work for both 10/100Mbps & 10/100/1000 Mbps Ethernet operation. This connector is physically located on top of the board as shown below.

GBE Conn (J25-Top)
USB Host (J25-Middle)
USB Host0 (J25-Bottom)
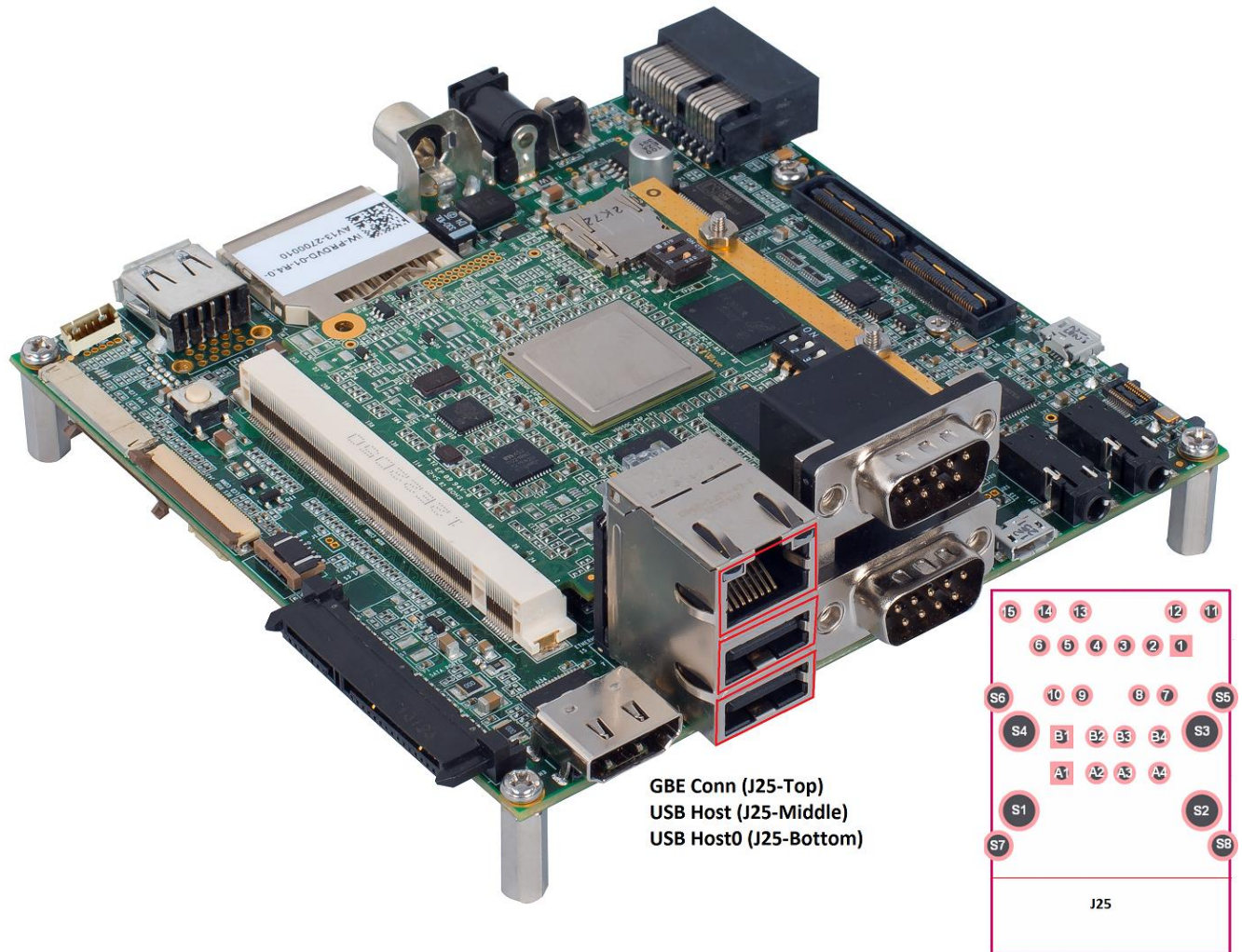
Figure 5: RJ45 (GBE), USB Host0 & Host2 Connector

Table 5: Gigabit Ethernet Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	TRD1+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 0 positive. Connected to 12th Pin of Qseven MXM Connector.
3	TRD1-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 0 negative. Connected to 10th Pin of Qseven MXM Connector.
4	TRD2+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 1 positive. Connected to 11th Pin of Qseven MXM Connector.
5	TRD2-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 1 negative. Connected to 9th Pin of Qseven MXM Connector.
6	CTREF	Power In	3.3V	Reference voltages for Gigabit Ethernet magnetics centre tap input. Connected to 15th Pin of Qseven MXM Connector.
7	TRD3+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 2 positive. Connected to 6th Pin of Qseven MXM Connector.
8	TRD3-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 2 negative. Connected to 4th Pin of Qseven MXM Connector.

9	TRD4+	Input/Output	Differential	Gigabit Ethernet MDI differential pair 3 positive. Connected to 5th Pin of Qseven MXM Connector.
10	TRD4-	Input/Output	Differential	Gigabit Ethernet MDI differential pair 3 negative. Connected to 3rd Pin of Qseven MXM Connector.
11	LED_Y-	Input	3.3V	Gigabit Ethernet Activity status LED Yellow Cathode. Connected to 14th Pin of Qseven MXM Connector.
12	LED_Y+	Input	3.3V	LED Yellow Anode. Connected to 3.3V power.
13	LED_G-	Input	3.3V	100Mbps Ethernet Link status LED Green Cathode. Connected to 7th Pin of Qseven MXM Connector.
14	LED_GO+	Input	3.3V	LED Green/Orange Anode. Connected to 3.3V power.
15	LED_O-	Input	3.3V	Gigabit Ethernet Link status LED Orange Cathode. Connected to 13th Pin of Qseven MXM Connector.
S5,S6,S7,S8	SHLD	Power	0V	Shield Ground Ethernet.

2.5.2 SDIO Ports

Qseven Generic Carrier Board supports SD/MMC connector and Wi-Fi Module connector through SDIO interface of Qseven MXM connector. Since SDIO interface is multiplexed between SD/MMC and Wi-Fi Module, either one only can be used at a time. This can be selected by controlling SDIO_PWR# signal from 47th pin of Qseven MXM connector. If SDIO_PWR# is low, SD/MMC is selected and if SDIO_PWR# is high, Wi-Fi module is selected.

2.5.2.1 SD/MMC Connector

Qseven Generic Carrier Board supports SD/MMC Connector (J6) to support SD cards/MMC cards/SDIO cards. This connector supports up to 8-bit data transfer with card detect & write protect feature. The main power to SD/MMC connector is 3.3V. SD/MMC connector is physically located on top of the board as shown below.
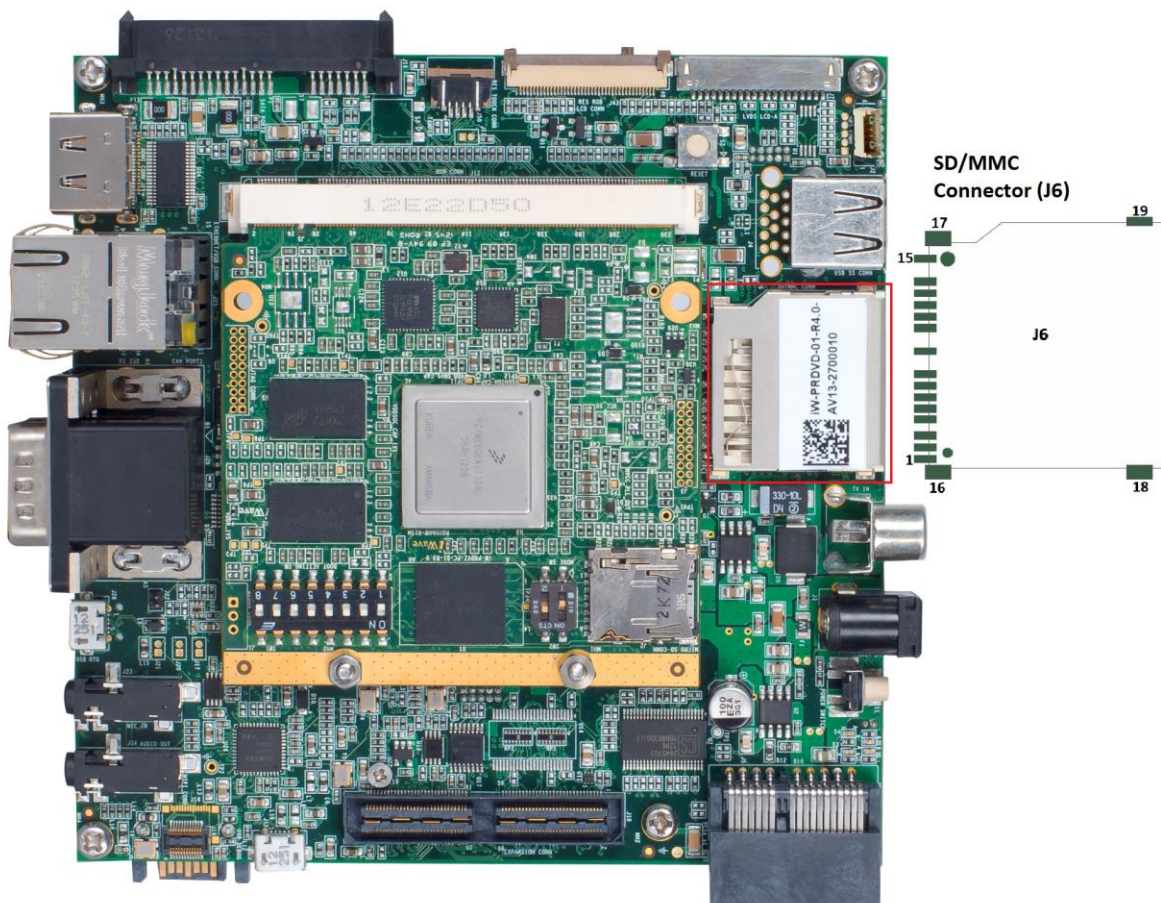
Figure 6: SD/MMC Card Connector

Table 6: SD/MMC Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	WP	Input	3.3V CMOS/ 2.2K Pull-up	SD/MMC Write Protect pin. Connected from 46th Pin of Qseven MXM Connector.
2	CD	Input	3.3V CMOS	SD/MMC card Detect pin. Connected from 43rd Pin of Qseven MXM Connector.
3	DAT1	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit1). Connected to 48th Pin of Qseven MXM Connector.
4	DAT0	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit0). Connected to 49th Pin of Qseven MXM Connector
5	DAT7	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit7). Connected to 54th Pin of Qseven MXM Connector.
6	GND/VSS2	Power	0V	Ground
7	DAT6	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit6). Connected to 55th Pin of Qseven MXM Connector.
8	CLK	Output	3.3V CMOS	SD/MMC Clock. Connected to 42nd Pin of Qseven MXM Connector.
9	VCC/VDD	Power	3.3V	Supply Voltage.
10	VSS1	Power	0V	Ground.
11	DAT5	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit5). Connected to 52nd Pin of Qseven MXM Connector.
12	CMD	Input/Output	3.3V CMOS/ 10K Pull-up	SD/MMC Command. Connected to 45th Pin of Qseven MXM Connector.
13	DAT4	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit4). Connected to 53rd Pin of Qseven MXM Connector.

14	DAT3	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit3). Connected to 50th Pin of Qseven MXM Connector.
15	DAT2	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit2). Connected to 51st Pin of Qseven MXM Connector.

2.5.2.2 SDIO Wi-Fi Module

Qseven Generic Carrier Board supports on-board Wi-Fi Module connector to connect SDIO Wi-Fi module. SDIO Wi-Fi module connector (J56) is physically located at the bottom of board as shown below.

SDIO Wi-Fi Connector:
Number of Pins: 20
Connector Part number: AXK720147G or AXK720247G or AXK720347G or AXK720447G from Panasonic Electric Works

Compatible Wi-Fi Module:
Part Number: WYSAAVDX7
Description: IEEE802.11b/g/n Wireless Module with Antenna
Manufacturer Name: TAIYO YUDEN

Note: Wi-Fi module will not be provided with the development kit and it is not part of the deliverable.
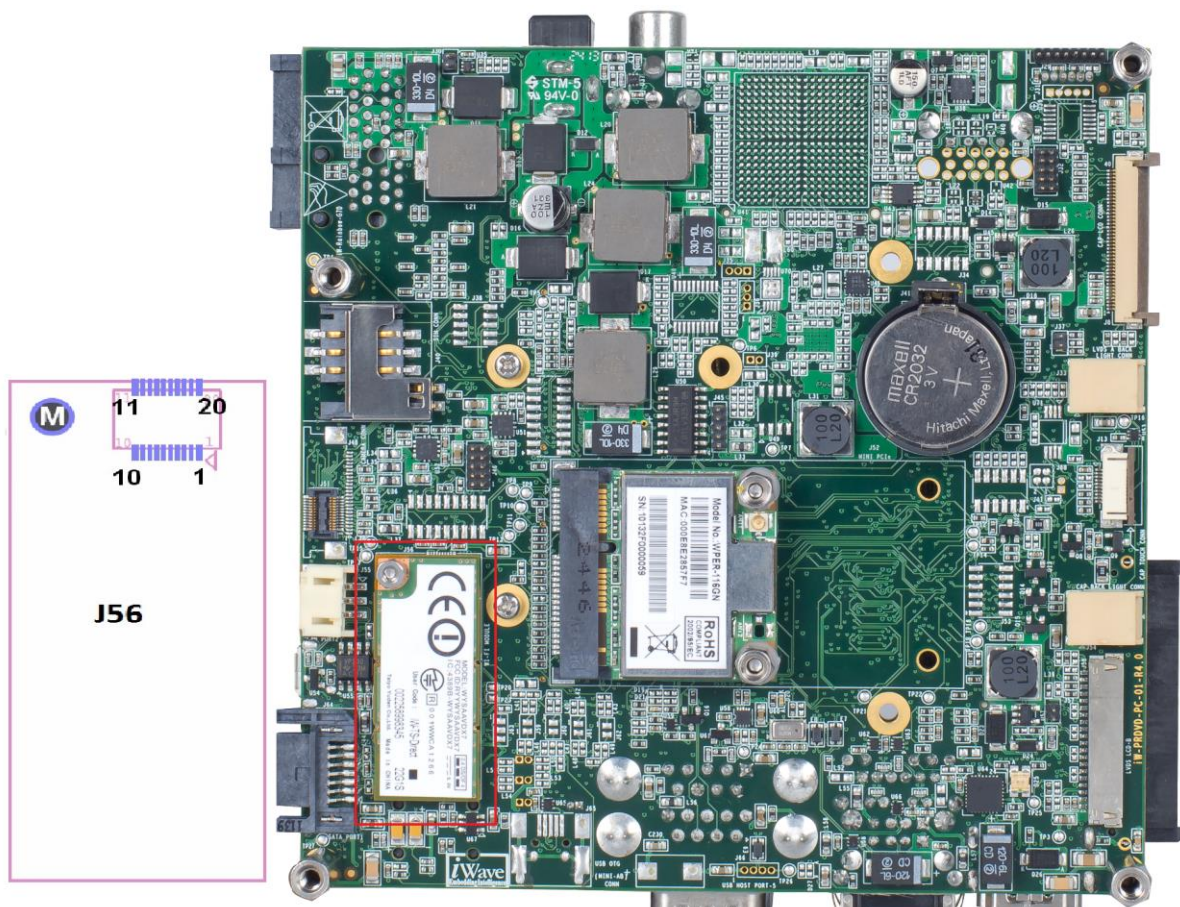
Figure 7: SDIO Wi-Fi Module Connector

Table 7: SDIO Wi-Fi Module Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	WiFi_DATA1	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit1). Connected to 48th Pin of Qseven MXM Connector.
3	WiFi_DATA0	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit0). Connected to 49th Pin of Qseven MXM Connector.
4	GND	Power	0V	Ground.

5	WiFi_CLK	Output	3.3V CMOS	SD/MMC Clock. Connected to 42nd Pin of Qseven MXM Connector.
6	VCC_3V3	Power	3.3V	Power Supply.
7	WiFi_CMD	Input/Output	3.3V CMOS/10K Pull-up	SD/MMC Command. Connected to 45th Pin of Qseven MXM Connector.
8	WiFi_DATA3	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit3). Connected to 50th Pin of Qseven MXM Connector.
9	WiFi_DATA2	Input/Output	3.3V CMOS	SD/MMC Data Line (Bit2). Connected to 51st Pin of Qseven MXM Connector.
10	GND	Power	0V	Ground.
11	GND	Power	0V	Ground.
12	SLEEP_CLK	Output	1.8V	External Sleep Clock (32.768KHz) For low power mode.
13	GND	Power	0V	Ground.
14	WIFI_PDN	Output	3.3V CMOS	Wi-Fi Power Down. Connected to 55th Pin of Expansion Connector1.
15	MAIN_RESET#	Output	3.3V CMOS	Main Reset.
16	WL_HOST_WKUP	Output	3.3V CMOS	WLAN Wakeup. Connected to 56th Pin of Expansion Connector1.
17	HOST_WL_WKUP	Input	3.3V CMOS	Host Wakeup. Connected from 57th Pin of Expansion Connector1.
18	GND	Power	0V	Ground.
19	VCC_5V	Power	5V	Power Supply.
20	VCC_5V	Power	5V	Power Supply.
M	Mechanical Support	Mechanical Support	Mechanical Support	Mechanical Support.

2.5.3 USB Ports

2.5.3.1 USB Host0 & Host2 Ports

USB Host0 & Host2 interfaces from Qseven MXM connector are connected to dual stack USB Type-A connector (J25B). Refer. **Figure 5** for the connector location.

Table 8: USB 2.0 Host Ports Connector Pin Outs

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
A1	VBUS1	Power	5V	USB Host Port 0, 5V Power (Bottom).
A2	D1-	Input/Output	Differential	USB Host Port 0, Data negative (Bottom). Connected to 94th Pin of Qseven MXM Connector.
A3	D1+	Input/Output	Differential	USB Host Port 0, Data Positive (Bottom). Connected to 96th Pin of Qseven MXM Connector.
A4	GND1	Power	0V	USB Host Port 0 Ground (Bottom).
B1	VBUS2	Power	5V	USB Host Port 2, 5V Power (Top).
B2	D2-	Input/Output	Differential	USB Host Port 2 Data negative (Top). Connected to 88th Pin of Qseven MXM Connector.
B3	D2+	Input/Output	Differential	USB Host Port 2 Data Positive (Top). Connected to 90th Pin of Qseven MXM Connector.
B4	GND2	Power	0V	USB Host Port 2 Ground (Top).
S1,S2	SHLD	Power	0V	Shield Ground (Bottom).
S3,S4	SHLD	Power	0V	Shield Ground USB2 (Top).

2.5.3.2 USB 2.0 OTG Port

USB port1 OTG signals from Qseven MXM connector are connected to USB Micro AB connector (J28). USB port1 supports OTG full functionality. By connecting proper USB Micro A Host cable or USB Micro B Device cable, USB OTG full functionality can be supported. USB Micro AB connector is physically located on the top of the board as shown below.
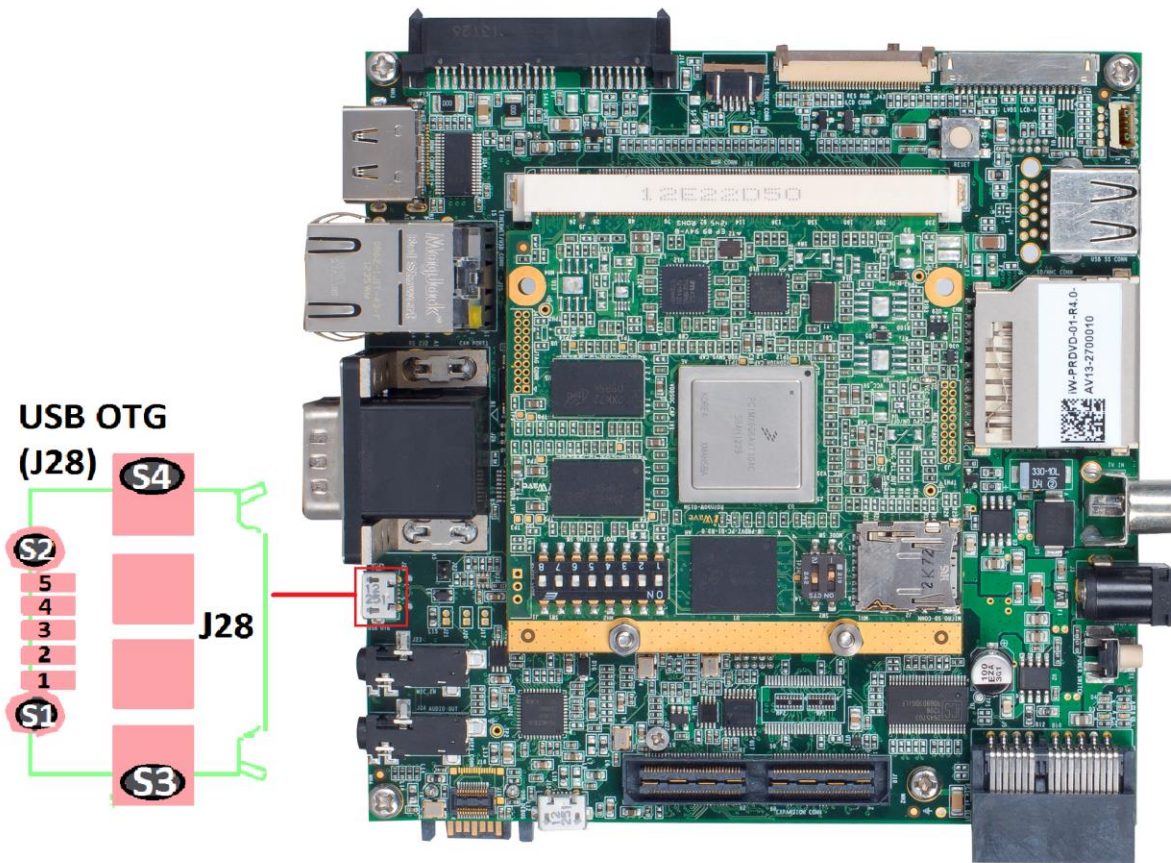
Figure 8: USB 2.0 OTG Connector

Table 9: USB 2.0 OTG Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/Termination	Description
1	VBUS	Power	5V	USB Port1 OTG, 5V Power.
2	D1-	Input/Output	Differential	USB Port1 OTG, Data negative. Connected to 93rd Pin of Qseven MXM Connector.
3	D1+	Input/Output	Differential	USB Port1 OTG, Data Positive. Connected to 95th Pin of Qseven MXM Connector.
4	ID	Input	3.3V CMOS	USD Port1 OTG, ID signal. Connected to 92nd Pin of Qseven MXM Connector.
5	GND	Power	0V	USB Port1 OTG Ground.

2.5.3.3 USB 2.0 Host Port4

USB2.0 Host Port4 signals from Qseven MXM connector are connected to USB Type-A connector (J4A) and it is physically located on top of the board as shown below.

Figure 9: USB 2.0 Connector

Table 10: USB 2.0 Host Port4 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/Termination	Description
1	VBUS	Power	5V	USB 3.0 Port 2 VBUS power.
2	D-	Input/Output	Differential	USB 2.0 Data Negative connected to 82nd pin of Qseven MXM connector from USB2.0 Hub controller port4. Optionally this pin is connected to USB3.0 Hub controller port2 and default not populated.
3	D+	Input/Output	Differential	USB 2.0 Data Positive connected to 84th pin of Qseven MXM connector from USB2.0 Hub controller port4. Optionally this pin is connected to USB3.0 Hub controller port2 and default not populated.
4	GND	Power	0V	Ground.

2.5.4 CAN Port1

CAN Transmit and Receive signals from Qseven MXM connector Pin 129 and 130 respectively are connected to CAN transceiver and the output signals from the transceiver are connected to DB9 connector (J26B). DB9 connector is physically located on top of the board as shown below.

Figure 10: CAN Port1 Connector

Table 11: CAN Port1 DB9 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/Termination	Description
B1	NC	NC	NC	No Connection.
B2	CAN0L	Input	Differential	CAN0 Differential negative.
B3	GND	Power	0V	Ground.
B4	NC	NC	NC	No Connection.

B5	CAN_SHLD_GND	Power	0V	CAN Shield Ground.
B6	GND	Power	0V	Ground.
B7	CAN0H	Input	Differential	CAN0 Differential positive.
B8	NC	NC	NC	No Connection.
B9	VCC_12V	Power	12V	12V Power supply.

2.6   High Speed Interface Features

2.6.1 SATA

2.6.1.1 SATA Port0

SATA port0 signals from Qseven MXM connector are connected to standard 22pin SATA connector with power. This connector (J16) is physically located on top of the board as shown below.
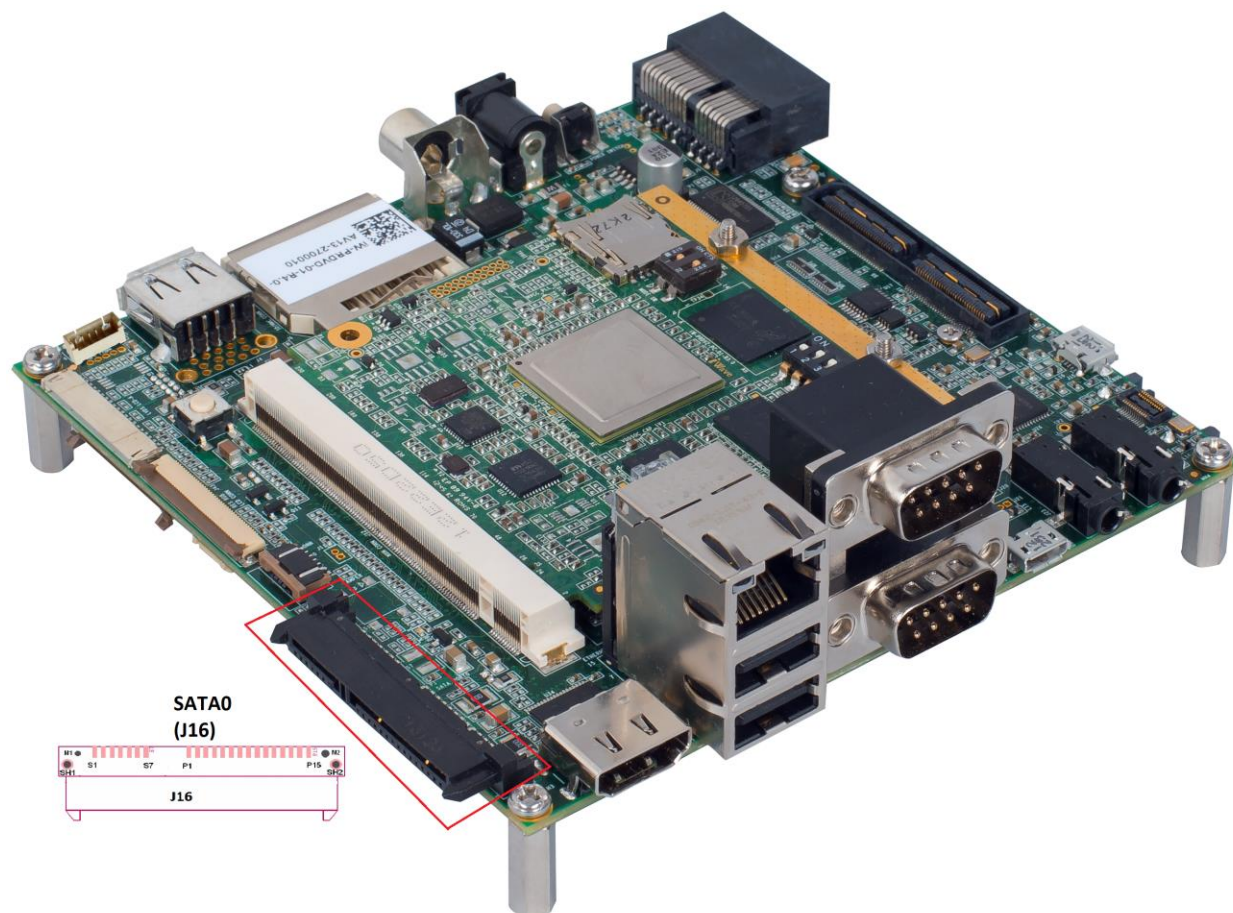
Figure 11: SATA Port0 Connector

Table 12: SATA Port0 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
S1	GND_S1	Power	0V	Ground
S2	TXP0	Output	Differential	SATA0 Transmit pair positive. Connected to 29th Pin of Qseven MXM Connector.
S3	TXN0	Output	Differential	SATA0 Transmit pair negative. Connected to 31st Pin of Qseven MXM Connector.
S4	GND_S4	Power	0V	Ground.
S5	RXN0	Input	Differential	SATA0 Receive pair negative. Connected from 37th Pin of Qseven MXM Connector.
S6	RXP0	Input	Differential	SATA0 Receive pair positive. Connected from 35th Pin of Qseven MXM Connector.
S7	GND_S7	Power	0V	Ground.
P1	VCC_3.3V	Power	3.3V	3.3V Power Supply.
P2	VCC_3.3V	Power	3.3V	3.3V Power Supply.
P3	VCC_3.3V	Power	3.3V	3.3V Power Supply.
P4	GND	Power	0V	Ground.
P5	GND	Power	0V	Ground.
P6	GND	Power	0V	Ground.
P7	VCC_5V	Power	5V	5V Power Supply.
P8	VCC_5V	Power	5V	5V Power Supply.
P9	VCC_5V	Power	5V	5V Power Supply.
P10	GND	Power	0V	Ground.
P11	GND	Power	0V	Ground.
P12	GND	Power	0V	Ground.
P13	VCC_12V	Power	12V	12V Power Supply.
P14	VCC_12V	Power	12V	12V Power Supply.
P15	VCC_12V	Power	12V	12V Power Supply.
SH1,SH2	SHLD	Power	0V	Shield Ground.
M1,M2	NC	NC	NC	Mechanical Support.

2.6.1.2 SATA Port1

SATA Port1 signals from Qseven MXM connector are connected to standard 7pin SATA connector without power. This connector (J64) is physically located on bottom of the board as shown below.
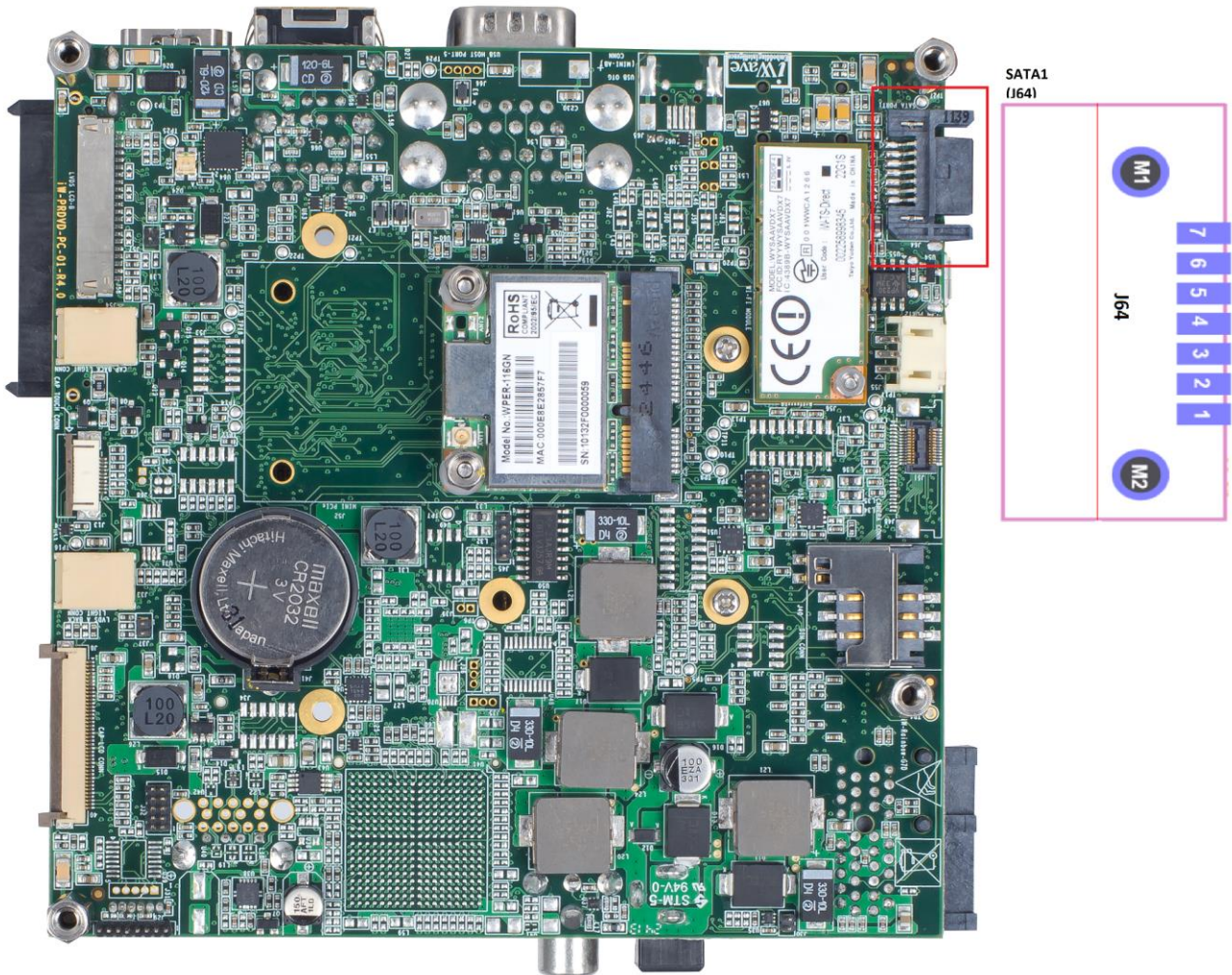
Figure 12: SATA Port1 Connector

Table 13: SATA Port1 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	TXP1	Output	Differential	SATA1 Transmit pair positive. Connected from 30th Pin of Qseven MXM Connector.
3	TXN1	Output	Differential	SATA1 Transmit pair negative. Connected from 32nd Pin of Qseven MXM Connector.
4	GND	Power	0V	Ground
5	RXN1	Input	Differential	SATA1 Receive pair negative. Connected to 38th Pin of Qseven MXM Connector.
6	RXP1	Input	Differential	SATA1 Receive pair positive. Connected to 36th Pin of Qseven MXM Connector.
7	GND	Power	0V	Ground.

2.6.2 PCI Express

2.6.2.1 PCIe x1 Connector

Qseven Generic Carrier Board supports PCIex1 connector. PCIe x1 signals are connected from Qseven MXM Connector. PCIe x1 connector (J5) is physically located on top of the board for external access.

Note: Optionally PCIe Port1 signals are connected from PCIe switch downstream port2 to this PCIex1 connector through resistors and this option is not supported by default.
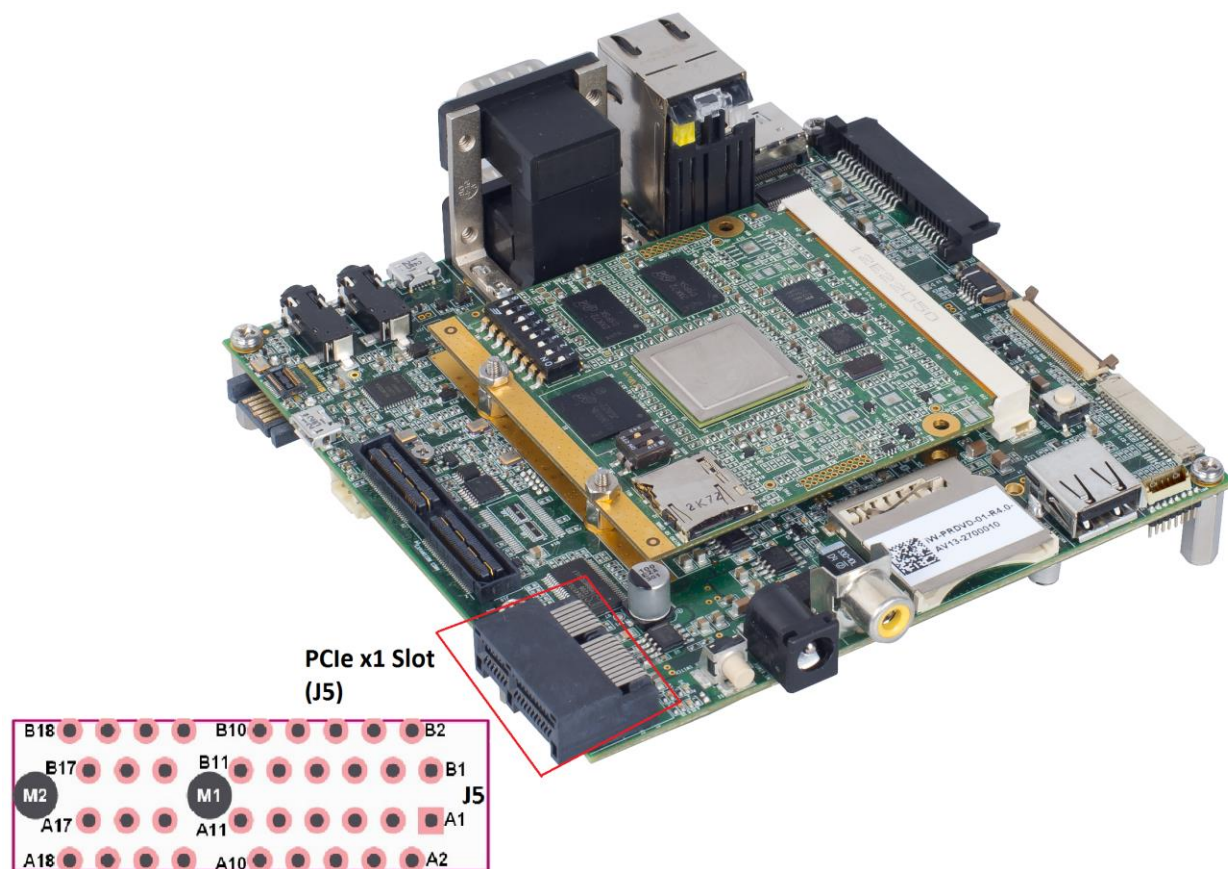
Figure 13: PCIe x1 Connector

Table 14: PCIe x1 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
A1	PRSNT1#	NC	NC	No Connection.
A2	+12V	Power	12V	12V Power Supply.
A3	+12V	Power	12V	12V Power Supply.
A4	GND6	Power	0V	Ground.
A5	TCK	NC	NC	No Connection.
A6	TDI	NC	NC	No Connection.
A7	TDO	NC	NC	No Connection.
A8	TMS	NC	NC	No Connection.
A9	+3.3V	Power	3.3V	3V Power Supply.
A10	+3.3V	Power	3.3V	3V Power Supply.

A11	PERST#	Output	3.3V CMOS	PCIe Reset. Connected to 158th Pin of Qseven MXM connector through buffer.
A12	GND7	Power	0V	Ground.
A13	REFCLK+	Output	Differential	PCIe reference clock positive. Connected to 155th Pin of Qseven MXM connector through Clock buffer.
A14	REFCLK-	Output	Differential	PCIe reference clock negative. Connected to 157th Pin of Qseven MXM connector through Clock buffer.
A15	GND8	Power	0V	Ground.
A16	PERp0	Input	Differential	PCIe Receive Pair positive. Connected to 180th Pin of Qseven MXM connector. Optionally connected to PCIe Switch downstream Port2 through resistors and default not populated.
A17	PERn0	Input	Differential	PCIe Receive Pair negative. Connected to 182nd Pin of Qseven MXM connector. Optionally connected to PCIe Switch downstream Port2 through resistors and default not populated.
A18	GND9	Power	0V	Ground.
B1	+12V	Power	12V	12V Power Supply.
B2	+12V	Power	12V	12V Power Supply.
B3	RSVD1	NC	NC	No Connection.
B4	GND1	Power	0V	Ground.
B5	SMCLK	Output	3.3V CMOS	System Management Bus Clock. Connected to 60th Pin of Qseven MXM Connector.
B6	SMDAT	Input/Output	3.3V CMOS	System Management Bus Data. Connected to 62nd Pin of Qseven MXM Connector.
B7	GND2	Power	0V	Ground.

B8	+3.3V	Power	3.3V	3V Power Supply.
B9	TRST#	NC	NC	No Connection.
B10	3V3AUX	Power	3.3V	3V Always Power Supply.
B11	WAKE#	Input	3.3V CMOS	PCIe interface wake up signal. Connected to 156th Pin of Qseven MXM Connector.
B12	RSVD2	NC	NC	No Connection.
B13	GND3	Power	0V	Ground.
B14	PETp0+	Output	Differential	PCIe Transmit Pair positive Connected to 179th Pin of Qseven MXM Connector. Optionally connected to PCIe Switch downstream Port2 through resistors and default not populated.
B15	PETn0	Output	Differential	PCIe Transmit Pair negative. Connected to 181st Pin of Qseven MXM Connector. Optionally connected to PCIe Switch downstream Port2 through resistors and default not populated.
B16	GND4	Power	0V	Ground.
B17	PRSNT2#	NC	NC	No Connection.
B18	GND5	Power	0V	Ground.
M1,M2	Mechanical Support	Mechanical Support	Mechanical Support	Mechanical Support.

2.6.2.2 PCIe Port 2 Header (Optional)

PCIe port 2 signals from the Qseven MXM Connector are connected to an 18 pin SMD pad header (J49) for add-on purpose. These SMD pads can be accessed at the bottom of the board as shown below, by default it is not populated in the design.
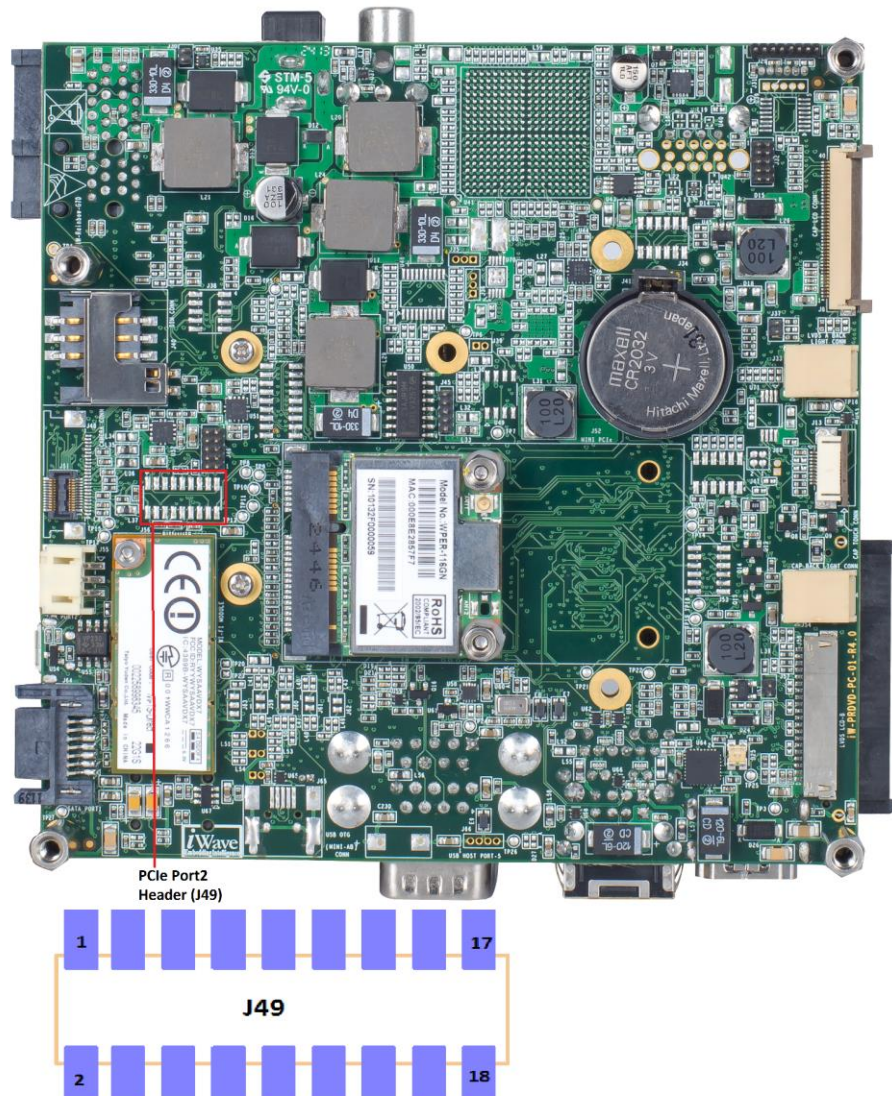
Figure 14: PCIe Port2 Header

Table 15: PCIe Port2 Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VCC_12V	Power	12V	Supply Voltage 12V.
2	VCC_3V3	Power	3.3V	Supply Voltage 3.3V.
3	PCIE2_TX+	Output	Differential	PCIe2 transmit pair positive. Connected to 167th Pin of Qseven MXM Connector.
4	VCC_3V3	Power	3.3V	Supply Voltage 3.3V.
5	PCIE2_TX-	Output	Differential	PCIe2 transmit pair negative. Connected to 169th Pin of Qseven MXM Connector.
6	PCIE2_RX+	Input	Differential	PCIe2 receive pair positive. Connected from 168th Pin of Qseven MXM Connector.
7	GND	Power	0V	Ground.
8	PCIE2_RX-	Input	Differential	PCIe2 differential receive line negative. Connected from 170th Pin of Qseven MXM Connector.
9	PCIE4_CLK-	Output	Differential	PCIe4 reference clock pair negative. Connected to 157th Pin of Qseven MXM connector through Clock buffer.
10	GND	Power	0V	Ground.
11	PCIE4_CLK+	Output	Differential	PCIe4 reference clock pair positive. Connected to 155th Pin of Qseven MXM connector through Clock buffer.
12	PCIE2_RST#	Output	3.3V CMOS	PCIe2 Reset. Connected to 158th Pin of Qseven MXM connector through buffer.
13,14	GND	Power	0V	Ground.
15	PCIECLK_OE4#	Input	3.3V CMOS	PCIe clock request.
16	VCC_3V3	Power	3.3V	Supply Voltage 3.3V.
17	SMB_DAT	Input/ Output	3.3V CMOS	System Management Bus Data. Connected to 62nd Pin of Qseven MXM Connector.
18	SMB_CLK	Input	3.3V CMOS	System Management Bus Clock. Connected to 60th Pin of Qseven MXM Connector.

2.6.2.3 PCIe Port 3 Header (Optional)

PCIe port 3 signals from the Qseven MXM Connector are connected to an 18 pin header (J44) for add-on purpose. These SMD pads can be accessed at the bottom of the board as shown below, by default it is not populated in the design.
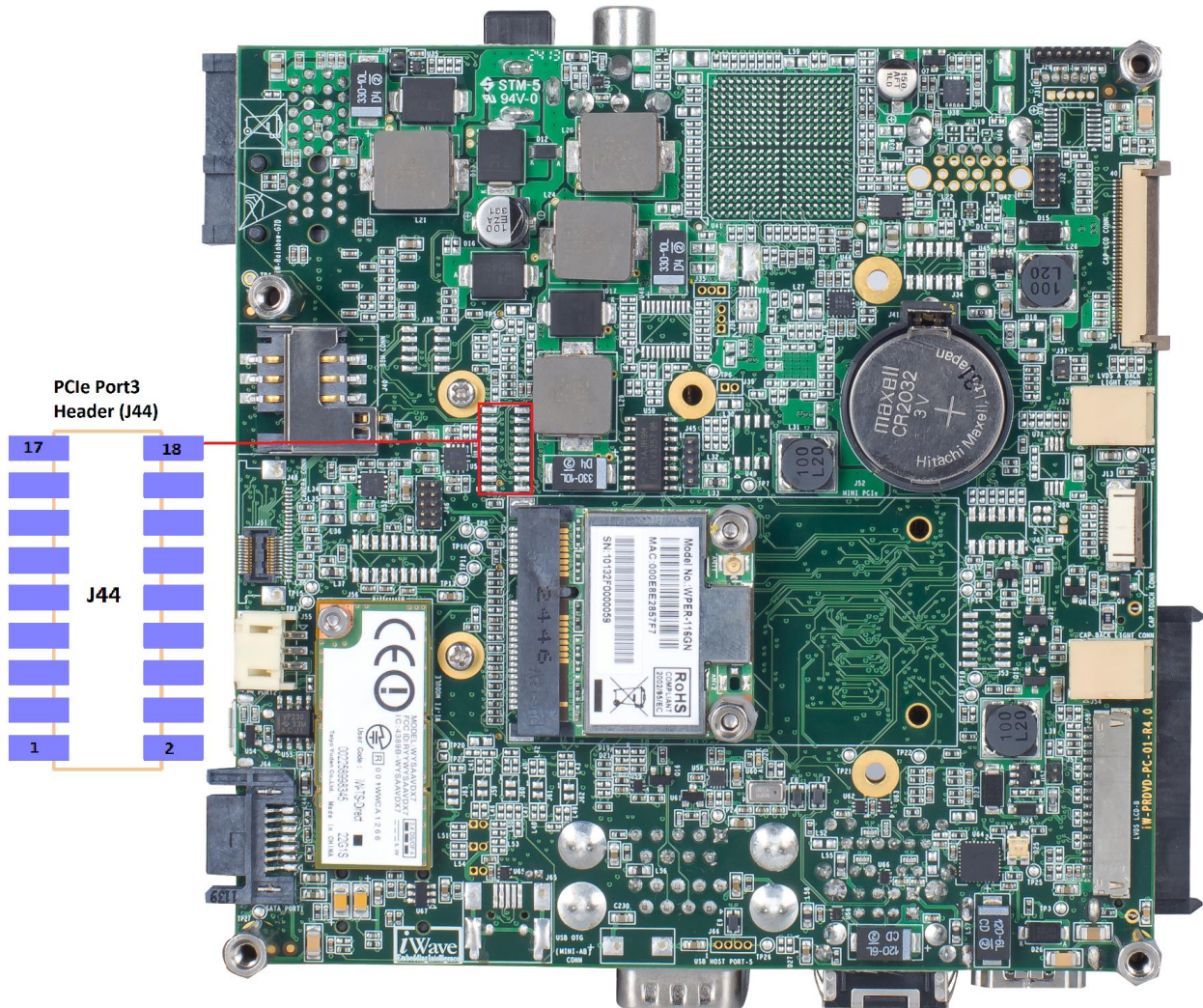
Figure 15: PCIe Port3 Header

Table 16: PCIe Port3 Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VCC_12V	Power	12V	Supply Voltage 12V.
2	VCC_3V3	Power	3.3V	Supply Voltage 3.3V.
3	PCIE3_TX+	Output	Differential	PCIe3 transmit pair positive. Connected to 161st Pin of Qseven MXM Connector.
4	VCC_3V3	Power	3.3V	Supply Voltage 3.3V.
5	PCIE3_TX-	Output	Differential	PCIe3 transmit pair negative. Connected to 163rd Pin of Qseven MXM Connector.
6	PCIE3_RX+	Input	Differential	PCIe3 receive pair positive. Connected from 162nd Pin of Qseven MXM Connector.
7	GND	Power	0V	Ground.
8	PCIE3_RX-	Input	Differential	PCIe3 receive pair negative. Connected from 164th Pin of Qseven MXM Connector.
9	PCIE5_CLK-	Output	Differential	PCIe5 reference clock pair negative. Connected to 157th Pin of Qseven MXM Connector through Clock buffer.
10	GND	Power	0V	Ground.
11	PCIE5_CLK+	Output	Differential	PCIe5 reference clock pair positive. Connected to 155th Pin of Qseven MXM Connector through Clock buffer.
12	PCIE2_RST#	Output	3.3V CMOS	PCIe2 Reset.
13,14	GND	Power	0V	Ground.
15	PCIECLK_OE5#	Input	3.3V CMOS	PCIe clock request.
16	VCC_3V3	Power	3.3V	Supply Voltage 3.3V.
17	SMB_DAT	Input/Output	3.3V CMOS	System Management Bus Data. Connected to 62nd Pin of Qseven MXM Connector.
18	SMB_CLK	Input	3.3V CMOS	System Management Bus Clock. Connected to 60th Pin of Qseven MXM Connector.

2.6.2.4 PCIe Switch

Qseven Generic Carrier Board supports on board 4-Port Gen2.0 PCI Express Switch. This PCIe Switch supports 1 upstream port and 3 downstream ports. The upstream port (PCIe switch Port0) of the PCIe switch is connected to PCIe port0 interface of Qseven MXM connector. The three downstream PCIe ports of the PCIe switch are connected respectively to,

- Mini PCIe Connector
- PCIe to USB 3.0 Hub controller

By default 4-Port PCIe switch and USB 3.0 controller are not populated.

2.6.2.4.1 Mini PCIe Connector

Qseven Generic Carrier Board supports Mini PCIe connector with PCIe interface from PCIe switch downstream port1 and USB Host3 interface from Qseven MXM connector. Since PCIe switch is not populated Mini PCIe connector and SIM slot cannot be used. Mini PCIe connector (J52) and SIM connector (J40) are physically located at bottom of the board as shown below.
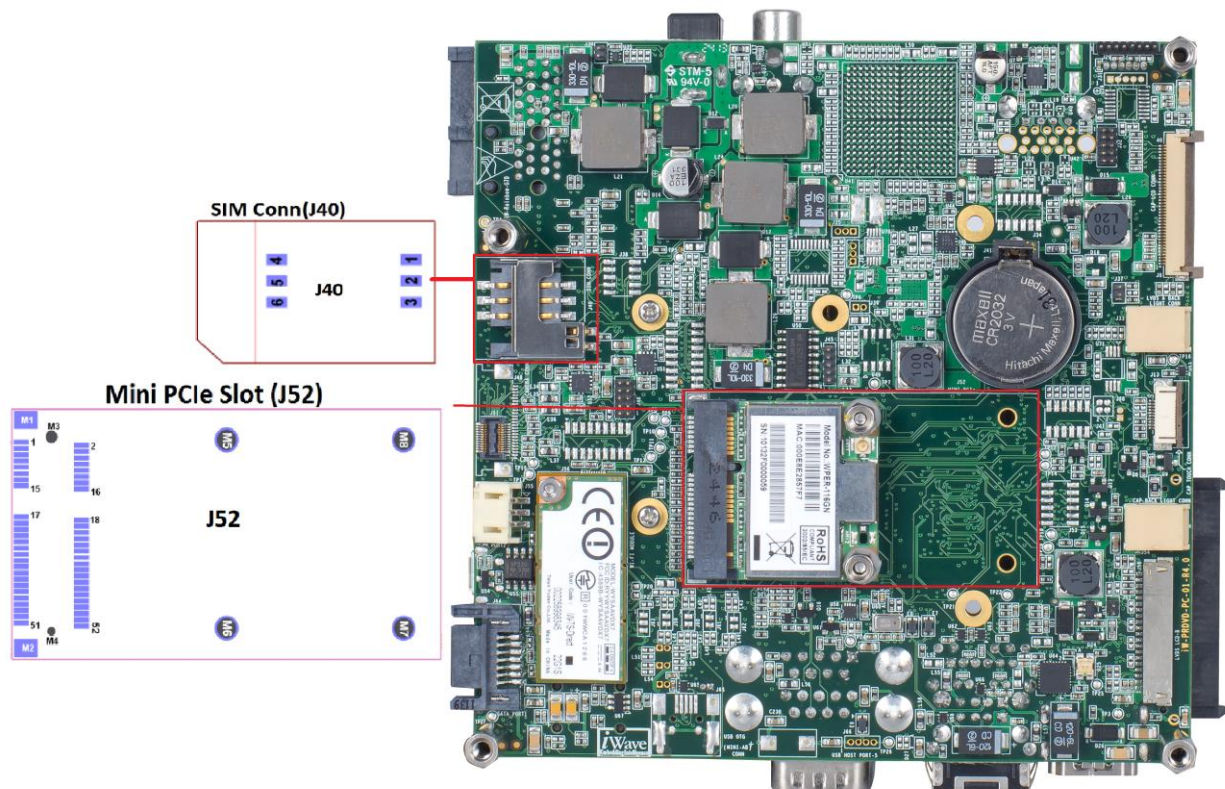
Figure 16: Mini PCIe Connector

Table 17: Mini PCIe Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	WAKE#	Input	3.3V CMOS	PCIe interface Wake Up Signal. Connected to 156th Pin of Qseven MXM Connector.
2	+3.3V_AUX	Power	3.3V	3.3V Power Supply.
3	COEX1	NC	NC	No Connection.
4	GND	Power	0V	Ground.
5	COEX2	NC	NC	No Connection.
6	1.5V	Power	1.5V	Optional 3G supply. Default NC.
7	CLKREQ#	Input	3.3V CMOS	Clock Request
8	UIM_PWR	Power	3V	SIM Supply. Connected to 1st pin of SIM connector (J40).
9	GND1	Power	0V	Ground.
10	UIM_DATA	Input/Output	3V	SIM Data. Connected to 6th pin of SIM connector (J40).
11	REFCLK-	Output	Differential	PCIe1 reference clock negative. Connected to 157th Pin of Qseven MXM connector through Clock buffer
12	UIM_CLK	Input	3V CMOS	SIM Clock. Connected to 3rd pin of SIM connector (J40).
13	REFCLK+	Output	Differential	PCIe1 reference clock positive. Connected to 155th Pin of Qseven MXM connector through Clock buffer.
14	UIM_RESET	Input	3V CMOS	SIM Reset. Connected to 2nd pin of SIM connector (J40).
15	GND2	Power	0V	Ground.
16	UIM_VPP	NC	NC	No Connection.
17	RSVD(UIM_C8)	NC	NC	No Connection.
18	GND3	Power	0V	Ground.

19	RSVD(UIM_C84	NC	NC	No Connection.
20	W_DISABLE#	Output	3.3V CMOS	Wireless Disable. Connected to 24th Pin of Expansion Connector1.
21	GND4	Power	0V	Ground.
22	PERST#	Output	3.3V CMOS	PCIe1 Reset. Connected to 158th Pin of Qseven MXM connector through buffer.
23	PERn0	Input	Differential	PCIe Receive Pair Negative. Connected to PCIe Switch downstream Port1.
24	+3.3V_AUX	Power	3.3V	3.3V Power Supply.
25	PERp0	Input	Differential	PCIe Receive Pair positive. Connected to PCIe Switch downstream Port1.
26	GND5	Power	0V	Ground.
27	GND6	Power	0V	Ground.
28	1.5V	Power	1.5V	Optional 3G supply. Default NC.
29	GND7	Power	0V	Ground.
30	SMB_CLK	Output	3.3V CMOS	System Management Bus Clock. Connected to 60th Pin of Qseven MXM Connector.
31	PETn0	Output	Differential	PCIe Transmit Pair negative Connected to PCIe Switch downstream Port1.
32	SMB_DATA	Input/Output	3.3V CMOS	System Management Data. Connected to 62nd Pin of Qseven MXM Connector.
33	PETp0	Output	Differential	PCIe Transmit Pair Positive Connected to PCIe Switch downstream Port1.
34	GND8	Power	0V	Ground.
35	GND9	Power	0V	Ground.
36	USB_D-	Input/Output	Differential	USB Host Port3 Data negative. Connected to 87th Pin of in Qseven MXM Connector.
37	GND10	Power	0V	Ground.

38	USB_D+	Input/Output	Differential	USB Host Port3 Data positive. Connected to 89th Pin of Qseven MXM Connector.
39	+3.3V_AUX	Power	3.3V	3.3V Power Supply.
40	GND11	Power	0V	Ground.
41	+3.3V_AUX	Power	3.3V	3.3V Power Supply.
42	LED_WWAN#	Input	3.3V CMOS	LED Enable. Connected to red LED D22 and default populated.
43	GND12	Power	0V	Ground.
44	LED_WLAN#	Input	3.3V CMOS	LED Enable. Connected to red LED D21 and default not populated.
45	RSVD	Input	3.3V CMOS	Default NC. Connected to 45th Pin of Expansion Connector2 through resistor and default not populated.
46	LED_WPAN#	Input	3.3V CMOS	LED Enable. Connected to red LED D19 and default not populated.
47	RSVD1	Input	3.3V CMOS	Default NC. Connected to 44th Pin of Expansion Connector2 through resistor and default not populated
48	1.5V	Power	1.5V	Optional 3G supply. Default NC.
49	RSVD2	Output	3.3V CMOS	Default NC. Connected to 41st Pin of Expansion Connector2 through resistor and default not populated
50	GND13	Power	0V	Ground
51	RSVD3	Input	3.3V CMOS	Default NC. Connected to 43rd Pin of Expansion Connector2 through resistor and default not populated
52	+3.3V_AUX	Power	3.3V	3.3V Power Supply.

38	USB_D+	Input/Output	Differential	USB Host Port3 Data positive. Connected to 89th Pin of Qseven MXM Connector.
39	+3.3V_AUX	Power	3.3V	3.3V Power Supply.
40	GND11	Power	0V	Ground.
41	+3.3V_AUX	Power	3.3V	3.3V Power Supply.
42	LED_WWAN#	Input	3.3V CMOS	LED Enable. Connected to red LED D22 and default populated.
43	GND12	Power	0V	Ground.
44	LED_WLAN#	Input	3.3V CMOS	LED Enable. Connected to red LED D21 and default not populated.
45	RSVD	Input	3.3V CMOS	Default NC. Connected to 45th Pin of Expansion Connector2 through resistor and default not populated.
46	LED_WPAN#	Input	3.3V CMOS	LED Enable. Connected to red LED D19 and default not populated.
47	RSVD1	Input	3.3V CMOS	Default NC. Connected to 44th Pin of Expansion Connector2 through resistor and default not populated
48	1.5V	Power	1.5V	Optional 3G supply. Default NC.
49	RSVD2	Output	3.3V CMOS	Default NC. Connected to 41st Pin of Expansion Connector2 through resistor and default not populated
50	GND13	Power	0V	Ground
51	RSVD3	Input	3.3V CMOS	Default NC. Connected to 43rd Pin of Expansion Connector2 through resistor and default not populated
52	+3.3V_AUX	Power	3.3V	3.3V Power Supply.

Table 18: SIM Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VCC	Power	3V	SIM Power Supply from Mini PCIe.
2	RST	Input	3V CMOS	SIM Reset from Mini PCIe.
3	CLK	Input	3V CMOS	SIM Clock from Mini PCIe.
4	GND	Power	0V	Ground.
5	VPP	Power	3V	SIM VPP Power from Mini PCIe.
6	IO	Input	3V	SIM IO Data from Mini PCIe.

2.6.2.4.2   PCIe to USB 3.0 Controller

Qseven Generic Carrier Board supports on board PCIe to USB 3.0 controller to support USB 3.0 Host port. PCIe switch downstream port3 signals are connected to USB 3.0 controller. By default 4-Port PCIe switch and USB 3.0 controller are not populated and USB 3.0 dual stack connector is not populated and instead a single Type A USB 2.0 port is populated in the design, refer **Figure** 9 to identify the location of the connector.

2.7   Audio/ Video Features

2.7.1 Audio In/Out

Four wire AC'97 signals from the Qseven MXM Connector are connected to AC'97 Audio Codec. The Audio CODEC used on the Qseven Generic Carrier Board is ALC5610 from Realtek with inbuilt Headphone amplifier & MIC which is used to provide a complete audio solution for portable products. Qseven Generic Carrier Board supports 3.5mm Audio out Stereo Jack (J24) and 3.5mm Audio In Mono Jack (J23) which are physically located on top of the board as shown below.
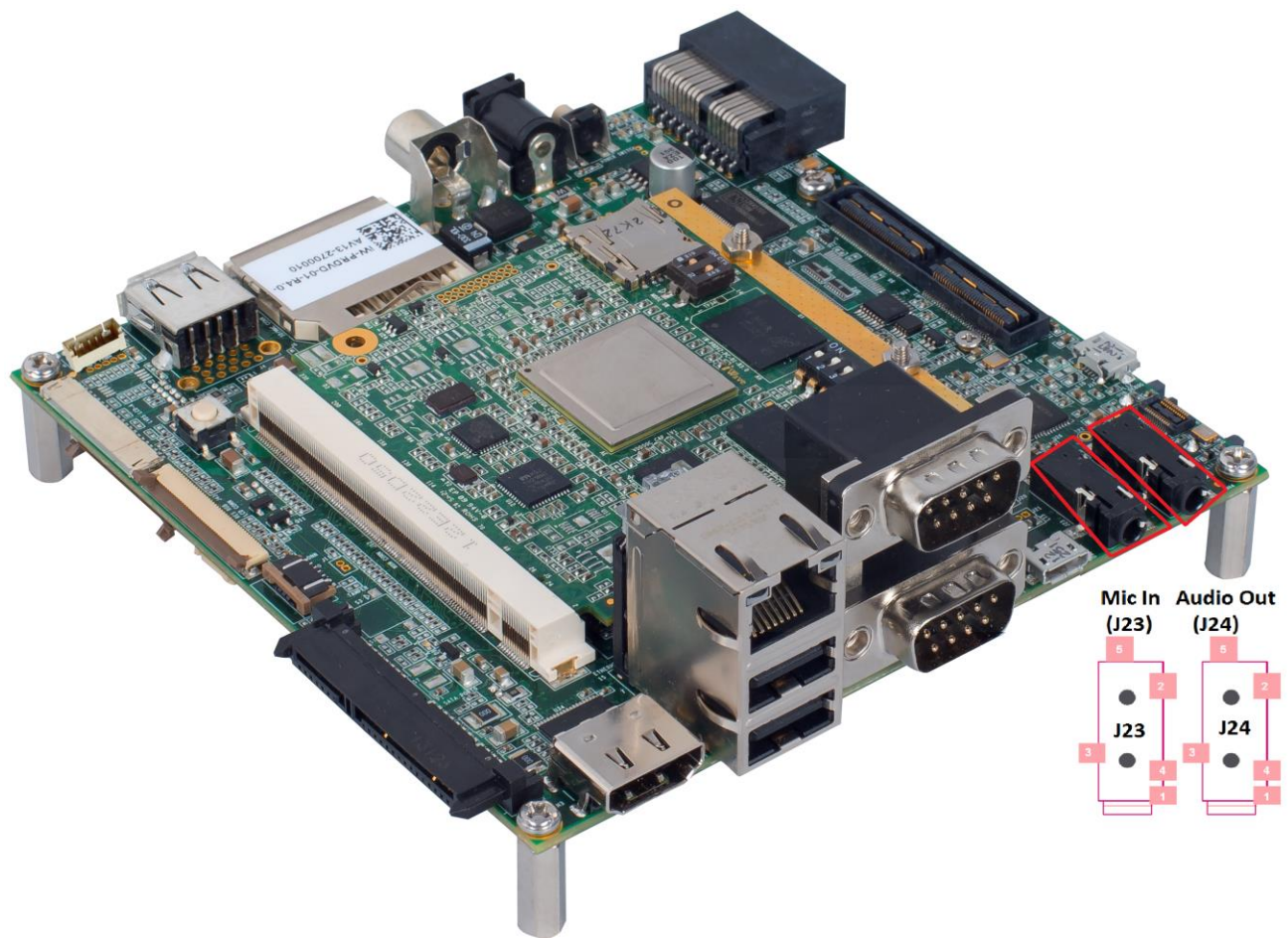
Figure 17: Audio Jack

Table 19: Audio OUT Jack Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground.
2	HP_L	Output	3.3V Analog	Headphone Left.
3	HP_R	Output	3.3V Analog	Headphone Right.
4	HP_DETECT	Output	3.3V Analog	Head Phone Detection. Connected from 38th Pin of Expansion Connector1.
5	NC	NC	NC	No Connection.

Table 20: Audio IN Jack Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground
2	MIC1P	Input	3.3V Analog	Microphone Signal
3	NC	NC	NC	No Connection
4	MIC_IN_DETECT	Input	3.3V CMOS	Microphone Detection. Connected from 31st Pin of Expansion Connector1.
5	MIC_INT	Input	3.3V CMOS	Internal MIC connection.

2.7.2 LVDS Display Interface

The Qseven Generic Carrier Board supports different displays through LVDS0 & LVDS1 interface from Qseven MXM connector. LVDS0 interface from Qseven MXM connector is connected to LVDS0 LCD connector and also on-board LVDS transmitter. This LVDS transmitter converts LVDS0 interface signals to RGB and connects to 7" RGB Resistive touch LCD or 7" RGB Capacitive touch LCD.LVDS1 interface from Qseven MXM connector is connected to LVDS1 LCD connector.

Note: Either LVDS0 connector or 7" RGB resistive touch LCD or 7" RGB capacitive touch LCD only can be used at a time

2.7.2.1 LVDS0 Connector

Qseven Generic Carrier Board supports LVDS0 connector to connect different LVDS LCDs. It also supports backlight connector with 15V 300mA output for LCD backlight. LVDS0 connector (J7) is physically located on top of the board & Backlight connector (J33) at the bottom of the board as shown below.

LVDS0 LCD Connector:
Number of Pins: 20
LVDS LCD Connector Part number: DF19G-20P-1H(54)

Backlight Connector:
Number of Pins: 2
Backlight Connector Part Number: SM02B-BHSS-1-TB
Mating Connector: SM02B-BHSS-1-TB from JST Sales America Inc

Compatible LCDs
1. Part Number: OSD104T0571-19TS
   Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution
   Manufacturer Name: OSD Displays

2. Part Number: T-51944D104J-FW-A-ABN
   Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution
   Manufacturer Name: OPTREX Corporation

3. Part Number: TLM-TA40T3130-01
   Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution
   Manufacturer Name: Varitronix
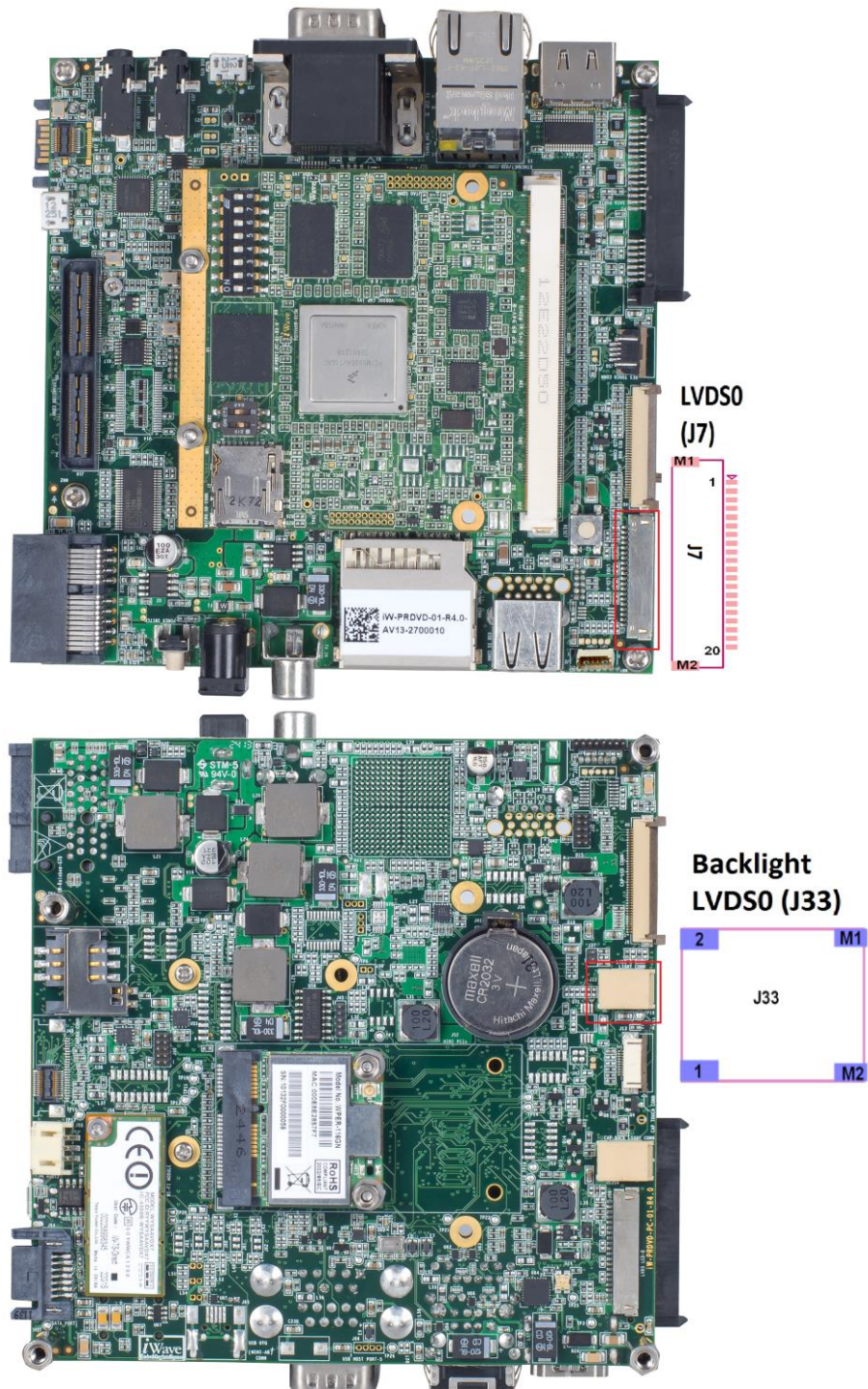
Figure 18: LVDS0 Connector

Table 21: LVDS0 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VDD1	Power	3.3V	Supply voltage for TFT.
2	VDD2	Power	3.3V	Supply voltage for TFT.
3	GND1	Power	0V	Ground.
4	GND2	Power	0V	Ground.
5	RIN0-	Output	LVDS	LVDS primary channel differential pair0 negative. Connected to 101st Pin of Qseven MXM Connector.
6	RIN0+	Output	LVDS	LVDS primary channel differential pair0 positive. Connected to 99th Pin of Qseven MXM Connector.
7	GND3	Power	0V	Ground.
8	RIN1-	Output	LVDS	LVDS primary channel differential pair1 negative. Connected to 105th Pin of Qseven MXM Connector.
9	RIN1+	Output	LVDS	LVDS primary channel differential pair1 positive. Connected to 103rd Pin of Qseven MXM Connector.
10	GND4	Power	0V	Ground.
11	RIN2-	Output	LVDS	LVDS primary channel differential pair2 negative. Connected to 109th Pin of Qseven MXM Connector.
12	RIN2+	Output	LVDS	LVDS primary channel differential pair2 positive. Connected to 107th Pin of Qseven MXM Connector.
13	GND5	Power	0V	Ground.

14	CLKIN-	Output	LVDS	LVDS primary channel differential clock negative. Connected to 121st Pin of Qseven MXM Connector.
15	CLKIN+	Output	LVDS	LVDS primary channel differential clock positive. Connected to 119th Pin of Qseven MXM Connector.
16	GND6	Power	0V	Ground.
17	RIN3-	Output	LVDS	LVDS primary channel differential pair3 negative. Connected to 115th Pin of Qseven MXM Connector.
18	RIN3+	Output	LVDS	LVDS primary channel differential pair3 positive. Connected to 113th Pin of Qseven MXM Connector.
19	GND7	Power	0V	Ground.
20	GND8	Power	0V	Ground.

Table 22: LVDS0 Backlight Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	LED_A0	Power	15V	LED Anode.
2	LED_K0	Power	0V	LED Cathode.

Note: To change the LVDS0 Backlight LED driver setting,
   1. *Change Current sensing resistor **R24 (R_{SET})** by calculating using the below formula*

$$\frac{V_{FB}}{R_{SET}} = I_{LED}$$

Where V_{FB} = 190mV, I_{LED} = Current required for LCD backlight LEDs.

   2. *Change **D14** Zener Diode from 15V to required voltage.*
      (Populated diode part number is BZT52C20-7-F)

*Note: Refer **APPENDIX I** for Silkscreen identifier details*

2.7.2.2 7" RGB Resistive Touch LCD (optional)

The Qseven Generic Carrier Board supports 7'' RGB LCD with resistive touch interface. LVDS0 interface from Qseven MXM connector is connected to LVDS transmitter and output of transmitter is connected to 7" RGB Resistive Touch LCD connector and 7" RGB Capacitive Touch LCD connector. Either one can be used at a time.7" RGB Resistive touch LCD supports 800x480 resolution with 18BPP depth. 7" RGB Resistive LCD connector (J43) and touch connector (J50) are physically located at the bottom of board as shown below.

LCD Connector:
Number of Pins: 40
LCD Connector Part number: FH12A-40S-0.5SH(55)

Touch Panel Connector:
Number of Pins: 4
Touch Connector Part number: SFW4R-3STE1LF

Compatible LCD:
Part Number: KWH070KQ13-F02
Description: 7 inch, LCD 18 bit with 800 x 480 (RGB) resolution
Manufacturer Name: Formike Electronic Co.Ltd
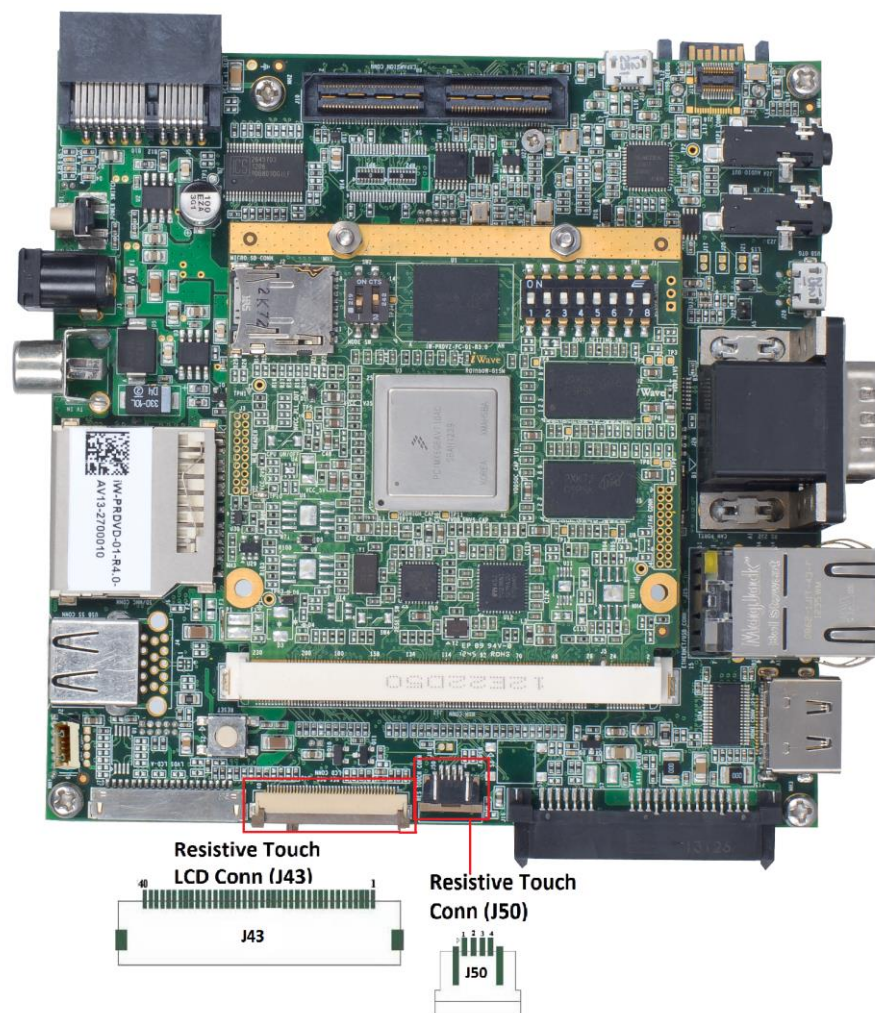
Figure 19: 7`` Resistive LCD Connector

Table 23: 7`` RGB Resistive LCD Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VLED1	Power	5V	Power Voltage for LED Driver.
2	VLED2	Power	5V	Power Voltage for LED Driver.
3	ADJ	Output	3.3V CMOS	LVDS Panel backlight brightness control. Connected to 123rd Pin of Qseven MXM Connector.
4	GLED1	Power	0V	Ground.

5	GLED2	Power	0V	Ground.
6	VCC1	Power	3.3V	Supply voltage for TFT.
7	VCC2	Power	3.3V	Supply voltage for TFT.
8	MODE	Output	3.3V CMOS	DE or HV mode control.
9	DE	Output	3.3V CMOS	Display Enable.
10	VS	Output	3.3V CMOS	Display VSYNC signal input.
11	HS	Output	3.3V CMOS	Display HSYNC signal input.
12	GND1	Power	0V	Ground.
13	B5	Output	3.3V CMOS	Display Blue Data 7 (MSB).
14	B4	Output	3.3V CMOS	Display Blue Data 6.
15	B3	Output	3.3V CMOS	Display Blue Data 5.
16	GND2	Power	0V	Ground.
17	B2	Output	3.3V CMOS	Display Blue Data 4.
18	B1	Output	3.3V CMOS	Display Blue Data 3.
19	B0	Output	3.3V CMOS	Display Blue Data 2 (LSB+2).
20	GND3	Power	0V	Ground.
21	G5	Output	3.3V CMOS	Display Green Data 7 (MSB).
22	G4	Output	3.3V CMOS	Display Green Data 6.
23	G3	Output	3.3V CMOS	Display Green Data 5.
24	GND4	Power	0V	Ground.
25	G2	Output	3.3V CMOS	Display Green Data 4.
26	G1	Output	3.3V CMOS	Display Green Data 3.
27	G0	Output	3.3V CMOS	Display Green Data 2 (LSB+2).
28	GND5	Power	0V	Ground.
29	R5	Input	3.3V CMOS	Display Red Data 7 (MSB).
30	R4	Input	3.3V CMOS	Display Red Data 6.
31	R3	Input	3.3V CMOS	Display Red Data 5.
32	GND6	Power	0V	Ground.
33	R2	Output	3.3V CMOS	Display Red Data 4.
34	R1	Output	3.3V CMOS	Display Red Data 3.
35	R0	Output	3.3V CMOS	Display Red Data 2 (LSB+2).
36	GND7	Power	0V	Ground.
37	DCLK	Output	3.3V CMOS	Display Clock.
38	GND8	Power	0V	Ground.
39	L/R	Output	3.3V CMOS	Left or Right Scanning Direction.
40	U/D	Output	3.3V CMOS	Up or Down Scanning Direction.

Qseven Generic Carrier Board supports on board Resistive Touch Controller MAX11801ETC+ (from Maxim Integrated) to support touch interface. This touch controller is connected to I2C interface of Qseven MXM connector (66th and 68th Pin).

Table 24: Resistive Touch Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	Y1	Input	Analog	Touch Left Signals.
2	X2	Input	Analog	Touch Up Signals.
3	Y2	Input	Analog	Touch Right Signals.
4	X1	Input	Analog	Touch Down Signals.

Note: *Optionally these touch signals are directly connected to Expansion Connector-2 (J9) through resistor and default not populated*.

2.7.2.3 Capacitive Touch LCD Interface

The Qseven Generic Carrier Board also supports 7'' RGB LCD with capacitive touch interface. LVDS0 interface from Qseven MXM connector is connected to LVDS transmitter and output of transmitter is connected to 7" RGB Resistive Touch LCD and 7" RGB Capacitive Touch LCD. Either one can be used at a time.7" RGB capacitive LCD (J8) and touch connector (J13) are physically located on bottom of board. The backlight connector (J54) with voltage 10V 160mA is physically located at the bottom of the board as shown below.

LCD Connector:

Number of Pins: 40
LCD Connector Part number: FH12A-40S-0.5SH(55)

Backlight Connector:

Number of Pins: 2
Backlight Connector Part Number: SM02B-BHSS-1-TB(LF)(SN)
Mating Connector: BHSR-02VS-1 from JST Sales America Inc

Touch Panel Connector:

Number of Pins: 10
Touch Connector Part number: 52746-1071

Compatible LCD:

Part Number: ETM070001ADH6

Description: 7 inch, LCD 18 bit with 800 x 480 (RGB) resolution
Manufacturer Name: Emerging Display Technologies Corporation
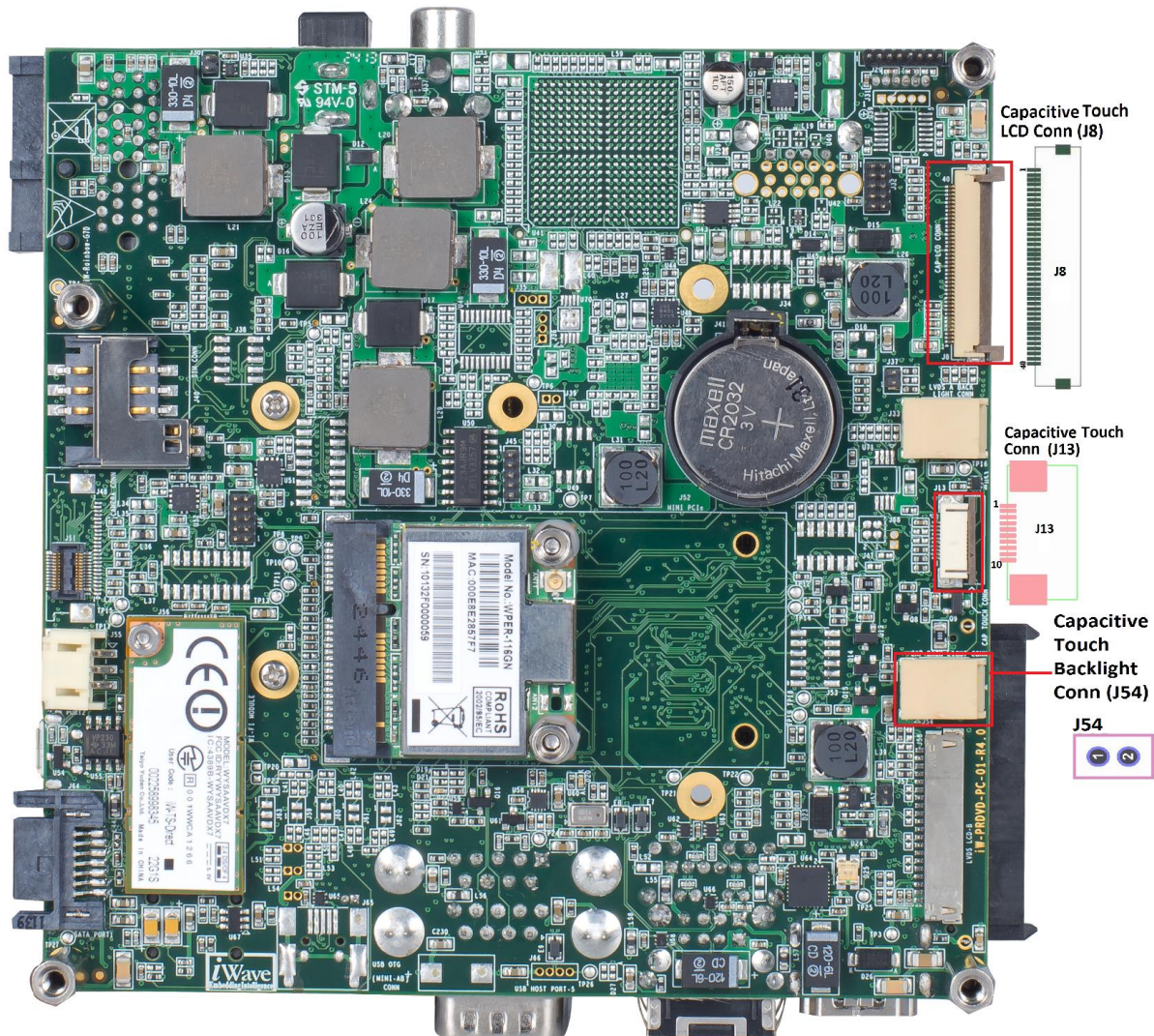
Figure 20: 7`` Capacitive Touch LCD Connector

Table 25: 7`` Capacitive Touch LCD Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	U/D	Output	3.3V CMOS	Up or Down Scanning Direction.
2	R/L	Output	3.3V CMOS	Left or Right Scanning Direction.
3	NC1	NC	NC	No Connection.
4	VCC1	Power	3.3V	Supply voltage for TFT.
5	VCC2	Power	3.3V	Supply voltage for TFT.
6	VCC3	Power	3.3V	Supply voltage for TFT.
7	VCC4	Power	3.3V	Supply voltage for TFT.
8	NC2	NC	NC	No Connection.
9	DE	Output	3.3V CMOS	Display Enable.
10	VSS1	Power	0V	Ground.
11	VSS2	Power	0V	Ground.
12	VSS3	Power	0V	Ground.
13	B5	Output	3.3V CMOS	Display Blue Data Input 7.
14	B4	Output	3.3V CMOS	Display Blue Data Input 6.
15	B3	Output	3.3V CMOS	Display Blue Data Input 5.
16	VSS4	Power	0V	Ground.
17	B2	Output	3.3V CMOS	Display Blue Data Input 4.
18	B1	Output	3.3V CMOS	Display Blue Data Input 3.
19	B0	Output	3.3V CMOS	Display Blue Data Input 2.
20	VSS5	Power	0V	Ground.
21	G5	Output	3.3V CMOS	Display Green Data Input 7.
22	G4	Output	3.3V CMOS	Display Green Data Input 6.
23	G3	Output	3.3V CMOS	Display Green Data Input 5.
24	VSS6	Power	0V	Ground.
25	G2	Output	3.3V CMOS	Display Green Data Input 4.
26	G1	Output	3.3V CMOS	Display Green Data Input 3.
27	G0	Output	3.3V CMOS	Display Green Data Input 2.
28	VSS7	Power	0V	Ground.
29	R5	Output	3.3V CMOS	Display Red Data Input 7.
30	R4	Output	3.3V CMOS	Display Red Data Input 6.
31	R3	Output	3.3V CMOS	Display Red Data Input 5.
32	VSS8	Power	0V	Ground.
33	R2	Output	3.3V CMOS	Display Red Data Input 4.
34	R1	Output	3.3V CMOS	Display Red Data Input 3.

35	R0	Output	3.3V CMOS	Display Red Data Input 2.
36	VSS9	Power	0V	Ground.
37	NC3	NC	NC	No Connection.
38	DCLK	Output	3.3V CMOS	Display Clock.
39	HSYNC	Output	3.3V CMOS	Display HSYNC signal input.
40	VSYNC	Output	3.3V CMOS	Display VSYNC signal input.

Table 26: Capacitive touch Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VSS1	Power	0V	Ground.
2	VDD	Power	3.3V	Supply voltage for TFT.
3	SCL	Output	3.3V CMOS	I2C Clock. Connected to 66th Pin of Qseven MXM Connector.
4	NC1	NC	NC	No Connection.
5	SDA	Input/Output	3.3V CMOS	I2C Data. Connected to 68th Pin of Qseven MXM Connector.
6	NC2	NC	NC	No Connection.
7	RST#	Input	3.3V CMOS	Reset.
8	WAKE#	Output	3.3V CMOS	Wake Interrupt. Connected to 17th Pin of Qseven MXM Connector.
9	INT#	Input	3.3V CMOS	Touch Interrupt. Connected to 41st Pin of Expansion Connector1.
10	VSS1	Power	0V	Ground.

Table 27: Backlight LED Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VBL+(A)	Power	9.9V	LED Anode.
2	VBL-(K)	Power	0V	LED Cathode.

2.7.2.4 LVDS1 Connector

Qseven Generic Carrier Board supports LVDS1 connector to connect different LVDS LCDs. It also supports backlight connector with 15V 300mA output for LCD backlight. LVDS1 connector (J58) and backlight connector (J57) are physically located at the bottom of the board as shown below.

LVDS1 LCD Connector:

Number of Pins: 20

LVDS LCD Connector Part number: DF19G-20P-1H(54)

Backlight Connector:

Number of Pins: 2

Backlight Connector Part Number: GRPB021VWVN-RC

Mating Connector: LPPB021NFFN-RC from Sullins Connector Solutions

Compatible LCDs

1. Part Number: OSD104T0571-19TS

   Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution

   Manufacturer Name: OSD Displays

2. Part Number: T-51944D104J-FW-A-ABN

   Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution

   Manufacturer Name: OPTREX Corporation

3. Part Number: TLM-TA40T3130-01

   Description: 10.4 inch LVDS 6 bits with 800 x 600 (RGB) resolution

   Manufacturer Name: Varitronix
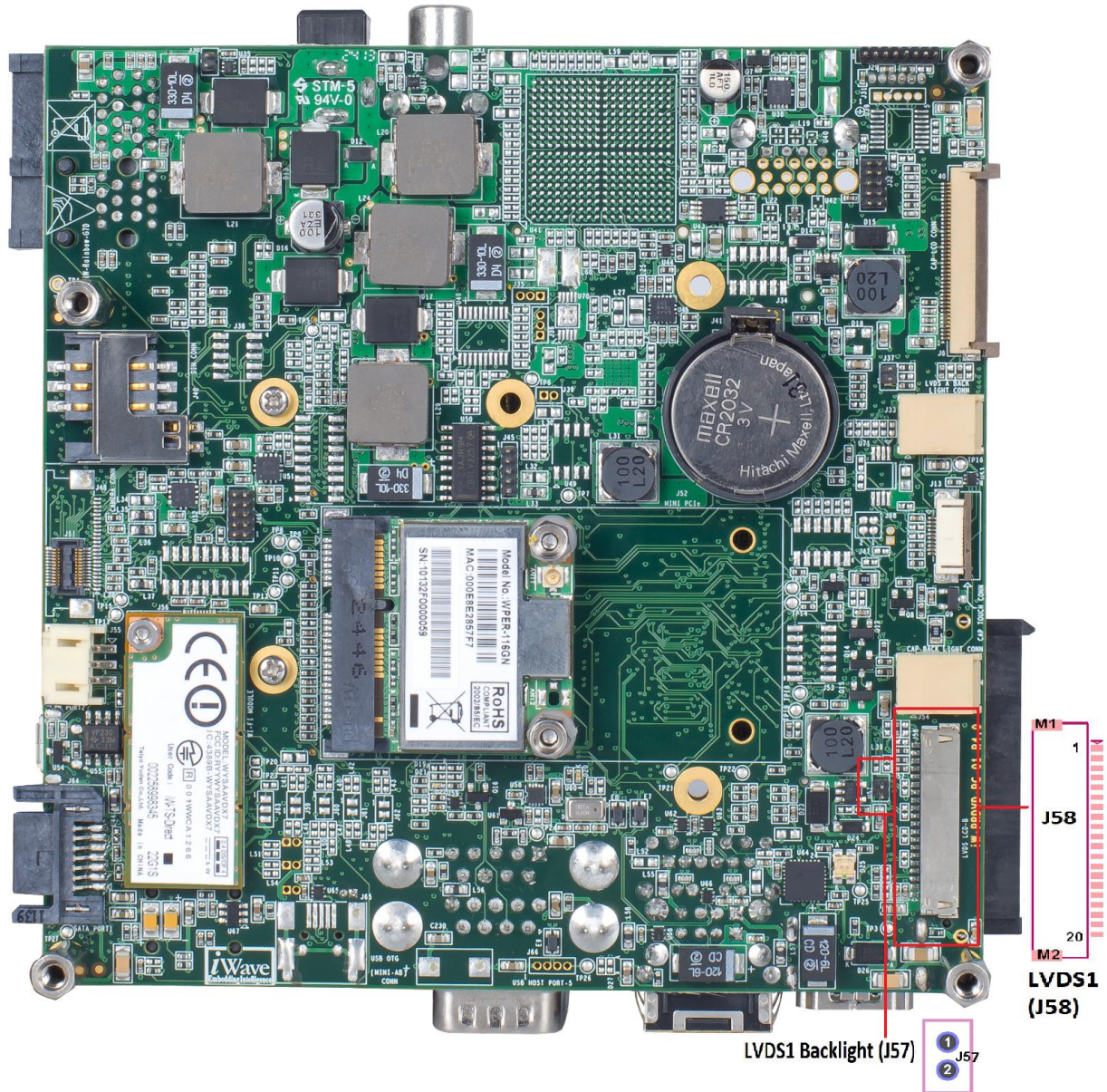
Figure 21: LVDS1 Connectors

Table 28: LVDS1 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VDD1	Power	3.3V	Supply voltage for TFT.
2	VDD2	Power	3.3V	Supply voltage for TFT.
3	GND1	Power	0V	Ground.
4	GND2	Power	0V	Ground.
5	RIN0-	Input	LVDS	LVDS secondary channel differential pair0 negative. Connected to 102nd Pin of Qseven MXM Connector.
6	RIN0+	Input	LVDS	LVDS secondary channel differential pair0 positive. Connected to 100th Pin of Qseven MXM Connector.
7	GND3	Power	0V	Ground.
8	RIN1-	Input	LVDS	LVDS secondary channel differential pair1 negative. Connected to 106th Pin of Qseven MXM Connector.
9	RIN1+	Input	LVDS	LVDS secondary channel differential pair1 positive. Connected to 104th Pin of Qseven MXM Connector.
10	GND4	Power	0V	Ground.
11	RIN2-	Input	LVDS	LVDS secondary channel differential pair2 negative. Connected to 110th Pin of Qseven MXM Connector.
12	RIN2+	Input	LVDS	LVDS secondary channel differential pair2 positive. Connected to 108th Pin of Qseven MXM Connector.
13	GND5	Power	0V	Ground.

14	CLKIN-	Input	LVDS	LVDS secondary channel differential clock negative. Connected to 122nd Pin of Qseven MXM Connector.
15	CLKIN+	Input	LVDS	LVDS secondary channel differential clock positive. Connected to 120th Pin of Qseven MXM Connector.
16	GND6	Power	0V	Ground
17	RIN3-	Input	LVDS	LVDS secondary channel differential pair3 negative. Connected to 116th Pin of Qseven MXM Connector.
18	RIN3+	Input	LVDS	LVDS secondary channel differential pair3 positive. Connected to 114th Pin of Qseven MXM Connector.
19	GND7	Power	0V	Ground.
20	GND8	Power	0V	Ground.

Table 29: LVDS1 Backlight Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	LED_A1	Power	15V	LED Anode.
2	LED_K1	Power	0V	LED Cathode.

Note: To change theLVDS1 Backlight LED driver setting,
   1. *Change Current sensing resistor **R361 (R$_{SET}$)** by calculating using the below formula*

$$\frac{V_{FB}}{R_{SET}} = I_{LED}$$

Where V$_{FB}$ = 190mV, I$_{LED}$ = Current required for LCD backlight LEDs.

   2. *Change **D24** Zener Diode from 15V to required voltage.*
      (Populated diode part number is BZT52C20-7-F)

*Note: Refer **APPENDIX I** for Silkscreen identifier details*

2.7.3 HDMI Interface

Qseven Generic Carrier Board supports HDMI port to support bigger monitor. TMDS signals from Qseven MXM connector are connected to Standard HDMI port with ESD protection circuitry. HDMI connector (J27) is physically located on top of the board as shown below.
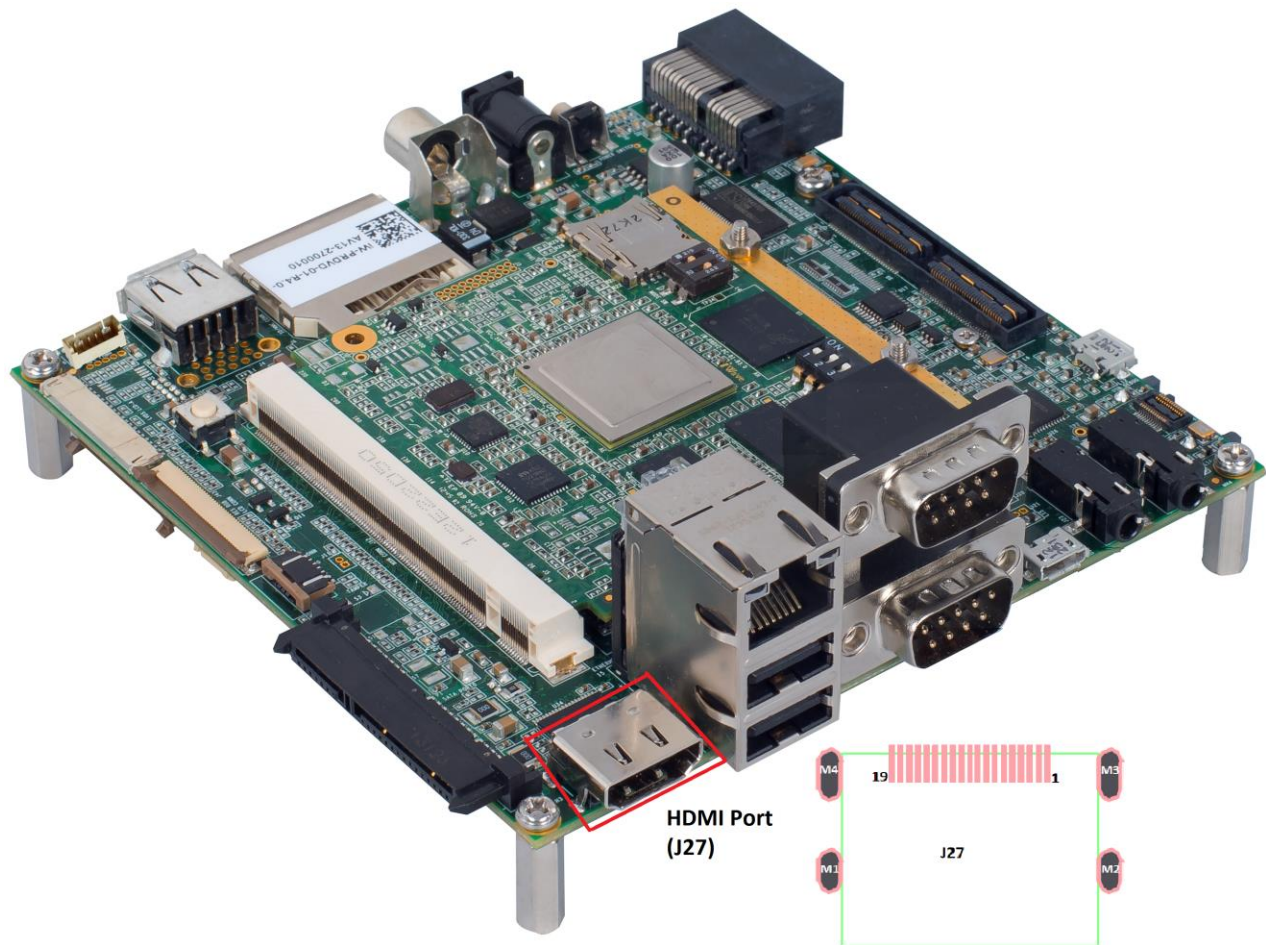
Figure 22: HDMI Port

Table 30: HDMI Port Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	D2+	Output	TMDS	HDMI data2 pair positive. Connected to 149th Pin of Qseven MXM Connector.
2	D2_GND	Power	0V	Red Pair Ground.
3	D2-	Output	TMDS	HDMI data2 pair negative. Connected to 151th Pin of Qseven MXM Connector.
4	D1+	Output	TMDS	HDMI data1 pair positive. Connected to 137th Pin of Qseven MXM Connector.
5	D1_GND	Power	0V	Green Pair Ground.
6	D1-	Output	TMDS	HDMI data1 pair positive. Connected to 139th Pin of Qseven MXM Connector
7	D0+	Output	TMDS	HDMI data0 pair positive. Connected to 143rd Pin of Qseven MXM Connector.
8	D0_GND	Power	0V	Blue Pair Ground.
9	D0-	Output	TMDS	HDMI data0 pair positive. Connected to 145th Pin of Qseven MXM Connector.
10	CLK+	Output	TMDS	Display Clock pair positive. Connected to 131st Pin of Qseven MXM Connector.
11	CLK_GND	Power	0V	Clock pair Ground.
12	CLK-	Output	TMDS	Display Clock pair negative. Connected to 133rd Pin of Qseven MXM Connector.
13	CEC	Input/Output	3.3V CMOS	Consumer Electronic Control. Connected to 124th Pin of Qseven MXM Connector.
14	RSV/NC	NC	NC	No Connection.

15	SCL	Output	3.3V CMOS	EDID I2C Clock. Connected to 152nd Pin of Qseven MXM Connector.
16	SDA	Input/Output	3.3V CMOS	EDID I2C Data. Connected to 150th Pin of Qseven MXM Connector.
17	DDC/CEC_GND	Power	0V	Ground.
18	+5V	Power	5V	5V Power Supply.
19	HPD	Input	3.3V CMOS	HDMI Cable Hot plug detect. Connected from 153rd Pin of Qseven MXM Connector.
M1,M2, M3,M4	Mechanical support	Mechanical support	Mechanical support	Mechanical support.

2.8   Additional Features

2.8.1 JTAG Connector

Qseven Generic Carrier Board supports 10-pin JTAG connector for debug purpose. Since both UART and JTAG share the same pins of Qseven MXM connector, a jumper option (J37) is provided to select either one. This Jumper is connected to 204th Pin of Qseven MXM connector. If the Jumper is open UART is selected as Debug port and if closed JTAG is selected as Debug port. For further information on these signals refer section "Manufacturing Signals" of Qseven-Spec_2.0. JTAG connector (J32) is physically located at the bottom of the board as shown below.

Number of Pins: 10
Connector Part number: GRPB052VWVN-RC
Mating Connector: LPPB052CFFN-RC from Sullins Connector Solutions
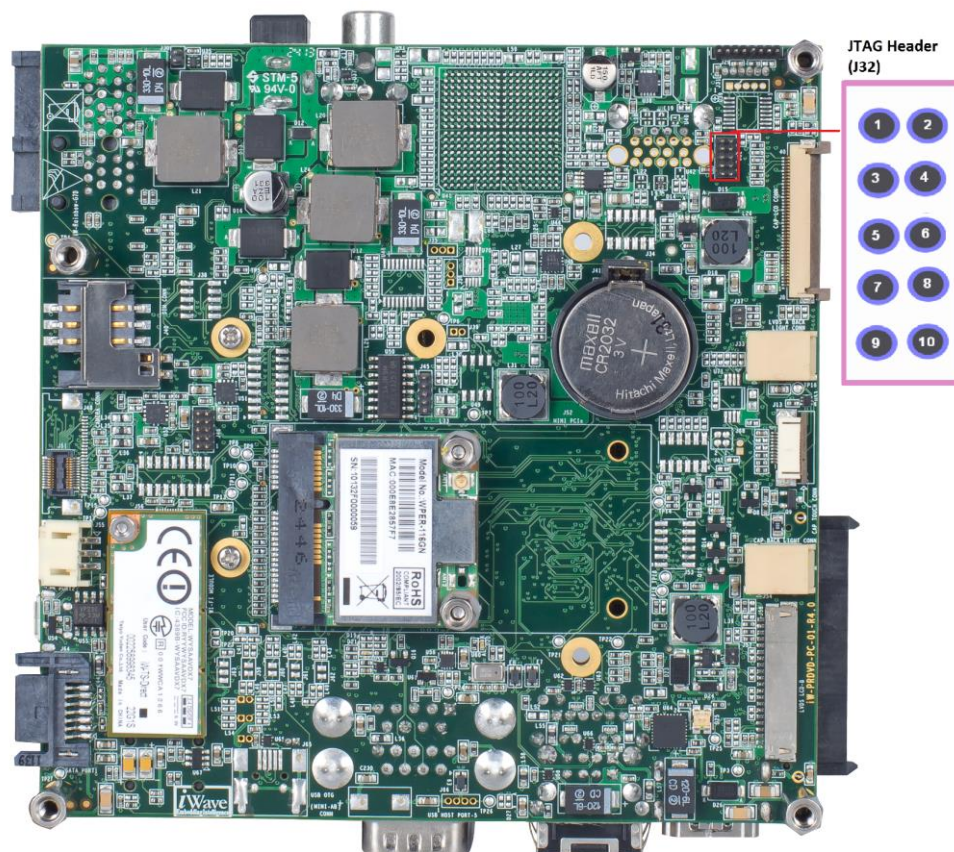
Figure 23: JTAG Connector

Note: To support this dynamic selection, Qseven module which is connected to this Generic carrier board also should support dynamic selection. By default jumper is open and UART is selected as Debug port.

Table 31: JTAG Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	VCC_3V3	Power	3V	Supply Voltage.
2	GND	Power	0V	Ground.
3	VCC_3V3	Power	3V	Supply Voltage.
4	MFG4_JTAG_TRST#	Input	3.3V CMOS	JTAG Reset. Connected from 204th Pin of Qseven MXM Connector.
5	MFG0_JTAG_TCK	Input	3.3V CMOS	JTAG Test Clock. Connected from 207th Pin of Qseven MXM Connector.
6	MFG2_JTAG_TDI	Input	3.3V CMOS	JTAG Test Data Input. Connected from 208th Pin of Qseven MXM Connector.
7	MFG1_JATG_TDO	Output	3.3V CMOS	JTAG Test Data Output. Connected to 209th Pin of Qseven MXM Connector.
8	MFG3_JTAG_TMS	Input	3.3V CMOS	JTAG Test Mode Select. Connected from 210th Pin of Qseven MXM Connector.
9	GND	Power	0V	Ground.
10	GND	Power	0V	Ground.

2.8.2 RTC Battery

The Qseven Generic Carrier Board supports on board RTC battery holder to connect 3V backup coin cell. This coin cell battery is connected to 193rd pin of Qseven MXM connector. This battery holder (J42) is physically located at the bottom of the board as shown below.

Number of Pins: 2
Connector Part number: ML-2020/V1AN
Compatible RTC Battery: CR2032 from Maxell
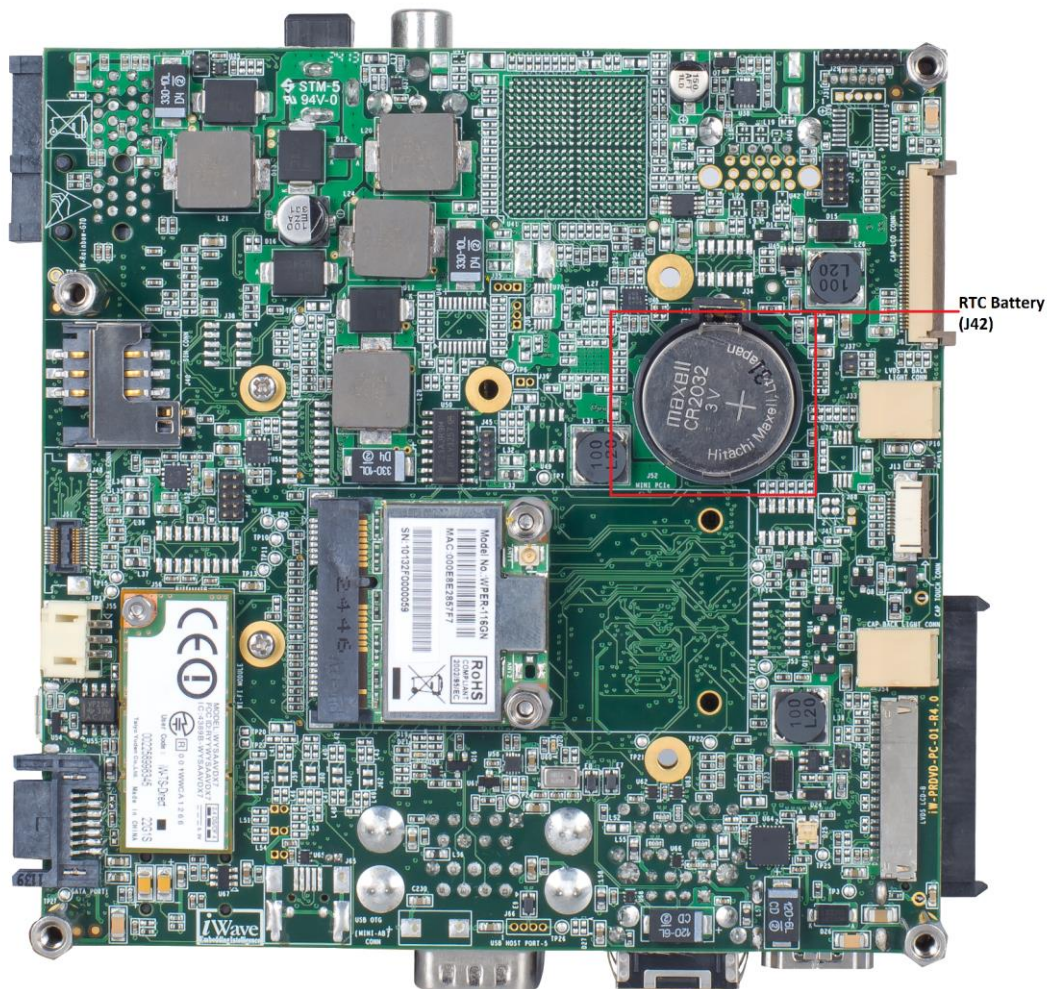
Figure 24: RTC Battery

2.8.3 Control Buttons

2.8.3.1 Power Button

The Qseven Generic Carrier Board supports on board Power push button to power on/off the Qseven SOM module. This power button (S1) is physically located at the top of the board as shown below and connected to 20th Pin of Qseven MXM Connector.
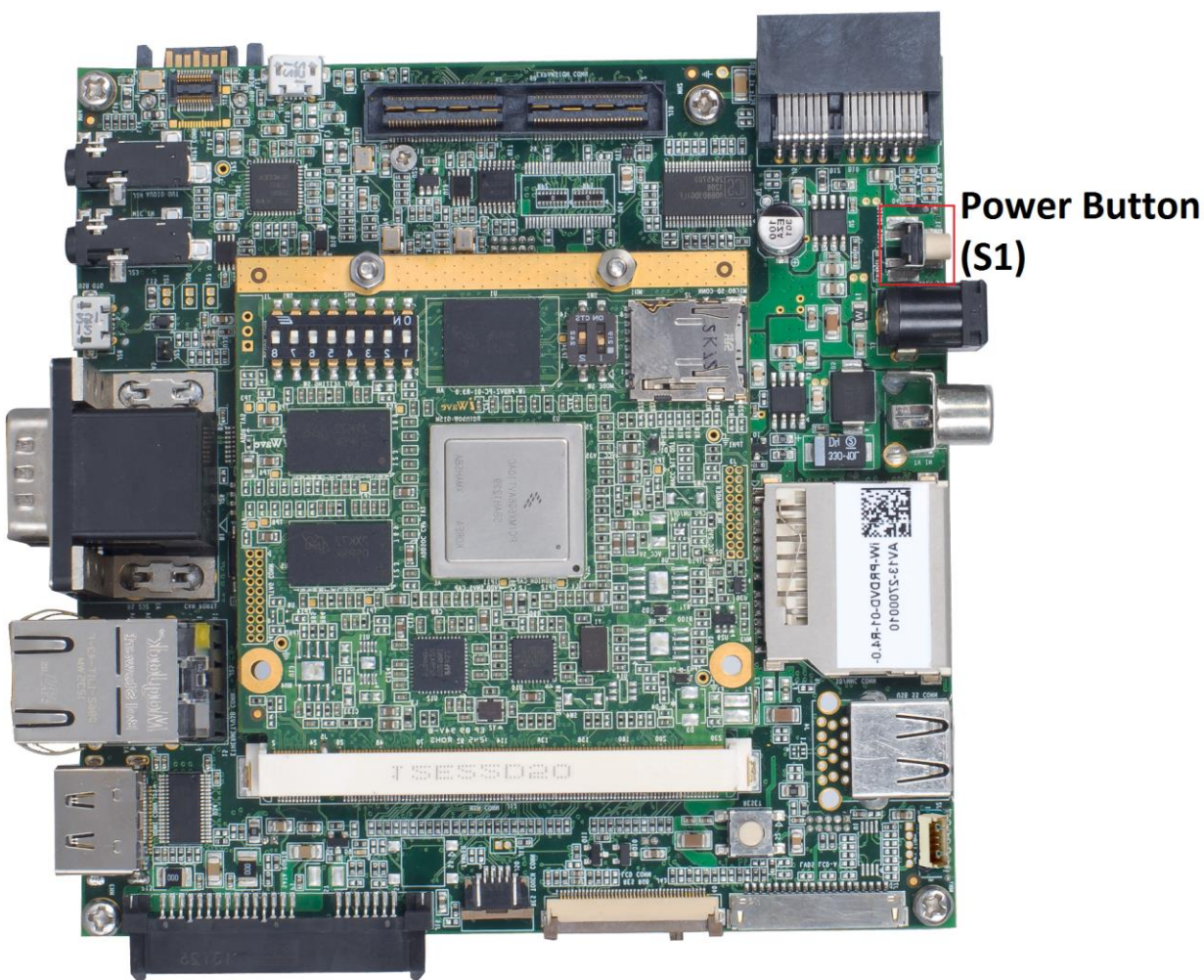
Figure 25: Power Button

2.8.3.2 Reset Button

The Qseven Generic Carrier Board supports on board Reset push button to reset the Qseven SOM module. This reset button (S2) is physically located at the top of the board as shown below and connected to 28th Pin of Qseven MXM Connector.
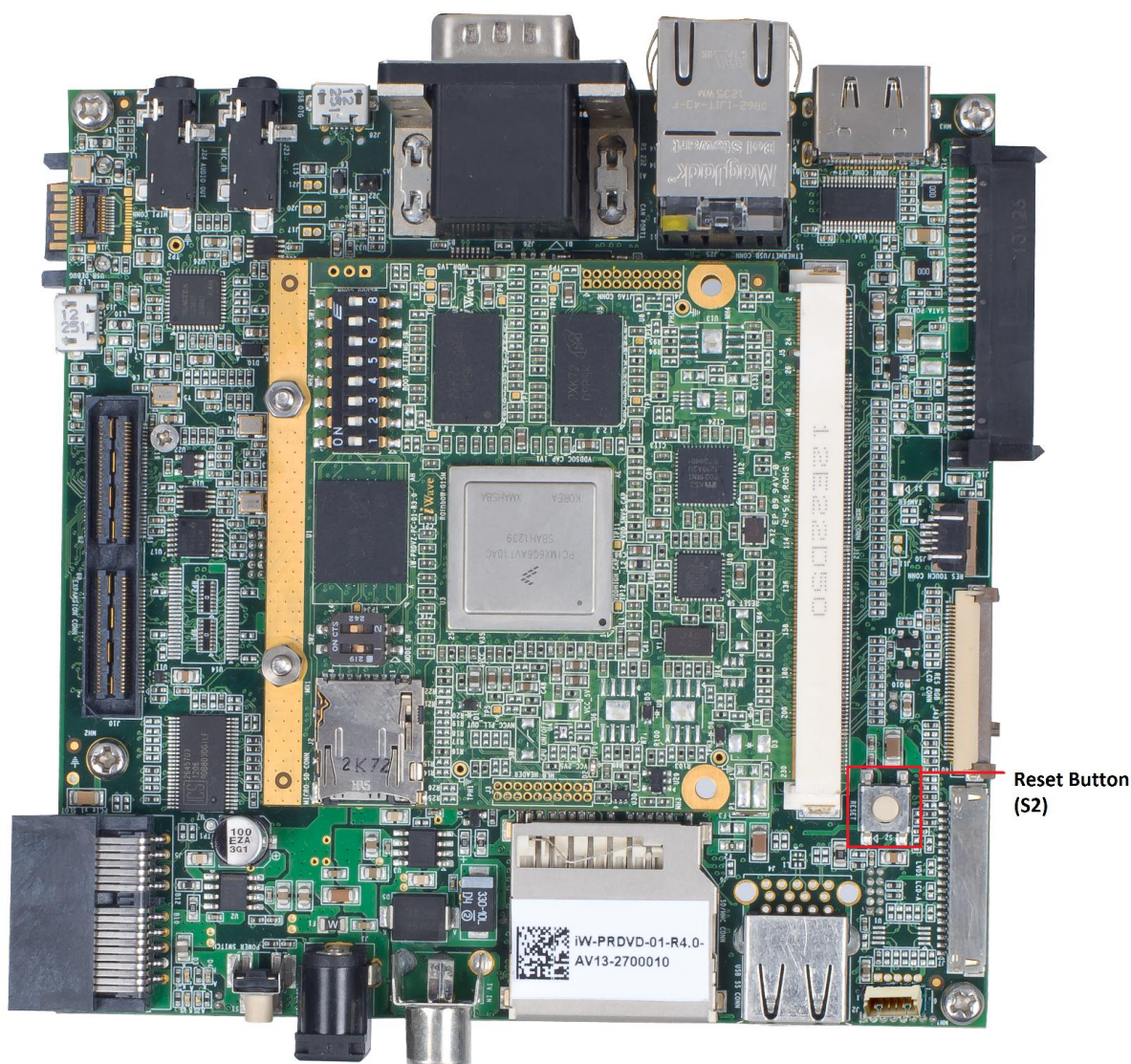
Reset Button (S2)

Figure 26: Reset Button

2.8.3.3 Tamper Switch (Optional)

The Qseven Generic Carrier Board supports on board Tamper Switch (S3). This switch is connected to 154th Pin of Qseven MXM connector through resistor and default not populated. This switch (S3) is physically located on the top of the board as shown below and not populated.
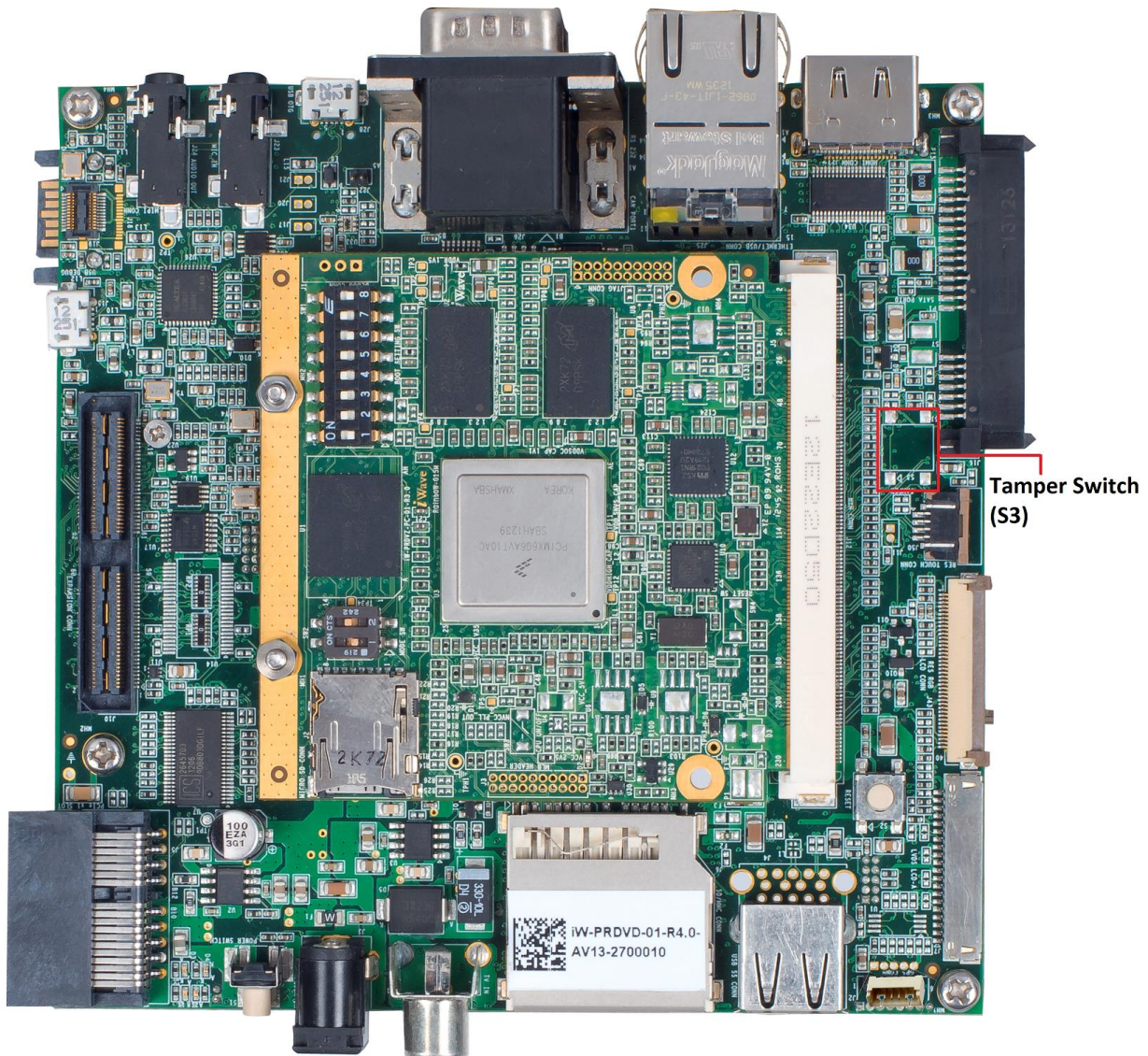
Figure 27: Tamper Switch

Note: This is not the standard feature of Qseven specification.

2.8.4 EEPROM (Optional)

The Qseven Generic Carrier Board supports on board EEPROM, this EEPROM is connected to I2C interface of Qseven MXM Connector (66th and 68th Pin) and it is physically located at the bottom of the board as shown below and not populated.
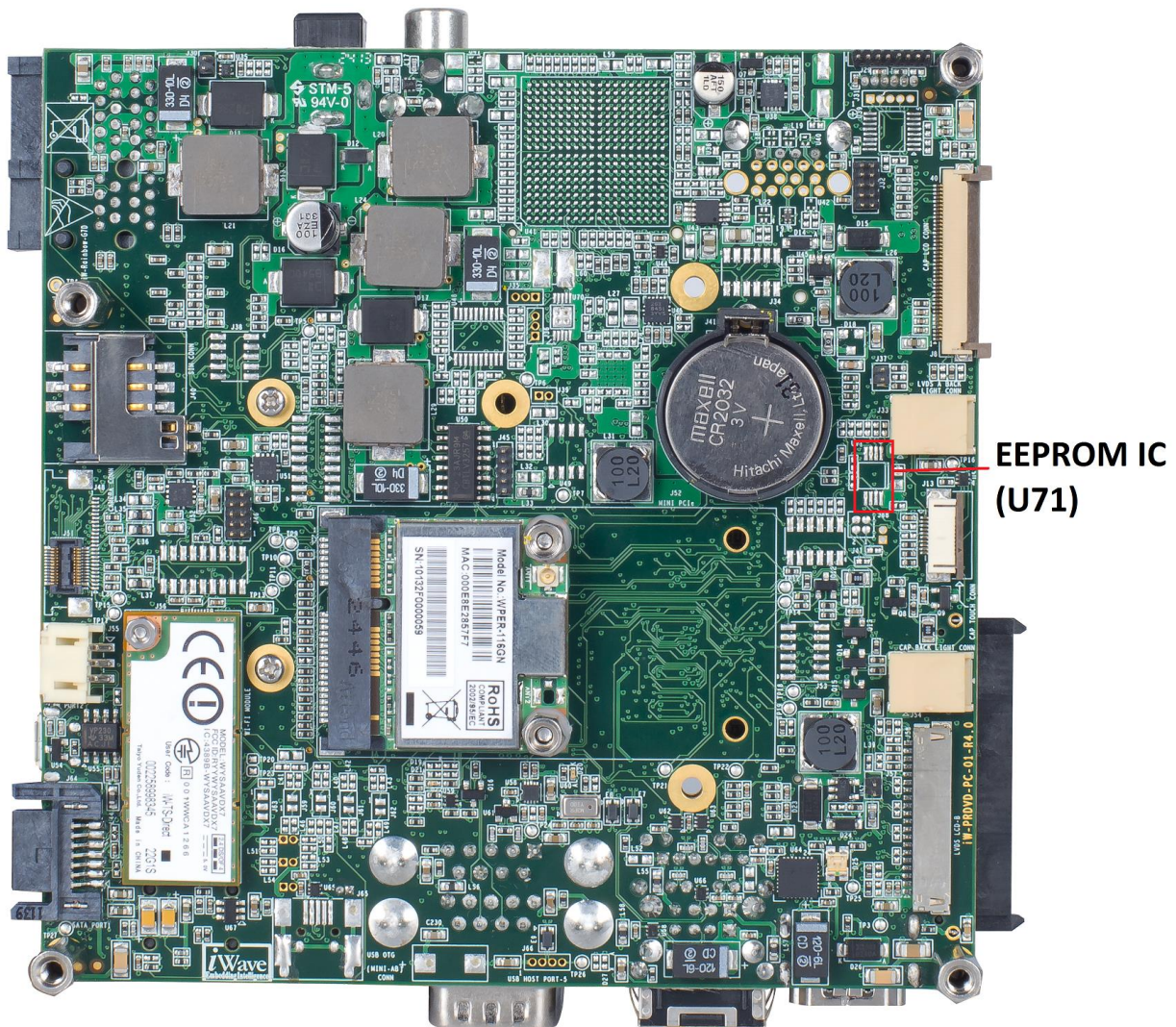
Figure 28: EEPROM

Note: This is not the standard feature of Qseven specification.

2.8.5 Sensors

The Qseven Generic Carrier Board supports 4 on board sensors,

- Ambient Light Sensor

- Digital eCompass

- 3-Axis accelerometer

- Altimeter/Barometer

Below figure shows the Sensor's physical location on the top and bottom of the board as shown below.
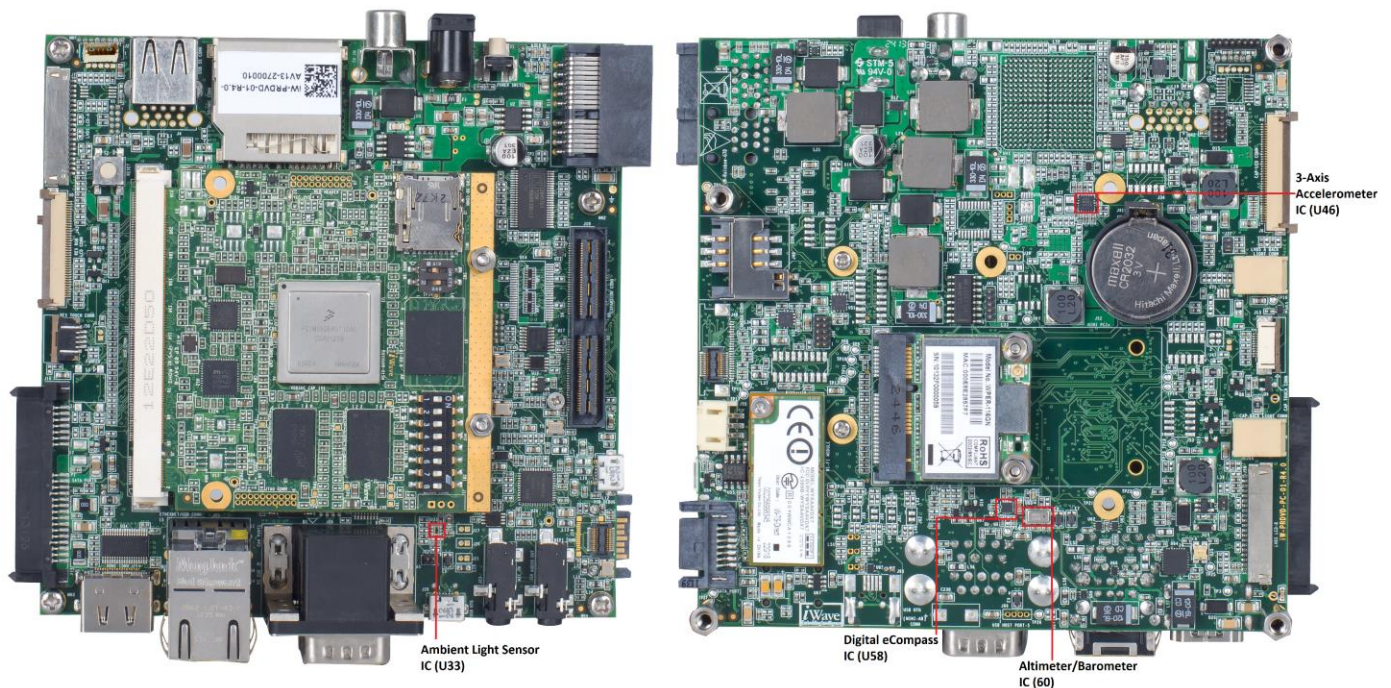
Figure 29: Sensors

2.8.5.1 Ambient Light Sensor

The Qseven Generic Carrier Board supports on board Ambient Light Sensor. This sensor is connected to I2C interface of Qseven MXM connector (66th and 68th Pin) and interrupt is connected to 188th Pin of Qseven MXM connector. This sensor (U33) is physically located on the top of the board as shown in **Figure 29**

2.8.5.2 Digital eCompass

The Qseven Generic Carrier Board supports on board Digital eCompass Sensor. This sensor is connected to I2C interface of Qseven MXM connector (66th and 68th Pin) and interrupt is connected to 186th Pin of Qseven MXM connector. This sensor (U58) is physically located on the bottom of the board as shown in **Figure 29**

2.8.5.3 3-Axis Accelerometer

The Qseven Generic Carrier Board supports on board 3-Axis Accelerometer. This sensor is connected to I2C interface of Qseven MXM connector (66th and 68th Pin) and interrupt is connected to 187th Pin of Qseven MXM connector. This sensor is physically located on the bottom (U46) of the board as shown in **Figure 29**

2.8.5.4 Altimeter/Barometer

The Qseven Generic Carrier Board supports on board Altimeter/Barometer. This sensor is connected to I2C interface of Qseven MXM connector (66th and 68th Pin) and interrupt is connected to 189th Pin of Qseven MXM connector. This sensor (U60) is physically located on the bottom of the board as shown in **Figure 29**

2.8.6 Add-on Headers

2.8.6.1 SPI Header

Qseven Generic Carrier Board supports SPI header for SPI interface expansion. SPI signals from Qseven MXM connector is connected to this SPI header (J29) and physically located at the bottom of board as shown below.

Number of Pins: 8
Connector Part number: GRPB081VWVN-RC
Mating Connector: LPPB081NFFN-RC from Sullins Connector Solutions
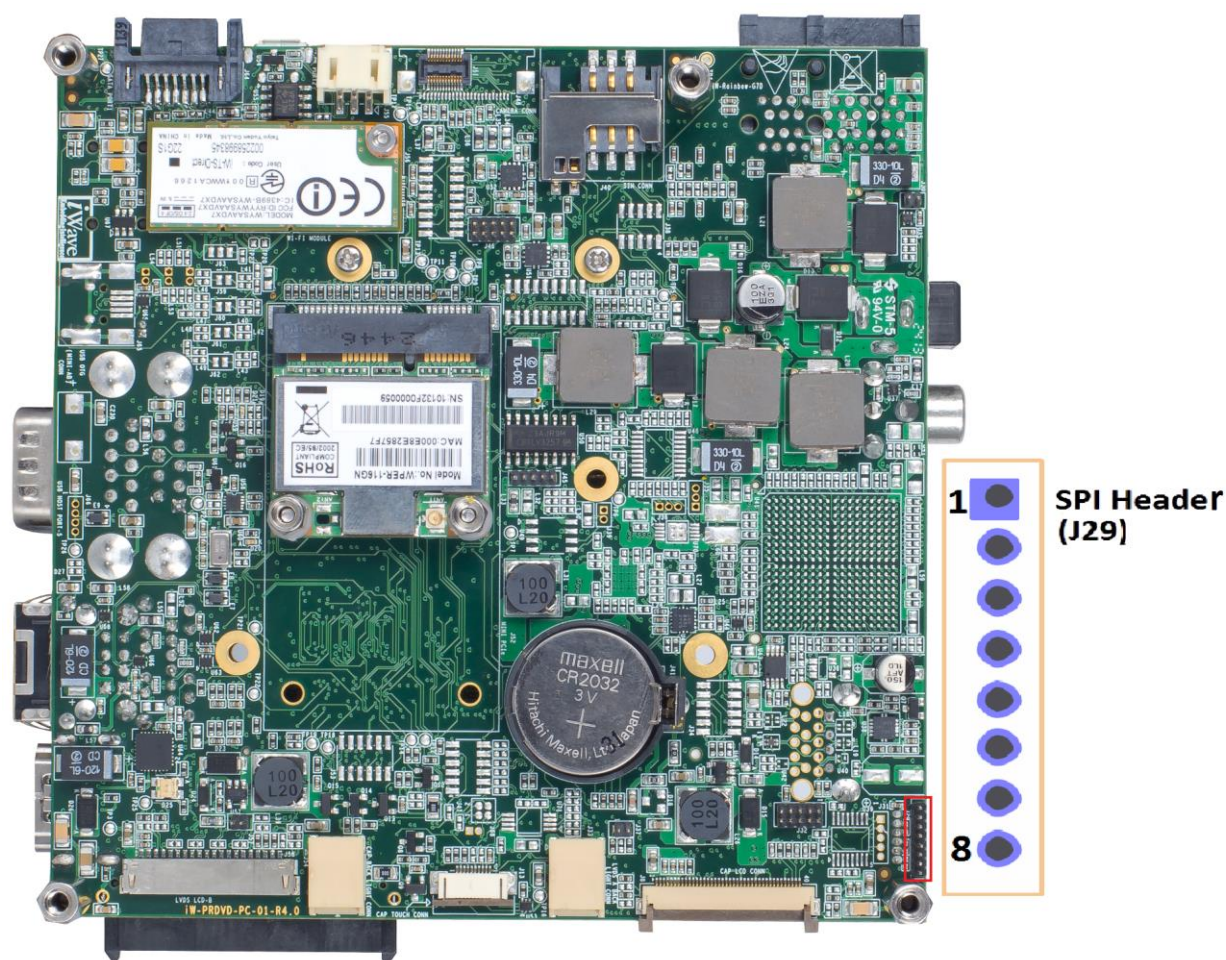
Figure 30: SPI Header

Table 32: SPI Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	SPI_CS0#	Output	3.3V CMOS	SPI Chip select 0. Connected to 200th Pin of Qseven MXM Connector.
2	SPI_MISO	Input/Output	3.3V CMOS	SPI Master In Slave Out. Connected to 201st Pin of Qseven MXM Connector.
3	GND	Power	0V	Ground.
4	SPI_MOSI	Input/Output	3.3V CMOS	SPI Master Out Slave In. Connected to 199th Pin of Qseven MXM Connector.
5	SPI_SCK	Output	3.3V CMOS	SPI clock. Connected to 203rd Pin of Qseven MXM Connector.
6	VCC_3V3	Power	3.3V	3.3V Power Supply.
7	SPI_CS1#	Output	3.3V CMOS	SPI Chip select1. Connected to 202nd Pin of Qseven MXM Connector.
8	GND	Power	0V	Ground.

2.8.6.2 LPC Header (Optional)

LPC signals from the Qseven MXM Connector are connected to a 12 pin SMD pad header (J34) for LPC interface. These SMD pads can be accessed at the bottom of the board as shown below.
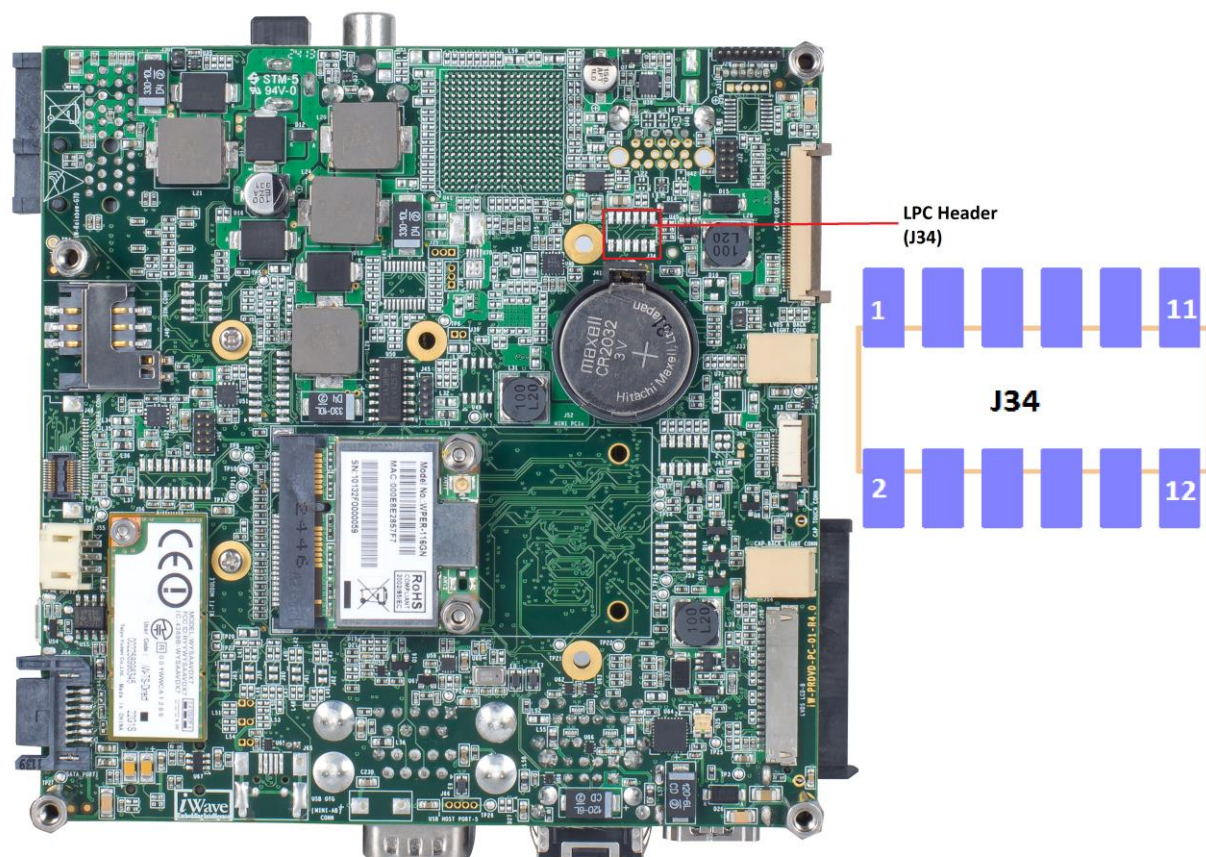
Figure 31: LPC Header

Table 33: LPC Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	NC	NC	NC	No Connection.
2	NC	NC	NC	No Connection.
3	VGA_HSYNC	Output	3.3V CMOS	VGA HSYNC. Connected to 74th Pin of Expansion Connector2.

4	VGA_VSYNC	Output	3.3V CMOS	VGA VSYNC. Connected to 76th Pin of Expansion Connector2.
5	LPC_AD0/GP0	Input/Output	3.3V CMOS	GPIO connected to Touch interrupt. Connected to 185th Pin of Qseven MXM Connector Pin.
6	LPC_AD1/GP1	Input/Output	3.3V CMOS	GPIO connected to Digital eCompass interrupt. Connected to 186th Pin of Qseven MXM Connector.
7	LPC_AD2/GP2	Input/Output	3.3V CMOS	GPIO connected to 3-Axis Accelerometer interrupt. Connected to 187th Pin of Qseven MXM Connector.
8	LPC_AD3/GP3	Input/Output	3.3V CMOS	GPIO connected to Ambient Light Sensor interrupt. Connected to 188th Pin of Qseven MXM Connector.
9	LPC_CLK/GP4	Input/Output	3.3V CMOS	GPIO connected to Altimeter/ Barometer interrupt. Connected to 189th Pin of Qseven MXM Connector Pin.
10	LPC_FRAME#/GP5	Input/Output	3.3V CMOS	GPIO connected to SATA. Connected to 190th Pin of Qseven MXM Connector.
11	SERIRQ/GP6	Input/Output	3.3V CMOS	GPIO connected to MIPI power down signal. Connected to 191st Pin of Qseven MXM Connector.
12	LPC_LDRQ#/GP7	Input/Output	3.3V CMOS	GPIO connected to USB power switch. Connected to 192nd Pin of Qseven MXM Connector.

2.8.6.3 SDVO Header (Optional)

SDVO signals from the Qseven MXM Connector are connected to a 12 pin SMD pad header (J47) for SDVO interface. These SMD pads can be accessed at the bottom of the board as shown below.
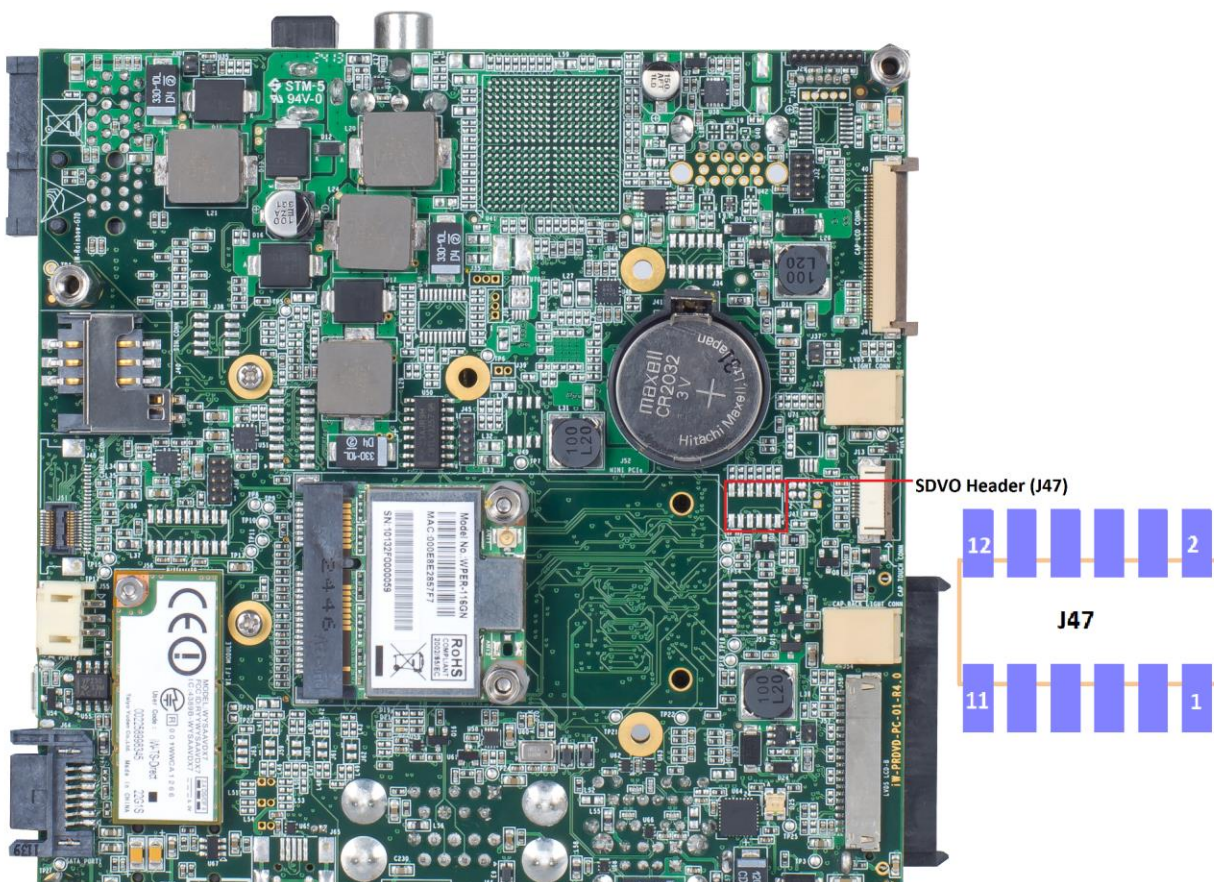
Figure 32: SDVO Header

Table 34: SDVO Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	GND	GND	Ground
2	NC_SDVO_INT+	Input	TMDS	HDMI differential interrupt positive. Connected to 132nd Pin of Qseven MXM Connector.

3	SMB_ALERT#	Output	3.3V CMOS	System Management Bus Alert. Connected to 64th Pin from Qseven MXM Connector.
4	NC_SDVO_INT-	Input	TMDS	HDMI differential interrupt positive. Connected to 134th of Qseven MXM Connector.
5	FAN_GP_TIMER_IN	Output	3.3V CMOS	Fan tachometer input. Connected from 195th Pin of Qseven MXM Connector.
6	NC_SDVO_FLDSTALL+	Input/Output	TMDS	HDMI differential device control data positive. Connected to 138th Pin of Qseven MXM Connector.
7	FAN_PWM_OUT1	Input	3.3V CMOS	Fan PWM. Connected to 196th Pin of Qseven MXM Connector.
8	NC_SDVO_FLDSTALL-	Input/Output	TMDS	HDMI differential device control data negative. Connected to 140th Pin of Qseven MXM Connector.
9	DP_HPD#	Output	3.3V CMOS	Tamper Switch. Connected from 154th Pin of Qseven MXM Connector.
10	NC_SDVO_TVCLKIN+	Input	TMDS	HDMI differential clock data positive. Connected to 144th Pin of Qseven MXM Connector.
11	GND	GND	GND	Ground.
12	NC_SDVO_TVCLKIN-	Input	TMDS	HDMI differential clock data negative. Connected to 146th Pin of Qseven MXM Connector.

2.8.6.4 Qseven Control Signal Header (Optional)

Control signals from the Qseven MXM Connector are connected to a 12 pin SMD pad header (J53) for Control Signal expansion. These SMD pads can be accessed at the bottom of the board as shown below.
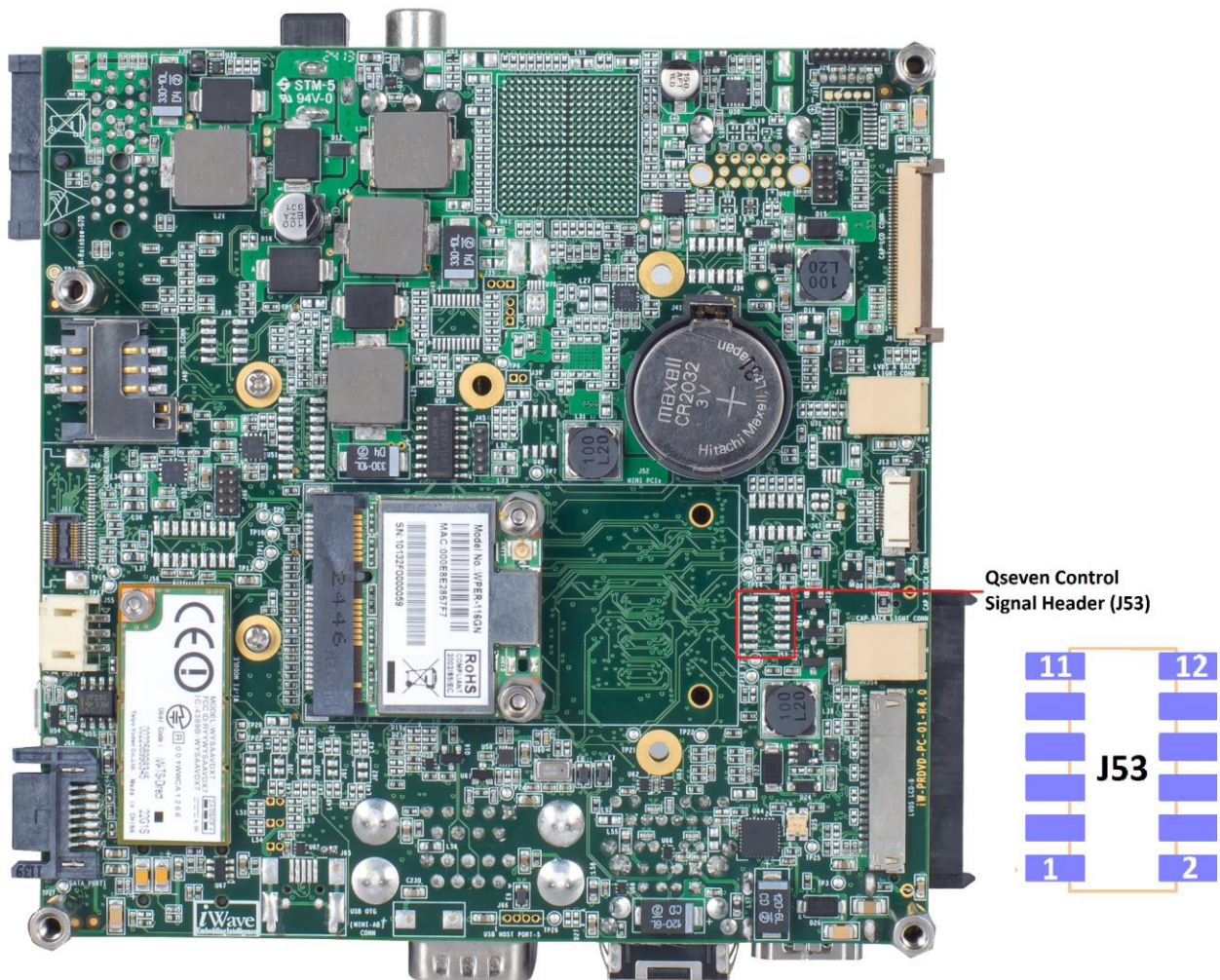

Figure 33: Qseven Control Signal

Table 35: Qseven Control Signal Header

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	NC_RSVD2	NC	NC	No Connection.
2	WDTRIG#	Input	3.3V CMOS	Watchdog trigger signal. Connected from 70th Pin of Qseven MXM Connector.
3	SUS_STAT#	Output	3.3V CMOS	Suspend Status. Connected to 19th Pin of Qseven MXM Connector.
4	WDOUT	Output	3.3V CMOS	Watchdog event indicator. Connected to 72nd Pin of Qseven MXM Connector.
5	SLP_BTN#	Input	3.3V CMOS	Sleep button. Connected from 21st Pin of Qseven MXM Connector.
6	LID_BTN#	Input	3.3V CMOS	LID Button. Connected from 22nd Pin of Qseven MXM Connector.
7	GND	Power	GND	Ground.
8	WAKE#	Input	3.3V CMOS	External system wake event. Connected from 17th Pin of Qseven MXM Connector.
9	BATLOW#	Input	3.3V CMOS	Battery low indication. Connected from 27th Pin of Qseven MXM Connector.
10	BIOS_DSIABLE#	Input	3.3V CMOS	Module BIOS disable. Connected from 41st Pin of Qseven MXM Connector.
11	THRM#	Input	3.3V CMOS	Thermal Alarm active low signal. Connected from 69th Pin of Qseven MXM Connector.
12	THRMTRIP#	Output	3.3V CMOS	Thermal Trip indicates an overheating condition of the Processor. Connected to 71st Pin of Qseven MXM Connector.

2.9   Expansion Connectors

The Qseven Generic Carrier Board has two 80pin board to board expansion connectors. Since Qseven edge connector pull-out only a selected set of interfaces as per Qseven standard, these two expansion connectors are used in iWave's Qseven CPU modules to bring more interfaces from CPU. These Expansion connectors Expansion Connector 1 (J14) and Expansion Connector 2 (J9) are physically located at the top of the board as shown in **Figure 34** & **Figure 35** respectively.

Number of Pins: 80

Connector Part number: DF17(3.0)-80DS-0.5V(57)

Mating Connector: DF17(2.0)-80DP-0.5V(57) from Hirose Electric Co Ltd

Note: iWave has made careful effort to make these expansion connectors pinout to be same for all iWave Qseven CPU modules. But there are some signals in these connectors may be different between CPU modules because of respective CPU supported interface. For more information about Expansion Connector pin out, refer corresponding Qseven CPU Module's Hardware User Manual.

Expansion Connector1 (J14)

J14
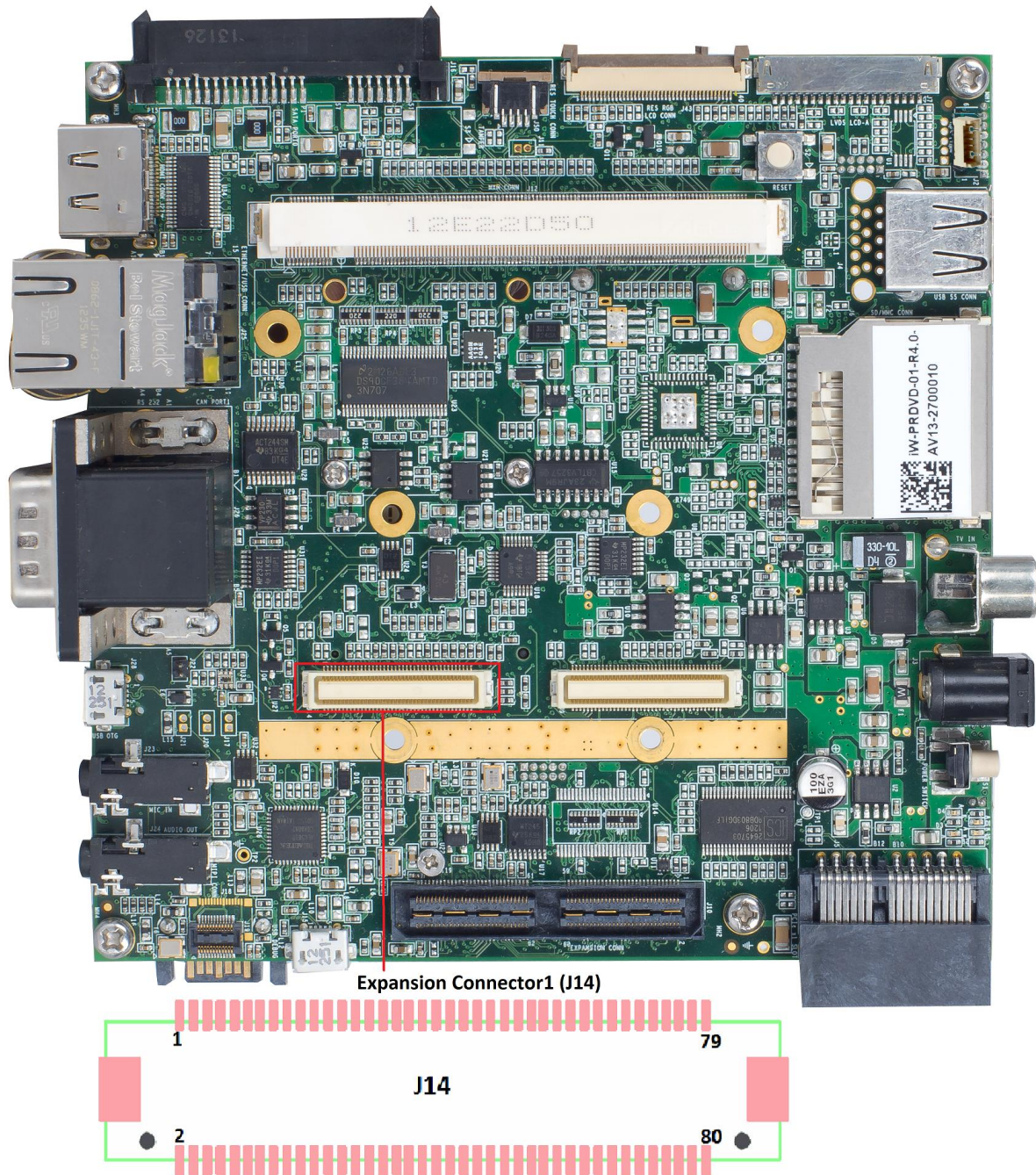
Figure 34: Expansion Connector 1

Table 36: Expansion Connector1 Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground.
2	GPPIN_0	Input/Output	3.3V CMOS	General Purpose Pin0. Connected to 96th Pin of Carrier Board Expansion Connector (J10).
3	GPPIN_1	Input/Output	3.3V CMOS	General Purpose Pin1. Connected to 95th Pin of Carrier Board Expansion Connector (J10).
4	GPPIN_2	Input/Output	3.3V CMOS	General Purpose Pin2. Connected to 94th Pin of Carrier Board Expansion Connector (J10).
5	GPPIN_3	Input/Output	3.3V CMOS	General Purpose Pin3. Connected to 93rd Pin of Carrier Board Expansion Connector (J10).
6	GPPIN_4	Input/Output	3.3V CMOS	General Purpose Pin4. Connected to 92nd Pin of Carrier Board Expansion Connector (J10).
7	GPPIN_5	Input/Output	3.3V CMOS	General Purpose Pin5. Connected to 91st Pin of Carrier Board Expansion Connector (J10).
8	GPPIN_6	Input/Output	3.3V CMOS	General Purpose Pin6. Connected to 90th Pin of Carrier Board Expansion Connector (J10).
9	GPPIN_7	Input/Output	3.3V CMOS	General Purpose Pin7. Connected to 89th Pin of Carrier Board Expansion Connector (J10).
10	GPPIN_8	Input/Output	3.3V CMOS	General Purpose Pin8. Connected to 88th Pin of Carrier Board Expansion Connector (J10).
11	GPPIN_9	Input/Output	3.3V CMOS	General Purpose Pin9. Connected to 87th Pin of Carrier Board Expansion Connector (J10).

12	GPPIN_10	Input/Output	3.3V CMOS	General Purpose Pin10. Connected to 86th Pin of Carrier Board Expansion Connector (J10).
13	GPPIN_11	Input/Output	3.3V CMOS	General Purpose Pin11. Connected to 85th Pin of Carrier Board Expansion Connector (J10).
14	GPPIN_12	Input/Output	3.3V CMOS	General Purpose Pin12. Connected to 84th Pin of Carrier Board Expansion Connector (J10).
15	GPPIN_13	Input/Output	3.3V CMOS	General Purpose Pin13. Connected to 83rd Pin of Carrier Board Expansion Connector (J10).
16	GPPIN_14	Input/Output	3.3V CMOS	General Purpose Pin14. Connected to 82nd Pin of Carrier Board Expansion Connector (J10).
17	GPPIN_15	Input/Output	3.3V CMOS	General Purpose Pin15. Connected to 81st Pin of Carrier Board Expansion Connector (J10).
18	GPPIN_16	Input/Output	3.3V CMOS	General Purpose Pin16. Connected to 78th Pin of Carrier Board Expansion Connector (J10).
19	GPPIN_PWM2	Input	3.3V CMOS	General Purpose Pin PWM2 input. Connected to 54th Pin of Carrier Board Expansion Connector (J10).
20	GPPIN_20	Input/Output	3.3V CMOS	General Purpose Pin20. Connected to 74th Pin of Carrier Board Expansion Connector (J10).
21	CAN2_PD	Input	3.3V CMOS	CAN2 Power Down. Connected 73rd Pin of Carrier Expansion Connector (J10). Optionally connected to CAN2 transceiver power down pin through resistor and default not populated.

22	CAN1_PD	Input	3.3V CMOS	CAN1 Power Down. Connected to CAN1 transceiver power down pin & to 72nd Pin of Carrier Expansion Connector (J10).
23	LVDS2_BLEN	Input	3.3V CMOS	LVDS2 Backlight enable. Connected to 71st pin of Carrier Expansion Connector (J10). Optionally connected to LVDS2 backlight enable through resistor and default not populated.
24	W_DISABLE	Input	3.3V CMOS	Wireless Disable. Connected to 20th Pin of Mini PCIe connector (J52) & to 70th Pin of Carrier Expansion Connector (J10).
25	LVDS2_PPEN	Input	3.3V CMOS	LVDS2 power enable. Connected to 69th Pin of Carrier Expansion Connector (J10) Optionally connected to LVDS2 power enable through resistor and default not populated.
26	LS_ADC1_PD	Input	3.3V CMOS	TV decoder Power down. Connected to TV decoder Power down pin & to 68th Pin of Carrier Expansion Connector (J10).
27	GND	Power	0V	Ground.
28	LS_ADC1_GLCO	Output	3.3V CMOS	TV decoder GLCO. Connected to TV decoder GLCO pin & to 67th Pin of Carrier Expansion Connector (J10).
29	ADC1_INTREQ	Output	3.3V CMOS	TV decoder interrupt. Connected to TV decoder INT pin & to 66th Pin of Carrier Expansion connector (J10).

30	LS_ADC1_AVID	Output	3.3V CMOS	TV decoder active video indicator. Connected to TV decoder AVID pin & to 65th Pin of Carrier Expansion connector (J10).
31	MIC_IN_DETECT	Output	3.3V CMOS	Micro phone input. Connected to 4th Pin of Audio In Mono Jack (J23) & to 64th Pin of Carrier Expansion Connector (J10).
32	GND	Power	0V	Ground.
33	GPAI_MCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 51st Pin of Carrier Expansion Connector (J10).
34	GPAI_LRCK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 52nd Pin of Carrier Expansion Connector (J10).
35	GPAI_BCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 49th Pin of Carrier Expansion Connector (J10).
36	GPAI_DATA	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 50th Pin of Carrier Expansion Connector (J10).
37	GND	Power	0V	Ground.
38	HP_DETECT	Output	3.3V CMOS	Headphone detect. Connected to 4th Pin of Audio Out Stereo Jack (J24) & to 58th Pin of Carrier Expansion Connector (J10).
39	GND	Power	0V	Ground.
40	LVDS_BLEN	Input	3.3V CMOS	LVDS backlight enable. Default NC. Optionally Connected to 114th Pin of Carrier Expansion Connector (J10) through resistor and default not populated.

41	TSC_INT#	Output	3.3V CMOS	Touch interrupt. Connected to touch interface interrupt & to 53rd Pin of Carrier Expansion connector (J10).
42	EXP1_PIN42	Power	0V	Ground. Connected to ground through resistor.
43	AC97_IRQOUT	Output	3.3V CMOS	AC'97 interrupt request. Connected to AC'97 Audio CODEC IRQOUT pin & to 55th Pin of Carrier Expansion Connector (J10).
44	GND	Power	0V	Ground.
45	GPAO_DATA	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 102nd Pin of Carrier Expansion Connector (J10).
46	GPAO_BCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 101st Pin of carrier Expansion Connector (J10).
47	GPAO_LRCK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 100th Pin of carrier Expansion Connector (J10).
48	AO_MCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 99th Pin of Carrier Expansion connector (J10).
49	GND	Power	0V	Ground.
50	UART1_TXD	Input	3.3V CMOS	UART1 Transmit signal. Default NC. Optionally Connected to Debug RS232 transceiver through resistor and default not populated.
51	UART1_RTS	Output	3.3V CMOS	UART1 Ready To Send signal. Default NC. Optionally Connected to Debug RS232 transceiver through resistor and default not populated.

52	UART1_RXD	Output	3.3V CMOS	UART1 Receive signal. Default NC. Optionally Connected to Debug RS232 transceiver through resistor and default not populated.
53	UART1_CTS	Input	3.3V CMOS	UART1 Clear to Send signal. Default NC. Optionally Connected to Debug RS232 transceiver through resistor and default not populated.
54	GND	Power	0V	Ground.
55	WIFI_PDN	Input	3.3V CMOS	Wi-Fi power down. Connected to 63rd Pin of Carrier Expansion Connector (J10). Optionally connected to 14th Pin of Wi-Fi Module connector (J56) through resistor and default not populated.
56	WL_HOST_WKUP	Input	3.3V CMOS	WLAN wake up. Connected to 59th Pin of Carrier Expansion Connector (J10). Optionally connected to 16th Pin of Wi-Fi Module Connector (J56) through resistor and default not populated.
57	HOST_WL_WKUP	Output	3.3V CMOS	Host wake up. Connected to 60th Pin of Carrier Expansion Connector (J10). Optionally connected to 17th Pin of Wi-Fi Module Connector (J56) through resistor and default not populated
58	CAM_PWDN	Input	3.3V CMOS	CMOS camera power down. Connected to 8th Pin of CMOS Camera Connector (J51) & to 57th Pin of Carrier Expansion Connector (J10).

59	GND	Power	0V	Ground.
60	UART2_RXD	Output	3.3V CMOS	UART2 Receive signal. Connected to 3rd pin of UART2 header (J45) through UART2 RS232 transceiver.
61	UART2_485RE#	Output	3.3V CMOS	UART2 Ready to Send signal. Connected to 4th pin of UART2 header (J45) through UART2 RS232 transceiver.
62	UART2_485DE	Input	3.3V CMOS	UART2 Clear to Send signal. Connected to 2nd pin of UART2 header (J45) through UART2 RS232 transceiver.
63	UART2_TXD	Input	3.3V CMOS	UART2 Transmit signal. Connected to 1st pin of UART2 header (J45) through UART2 RS232 transceiver.
64	CSI1_MCLK	Input	3.3V CMOS	CSI port1 Master clock. Default NC. Optionally Connected to TV decoder reference clock input through resistor and default not populated.
65	CSI1_PCLK	Output	3.3V CMOS	CSI port1 Pixel clock. Connected to TV decoder PCLK pin.
66	CSI1_HSYNC	Output	3.3V CMOS	CSI port1 HSYNC. Connected to TV decoder HSYNC pin.
67	CS1_VCLK	Output	3.3V CMOS	CSI port1 data enable. Default NC. Optionally Connected to 13th Pin of CMOS Camera Connector (J51) through resistor and default not populated.

68	CSI1_VSYNC	Output	3.3V CMOS	CSI port1 VSYNC. Connected to TV decoder VSYNC pin.
69	CSI1_DAT0	Output	3.3V CMOS	CSI port1 data bit0. Connected to TV decoder Data0 pin.
70	CSI1_DAT1	Output	3.3V CMOS	CSI port1 data bit1. Connected to TV decoder Data1 pin.
71	CSI1_DAT2	Output	3.3V CMOS	CSI port1 data bit2. Connected to TV decoder Data2 pin.
72	CSI1_DAT3	Output	3.3V CMOS	CSI port1 data bit3. Connected to TV decoder Data3 pin.
73	CSI1_DAT4	Output	3.3V CMOS	CSI port1 data bit4. Connected to TV decoder Data4 pin.
74	CSI1_DAT6	Output	3.3V CMOS	CSI port1 data bit6. Connected to TV decoder Data6 pin.
75	CSI1_DAT7	Output	3.3V CMOS	CSI port1 data bit7. Connected to TV decoder Data7 pin.
76	CSI1_DAT5	Output	3.3V CMOS	CSI port1 data bit5. Connected to TV decoder Data5 pin.
77	GPPIN_17	Input/Output	3.3V CMOS	General Purpose Pin 17. Connected to 77th Pin of Carrier Expansion Connector (J10).
78	GPIN18_CAN1_RXD	Output	3.3V CMOS	CAN2 Receive signal. Connected to CAN2 transceiver & to 76th Pin of Carrier Expansion Connector (J10).
79	GPIN19_CAN1_TXD	Input	3.3V CMOS	CAN2 Transmit signal. Connected to CAN2 transceiver & to 75th Pin of Carrier Expansion Connector (J10).
80	GND	Power	0V	Ground.

Expansion Connector2 (J9)
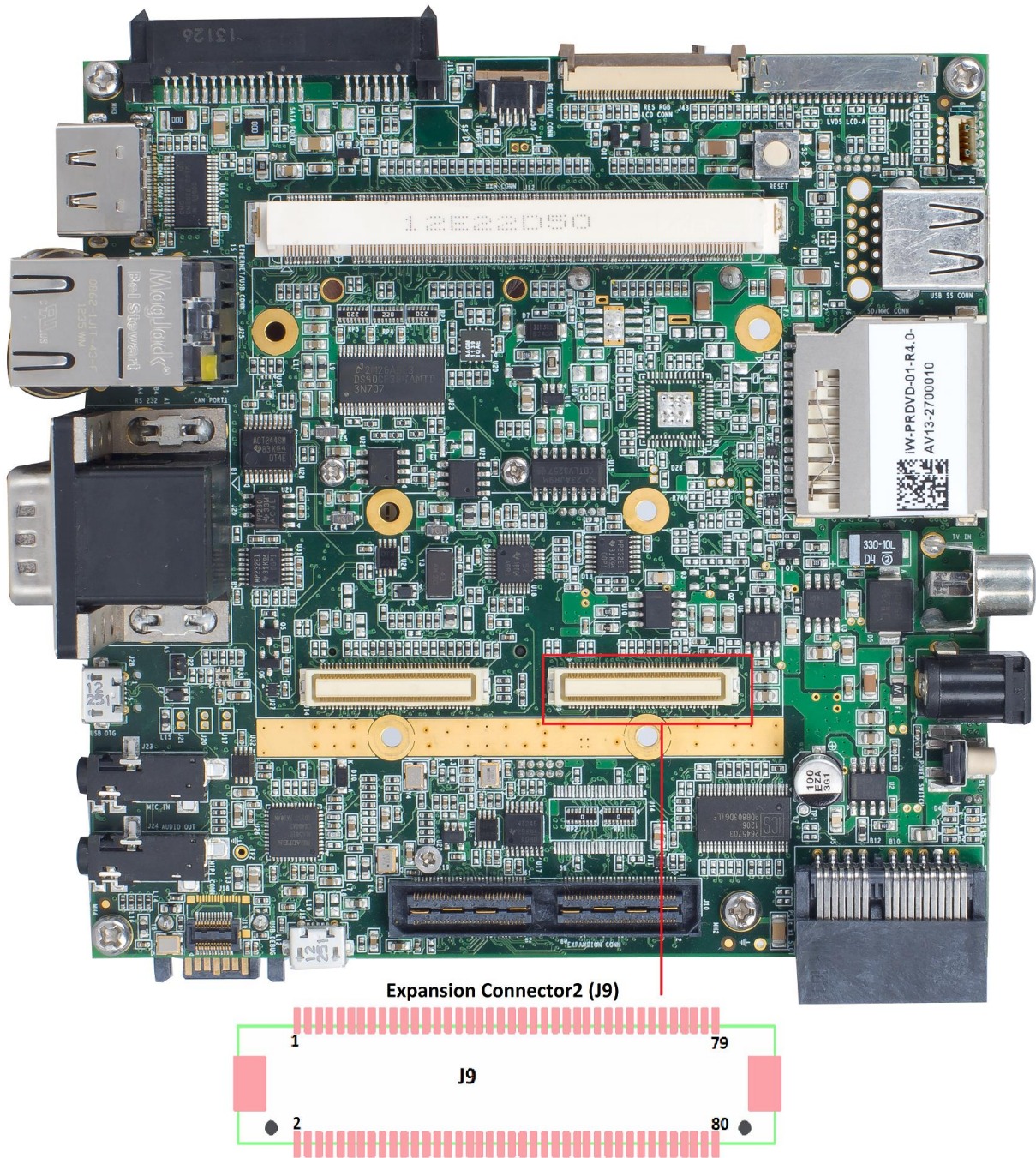
Figure 35: Expansion Connector 2

Table 37: Expansion Connector2 Pin Out

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	TSC_X2	Output	Analog	Touch X2-axis. Connected to 1st Pin of VGA Interface Header (J38). Optionally connected to 2nd Pin of touch Connector (J50) through resistor and default not populated.
2	TSC_X1	Output	Analog	Touch X1-axis. Connected to 2nd Pin of VGA Interface Header (J38). Optionally connected to 4th Pin of touch Connector (J50) through resistor and default not populated.
3	TSC_Y2	Output	Analog	Touch Y2-axis. Connected to 3rd Pin of VGA Interface Header (J38). Optionally connected to 3rd Pin of touch Connector (J50) through resistor and default not populated.
4	TSC_Y1	Output	Analog	Touch Y1-axis. Connected to 4th Pin of VGA Interface Header (J38). Optionally connected to 1st Pin of touch Connector (J50) through resistor and default not populated
5	GND	Power	0V	Ground.
6	GND	Power	0V	Ground.
7	KP_ROW0	Input/Output	3.3V CMOS	Keypad Row0. Connected to 1st Pin of Keypad Header (J46).
8	KP_ROW1	Input/Output	3.3V CMOS	Keypad Row1. Connected to 2nd Pin of Keypad Header (J46).

9	KP_ROW2	Input/Output	3.3V CMOS	Keypad Row2. Connected to 3rd Pin of Keypad Header (J46).
10	KP_ROW3	Input/Output	3.3V CMOS	Keypad Row3. Connected to 4th Pin of Keypad Header (J46).
11	KP_COL0	Input/Output	3.3V CMOS	Keypad Column0. Connected to 7th Pin of Keypad Header (J46).
12	KP_COL1	Input/Output	3.3V CMOS	Keypad Column1. Connected to 8th Pin of Keypad Header (J46).
13	KP_COL2	Input/Output	3.3V CMOS	Keypad Column2. Connected to 9th Pin of Keypad Header (J46).
14	KP_COL3	Input/Output	3.3V CMOS	Keypad Column3. Connected to 10th Pin of Keypad Header (J46).
15	GND	Power	0V	Ground.
16	GND	Power	0V	Ground.
17	GPEM_DA1	Input/Output	3.3V CMOS	EIM Data & address line 1. Connected to 45th Pin of Carrier Expansion Connector (J10).
18	GPEM_DA0	Input/Output	3.3V CMOS	EIM Data & address line 0. Connected to 46th Pin of Carrier Expansion Connector (J10).
19	GPEM_DA3	Input/Output	3.3V CMOS	EIM Data & address line 3. Connected to 43rd Pin of Carrier Expansion Connector (J10).
20	GPEM_DA2	Input/Output	3.3V CMOS	EIM Data & address line 2. Connected to 44th Pin of Carrier Expansion Connector (J10).
21	GPEM_DA5	Input/Output	3.3V CMOS	EIM Data & address line 5. Connected to 41st Pin of Carrier Expansion Connector (J10).
22	GPEM_DA4	Input/Output	3.3V CMOS	EIM Data & address line 4. Connected to 42nd Pin of Carrier Expansion Connector (J10).

23	GPEM_DA7	Input/Output	3.3V CMOS	EIM Data & address line 7. Connected to 39th Pin of Carrier Expansion Connector (J10).
24	GPEM_DA6	Input/Output	3.3V CMOS	EIM Data & address line 6. Connected to 40th Pin of Carrier Expansion Connector (J10).
25	GPEM_DA9	Input/Output	3.3V CMOS	EIM Data & address line 9. Connected to 37th Pin of Carrier Expansion Connector (J10).
26	GPEM_DA8	Input/Output	3.3V CMOS	EIM Data & address line 8. Connected to 38th Pin of Carrier Expansion Connector (J10).
27	GPEM_DA11	Input/Output	3.3V CMOS	EIM Data & address line 11. Connected to 35th Pin of Carrier Expansion Connector (J10).
28	GPEM_DA10	Input/Output	3.3V CMOS	EIM Data & address line 10. Connected to 36th Pin of Carrier Expansion Connector (J10).
29	GPEM_DA13	Input/Output	3.3V CMOS	EIM Data & address line 13. Connected to 33rd Pin of Carrier Expansion Connector (J10).
30	GPEM_DA12	Input/Output	3.3V CMOS	EIM Data & address line 12. Connected to 34th Pin of Carrier Expansion Connector (J10).
31	GPEM_DA15	Input/Output	3.3V CMOS	EIM Data & address line 15. Connected to 31st Pin of Carrier Expansion Connector (J10).
32	GPEM_DA14	Input/Output	3.3V CMOS	EIM Data & address line 14. Connected to 32nd Pin of Carrier Expansion Connector (J10).
33	GND	Power	0V	Ground.
34	GND	Power	0V	Ground.
35	GPEM_RW	Input	3.3V CMOS	EIM Read/Write Enable. Connected to 27th Pin of Carrier Expansion Connector (J10).
36	GPEM_CS0	Input	3.3V CMOS	EIM Chip Select0. Connected to 28th Pin of Carrier Expansion Connector (J10).

37	GPEM_BCLK	Input	3.3V CMOS	EIM Burst Clock. Connected to 25th Pin of Carrier Expansion Connector (J10).
38	GPEM_CRE	Input	3.3V CMOS	EIM Memory Register Set. Connected to 26th Pin of Carrier Expansion Connector (J10).
39	GPEM_EB1	Input	3.3V CMOS	EIM Enable Byte1. Connected to 23rd Pin of Carrier Expansion Connector (J10).
40	GPEM_WAIT	Output	3.3V CMOS	EIM Ready/Busy/Wait. Connected to 24th Pin of Carrier Expansion Connector (J10).
41	SSI_RXD	Output	3.3V CMOS	SSI Receive Signal. Connected to 21st Pin of Carrier Expansion Connector (J10). Optionally connected to 49th Pin of Mini PCIe Connector (J52) through resistor and default not populated.
42	GPEM_EB0	Input	3.3V CMOS	EIM Enable Byte0. Connected to 22nd Pin of Carrier Expansion Connector (J10).
43	SSI_TXFS	Input	3.3V CMOS	SSI Transmit Frame. Connected to 19th Pin of Carrier Expansion Connector (J10). Optionally connected to 51st Pin of Mini PCIe Connector (J52) through resistor and default not populated.
44	SSI_TXD	Input	3.3V CMOS	SSI Transmit. Connected to 20th Pin of Carrier Expansion Connector (J10). Optionally connected to 47th Pin of Mini PCIe Connector (J52) through resistor and default not populated.

45	SSI_TXC	Output	3.3V CMOS	SSI Transmit clock. Connected to 18th Pin of Carrier Expansion Connector (J10). Optionally connected to 45th Pin of Mini PCIe Connector (J52) through resistor and default not populated.
46	GND	Power	0V	Ground.
47	GND	Power	0V	Ground.
48	CSI2_D3	Output	3.3V CMOS	CSI Port2 data bit3. Connected to 21st Pin of CMOS Camera Connector (J51).
49	CSI2_D2	Output	3.3V CMOS	CSI Port2 data bit2. Connected to 19th Pin of CMOS Camera Connector (J51).
50	CSI2_D5	Output	3.3V CMOS	CSI Port2 data bit5. Connected to 22nd Pin of CMOS Camera Connector (J51).
51	CSI2_D4	Output	3.3V CMOS	CSI Port2 data bit4. Connected to 20th Pin of CMOS Camera Connector (J51).
52	CSI2_D7	Output	3.3V CMOS	CSI Port2 data bit7. Connected to 16th Pin of CMOS Camera Connector (J51).
53	CSI2_D6	Output	3.3V CMOS	CSI Port2 data bit6. Connected to 18th Pin of CMOS Camera Connector (J51).
54	CSI2_D8	Output	3.3V CMOS	CSI Port2 data bit8. Connected to 14th Pin of CMOS Camera Connector (J51).
55	CSI2_D9	Output	3.3V CMOS	CSI Port2 data bit9. Connected to 12th Pin of CMOS Camera Connector (J51).
56	CSI2_HSYNC	Output	3.3V CMOS	CSI Port2 HSYNC. Connected to 9th Pin of CMOS Camera Connector (J51).

57	CSI2_VSYNC	Output	3.3V CMOS	CSI Port2 VSYNC. Connected to 7th Pin of CMOS Camera Connector (J51).
58	CSI2_PIXCLK	Output	3.3V CMOS	CSI Port2 Pixel Clock. Connected to 17th Pin of CMOS Camera Connector (J51).
59	GND	Power	0V	Ground.
60	GND	Power	0V	Ground.
61	IOUTF/ CSI_CLK0P	Output	Differential	MIPI CSI clock positive. Connected to 16th Pin of MIPI Camera Connector (J19) and to 15th Pin of Carrier Expansion Connector (J10)
62	VGA_TV_RED	Input	Analog	VGA_TV Red Signal. Connected to 2nd Pin of TV Out Header (J30) & to 6th Pin of VGA Interface Header (J38).
63	GPIF_P2 / CSI_CLK0M	Output	3.3V CMOS	MIPI CSI clock negative. Connected to 18th Pin of MIPI Camera Connector (J19) and to 14th Pin of Carrier Expansion Connector (J10).
64	GPIF_P9	Power	0V	General Purpose Pin 9. Connected to 7th Pin of Carrier Expansion Connector (J10). Optionally Connected to Ground through resistor and default not populated.
65	IOUTE/CSI_D0P	Output	Differential	MIPI CSI data0 positive. Connected to 20th Pin of MIPI Camera Connector (J19) and to 13th Pin of Carrier Expansion Connector (J10)
66	VGA_TV_GRN	Input	Analog	VGA_TV Green Signal. Connected to 5th Pin of VGA Signal Header (J38).

67	GPIF_P4/CSI_D0M	Output	Differential	MIPI CSI data0 negative. Connected to 22nd Pin of MIPI Camera Connector (J19) and 12th Pin of Carrier Expansion Connector (J10).
68	GPIF_P10	Power	0V	General Purpose Pin 10. Connected to 6th Pin of Carrier Expansion Connector (J10). Optionally Connected to Ground through resistor and default not populated.
69	IOUTD/CSI_D1P	Output	Differential	MIPI CSI differential data1 positive. Connected to 12th Pin of MIPI Camera Connector (J19) and to 11th Pin of Carrier Expansion Connector (J10)
70	VGA_TV_BLU	Input	Analog Video Output	VGA_TV Blue Signal. Connected to 10th Pin of VGA Signal Header (J38).
71	GPIF_P6/CSI_D1M	Output	Differential	MIPI CSI differential data1 negative. Connected to 14th Pin of MIPI Camera Connector (J19) and to 10th Pin of Carrier Expansion Connector (J10).
72	GPIF_P11	Power	0V	General Purpose Pin 11.. Connected to 5th Pin of Carrier Expansion Connector (J10). Optionally Connected to Ground through resistor and default not populated.
73	GPIF_P7	Input/Output	3.3V CMOS	General Purpose Pin 7. Connected to 9th Pin of Carrier Expansion Connector (J10).

74	VGA_HSYNC	Input	3.3V CMOS	VGA HSYNC. Connected to 7th Pin of VGA Signal Header (J38) & to 3rd Pin of LPC Header (J34).
75	RFOUT	NC	NC	RFOUT Connected to 8th Pin of Carrier Expansion Connector (J10).
76	VGA_VSYNC	Input	3.3V CMOS	VGA VSYNC. Connected to 9th Pin of VGA Signal Header (J38) & to 4th Pin of LPC Header (J34).
77	GND	Power	0V	Ground.
78	GND	Power	0V	Ground.
79	CSI2_D1	Input/Output	3.3V CMOS	CSI Port2 data bit1. Connected to 23rd Pin of CMOS Camera Connector (J51) & to 4th Pin of Carrier Expansion Connector (J10).
80	CSI2_D0	Input/Output	3.3V CMOS	CSI Port2 data bit0. Connected to 24th Pin of CMOS Camera Connector (J51) & to 3rd Pin of Carrier Expansion Connector (J10).

2.9.1 UART2 Header

The Qseven Generic Carrier Board supports 5 pin UART2 header for external UART interface. UART signals from Expansion connector1 is connected to this header through RS232 transceiver. UART2 header (J45) is physically located at the bottom of the board as shown below.

Number of Pins: 5
Connector Part number: GRPB051VWVN-RC
Mating Connector: LPPB051NFFN-RC from Sullins Connector Solutions
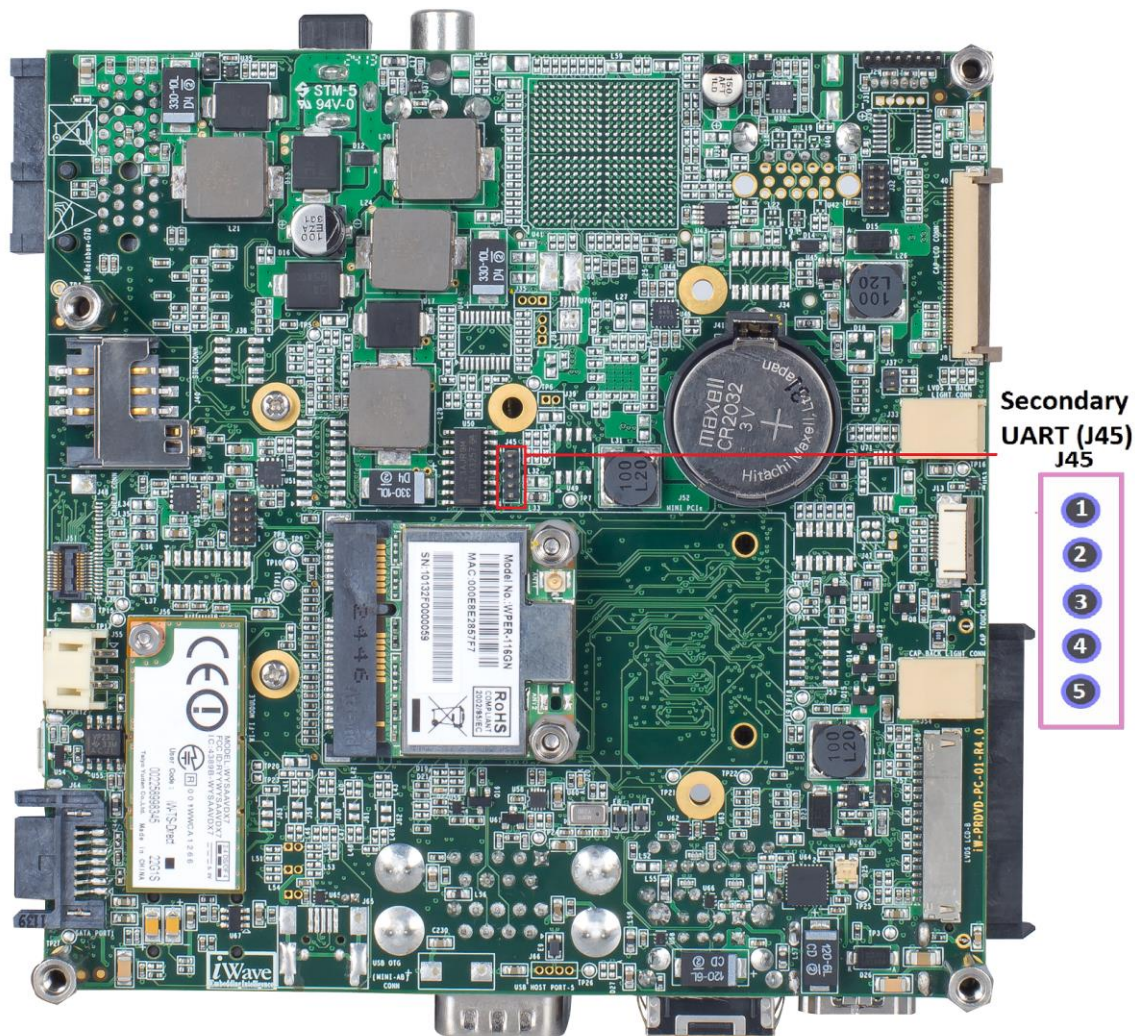
Figure 36: Secondary UART Connector

Table 38: Secondary UART Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	UART2_TXD	Output	RS232	UART2 transmit signal. Connected from 63rd Pin of Expansion Connector1.
2	UART2_CTS	Input	RS232	UART2 Clear to Send. Connected to 62nd Pin of Expansion Connector1.
3	UART2_RXD	Input	RS232	UART2 receive signal. Connected to 60th Pin of Expansion Connector1.
4	UART2_RTS	Output	RS232	UART2 Request to Send. Connected from 61st Pin of Expansion Connector1.
5	GND	Power	0V	Ground.

2.9.2 CAN Port2

CAN Transmit and Receive signals from Expansion connector1 Pin 79 and 78 respectively are connected to CAN transceiver and the output signals from the transceiver are connected to 3Pin CAN Port2 connector (J55). This connector is physically located on top of the board as shown below.

Number of Pins: 3
Connector Part number: S3B-PH-SM4-TB(LF)(SN)
Mating Connector: PHR-3 from JST Sales America Inc
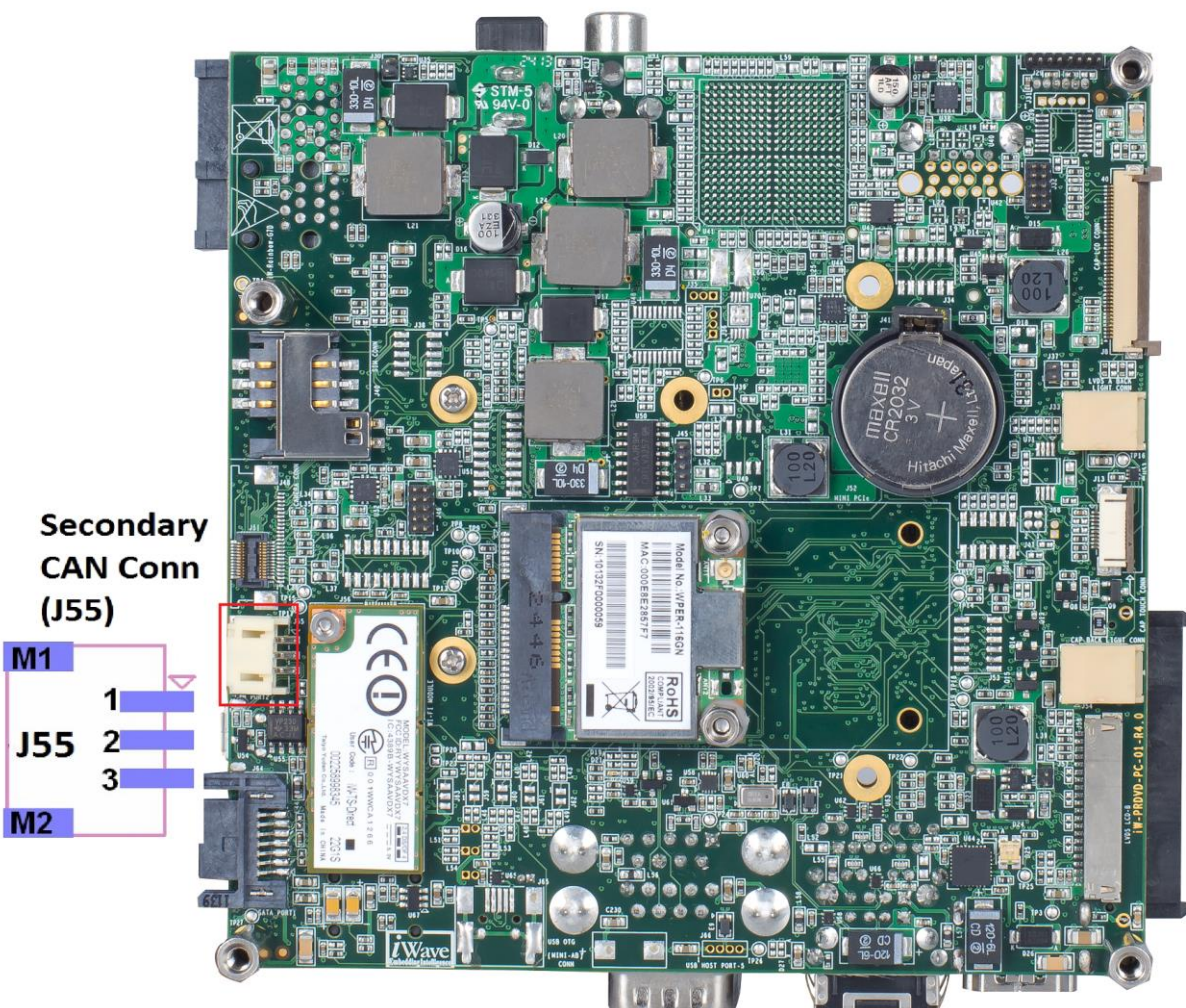
Figure 37: Secondary CAN Connector

Table 39: CAN Port2 Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground.
2	CAN1H	Input	Differential	CAN1 Differential Pair High Side.
3	CAN1L	Input	Differential	CAN1 Differential Pair Low Side.
M1,M2	Mechanical Support	Mechanical Support	Mechanical Support	Mechanical Support.

2.9.3 TV-In RCA Jack

The Qseven Generic Carrier Board supports TV-In interface through On-board TV-In Decoder chip "TVP5150AM1" from Texas Instruments. This decoder chip converts NTSC/PAL composite video input from TV IN RCA jack (J1) to CMOS camera interface signals. This CMOS camera interface signals are connected to CSI port1 pins of Expansion connector1. TV-In RCA Jack (J1) is physically located on top of board as shown below.
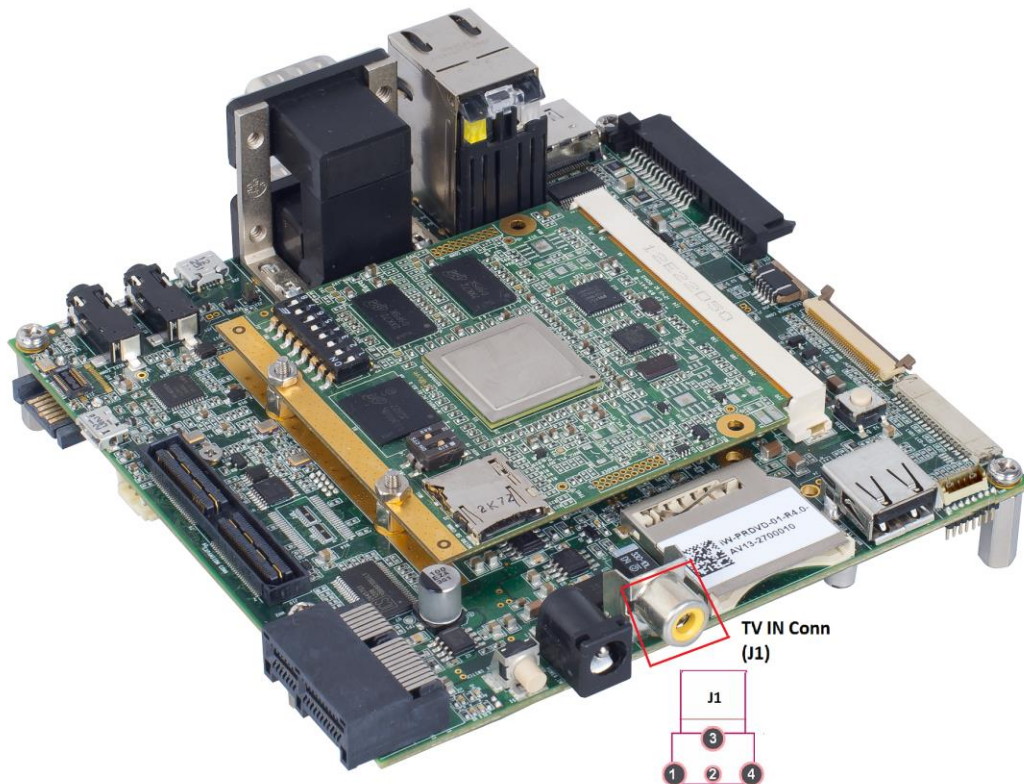
Figure 38: TV-IN Connector

Table 40: TV-In Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground.
2	VIDEO_IN_A	Input	Analog	Analog Video input.
3	GND	Power	0V	Ground.
4	GND	Power	0V	Ground.

2.9.4 CMOS Camera Connector

The Qseven Generic Carrier Board supports 24pin CMOS Camera connector (J51) for CMOS camera interface. This connector supports 8bit CMOS camera interface signals and connected to CSI port2 pins of Expansion connector2 through 2.8V to 3.3V Voltage translator. External reference clock for camera is provided by using on-board 26MHz Oscillator. This Camera connector (J51) is physically located at the bottom of the board as shown below.

Compatible Camera

Part Number: CN003VEF2052
Description: VGA lens of 640x480 pixel CMOS camera based on OV7725 sensor
Manufacturer Name: Global Optics Limited
Global Optics CMOS Camera Web link: http://www.globaloptics.cn/
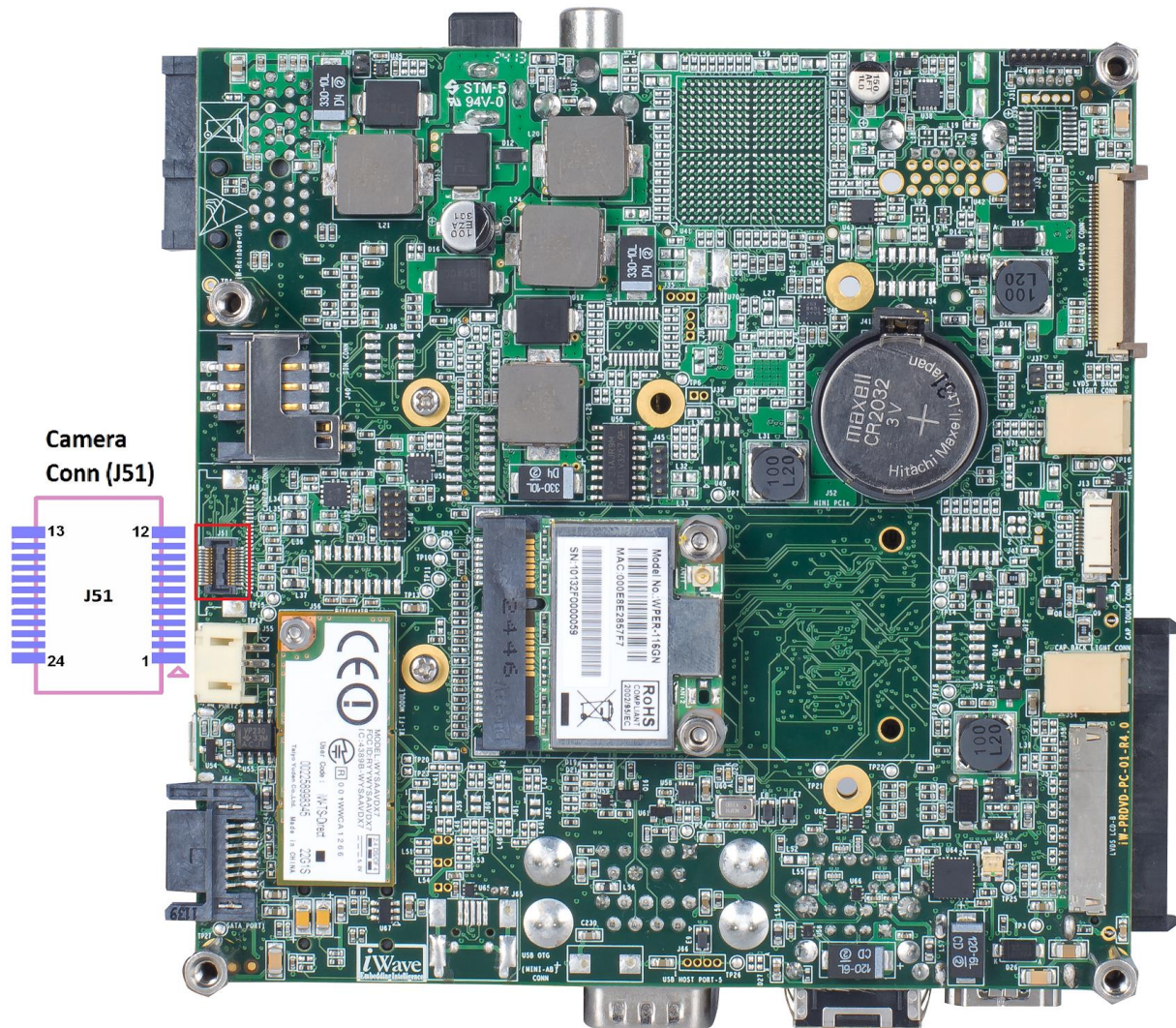
Figure 39: Camera Connector

Table 41: Camera Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	STROBE	NC	NC	No Connection.
2	AGND	Power	0V	Analog Ground.
3	SIOD	Input/Output	2.8V CMOS	I2C Data. Connected to 68th Pin of Qseven MXM Connector through Voltage translator.
4	AVDD	Power	2.8V	Analog Power Supply.
5	SIOC	Output	2.8V CMOS	I2C Clock. Connected to 66th Pin of Qseven MXM Connector through Voltage translator.
6	RESETB	Output	2.8V	Reset Out, Active Low.
7	VSYNC	Input	2.8V CMOS	Vertical Synchronization. Connected to 57th Pin of Expansion Connector2.
8	PWDN	Output	2.8V CMOS	Power Down. Connected to 58th Pin of Expansion Connector1.
9	HREF	Input	2.8V CMOS	Horizontal Synchronization. Connected to 56th Pin of Expansion Connector2.
10	DVDD	Power	1.8V	Digital Power Supply.
11	DOVDD	Power	2.8V	IO Power Supply.
12	D9	Input	2.8V CMOS	Camera Data9. Connected to 55th Pin of Expansion Connector2.

13	XCLK	Output	2.8V CMOS	Camera Reference Clock. Connected to On-board 26Mhz Oscillator. Also this pin is optionally Connected to 67th Pin of Expansion Connector1 through resistor and default not populated.
14	D8	Input	2.8V CMOS	Camera Data8. Connected to 54th Pin of Expansion Connector2.
15	DGND	Power	0V	Digital Ground.
16	D7	Input	2.8V CMOS	Camera Data7. Connected to 52nd Pin of Expansion Connector2.
17	PCLK	Input	2.8V CMOS	Camera Pixel Clock. Connected to 58th Pin of Expansion Connector2.
18	D6	Input	2.8V CMOS	Camera Data6. Connected to 53rd Pin of Expansion Connector2.
19	D2	Input	2.8V CMOS	Camera Data12. Connected to 49th Pin of Expansion Connector2.
20	D5	Input	2.8V CMOS	Camera Data5. Connected to 50th Pin of Expansion Connector2.
21	D3	Input	2.8V CMOS	Camera Data3 Connected to 48th Pin of Expansion Connector2.
22	D4	Input	2.8V CMOS	Camera Data4. Connected to 51st Pin of Expansion Connector2.
23	D1	Input	2.8V CMOS	Camera Data1. Connected to 79th Pin of Expansion Connector2.
24	D0	Input	2.8V CMOS	Camera Data0. Connected to 80th Pin of Expansion Connector2.

2.9.5 MIPI Camera Connector

The Qseven Generic Carrier Board supports 30pin MIPI Camera connector (J19) for MIPI camera interface. This connector supports 2 Lane MIPI camera interface signals and connected to MIPI Interface pins of Expansion connector2. External reference clock for MIPI camera is provided by using on-board 26MHz Oscillator. This Camera connector (J19) is physically located at the bottom of the board as shown below.

Compatible Camera

>   Part Number: LI-OV5640-MIPI-AF
>   Description: 5MegaPixel MIPI Camera based on OV5640 sensor
>   Manufacturer Name: Leopard
>   Leopard's MIPI Camera Web link: https://www.leopardimaging.com/LI-OV5640-MIPI-AF.html
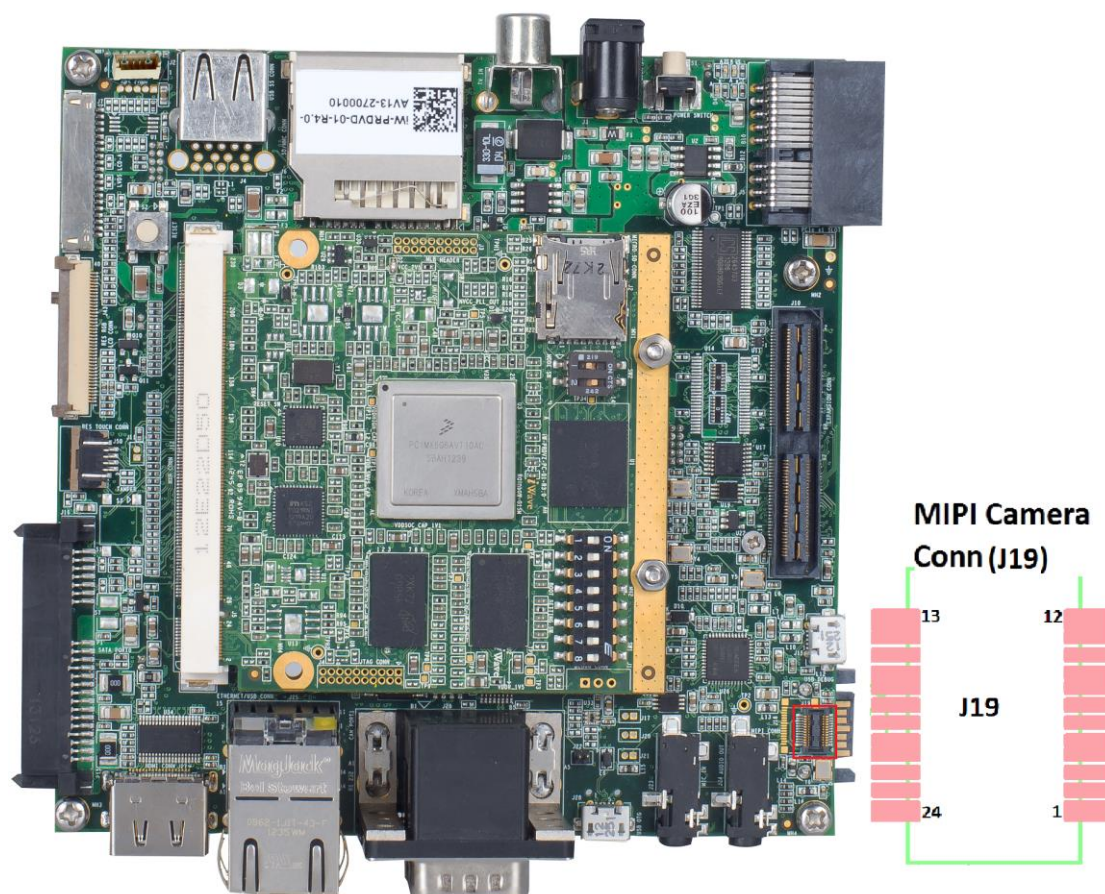
Figure 40: 5MP MIPI Camera connector

Table 42: MIPI Camera Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	Strobe (NC)	NC	NC	No Connection
2	AGND	Power	0V	Analog Ground
3	SDA	Input/Output	1.8V	I2C Data. Connected to 68th Pin of Qseven MXM Connector.
4	AVDD	Power	2.8V	Analog Power 2.8V
5	SCL	Output	1.8V	I2C Clock. Connected to 66th Pin of Qseven MXM Connector.
6	RESET	Output	1.8V/ 10K pull-up	MIPI CSI Reset
7	NC1	NC	NC	No Connection
8	PWDN	Output	1.8V	MIPI CSI Power Down. Connected to 191st Pin of Qseven MXM Connector.
9	NC2	NC	NC	No Connection
10	DVDD	Power	1.5V	Digital Power 1.5V
11	DOVDD	Power	1.8V	Digital Power 1.8V
12	MDP1	Input	Differential	MIPI Lane1 Data Positive. Connected from 69th Pin of Expansion Connector2.
13	XCLK	Output	1.8V	MIPI CSI Master Clock. Connected to on-board 26Mhz Oscillator.
14	MDN1	Input	Differential	MIPI Lane1 Data Negative. Connected from 71st Pin of Expansion Connector2.
15	DGND	Power	0V	Ground.
16	MCP	Input	Differential	MIPI Clock Positive. Connected to 61st Pin of Expansion Connector2.
17	NC3	NC	NC	No Connection

18	MCN	Input	Differential	MIPI Clock Negative. Connected from 63rd Pin of Expansion Connector2.
19	NC4	NC	NC	No Connection
20	MDP0	Input	Differential	MIPI Lane0 Data Positive. Connected to 65th Pin of Expansion Connector2.
21	NC5	NC	NC	No Connection
22	MDN0	Input	Differential	MIPI Lane0 Data Negative. Connected from 67th Pin of Expansion Connector2.
23	AF-VCC	Power	1.8V	MIPI AF Power 1.8V.
24	AF-GND	Power	0V	Analog Field Ground.

2.9.6 Keypad Header

The Qseven Generic Carrier Board supports 10pin keypad interface header (J46) for Keypad interface. This header supports 4X4 keypad interface signals and connected to Expansion connector2. Keypad Header (J46) is physically located at the bottom of board as shown below.

Number of Pins: 10
Connector Part number: GRPB052VWVN-RC
Mating Connector: LPPB052CFFN-RC from Sullins Connector Solutions
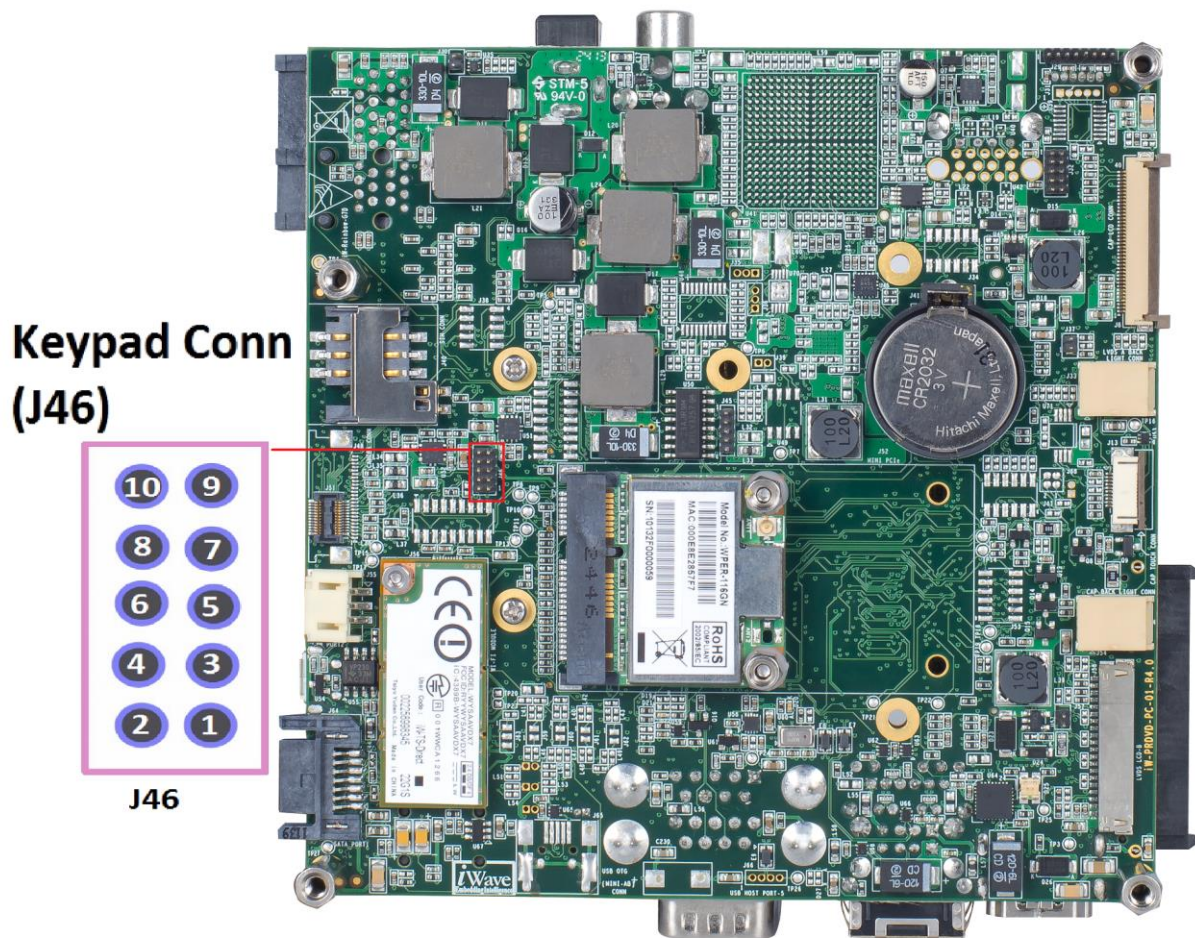
Figure 41: Keypad Connector

Table 43: Keypad Connector Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	KP_ROW0	Input/Output	3.3V CMOS	Keypad Row0. Connected to 7th Pin of Expansion Connector2.
2	KP_ROW1	Input/Output	3.3V CMOS	Keypad Row1. Connected to 8th Pin of Expansion Connector2.
3	KP_ROW2	Input/Output	3.3V CMOS	Keypad Row2. Connected to 9th Pin of Expansion Connector2.
4	KP_ROW3	Input/Output	3.3V CMOS	Keypad Row3. Connected to 10th Pin of Expansion Connector2.
5	GND	Power	0V	Ground.
6	GND	Power	0V	Ground.
7	KP_COL0	Input/Output	3.3V CMOS	Keypad Column0. Connected to 11th Pin of Expansion Connector2.
8	KP_COL1	Input/Output	3.3V CMOS	Keypad Column1. Connected to 12th Pin of Expansion Connector2.
9	KP_COL2	Input/Output	3.3V CMOS	Keypad Column2. Connected to 13th Pin of Expansion Connector2.
10	KP_COL3	Input/Output	3.3V CMOS	Keypad Column3. Connected to 14th Pin of Expansion Connector2.

2.9.7 TV Out Header

NTSC/PAL composite video out signal from Expansion connector2 is connected to 2-pin header to support TV Out interface. This header (J30) is physically is located on the bottom of the board as shown below.

Number of Pins: 2
Connector Part number: GRPB021VWVN-RC
Mating Connector: LPPB021NFFN-RC from Sullins Connector Solutions
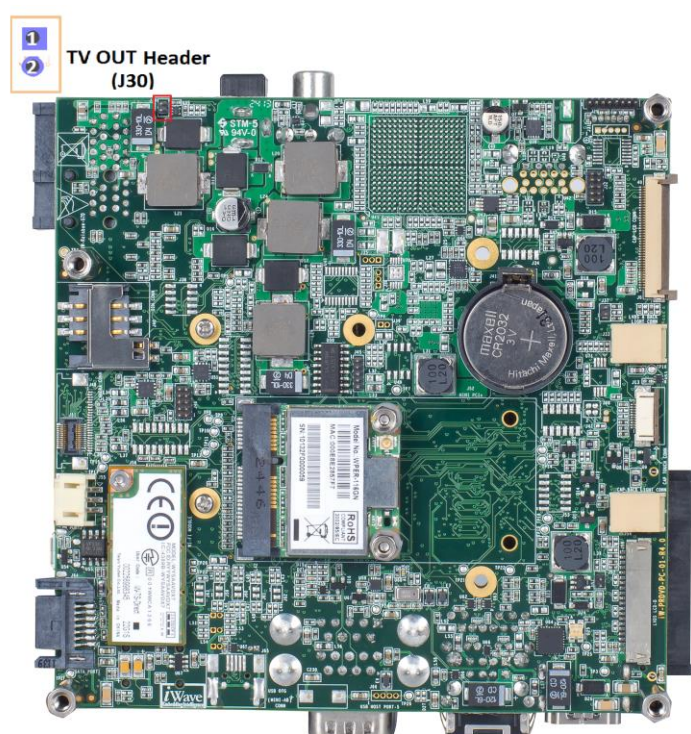
Figure 42: TV Out Interface Header

Table 44: TV Out Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground.
2	VGA_TV_RED	Output	Analog	Composite Video Output. Connected to 62nd Pin of Expansion Connector2.

2.9.8 VGA Interface Header (Optional)

VGA interface signals from the Expansion connector2 is connected to 10-pin SMD pad header (J38).This SMD pads can be accessed at the bottom of the board as shown below. By default this header will not be populated.
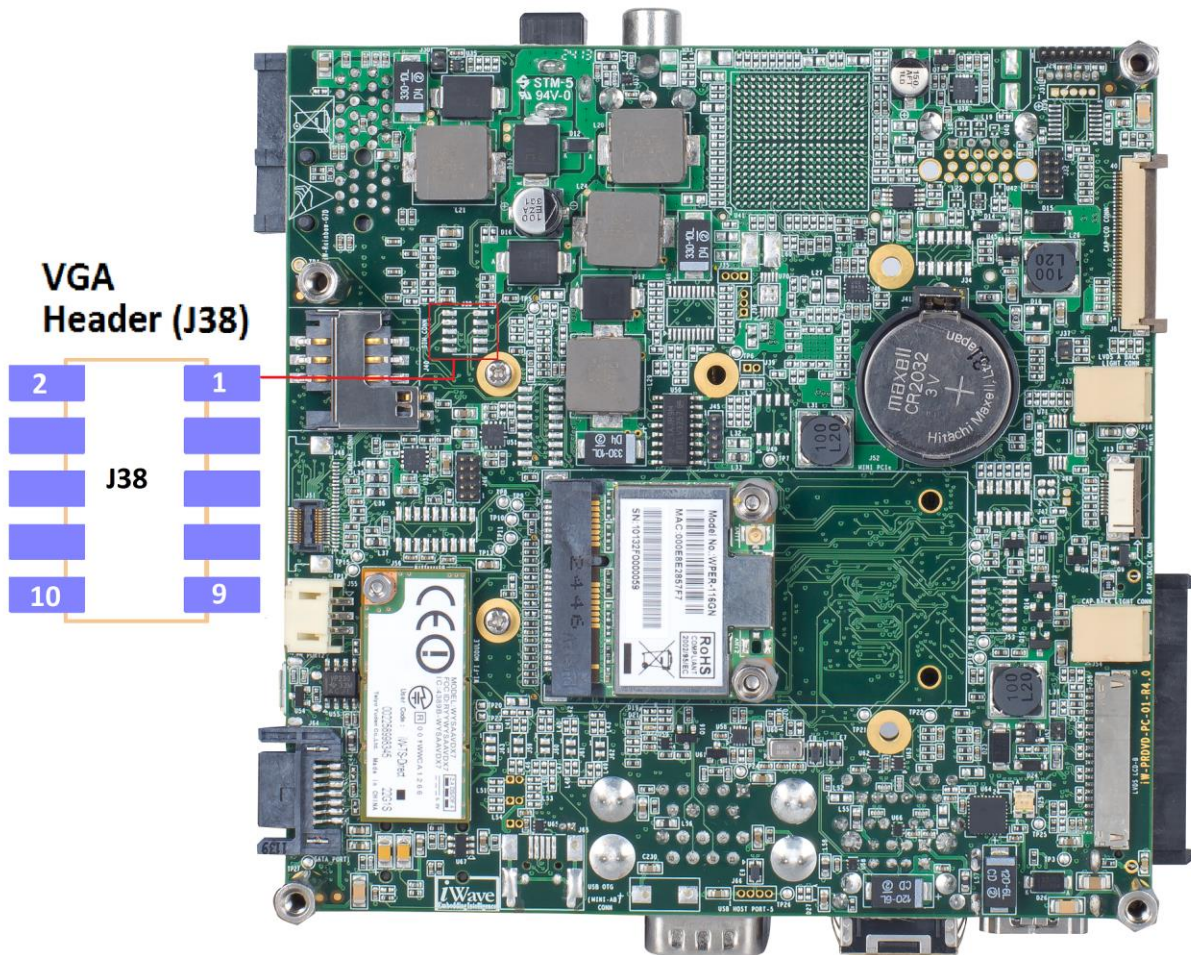
Figure 43: VGA Signal Header

Table 45: VGA Header Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	Expn2_p1	Input/Output	3.3V CMOS	General Purpose Pin. Connected to 1st Pin of Expansion Connector2.
2	Expn2_p2	Input/Output	3.3V CMOS	General Purpose Pin. Connected to 2nd Pin of Expansion Connector2.
3	Expn2_p3	Input/Output	3.3V CMOS	General Purpose Pin. Connected to 3rd Pin of Expansion Connector2.
4	Expn2_p4	Input/Output	3.3V CMOS	General Purpose Pin. Connected to 4th Pin of Expansion Connector2.
5	VGA_TV_GRN	Output	Analog	VGA-Green. Connected to 66th Pin of Expansion Connector2.
6	VGA_TV_RED	Output	Analog	VGA-Red. Connected to 62nd Pin of Expansion Connector2.
7	VGA_HSYNC	Output	Analog	VGA-HSYNC. Connected to 74th Pin of Expansion Connector2.
8	GND	Power	0V	Ground.
9	VGA_VSYNC	Output	Analog	VGA-VSYNC. Connected to 76th Pin of Expansion Connector2.
10	VGA_TV_BLU	Output	Analog	VGA-Blue. Connected to 70th Pin of Expansion Connector2.

2.9.9 Carrier Board Expansion Connector

The Qseven Generic Carrier Board has one 120pin board to board expansion connector for external carrier board expansion. The unused signals from Qseven Module Expansion Connectors are brought to this connector. This Carrier Expansion Connector (J10) is physically located at the top of the board as shown below.

Number of Pins: 120
Connector Part number: QSH-060-01-L-D-A
Mating Connector: QTH-060-02-F-D-A from Samtec Inc
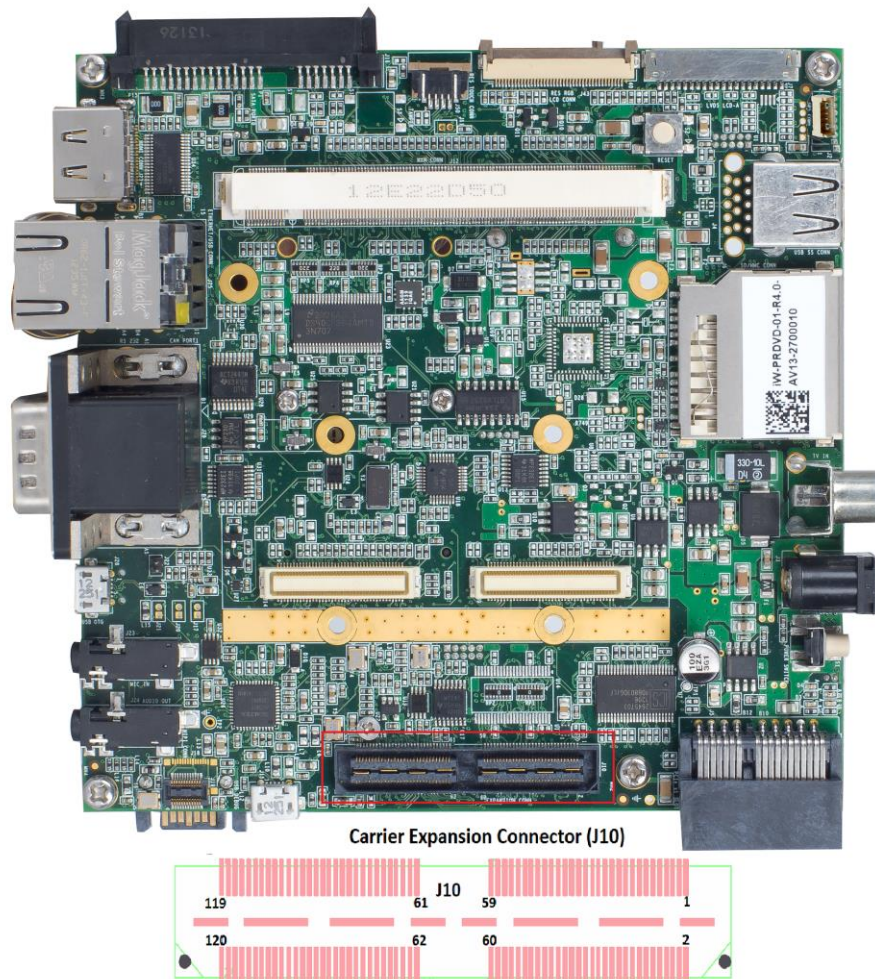
Figure 44: Carrier Expansion Connector

Table 46: Carrier Expansion Connector Pin Outs

Pin No	Signal Name	Signal Type	Voltage Level/ Termination	Description
1	GND	Power	0V	Ground.
2	GND	Power	0V	Ground.
3	GPIF_P13	Input/Output	3.3V CMOS	General Purpose Pin 13. Connected to 80th Pin of Expansion Connector2 (J9).
4	GPIF_P12	Input/Output	3.3V CMOS	General Purpose Pin 12. Connected to 79th Pin of Expansion Connector2 (J9).
5	GPIF_P11	Input/Output	3.3V CMOS	General Purpose Pin 11. Connected to 72nd Pin of Expansion Connector2 (J9).
6	GPIF_P10	Input/Output	3.3V CMOS	General Purpose Pin 10. Connected to 68th Pin of Expansion Connector2 (J9).
7	GPIF_P9	Input/Output	3.3V CMOS	General Purpose Pin 9. Connected to 64th Pin of Expansion Connector2 (J9).
8	GPIF_P8	Input/Output	3.3V CMOS	General Purpose Pin 8. Connected to 75th Pin of Expansion Connector2 (J9).
9	GPIF_P7	Input/Output	3.3V CMOS	General Purpose Pin 7. Connected to 73rd Pin of Expansion Connector2 (J9).
10	GPIF_P6	Input/Output	3.3V CMOS	General Purpose Pin 6. Connected to 71st Pin of Expansion Connector2 (J9).
11	GPIF_P5	Input/Output	3.3V CMOS	General Purpose Pin 5. Connected to 69th Pin of Expansion Connector2 (J9).
12	GPIF_P4	Input/Output	3.3V CMOS	General Purpose Pin 4. Connected to 67th Pin of Expansion Conenctor2 (J9).

13	GPIF_P3	Input/Output	3.3V CMOS	General Purpose Pin 3. Connected to 65th Pin of Expansion Connector2 (J9).
14	GPIF_P2	Input/Output	3.3V CMOS	General Purpose Pin 2. Connected to 63rd Pin of Expansion Connector2 (J9).
15	GPIF_P1	Input/Output	3.3V CMOS	General Purpose Pin 1. Connected to 61st Pin of Expansion Connector2 (J9).
16	GND	Power	0V	Ground.
17	GND	Power	0V	Ground.
18	GPSSI_TXC	Input	3.3V CMOS	SSI Transmit clock. Connected to 45th Pin of Expansion Conenctor2 (J9).
19	GPSSI_TXFS	Output	3.3V CMOS	SSI Transmit Frame. Connected to 43rd Pin of Expansion Conenctor2 (J9).
20	GPSSI_TXD	Output	3.3V CMOS	SSI Transmit. Connected to 44th Pin of Expansion Conenctor2 (J9).
21	GPSSI_RXD	Input	3.3V CMOS	SSI Receive. Connected to 41st Pin of Expansion Conenctor2 (J9).
22	GPEM_EB0	Output	3.3V CMOS	EIM Enable Byte0. Connected to 42nd Pin of Expansion Connector2 (J9).
23	GPEM_EB1	Output	3.3V CMOS	EIM Enable Byte1. Connected to 39th Pin of Expansion Connector2 (J9).
24	GPEM_WAIT	Input	3.3V CMOS	EIM Ready/Busy/Wait. Connected to 40th Pin of Expansion Connector2 (J9).
25	GPEM_BCLK	Output	3.3V CMOS	EIM Burst Clock. Connected to 37th Pin of Expansion Connector2 (J9).
26	GPEM_CRE	Input	3.3V CMOS	EIM Memory Register Set. Connected to 38th Pin of Expansion Connector2 (J9).

27	GPEM_RW	Output	3.3V CMOS	EIM Read/Write Enable. Connected to 35th Pin of Expansion Connector2 (J9).
28	GPEM_CS0	Output	3.3V CMOS	EIM Chip Select0. Connected to 36th Pin of Expansion Connector2 (J9).
29	GND	Power	0V	Ground.
30	GND	Power	0V	Ground.
31	GPEM_DA15	Input/Output	3.3V CMOS	EIM Data & address line 15. Connected to 31st Pin of Expansion Connector2 (J9).
32	GPEM_DA14	Input/Output	3.3V CMOS	EIM Data & address line 14. Connected to 32nd Pin of Expansion Connector2 (J9).
33	GPEM_DA13	Input/Output	3.3V CMOS	EIM Data & address line 13. Connected to 29th Pin of Expansion Connector2 (J9).
34	GPEM_DA12	Input/Output	3.3V CMOS	EIM Data & address line 12. Connected to 30th Pin of Expansion Connector2 (J9).
35	GPEM_DA11	Input/Output	3.3V CMOS	EIM Data & address line 11. Connected to 27th Pin of Expansion Connector2 (J9).
36	GPEM_DA10	Input/Output	3.3V CMOS	EIM Data & address line 10. Connected to 28th Pin of Expansion Connector2 (J9).
37	GPEM_DA9	Input/Output	3.3V CMOS	EIM Data & address line 9. Connected to 25th Pin of Expansion Connector2 (J9).
38	GPEM_DA8	Input/Output	3.3V CMOS	EIM Data & address line 8. Connected to 26th Pin of Expansion Connector2 (J9).
39	GPEM_DA7	Input/Output	3.3V CMOS	EIM Data & address line 7. Connected to 23rd Pin of Expansion Connector2 (J9).
40	GPEM_DA6	Input/Output	3.3V CMOS	EIM Data & address line 6. Connected to 24th Pin of Expansion Connector2 (J9).

41	GPEM_DA5	Input/Output	3.3V CMOS	EIM Data & address line 5. Connected to 21st Pin of Expansion Connector2 (J9).
42	GPEM_DA4	Input/Output	3.3V CMOS	EIM Data & address line 4. Connected to 22nd Pin of Expansion Connector2 (J9).
43	GPEM_DA3	Input/Output	3.3V CMOS	EIM Data & address line 3. Connected to 19th Pin of Expansion Connector2 (J9).
44	GPEM_DA2	Input/Output	3.3V CMOS	EIM Data & address line 2. Connected to 20th Pin of Expansion Connector2 (J9).
45	GPEM_DA1	Input/Output	3.3V CMOS	EIM Data & address line 1. Connected to 17th Pin of Expansion Connector2 (J9).
46	GPEM_DA0	Input/Output	3.3V CMOS	EIM Data & address line 0. Connected to 18th Pin of Expansion Connector2 (J9).
47	GND	Power	0V	Ground.
48	GND	Power	0V	Ground.
49	GPAI_BCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 35th Pin of Expansion Connector1 (J14).
50	GPAI_DATA	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 36th Pin of Expansion Connector1 (J14).
51	GPAI_MCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 33rd Pin of Expansion Connector1 (J14).
52	GPAI_LRCK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 34th Pin of Expansion Connector1 (J14).
53	GPPIN_38	Input/Output	3.3V CMOS	General Purpose Pin 38. Connected to 41st Pin of Expansion Connector1 (J14).

54	GPPIN_PWM2	Output	3.3V CMOS	General Purpose PWM. Connected to 19th Pin of Expansion Connector1 (J14).
55	GPPIN_36	Input/Output	3.3V CMOS	General Purpose Pin 36. Connected to 43rd Pin of Expansion Connector1 (J14).
56	GND	Power	0V	Ground.
57	GPPIN_34	Input/Output	3.3V CMOS	General Purpose Pin 34. Connected to 58th Pin of Expansion Connector1 (J14).
58	GPPIN_35	Input/Output	3.3V CMOS	General Purpose Pin 35. Connected to 38th Pin of Expansion Connector1 (J14).
59	GPPIN_32	Input/Output	3.3V CMOS	General Purpose Pin 32. Connected to 56th Pin of Expansion Conenctor1 (J14).
60	GPPIN_33	Input/Output	3.3V CMOS	General Purpose Pin 33. Connected to 57th Pin of Expansion Conenctor1 (J14).
61	GND	Power	0V	Ground.
62	GND	Power	0V	Ground.
63	GPPIN_31	Input/Output	3.3V CMOS	General Purpose Pin 31. Connected to 55th Pin of Expansion Conenctor1 (J14).
64	GPPIN_30	Input/Output	3.3V CMOS	General Purpose Pin 30. Connected to 31st Pin of Expansion Connector1 (J14).
65	GPPIN_29	Input/Output	3.3V CMOS	General Purpose Pin 29. Connected to 30th Pin of Expansion Connector1 (J14).
66	GPPIN_28	Input/Output	3.3V CMOS	General Purpose Pin 28. Connected to 29th Pin of Expansion Connector1 (J14).
67	GPPIN_27	Input/Output	3.3V CMOS	General Purpose Pin 27. Connected to 28th Pin of Expansion Connector1 (J14).

68	GPPIN_26	Input/Output	3.3V CMOS	General Purpose Pin 26. Connected to 26th Pin of Expansion Connector1 (J14).
69	GPPIN_25	Input/Output	3.3V CMOS	General Purpose Pin 25. Connected to 25th Pin of Expansion Connector1 (J14).
70	GPPIN_24	Input/Output	3.3V CMOS	General Purpose Pin 24. Connected to 24th Pin of Expansion Connector1 (J14).
71	GPPIN_23	Input/Output	3.3V CMOS	General Purpose Pin 23. Connected to 23rd Pin of Expansion Connector1 (J14).
72	GPPIN_22	Input/Output	3.3V CMOS	General Purpose Pin 22. Connected to 22nd Pin of Expansion Connector1 (J14).
73	GPPIN_21	Input/Output	3.3V CMOS	General Purpose Pin 21. Connected to 21st Pin of Expansion Connector1 (J14).
74	GPPIN_20	Input/Output	3.3V CMOS	General Purpose Pin 20. Connected to 20th Pin of Expansion Connector1 (J14).
75	GPPIN_19	Input/Output	3.3V CMOS	General Purpose Pin 19. Connected to 79th Pin of Expansion Conenctor1 (J14).
76	GPPIN_18	Input/Output	3.3V CMOS	General Purpose Pin 18. Connected to 78th Pin of Expansion Conenctor1 (J14).
77	GPPIN_17	Input/Output	3.3V CMOS	General Purpose Pin 17. Connected to 77th Pin of Expansion Connector1 (J14).
78	GPPIN_16	Input/Output	3.3V CMOS	General Purpose Pin 16. Connected to 18th Pin of Expansion Connector1 (J14).
79	GND	Power	0V	Ground.
80	GND	Power	0V	Ground.
81	GPPIN_15	Input/Output	3.3V CMOS	General Purpose Pin 15. Connected to 17th Pin of Expansion Connector1 (J14).

82	GPPIN_14	Input/Output	3.3V CMOS	General Purpose Pin 14. Connected to 16th Pin of Expansion Connector1 (J14).
83	GPPIN_13	Input/Output	3.3V CMOS	General Purpose Pin 15. Connected to 15th Pin of Expansion Connector1 (J14).
84	GPPIN_12	Input/Output	3.3V CMOS	General Purpose Pin 12. Connected to 14th Pin of Expansion Connector1 (J14).
85	GPPIN_11	Input/Output	3.3V CMOS	General Purpose Pin 11. Connected to 13th Pin of Expansion Connector1 (J14).
86	GPPIN_10	Input/Output	3.3V CMOS	General Purpose Pin 10. Connected to 12th Pin of Expansion Connector1 (J14).
87	GPPIN_9	Input/Output	3.3V CMOS	General Purpose Pin 9. Connected to 11th Pin of Expansion Connector1 (J14).
88	GPPIN_8	Input/Output	3.3V CMOS	General Purpose Pin 8. Connected to 10th Pin of Expansion Connector1 (J14).
89	GPPIN_7	Input/Output	3.3V CMOS	General Purpose Pin 7. Connected to 9th Pin of Expansion Connector1 (J14).
90	GPPIN_6	Input/Output	3.3V CMOS	General Purpose Pin 6. Connected to 8th Pin of Expansion Connector1 (J14).
91	GPPIN_5	Input/Output	3.3V CMOS	General Purpose Pin 5. Connected to 7th Pin of Expansion Connector1 (J14).
92	GPPIN_4	Input/Output	3.3V CMOS	General Purpose Pin 4. Connected to 6th Pin of Expansion Connector1 (J14).
93	GPPIN_3	Input/Output	3.3V CMOS	General Purpose Pin 3. Connected to 5th Pin of Expansion Connector1 (J14).

94	GPPIN_2	Input/Output	3.3V CMOS	General Purpose Pin 2. Connected to 4th Pin of Expansion Connector1 (J14).
95	GPPIN_1	Input/Output	3.3V CMOS	General Purpose Pin 1. Connected to 3rd Pin of Expansion Connector1 (J14).
96	GPPIN_0	Input/Output	3.3V CMOS	General Purpose Pin 0. Connected to 2nd Pin of Expansion Connector1 (J14).
97	GND	Power	0V	Ground.
98	GND	Power	0V	Ground.
99	GPAO_MCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 48th Pin of Expansion Connector1 (J14).
100	GPAO_LRCK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 47th Pin of Expansion Connector1 (14).
101	GPAO_BCLK	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 46th Pin of Expansion Connector1 (14).
102	GPAO_DATA	Input/Output	3.3V CMOS	General Purpose Interface. Connected to 45th Pin of Expansion Connector1 (14).
103	GND	Power	0V	Ground.
104	GND	Power	0V	Ground.
105	NC_USB_P7-	Input/Output	Differential	USB Host Port7 Data negative. Connected to 75th Pin of Qseven MXM Connector (J12) through resistor.
106	NC_USB_P6-	Input/Output	Differential	USB Host Port6 Data negative. Connected to 76th Pin of Qseven MXM Connector (J12) through resistor.
107	NC_USB_P7+	Input/Output	Differential	USB Host Port7 Data positive. Connected to 77th Pin of Qseven MXM Connector (J12) through resistor.
108	NC_USB_P6+	Input/Output	Differential	USB Host Port6 Data positive. Connected to 78th Pin of Qseven MXM Connector (J12) through resistor.
109	GND	Power	0V	Ground.

110	GND	Power	0V	Ground.
111	NC_USB_P5-	Input/Output	Differential	USB Host Port5 Data Negative. Connected to 81st Pin of Qseven MXM Connector (J12) through resistor.
112	USB_4_5_OC#	Input	3.3V CMOS	Over current sense for USB port 4 & 5. Connected to 80th Pin of Qseven MXM Connector (J12) through resistor.
113	NC_USB_P5+	Input/Output	Differential	USB Host Port5 Data Positive. Connected to 83rd Pin of Qseven MXM Connector (J12) through resistor.
114	NC_USB_6_7_OC#	Input	3.3V CMOS	Over current sense for USB ports 6 & 7. Connected to 79th Pin of Qseven MXM Connector (J12) through resistor.
115	GND	Power	0V	Ground.
116	GND	Power	0V	Ground.
117	VCC_5V	Power	5V	VCC Power Supply, 5V.
118	VCC_5V	Power	5V	VCC Power Supply, 5V.
119	VCC_5V	Power	5V	VCC Power Supply, 5V.
120	VCC_5V	Power	5V	VCC Power Supply, 5V.

Note: Carrier Board Expansion connector pin-out details of all iWave's Qseven CPU Modules are mentioned in the **APPENDIX II** *section.*

3   ELECTRICAL SPECIFICATION

3.1   Qseven Generic Carrier Board Power Input Requirement

The Qseven Generic Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Qseven Generic Carrier Board through Power Jack (J3). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed on the top of the board as shown below.
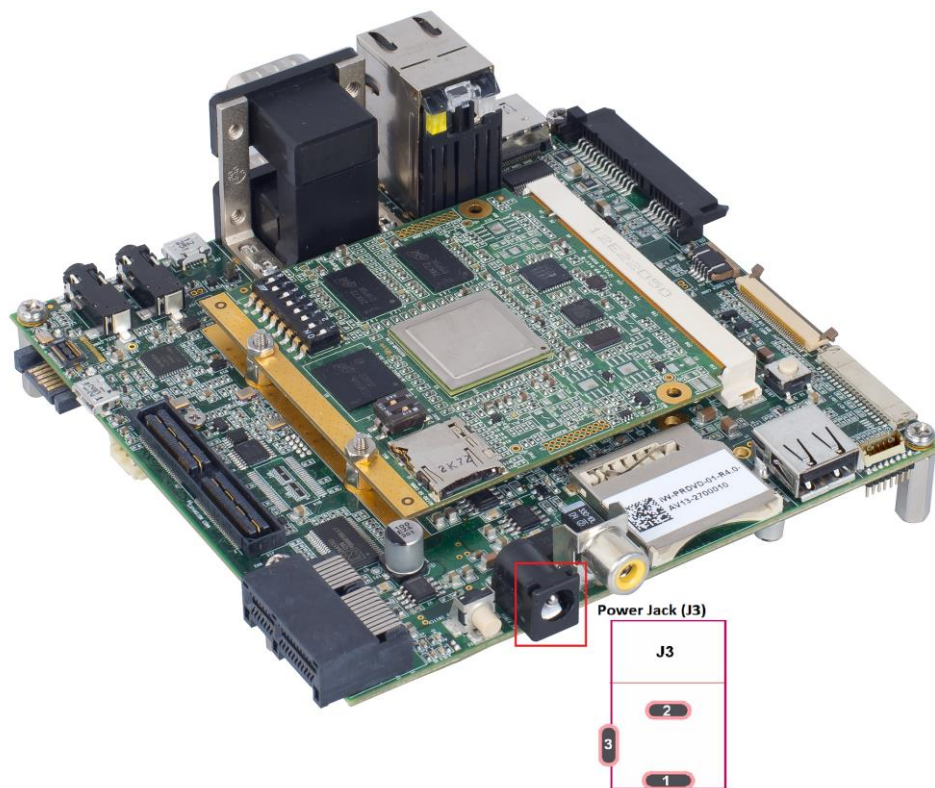
Figure 45: Power Jack

Table 47: Power Jack Pin Out

Pin No	Pin Name	Signal Type	Voltage Level/ Termination	Description
1	12V	Power	12V	Positive Terminal.
2	Ground	Power	0V	Negative Terminal.
3	Ground	Power	0V	Negative Terminal.

3.2   Power Output to Qseven CPU Module

The Qseven Generic Carrier Board provides all the necessary power to Qseven CPU Modules as mentioned in the Qseven Specification. Qseven CPU modules require +5V (VCC) as a Main power input and two optional power rails for +5V standby voltage & +3V RTC supply voltage.

Table 48: Power Output to Qseven CPU Modules

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)
1	VCC	4.75V	5V	5.25V
2	VCC_5V_SB	4.75V	5V	5.25V
3	VCC_RTC	-	3V	-

The Qseven Generic Carrier Board Power Output sequencing to Qseven CPU modules are explained below.
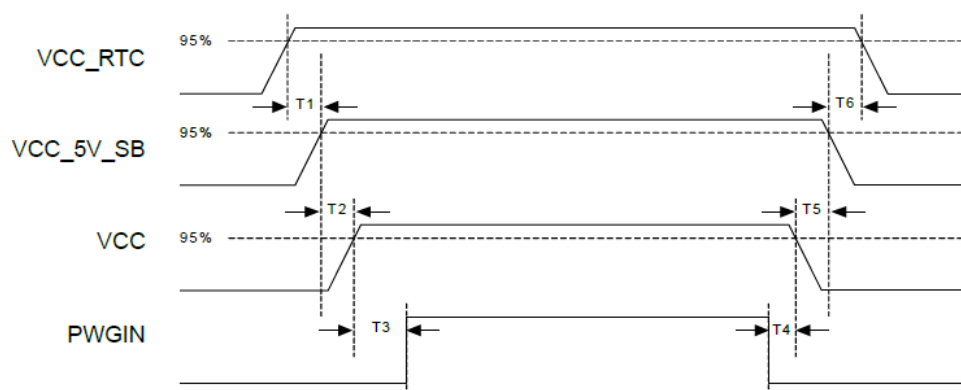
Figure 46: Power Sequence to Qseven CPU Module

Table 49: Power Sequence Timing to Qseven CPU Module

Item		Description	Value
Power Up Sequence	T1	VCC_RTC rise time to VCC_5V_SB rise time	≥ 0 ms
	T2	VCC_5V_SB rise time to VCC rise time	0 ms
	T3	VCC rise time to PWGIN rise time	0 ms
Power Down Sequence	T4	PWGIN fall time to VCC fall time	0 ms
	T5	VCC fall time to VCC_5V_SB fall time	0 ms
	T6	VCC_5V_SB fall time to VCC_RTC fall time	≥ 0 ms

Note: PWGIN is the Power Good output to Qseven CPU module. This pin is default pulled to VCC_5V_SB power in Qseven Generic Carrier Board. Generic Carrier Board also optionally supports Power Good circuit and default not populated.

4   MECHANICAL SPECIFICATION

Qseven Generic Carrier Board PCB form factor is Nano-ITX with size of 120 × 120 mm (4.7inch × 4.7 inch). Qseven Generic Carrier Board PCB dimension with Mounting hole placement detail is shown in the below figure.
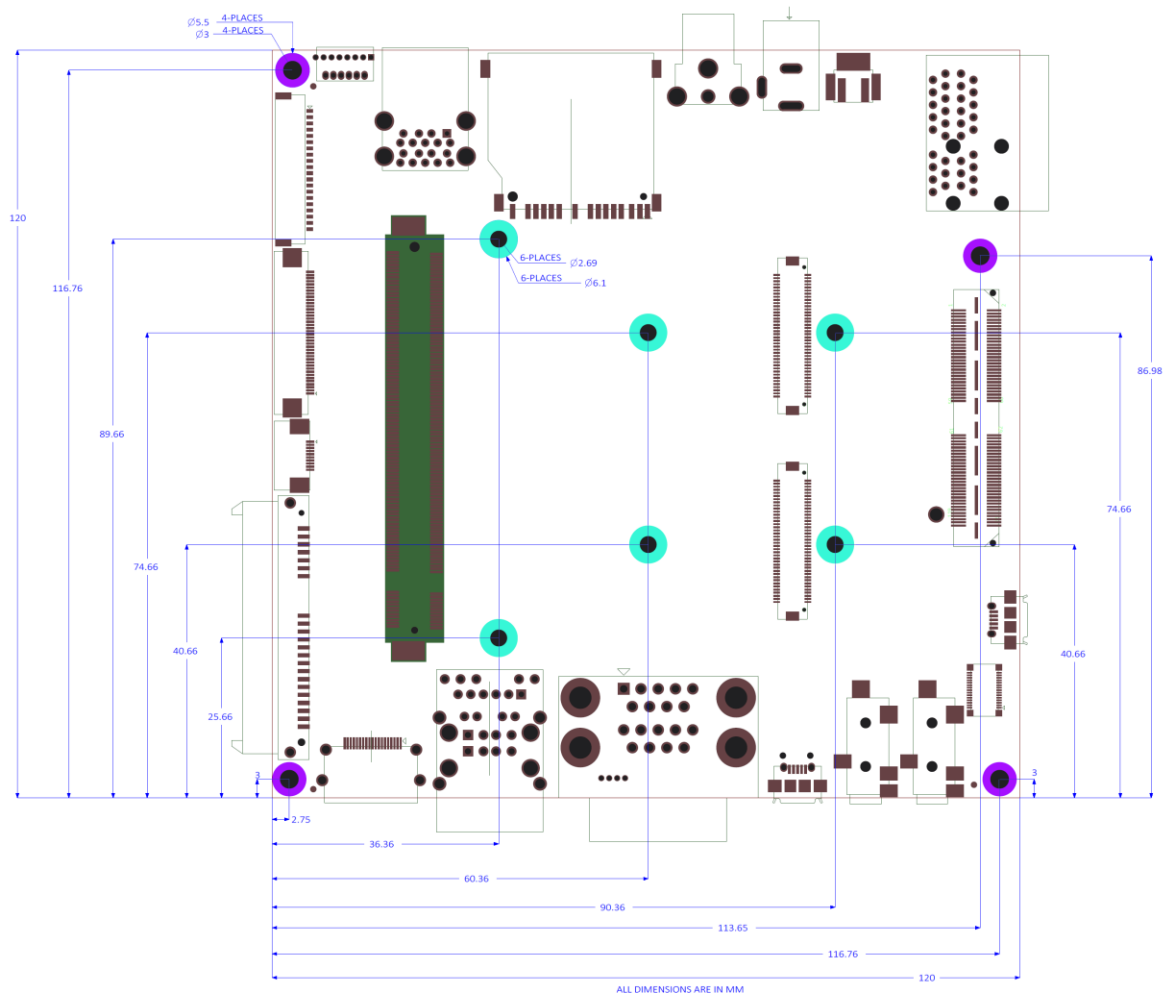
Figure 47: Board Mechanical Dimension

5   APPENDIX I

5.1   Generic Qseven Carrier Board PCB Silk Screen

Generic Qseven Carrier Board PCB silkscreen top view and bottom view with Optional Feature's Identifier highlighted are shown in the below Figures. This will be useful while mounting the Optional Features in Qseven Carrier board.

Figure 48: PCB Silkscreen Top
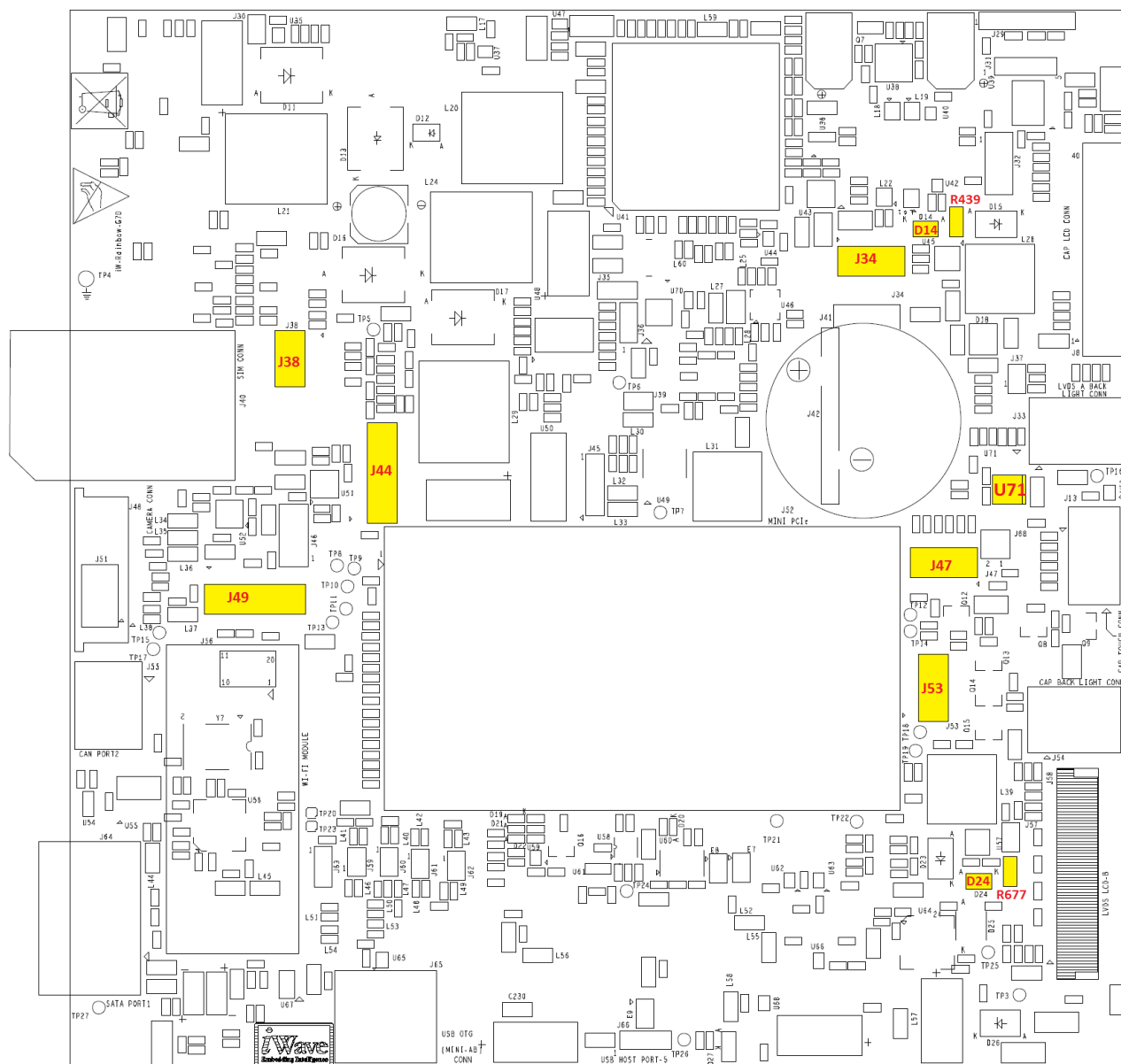
Figure 49: PCB Silkscreen Bottom

6   APPENDIX II

The Qseven Generic Carrier Board Expansion connector pin-out for all iWave's Qseven CPU Modules is mentioned in below Tables.

6.1   Expansion Pin-out based on i.MX6 SOM

Table 50: Carrier Board Expansion Connector pin-out based on i.MX6 SOM

Pin No	Pin Name based on i.MX6 SOM	Pin Connection	Signal Type	Voltage Level/ Termination	Description
1	GND	GND	Power	0V	Ground.
2	GND	GND	Power	0V	Ground.
3	CSI_D3M	Connected to 80th Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data3 negative.
4	CSI_D3P	Connected to 79th Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data3 positive.
5	SD4_DAT1	Connected to 72nd Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	General Purpose I/O.
6	UART4_RXD (KEY_ROW0)	Connected to 68th Pin of Expansion Connector 2	Input	3.3V CMOS	UART4 Receive data line.
7	UART4_TXD (KEY_COL0)	Connected to 64th Pin of Expansion Connector 2	Output	3.3V CMOS	UART4 Transmit data line.
8	CSI_D2M	Connected to 75th Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data2 negative.
9	CSI_D2P	Connected to 73rd Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data2 positive.
10	CSI_D1M	Connected to 71st Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data1 negative.
11	CSI_D1P	Connected to 69th Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data1 positive.
12	CSI_D0M	Connected to 67th Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data0 negative.
13	CSI_D0P	Connected to 65th Pin of Expansion Connector 2	Input	Differential	MIPI CSI differential data0 positive.
14	CSI_CLK0M	Connected to 63rd Pin of Expansion Connector 2	Input	3.3V CMOS	MIPI CSI differential clock negative.
15	CSI_CLK0P	Connected to 61st Pin of Expansion Connector 2	Input	3.3V CMOS	MIPI CSI differential clock positive.
16	GND	GND	Power	0V	Ground.

17	GND	GND	Power	0V	Ground.
18	DI0_PIN15	Connected to 45th Pin of Expansion Connector 2	Output	3.3V CMOS	Parallel LCD Data Enable (DRDY).
19	DI0_PIN3	Connected to 43rd Pin of Expansion Connector 2	Output	3.3V CMOS	Parallel LCD Vsync.
20	DI0_PIN2	Connected to 44th Pin of Expansion Connector 2	Output	3.3V CMOS	Parallel LCD Hsync.
21	DI0_PIN4	Connected to 41st Pin of Expansion Connector 2	Output	3.3V CMOS	Parallel LCD Contrast control.
22	EIM_EB0	Connected to 42nd Pin of Expansion Connector 2	Output	3.3V CMOS	EIM Enable Byte0.
23	EIM_EB1	Connected to 39th Pin of Expansion Connector 2	Output	3.3V CMOS	EIM Enable Byte1.
24	EIM_WAIT	Connected to 40th Pin of Expansion Connector 2	Input	3.3V CMOS	EIM Ready/Busy/Wait.
25	EIM_BCLK	Connected to 37th Pin of Expansion Connector 2	Output	3.3V CMOS	EIM Burst Clock.
26	EIM_CRE (NANDF_CS2)	Connected to 38th Pin of Expansion Connector 2	Output	3.3V CMOS	EIM Memory Register Set.
27	EIM_RW	Connected to 35th Pin of Expansion Connector 2	Output	3.3V CMOS	EIM Read/Write Enable.
28	EIM_CS0	Connected to 36th Pin of Expansion Connector 2	Output	3.3V CMOS	EIM Chip Select0.
29	GND	GND	Power	0V	Ground.
30	GND	GND	Power	0V	Ground.
31	EIM_DA15	Connected to 31st Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 15.
32	EIM_DA14	Connected to 32nd Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 14.
33	EIM_DA13	Connected to 29th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 13.
34	EIM_DA12	Connected to 30th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 12.
35	EIM_DA11	Connected to 27th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 11.
36	EIM_DA10	Connected to 28th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 10.
37	EIM_DA9	Connected to 25th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 9.

38	EIM_DA8	Connected to 26th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 8.
39	EIM_DA7	Connected to 23rd Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 7.
40	EIM_DA6	Connected to 24th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 6.
41	EIM_DA5	Connected to 21st Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 5.
42	EIM_DA4	Connected to 22nd Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 4.
43	EIM_DA3	Connected to 19th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 3.
44	EIM_DA2	Connected to 20th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 2.
45	EIM_DA1	Connected to 17th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 1.
46	EIM_DA0	Connected to 18th Pin of Expansion Connector 2	Input/ Output	3.3V CMOS	EIM Data & address line 0.
47	GND	GND	Power	0V	Ground.
48	GND	GND	Power	0V	Ground.
49	DISP0_DAT20	Connected to 35th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data20 (Red Data4).
50	DISP0_DAT19	Connected to 36th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data19 (Red Data3).
51	DISP0_DAT21	Connected to 33rd Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data21 (Red Data5).
52	DISP0_DAT16	Connected to 34th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data16 (Red Data0).
53	DISP0_DAT2	Connected to 41st Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data2 (Blue Data2).
54	PWM2_PWMO(GPIO_1)	Connected to 19th Pin of Expansion Connector 1	Output	3.3V CMOS	PWM2 output.
55	DISP0_DAT1	Connected to 43rd Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data1 (Blue Data1).
56	GND	GND	Power	0V	Ground.
57	DSI_D0M	Connected to 58th Pin of Expansion Connector 1	Output	Differential	MIPI DSI differential data negative.
58	DISP0_DAT11	Connected to 38th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data11 (Green Data3).
59	DSI_D0P	Connected to 56th Pin of	Output	Differential	MIPI DSI differential data

		Expansion Connector 1			Positive.
60	DSI_CLK0M	Connected to 57th Pin of Expansion Connector 1	Output	Differential	MIPI DSI differential clock negative.
61	GND	GND	Power	0V	Ground.
62	GND	GND	Power	0V	Ground.
63	DSI_CLK0P	Connected to 55th Pin of Expansion Connector 1	Output	Differential	MIPI DSI differential clock positive.
64	DISP0_DAT13	Connected to 31st Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data13 (Green Data5).
65	DISP0_DAT4	Connected to 30th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data4 (Blue Data 4).
66	DISP0_DAT10	Connected to 29th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data10 (Green Data2.)
67	DISP0_DAT3	Connected to 28th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data3 (Blue Data 3).
68	DISP0_DAT0	Connected to 26th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data0 (Blue Data0).
69	DISP0_DAT5	Connected to 25th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data5 (Blue Data5).
70	DISP0_DAT7	Connected to 24th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data7 (Blue Data7).
71	DISP0_DAT9	Connected to 23rd Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data9 (Green Data1).
72	DISP0_DAT12	Connected to 22nd Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data12 (Green Data4).
73	DISP0_DAT14	Connected to 21st Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data14 (Green Data6).
74	DISP0_DAT17	Connected to 20th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data17 (Red Data1).
75	CAN2_TX (KEY_COL4)	Connected to 79th Pin of Expansion Connector 1	Output	3.3V CMOS	CAN channel2 Transmit line.
76	CAN2_RX (KEY_ROW4)	Connected to 78th Pin of Expansion Connector 1	Input	3.3V CMOS	CAN channel2 Receive line.
77	DI0_DISP_CLK	Connected to 77th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Clock.
78	ESAI_HCKT (ENET_RXD0)	Connected to 18th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI High Frequency Clock for Transmitter.
79	GND	GND	Power	0V	Ground.
80	GND	GND	Power	0V	Ground.
81	SPDIF_OUT1 (GPIO_19)	Connected to 17th Pin of Expansion Connector 1	Output	3.3V CMOS	SPDIF output line.

82	ESAI_FST (ENET_RXD1)	Connected to 16th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI Frame Sync for Transmitter.
83	SPDIF_IN1 (GPIO_16)	Connected to 15th Pin of Expansion Connector 1	Input	3.3V CMOS	SPDIF input line.
84	ESAI_SCKT(ENET_CRS_DV)	Connected to 14th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI Transmitter Serial Clock.
85	ESAI_TX0 (GPIO_17)	Connected to 13th Pin of Expansion Connector 1	Output	3.3V CMOS	ESAI Serial Transmit0 Data.
86	PWM2_PWMO(GPIO_1)	Connected to 12th Pin of Expansion Connector 1	Output	3.3V CMOS	PWM2 Output.
87	ESAI_TX1 (GPIO_18)	Connected to 11th Pin of Expansion Connector 1	Output	3.3V CMOS	ESAI Serial Transmit1 Data.
88	ESAI_HCKR (GPIO_3)	Connected to 10th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	General Purpose Pin 3.
89	ESAI_TX3_RX2 (ENET_TX_EN)	Connected to 9th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI Serial Transmit3/Receive2 Data.
90	ESAI_FSR (GPIO_9)	Connected to 8th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	General Purpose Pin 9.
91	ESAI_TX2_RX3 (ENET_TXD1)	Connected to 7th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI Serial Transmit2/Receive3 Data.
92	DISP0_DAT18	Connected to 6th Pin of Expansion Connector 1	Output	3.3V CMOS	LCD Data 18 (Red Data 2).
93	ESAI_TX4_RX1 (ENET_TXD0)	Connected to 5th Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI Serial Transmit4/Receive1 Data.
94	DISP0_DAT22	Connected to 4th Pin of Expansion Connector 1	Output	3.3V CMOS	LCD Data 22 (Red Data 6).
95	ESAI_TX5_RX0 (GPIO_8)	Connected to 3rd Pin of Expansion Connector 1	Input/ Output	3.3V CMOS	ESAI Serial Transmit5/Receive0 Data.
96	DISP0_DAT23	Connected to 2nd Pin of Expansion Connector 1	Output	3.3V CMOS	LCD Data 23 (Red Data 7).
97	GND	GND	Power	0V	Ground.
98	GND	GND	Power	0V	Ground.
99	DSI_D1M	Connected to 48th Pin of Expansion Connector 1	Output	Differential	MIPI DSI differential data1 negative.
100	DISP0_DAT15	Connected to 47th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data15 (Green Data7).
101	DSI_D1P	Connected to 46th Pin of Expansion Connector 1	Output	Differential	MIPI DSI differential data1 positive.
102	DISP0_DAT8	Connected to 45th Pin of Expansion Connector 1	Output	3.3V CMOS	Parallel LCD Data8 (Green Data0).
103	GND	GND	Power	0V	Ground.

104	GND	GND	Power	0V	Ground.
105	NC	Connected to 75th Pin of Qseven Edge Connector	NC	NC	No Connection.
106	NC	Connected to 76th Pin of Qseven Edge Connector	NC	NC	No Connection.
107	NC	Connected to 77th Pin of Qseven Edge Connector	NC	NC	No Connection.
108	NC	Connected to 78th Pin of Qseven Edge Connector	NC	NC	No Connection.
109	GND	GND	Power	0V	Ground.
110	GND	GND	Power	0V	Ground.
111	NC	Connected to 81st Pin of Qseven Edge Connector	NC	NC	No Connection.
112	USB_4_5_OC	Connected to 80th Pin of Qseven Edge Connector	Input	3.3V CMOS	Over current sense for USB port 4 & 5.
113	NC	Connected to 83rd Pin of Qseven Edge Connector	NC	NC	No Connection.
114	NC	Connected to 79th Pin of Qseven Edge Connector	NC	NC	No Connection.
115	GND	GND	Power	0V	Ground.
116	GND	GND	Power	0V	Ground.
117	Power	VCC_5V	Power	5V	VCC Power Supply.
118	Power	VCC_5V	Power	5V	VCC Power Supply.
119	Power	VCC_5V	Power	5V	VCC Power Supply.
120	Power	VCC_5V	Power	5V	VCC Power Supply.

6.2 Expansion Pin-out based on AM389x SOM

Table 51: Carrier Board Expansion Connector pin-out based on AM389x SOM

Pin No	Pin Name based on AM389x SOM	Pin Connection	Signal Type	Voltage Level/ Termination	Description
1	GND	GND	Power	0V	Ground.
2	GND	GND	Power	0V	Ground.
3	NC	Connected to 80th Pin of Expansion Connector 2	NC	NC	No Connection.
4	NC	Connected to 79th Pin of Expansion Connector 2	NC	NC	No Connection.
5	GND	Connected to 72nd Pin of Expansion Connector 2	Power	0V	Ground.
6	GND	Connected to 68th Pin of Expansion Connector 2	Power	0V	Ground.
7	GND	Connected to 64th Pin of Expansion Connector 2	Power	0V	Ground.
8	RFOUT	Connected to 75th Pin of Expansion Connector 2	Analog	3.3V	RF Out Analog Signal.
9	IOUTG	Connected to 73rd Pin of Expansion Connector 2	Analog	3.3V	TV Out Analog Signal.
10	NC	Connected to 71st Pin of Expansion Connector 2	NC	NC	No Connection.
11	IOUTD	Connected to 69th Pin of Expansion Connector 2	Analog	3.3V	TV Out Analog Signal.
12	NC	Connected to 67th Pin of Expansion Connector 2	NC	NC	No Connection.
13	IOUTE	Connected to 65th Pin of Expansion Connector 2	Analog	3.3V	TV Out Analog Signal.
14	NC	Connected to 63rd Pin of Expansion Connector 2	NC	NC	No Connection.
15	IOUTF	Connected to 61st Pin of Expansion Connector 2	Analog	3.3V	TV Out Analog Signal.
16	GND	GND	Power	0V	Ground.
17	GND	GND	Power	0V	Ground.
18	MDIO_MDCLK	Connected to 45th Pin of Expansion Connector 2	Output	3.3V	Ethernet Clock.
19	EMAC1_TXD4	Connected to 43rd Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 4.

20	EMAC1_GMTCLK	Connected to 44th Pin of Expansion Connector 2	Output	3.3V	Ethernet Clock.
21	MCA1_AXR0	Connected to 41st Pin of Expansion Connector 2	Input	3.3V	McASP Audio Port1.
22	EMAC1_RXD0	Connected to 42nd Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 0.
23	EMAC1_TXD7	Connected to 39th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 7.
24	EMAC1_RXD2	Connected to 40th Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 2.
25	EMAC1_TXD5	Connected to 37th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 5.
26	EMAC1_RXDV	Connected to 38th Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data Valid Input.
27	EMAC1_TXEN	Connected to 35th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Enable.
28	MDIO_MDIO	Connected to 36th Pin of Expansion Connector 2	Input/Output	3.3V	Ethernet MDIO.
29	GND	GND	Power	0V	Ground.
30	GND	GND	Power	0V	Ground.
31	EMAC1_RXCLK	Connected to 31st Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Clock.
32	EMAC1_RXD6	Connected to 32nd Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 6.
33	EMAC1_RXD5	Connected to 29th Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 5.
34	EMAC1_TXD6	Connected to 30th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 6.
35	EMAC1_RXD1	Connected to 27th Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 1.
36	EMAC1_RXD4	Connected to 28th Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 4.
37	EMAC1_COL	Connected to 25th Pin of Expansion Connector 2	Input	3.3V	Ethernet Column.
38	EMAC1_TXCLK	Connected to 26th Pin of Expansion Connector 2	Input	3.3V	Ethernet Transmit Clock.
39	EMAC1_RXD3	Connected to 23rd Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 3.

40	EMAC1_TXD3	Connected to 24th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 3.
41	EMAC1_RXD7	Connected to 21st Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Data 7.
42	EMAC1_TXD2	Connected to 22nd Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 2.
43	EMAC1_CRS	Connected to 19th Pin of Expansion Connector 2	Input	3.3V	Ethernet CRS.
44	EMAC1_TXD1	Connected to 20th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 1.
45	EMAC1_RXER	Connected to 17th Pin of Expansion Connector 2	Input	3.3V	Ethernet Receive Error.
46	EMAC1_TXD0	Connected to 18th Pin of Expansion Connector 2	Output	3.3V	Ethernet Transmit Data 0.
47	GND	GND	Power	0V	Ground.
48	GND	GND	Power	0V	Ground.
49	VIN[0]A_D[10]	Connected to 35th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 10.
50	VIN[0]A_D[12]	Connected to 36th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 12.
51	VIN[0]A_D[9]	Connected to 33rd Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 9.
52	VIN[0]A_D[11]	Connected to 34th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 11.
53	GP0[27]	Connected to 41st Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 27.
54	TIM7_OUT	Connected to 19th Pin of Expansion Connector 1	Output	3.3V	PMW output.
55	UART0_RINn/ GP1[19]	Connected to 43rd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 19.
56	GND	GND	Power	0V	Ground.
57	GP0[18]	Connected to 58th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 18.
58	GP1[22]	Connected to 38th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 22.
59	GP0[7]	Connected to 56th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 7.
60	GP1[21]	Connected to 57th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 21.

61	GND	GND	Power	0V	Ground.
62	GND	GND	Power	0V	Ground.
63	GP1[20]	Connected to 55th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 20.
64	GP0[26]	Connected to 31st Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 26.
65	UART0_DTRn/ GP1[16]	Connected to 30th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 16.
66	UART0_RTSn/ GP1[27]	Connected to 29th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 27.
67	UART0_DCD/ GP1[18]	Connected to 28th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 18.
68	UART0_CTSn/ GP1[28]	Connected to 26th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 28.
69	SATA_ACT1#/ GP1[31]	Connected to 25th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 31.
70	UART0_DSRn/ GP1[17]	Connected to 24th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 17.
71	GP1[29]	Connected to 23rd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 29.
72	GP0[6]	Connected to 22nd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 6.
73	GP0[15]	Connected to 21st Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 15.
74	MCA0_ AMUTE	Connected to 20th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port 0 Mute.
75	NC	Connected to 79th Pin of Expansion Connector 1	NC	NC	No Connection.
76	NC	Connected to 78th Pin of Expansion Connector 1	NC	NC	No Connection.
77	VIN[0]A_D[8]	Connected to 77th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 8.
78	MCA0_AHCLK X	Connected to 18th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Clock.
79	GND	GND	Power	0V	Ground.
80	GND	GND	Power	0V	Ground.
81	GP0[8]	Connected to 17th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 8.
82	MCA0_AFSX	Connected to 16th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port.

83	GP0[24]	Connected to 15th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 24.
84	MCA0_ACLKX	Connected to 14th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Clock.
85	MCA0_AXR0	Connected to 13th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive 0.
86	MCA0_ACLKR	Connected to 12th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive Clock.
87	MCA0_AXR1	Connected to 11th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive 1.
88	MCA0_AHCLKR	Connected to 10th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Clock.
89	MCA0_AXR2	Connected to 9th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive 2.
90	MCA0_AFSR	Connected to 8th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port.
91	MCA0_AXR3	Connected to 7th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive 3.
92	NC	Connected to 6th Pin of Expansion Connector 1	NC	NC	No Connection.
93	MCA0_AXR4	Connected to 5th Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive 4.
94	UART0_RXD	Connected to 4th Pin of Expansion Connector 1	Input	3.3V	UART 0 Receive Data Signal.
95	MCA0_AXR5	Connected to 3rd Pin of Expansion Connector 1	Input	3.3V	McASP Audio Port Receive 5.
96	UART0_TXD	Connected to 2nd Pin of Expansion Connector 1	Output	3.3V	UART 0 Transmit Data Signal.
97	GND	GND	Power	0V	Ground.
98	GND	GND	Power	0V	Ground.
99	NC	Connected to 48th Pin of Expansion Connector 1	NC	NC	No Connection.
100	VIN[0]A_D[15]	Connected to 47th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 15.
101	VIN[0]A_D[14]	Connected to 46th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 14.
102	VIN[0]A_D[13]	Connected to 45th Pin of Expansion Connector 1	Input	3.3V	Video Input 0 Port A data input 13.

103	GND	GND	Power	0V	Ground.
104	GND	GND	Power	0V	Ground.
105	NC	Connected to 75th Pin of Qseven Edge Connector	NC	NC	No Connection.
106	NC	Connected to 76th Pin of Qseven Edge Connector	NC	NC	No Connection.
107	NC	Connected to 77th Pin of Qseven Edge Connector	NC	NC	No Connection.
108	NC	Connected to 78th Pin of Qseven Edge Connector	NC	NC	No Connection.
109	GND	GND	Power	0V	Ground.
110	GND	GND	Power	0V	Ground.
111	NC	Connected to 81st Pin of Qseven Edge Connector	NC	NC	No Connection.
112	USB_4_5_OC#	Connected to 80th Pin of Qseven Edge Connector	Input	3.3V CMOS	Over current sense for USB port 4 & 5.
113	NC	Connected to 83rd Pin of Qseven Edge Connector	NC	NC	No Connection.
114	NC	Connected to 79th Pin of Qseven Edge Connector	NC	NC	No Connection.
115	GND	GND	Power	0V	Ground.
116	GND	GND	Power	0V	Ground.
117	Power	VCC_5V	Power	5V	VCC Power Supply.
118	Power	VCC_5V	Power	5V	VCC Power Supply.
119	Power	VCC_5V	Power	5V	VCC Power Supply.
120	Power	VCC_5V	Power	5V	VCC Power Supply.

6.3 Expansion Pin-out based on i.MX51 SOM

Table 52: Carrier Board Expansion Connector pin-out based on i.MX51 SOM

Pin No	Pin Name based on i.MX51 SOM	Pin Connection	Signal Type	Voltage Level/ Termination	Description
1	GND	GND	Power	0V	Ground.
2	GND	GND	Power	0V	Ground.
3	VBAT	Connected to 80th Pin of Expansion Connector 2	Power	4.7V	PMIC Battery Power Input.
4	VBAT	Connected to 79th Pin of Expansion Connector 2	Power	4.7V	PMIC Battery Power Input.
5	GND	Connected to 72nd Pin of Expansion Connector 2	Power	0V	Ground.
6	GND	Connected to 68th Pin of Expansion Connector 2	Power	0V	Ground.
7	GND	Connected to 64th Pin of Expansion Connector 2	Power	0V	Ground.
8	ADIN5	Connected to 75th Pin of Expansion Connector 2	Analog	Analog	PMIC Analog to Digital Convertor input 5.
9	ADIN6	Connected to 73rd Pin of Expansion Connector 2	Analog	Analog	PMIC Analog to Digital Convertor input6.
10	ADIN7	Connected to 71st Pin of Expansion Connector 2	Analog	Analog	PMIC Analog to Digital Convertor input7.
11	DI1_PIN12	Connected to 69th Pin of Expansion Connector 2	Input	2.75V	Digital Input Pin 12.
12	PWRON3	Connected to 67th Pin of Expansion Connector 2	Output	3.3V	Power ON/OFF button connection.
13	PWGTDRIV1	Connected to 65th Pin of Expansion Connector 2	Input	4.7V	Power Gate Driver 1.
14	PWGTDRIV2	Connected to 63rd Pin of Expansion Connector 2	Input	4.7V	Power Gate Driver 2.
15	CLK32K	Connected to 61st Pin of Expansion Connector 2	Output	3.3V	32KHz clock output for peripherals.
16	GND	GND	Power	0V	Ground.
17	GND	GND	Power	0V	Ground.
18	AUD6_TXC	Connected to 45th Pin of Expansion Connector 2	Output	1.8V	Audio Transmit Clock.
19	AUD6_TXFS	Connected to 43rd Pin of Expansion Connector 2	Output	1.8V	Audio Transmit Frame.

20	AUD6_TXD	Connected to 44th Pin of Expansion Connector 2	Output	1.8V	Audio Transmit.
21	AUD6_RXD	Connected to 41st Pin of Expansion Connector 2	Input	1.8V	Audio Receive.
22	EIM_EB0	Connected to 42nd Pin of Expansion Connector 2	Output	1.8V	EIM Enable Byte0.
23	EIM_EB1	Connected to 39th Pin of Expansion Connector 2	Output	1.8V	EIM Enable Byte1.
24	EIM_WAIT	Connected to 40th Pin of Expansion Connector 2	Input	1.8V	EIM Ready/Busy/Wait.
25	EIM_BCLK	Connected to 37th Pin of Expansion Connector 2	Output	1.8V	EIM Burst Clock.
26	EIM_CRE	Connected to 38th Pin of Expansion Connector 2	Output	1.8V	EIM Memory Register Set.
27	EIM_RW	Connected to 35th Pin of Expansion Connector 2	Output	1.8V	EIM Read/Write Enable.
28	EIM_CS0	Connected to 36th Pin of Expansion Connector 2	Output	1.8V	EIM Chip Select0.
29	GND	GND	Power	0V	Ground.
30	GND	GND	Power	0V	Ground.
31	EIM_DA15	Connected to 31st Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 15.
32	EIM_DA14	Connected to 32nd Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 14.
33	EIM_DA13	Connected to 29th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 13.
34	EIM_DA12	Connected to 30th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 12.
35	EIM_DA11	Connected to 27th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 11.
36	EIM_DA10	Connected to 28th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 10.
37	EIM_DA9	Connected to 25th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 9.
38	EIM_DA8	Connected to 26th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 8.
39	EIM_DA7	Connected to 23rd Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 7.

40	EIM_DA6	Connected to 24th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 6.
41	EIM_DA5	Connected to 21st Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 5.
42	EIM_DA4	Connected to 22nd Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 4.
43	EIM_DA3	Connected to 19th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 3.
44	EIM_DA2	Connected to 20th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 2.
45	EIM_DA1	Connected to 17th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 1.
46	EIM_DA0	Connected to 18th Pin of Expansion Connector 2	Input/ Output	1.8V	EIM Data & address line 0.
47	GND	GND	Power	0V	Ground.
48	GND	GND	Power	0V	Ground.
49	AI_BCLK	Connected to 35th Pin of Expansion Connector 1	Output	3.3V	Audio Input Bit Clock.
50	AI_DATA	Connected to 36th Pin of Expansion Connector 1	Output	3.3V	Audio Input Data.
51	AI_MCLK	Connected to 33rd Pin of Expansion Connector 1	Output	3.3V	Audio Input Master Clock.
52	AI_LRCK	Connected to 34th Pin of Expansion Connector 1	Output	3.3V	Audio Input Clock.
53	TS_INT#	Connected to 41st Pin of Expansion Connector 1	Input	3.3V	Touch Interrupt.
54	B_PWM2_ OUT	Connected to 19th Pin of Expansion Connector 1	Input	3.3V	General Purpose PWM.
55	B_GPIO21	Connected to 43rd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 21.
56	GND	GND	Power	0V	Ground.
57	B_GPIO34	Connected to 58th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 34.
58	B_GPIO20	Connected to 38th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 20.
59	B_GPIO32	Connected to 56th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 32.
60	B_GPIO33	Connected to 57th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 33.
61	GND	GND	Power	0V	Ground.

62	GND	GND	Power	0V	Ground.
63	B_GPIO31	Connected to 55th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 31.
64	B_GPIO30	Connected to 31st Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 30.
65	B_GPIO29	Connected to 30th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 29.
66	B_GPIO28	Connected to 29th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 28.
67	B_GPIO27	Connected to 28th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 27.
68	B_GPIO26	Connected to 26th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 26.
69	B_GPIO25	Connected to 25th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 25.
70	B_GPIO24	Connected to 24th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 24.
71	B_GPIO23	Connected to 23rd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 23.
72	B_GPIO22	Connected to 22nd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 22.
73	IS1	Connected to 21st Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin IS1.
74	IS0	Connected to 20th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin IS0.
75	B_GPIO19	Connected to 79th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 19.
76	B_GPIO18	Connected to 78th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 18.
77	B_GPIO17	Connected to 77th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 17.
78	B_GPIO16	Connected to 18th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 16.
79	GND	GND	Power	0V	Ground.
80	GND	GND	Power	0V	Ground.
81	B_GPIO15	Connected to 17th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 15.
82	B_GPIO14	Connected to 16th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 14.
83	B_GPIO13	Connected to 15th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 13.

84	B_GPIO12	Connected to 14th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 12.
85	B_GPIO11	Connected to 13th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 11.
86	B_GPIO10	Connected to 12th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 10.
87	B_GPIO9	Connected to 11th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 9.
88	B_GPIO8	Connected to 10th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 8.
89	B_GPIO7	Connected to 9th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 7.
90	B_GPIO6	Connected to 8th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 6.
91	B_GPIO5	Connected to 7th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 5.
92	B_GPIO4	Connected to 6th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 4.
93	B_GPIO3	Connected to 5th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 3.
94	B_GPIO2	Connected to 4th Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 2.
95	B_GPIO1	Connected to 3rd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 1.
96	B_GPIO0	Connected to 2nd Pin of Expansion Connector 1	Input/ Output	3.3V	General Purpose Pin 0.
97	GND	GND	Power	0V	Ground.
98	GND	GND	Power	0V	Ground.
99	AO_MCLK	Connected to 48th Pin of Expansion Connector 1	Output	3.3V	Audio Output Master Clock.
100	AO_LRCK	Connected to 47th Pin of Expansion Connector 1	Output	3.3V	Audio Output Clock.
101	AO_BCLK	Connected to 46th Pin of Expansion Connector 1	Output	3.3V	Audio Output Bit Clock.
102	AO_DATA	Connected to 45th Pin of Expansion Connector 1	Output	3.3V	Audio Output Data.
103	GND	GND	Power	0V	Ground.
104	GND	GND	Power	0V	Ground.
105	NC	Connected to 75th Pin of Qseven Edge Connector	NC	NC	No Connection.

106	NC	Connected to 76th Pin of Qseven Edge Connector	NC	NC	No Connection.
107	NC	Connected to 77th Pin of Qseven Edge Connector	NC	NC	No Connection.
108	NC	Connected to 78th Pin of Qseven Edge Connector	NC	NC	No Connection.
109	GND	GND	Power	0V	Ground.
110	GND	GND	Power	0V	Ground.
111	NC	Connected to 81st Pin of Qseven Edge Connector	NC	NC	No Connection.
112	USB_4_5_OC#	Connected to 80th Pin of Qseven Edge Connector	Input	3.3V CMOS	Over current sense for USB port 4 & 5.
113	NC	Connected to 83rd Pin of Qseven Edge Connector	NC	NC	No Connection.
114	NC	Connected to 79th Pin of Qseven Edge Connector	NC	NC	No Connection.
115	GND	GND	Power	0V	Ground.
116	GND	GND	Power	0V	Ground.
117	Power	VCC_5V	Power	5V	VCC Power Supply.
118	Power	VCC_5V	Power	5V	VCC Power Supply.
119	Power	VCC_5V	Power	5V	VCC Power Supply.
120	Power	VCC_5V	Power	5V	VCC Power Supply.

7   APPENDIX III

7.1   iWave's Compatible Qseven CPU Modules

Generic Qseven Carrier Board is board is compatible with the following iWave's Qseven CPU modules.

- Rainbow-G17M (Cyclone V Qseven CPU Module)
  http://www.iwavesystems.com/iwave-new-cyclone-v-soc-based-som-overview

- Rainbow-G15M-Q7 (i.MX6 Qseven CPU Module):
  http://www.iwavesystems.com/product/cpu-modules/i-mx6-q7-som/i-mx6-qseven-som.html

- Rainbow G12M-Q7 (AM389x Qseven CPU Module):
  http://www.iwavesystems.com/product/cpu-modules/am389x-dm816x-som/am389x-dm816x-q7-module.html

- Rainbow G8M-Q7 (i.MX51 Qseven CPU Module):
  http://www.iwavesystems.com/product/cpu-modules/i-mx51-q7-module/i-mx51-q7-som.html

- Rainbow G6M-Q7 (Atom Qseven Module):
  http://www.iwavesystems.com/product/cpu-modules/atom-z5xx-q7-som-12.html

8   APPENDIX IV

8.1   Debug USB Cable Connecting Procedure

Due to the hardware errata of carrier board, there is chance of Debug UART interface misbehaving if the below Power ON and Power OFF procedure is not followed in carrier board.

While Powering On the carrier board:

➢ Power ON the Generic Qseven Carrier Board.

➢ ONLY then connect the Debug USB Cable "Type A to Micro B" between PC and carrier Board Debug USB connector (J15).

Important Note: Make sure that the Debug USB Cable is connected only after Generic Qseven Carrier Board Power is ON.

While Powering OFF the carrier board:

➢ Remove the Debug USB Cable "Type A to Micro B" between PC and carrier Board Debug USB connector (J15).

➢ Power OFF the Generic Qseven Carrier Board.

Important Note: Make sure that the Debug USB Cable is removed before Generic Qseven Carrier Board Power is OFF.