Advanced Synchronous Rectifier Controller for LLC Resonant Converter

NCP4318

NCP4318 is an advanced synchronous rectification (SR) controller for LLC resonant converter with minimum external components. It has two gate driver stages for driving the SR MOSFETs which are rectifying the outputs of the secondary transformer windings. The two gate driver stages have their own Drain and Source sensing inputs and operate independently of each other. The advanced adaptive dead time control compensates a voltage across parasitic inductance to minimize the body diode conduction and maximize the system efficiency. The advanced turn−off control algorithm allows stable SR operation over entire load range. NCP4318 has two versions of pin assignment – NCP4318AXX, NCP4318BXX.

Features

- Mixed Mode SR Turn−off Control
- Anti Shoot−through Control for Reliable SR Operation
- Separate 200 V Rated Sense Pins for the Drain and Dedicated Source Sense Pins
- Advanced Adaptive Dead Time Control
- SR Current Inversion Detection
- Adaptive Minimum Turn−on Time for Noise Immunity
- SR Conduction Time Increase Rate Limitation
- Multi−level Turn−off Threshold Voltage
- Adaptive Gate Voltage Control (10 V, 6 V)
- Low Operating Current (100 μA) in Green Mode
- Soft Start for 512 Switching Cycle with 0 V/6 V Gate Output Voltage
- Very Fast Turn−on and Turn−off Delay Time (30 ns/30 ns)
- Large Gate Sourcing and Sinking Current (1.5 A/4.5 A)
- Wide Operating Supply Voltage Range from 6.5 V to 35 V
- Wide Operating Frequency Range (22 kHz to 500 kHz)
- SOIC−8 Package
- These Devices are Pb−Free and are RoHS Compliant

Applications

- High Power Density Adapters
- Large Screen LED−TV and OLED−TV Power Supplies
- High Efficiency Desktop and Server Power Supplies
- Networking and Telecom Power Supplies
- High Power LED Lighting

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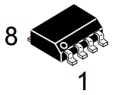
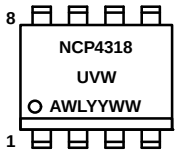


SOIC 8, 150 mils
CASE 751BD

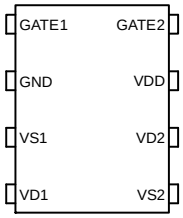
MARKING DIAGRAM



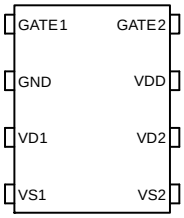
U = Pin Layout, A and B
V = Frequency, H: High, L: Low
W = Additional IPT option
A = Assembly Location
WL = Wafer Lot Traceability
YYWW = Date Code

PIN CONNECTIONS

NCP4318AXX



NCP4318BXX



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 3 of this data sheet.

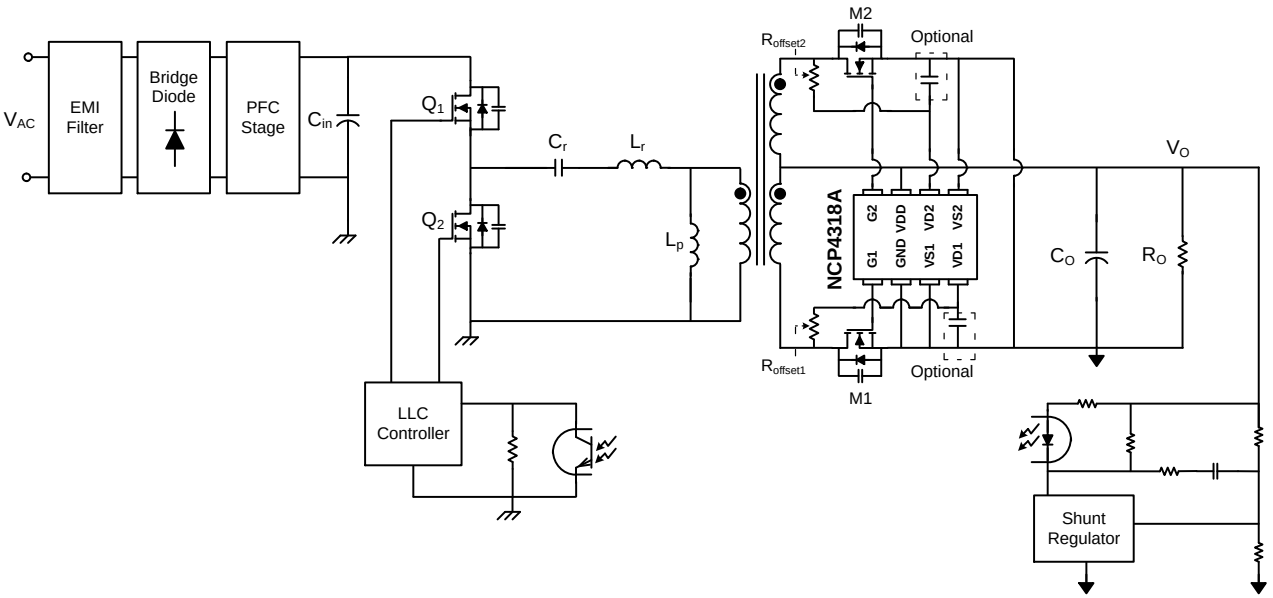


Figure 1. Typical Application Schematic of NCP4318

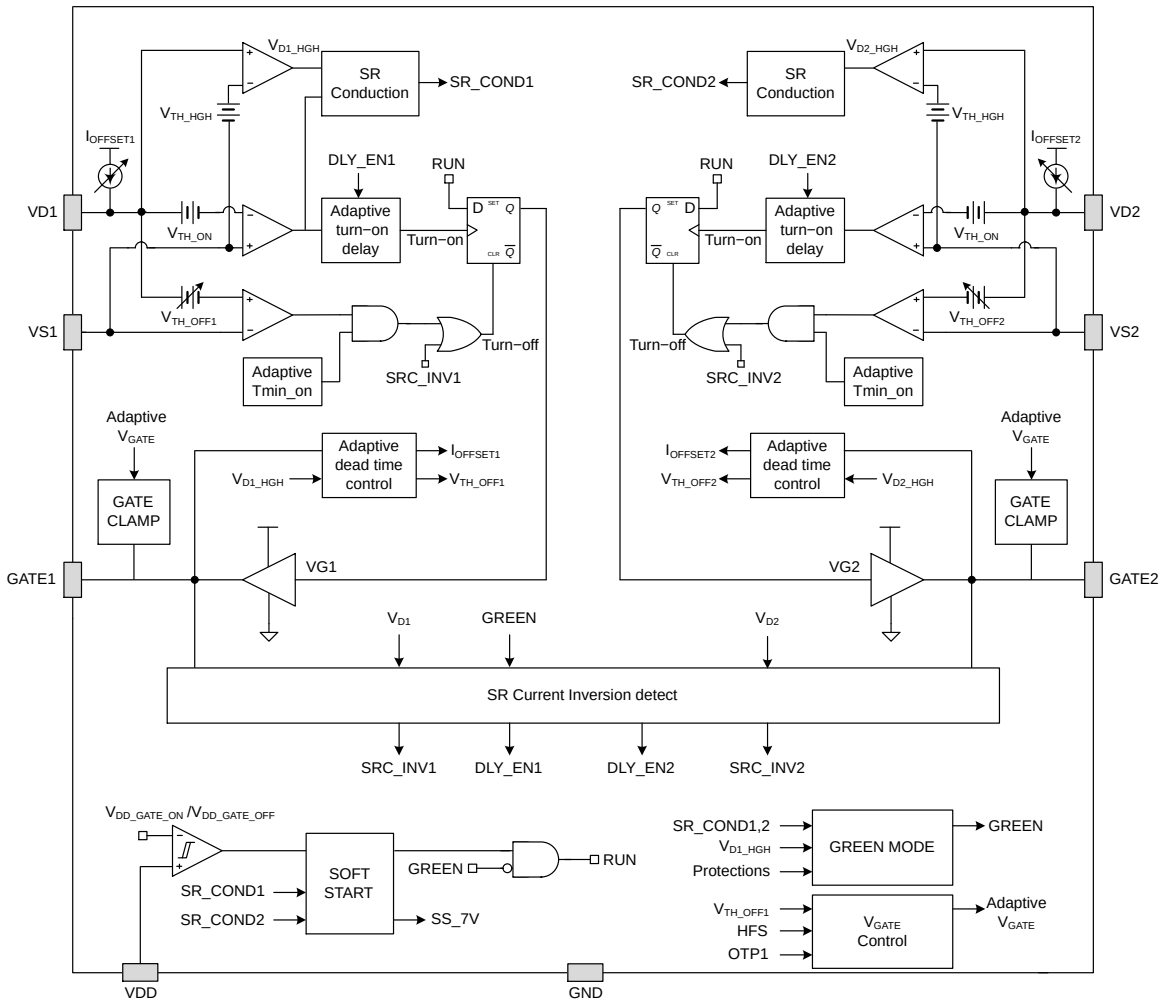


Figure 2. Internal Block Diagram of NCP4318

PIN DESCRIPTION

Pin Number		Name	Description
NCP4318A	NCP4318B		
1	1	GATE1	Gate drive output for SR MOSFET1
2	2	GND	Ground
3	4	VS1	Synchronous rectifier source sense input for SR1
4	3	VD1	Synchronous rectifier drain sense input. $I_{OFFSET1}$ current source flows out of the VD1 pin such that an external series resistor can be used to adjust the synchronous rectifier turn−off threshold. The $I_{OFFSET1}$ current source is turned off when V_{DD} is under−voltage or when switching is disabled in green mode
5	5	VS2	Synchronous rectifier source sense input for SR2
6	6	VD2	Synchronous rectifier drain sense input. $I_{OFFSET2}$ current source flows out of the VD2 pin such that an external series resistor can be used to adjust the synchronous rectifier turn−off threshold. The $I_{OFFSET2}$ current source is turned off when V_{DD} is under−voltage or when switching is disabled in green mode
7	7	VDD	Supply Voltage
8	8	GATE2	Gate drive output for SR MOSFET2

ORDERING INFORMATION

Device (Ordering Code)	Device Marking	Package	Shipping†
NCP4318ALC	NCP4318ALC	SOIC 8 (Pb−Free)	2500 / Tape & Reel
NCP4318BLC	NCP4318BLC		
NCP4318ALS	NCP4318ALS		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{DD}	Power Supply Input Pin Voltage		−0.3	37	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage		−4	200	V
V_{GATE1}, V_{GATE2}	Gate Drive Output Pin Voltage		−0.3	17	V
V_{S1}, V_{S2}	Source Sense Input Pin Voltage		−0.3	5.5	V
V_{S1_DYN}, V_{S2_DYN}	Source Sense Dynamic Input Pin Voltage (pulse width = 200 ns)		−4	5.5	V
P_D	Power Dissipation (T_A = 25°C)			0.625	W
T_J	Maximum Junction Temperature		−40	150	°C
T_{STG}	Storage Temperature Range		−60	150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS−001−2012 (except VD1, VD2 pin)		3	kV
		Human Body Model, VD1−GND, VD2−GND pin to pin with 330pF[2] capacitance on VD1 and VD2 pin		2	
		Charged Device Model, JESD22−C101		1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values are with respect to the GND pin.
2. The capacitance can be replaced by C_{OSS} of MOSFET.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics	$R_{\psi JT}$	22	°C/W
Thermal Characteristics	$R_{\theta JA}$	165	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD} (3)	VDD Pin Supply Voltage to GND	0	35	V
V_{D1} ,V_{D2}	Drain Sense Input Pin Voltage	−0.7	180	V
V_{S1} V_{S2}	Source Sense Input Pin Voltage	−0.3	5	V
T_J	Operating Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Allowable operating supply voltage V_{DD} can be limited by the power dissipation of NCP4318 related to switching frequency, load capacitance and ambient temperature.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage and Current Section						
V_{DD_ON}	Turn−on threshold	V_{DD} rising with 4.3 V / 1 ms		4.0	4.3	V
V_{DD_OFF}	Turn−off threshold	$V_{DD} < V_{DD\_OFF}$	3.6	3.8		V
$V_{DD\_GATE\_ON}$	SR gate enable threshold voltage	$V_{DD} > V_{DD\_GATE\_ON}$		6.5	7.1	V
$V_{DD\_GATE\_OFF}$ (4)	SR gate disable threshold voltage	$V_{DD} < V_{DD\_GATE\_OFF}$	5.0	6.0		V
I_{DD_OP1}	Operating current	f_{SW} = 100 kHz, C_{GATE} = 1 nF		8	10	mA
I_{DD_OP0}	Operating current	f_{SW} = 100 kHz, C_{GATE} = 0 nF			6	mA
I_{DD_START}	Start−up current	$V_{DD} = V_{DD\_ON}$ - 0.1 V			100	μA
I_{DD_GREEN}	Operating current in green mode1	V_{DD} = 12 V (no $V_{D1/2}$ switching) GREEN1 enable at T_J = 25°C		100	210	μA
η_{SS_SKIP}	Number of $V_{D1/2}$ alternative switching for soft start skip range	$V_{D1/2}$ falling lower than V_{TH_ON} & $V_{D1/2}$ rising higher than V_{TH_HGH} & No GATE output at f_{SW} = 200 kHz, C_{GATE} = 0 nF		255		Cycle
Drain Voltage Sensing Section						
V_{OSI} (4)	Comparator input offset voltage		−1	0	1	mV
I_{DRAIN_LKG}	Drain pin leakage current	$V_{D1/2}$ = 200 V			1	μA
V_{TH_ON} (4)	Turn−on threshold	R_{OFFSET} = 0 Ω (includes comparator input offset voltage)		−100		mV
t_{OFF_MIN}	Minimum off-time	From $V_{D1/2}$ higher than V_{TH_HGH} in ALC, BLC	1400	2000	2800	ns
		in ALS	450	800	1150	ns
t_{ON_DLY}	Turn−on propagation delay	Turn−on comparator delay From $V_{D1/2}$ = −0.2 to V_{GATE} = 1 V, when DLY_EN = 0		30	80	ns
t_{ON_DLY2} (4)	Turn−on de−bounce time for L−version when additional turn−on delay is enabled in light load condition	Turn−on comparator delay From $V_{D1/2}$ = −0.2 to V_{GATE} = 1 V, when DLY_EN = 1 in ALC, BLC, ALS		240		ns
t_{OFF_DLY}	Turn−off propagation delay	Turn−off comparator delay From $V_{D1/2}$ = 0.6 to V_{GATE} = 5.7 V		30	80	ns
$V_{TH\_OFF\_MIN}$ (4)	Minimum turn−off threshold voltage	R_{OFFSET} = 0 Ω (includes comparator input offset voltage) in ALC, BLC, ALS		−6		mV
$V_{TH\_OFF\_STEP}$ (4)	One step size of turn−off threshold voltage	R_{OFFSET} = 0 Ω, in ALC, BLC		4		mV
		in ALS		8		mV
$V_{TH\_OFF\_MAX}$ (4)	Maximum turn−off threshold voltage	R_{OFFSET} = 0 Ω, in ALC, BLC		118		mV
		in ALS		242		mV
$V_{TH\_OFF\_RST}$ (4)	Turn−off threshold voltage reset value	R_{OFFSET} = 0 Ω, in ALC, BLC		2		mV
		in ALS		10		mV
K_{2ND_VOFF} (4)	Ratio of the second step V_{TH_OFF} based on nominal V_{TH_OFF} in one switching cycle	LLD1 is low. If LLD1 is high, 2nd step V_{TH_OFF} = 3rd step V_{TH_OFF}		60		%
K_{2nd_TOFF} (4)	Effective time ratio based on $t_{VG1}(n-1)$ for the 2nd step V_{TH_OFF} in one switching cycle	LLD1 = 0 & $t_{VG1}(n-1)$ = 8 μs & $t_{MIN\_ON} < K_{2nd\_TOFF} * t_{VG1}(n-1)$. If $t_{MIN\_ON} > K_{2nd\_TOFF} * t_{VG1}(n-1)$, $t_{VG1\_70} = t_{MIN\_ON}$		70		%
V_{TH_HGH} (4)	Drain voltage high detect threshold voltage	$V_{D1/2}$ Rising in ALC, BLC		0.85		V
		in ALS		1.5		V
$t_{GATE\_SKIP\_L1}$	Minimum SR conduction time to enable SR when DLY_EN = 0 (3 steps $V_{TH\_OFF1\ or\ 2}$ decrease when gate skip is triggered)	The duration from turn−on trigger to $V_{D1/2}$ rising higher than V_{TH_HGH} ,when DLY_EN = 0 in ALC, BLC, ALS	500	710		ns

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{GATE\_SKIP\_L2}$ (4)	Minimum SR conduction time to enable SR when DLY_EN = 1 (3 steps $V_{TH\_OFF1\ or\ 2}$ decrease when gate skip is triggered)	The duration from turn−on trigger to $V_{D1/2}$ rising higher than V_{TH_HGH} ,when DLY_EN=1 in ALC, BLC, ALS		510		ns
Minimum On−Time and Maximum On−Time Section						
K_{TON1}	Adaptive minimum on time ratio when DLY_EN = 0	DLY_EN=0 & t_{SR_COND}(n−1) = 8 μs $K_{TON} = t_{MIN\_ON} / t_{SR\_COND}$(n−1)	43	50	57	%
K_{TON2}	Adaptive minimum on time ratio when DLY_EN = 1	DLY_EN=1 & t_{SR_COND}(n−1) = 8 μs $K_{TON} = t_{MIN\_ON} / t_{SR\_COND}$(n−1)		20		%
$t_{MIN\_ON\_U1}$	Minimum on−time upper limit when DLY_EN = 0	$t_{MIN\_ON\_L} < t_{MIN\_ON} < t_{MIN\_ON\_U}$, when DLY_EN = 0	4	5	6	μs
$t_{MIN\_ON\_U2}$	Minimum on−time upper limit when DLY_EN = 1	$t_{MIN\_ON\_L} < t_{MIN\_ON} < t_{MIN\_ON\_U}$, when DLY_EN = 1	2	2.5	3	μs
K_{INV1}	Adaptive SR current inversion detection window ratio when DLY_EN = 0	$K_{TON1} = K_{INV1,}$ when DLY_EN = 0 $t_{INV\_WIN} = t_{MIN\_ON}$	43	50	57	%
K_{INV2}	Adaptive SR current inversion detection window ratio when DLY_EN = 1	$K_{TON2} = K_{INV2,}$ when DLY_EN = 1 $t_{INV\_WIN} = t_{MIN\_ON}$		20		%
η_{INV_EXT} (4)	Normal consecutive switching cycles to exit SR current inversion state which has t_{ON_DLY2}	Without parasitic $V_{D1/2}$ oscillation		16k		cycle
$t_{SR\_MAX\_ON}$ (4)	Maximum SR turn−on time		21	30	39	μs
f_{MIN} (4)	Minimum switching frequency	$1/(t_{SR\_MAX\_ON\_CH1} + t_{SR\_MAX\_ON\_CH2})$			22	kHz
Dead Time Regulation Section						
I_{OFFSET}	Maximum of adaptive offset current which have 31 steps and 10μA of resolution	$V_{D1} = V_{D2} = 0$	285	310	335	μA
t_{DEAD_LBAND} (4)	Lower band of dead time regulation	From V_{GATE} falling below V_{GATE_LOW} in ALC, BLC, ALS		90		ns
t_{DEAD_HBAND} (4)	Upper band of dead time regulation	From V_{GATE} falling below V_{GATE_LOW}, when LLD1 = 0		t_{DEAD_LBAND} +90		ns
η_{LLD1} (4)	First light load detection (LLD1) threshold number of V_{TH_OFF} modulator output	$\eta V_{TH\_OFF\_CNT} \leq \eta_{LLD1}$		7		
η_{LLD2} (4)	Second light load detection (LLD2) threshold number of V_{TH_OFF} modulator output	$\eta V_{TH\_OFF\_CNT} \leq \eta_{LLD2}$		3		
Green Mode Section						
t_{GRN1_ENT}	Non−switching period of SR gate to Enter Green Mode 1 for L−version	When SR_COND1, 2 are both low for $t_{GRN1\_ENT\_L}$, the green mode1 is enabled in ALC, BLC, ALS	45	60	75	μs
t_{GRN2_ENT}	Non−switching period of SR gate to Enter Green Mode 2 for L−version	When SR_COND1, 2 are both low for $t_{GRN2\_ENT\_L}$, the green mode2 is enabled in ALC, BLC, ALS	4.5	6	7.5	μs
η_{CSW_EXT} (4)	Number of buffer switching cycle to recover I_{DD_OP} when IC exits from green mode 1.	Number of switching with $V_{D1} > V_{TH\_HGH}$ GREEN1 exit only		4		cycle

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 12 V and T_J = −40°C to 125°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Protection Section						
V_{SRC_INV} (4)	Threshold voltage of current inversion detection	LLD1 = 0		0		mV
		LLD1 = 1, Virtual V_{TH_OFF}		V_{TH_OFF}		
t_{INV} (4)	Debounce time of SR current inversion detection for L−version	$V_{GATE1/2}$ > 4.5 V & $V_{D1/2}$ > V_{SRC_INV} for t_{INV} In ALC, BLC		320		ns
		In ALS		520		ns
V_{SD_PRI} (4)	Drain threshold voltage for the primary shutdown protection	$V_{GATE1/2}$ > 4.5 V with 200 ns delay & $V_{D1/2}$ > V_{SD_PRI} when DLY_EN = 0, $V_{GATE1/2}$ > 4.5 V with 100 ns delay & $V_{D1/2}$ > V_{SD_PRI} when DLY_EN = 1 in ALC, BLC		150		mV
		in ALS		200		mV
K_{SD_PRI} (4)	Detection window time ratio based on t_{VG1}(n−1) for the primary shutdown protection	LLD1 = 0 & t_{VG1}(n−1) = 8 μs & t_{MIN_ON} < K_{2nd_TOFF}*t_{VG1}(n−1). If t_{MIN_ON} > K_{2nd_TOFF} *t_{VG1}(n−1), t_{VG1_70} = t_{MIN_ON}	65	70	75	%
V_{ABN_VD} (4)	Drain threshold voltage to trigger abnormal VD sensing protection	$V_{D1/2}$ > V_{ABN_VD} & $V_{GATE1/2}$ > 4.5V with 100 ns delay within K_{SD_PRI} in ALC, BLC V_{ABN_VD} = V_{TH_HGH}		0.85		V
		in ALS		1.5		V
T_{OTP1} (4)	Over temperature protection1	T_J > T_{OTP1} & V_{GATE} = 6.7 V in ALC, BLC		105		°C
		in ALS		130		°C
T_{OTP2} (4)	Over temperature protection2	T_J > T_{OTP2} & No gate output in ALC, BLC		140		°C
		in ALS		disable		
T_{OTP_RST} (4)	Over temperature protection reset	T_J < T_{OTP_RST}, OTP1 and OTP2 are reset		80		°C
Gate Driver Section						
V_{GATE_MAX} (4)	Gate clamping voltage	12 V < V_{DD} < 33 V, C_{GATE} = 4.7 nF at T_J < T_{OTP1}	9	10.5	12	V
$V_{GATE\_MAX\_7V}$ (4)	Gate clamping voltage for adaptive gate voltage control	V_{DD} = 12 V, C_{GATE} = 4.7 nF	5.0	6.7	8.2	V
t_{HFS1_EN} (4)	Adaptive gate control enabling switching period	The time t_s from V_{GATE1}(n−1) rising edge to V_{GATE1}(n) rising edge at T_J < T_{OTP1} in ALC, BLC, ALS	4	5	6.1	μs
I_{SOURCE} (4)	Peak sourcing current of gate driver			1.5		A
I_{SINK} (4)	Peak sinking current of gate driver			4.5		A
R_{DRV_SOURCE} (4)	Gate driver sourcing resistance			8		Ω
R_{DRV_SINK} (4)	Gate driver sinking resistance			1.5		Ω
t_R	Rise time	V_{DD} = 12 V, C_L = 3.3 nF, V_{GATE} = 1 V → 6 V at T_J = 25°C		50	150	ns
t_F	Fall time	V_{DD} = 12 V, C_L = 3.3 nF, V_{GATE} = 6 V → 1 V at T_J = 25°C		30	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Not tested but guaranteed by design

KEY PARAMETERS FOR IPT OPTIONS

	NCP4318ALC	NCP4318BLC	NCP4318ALS
Drain sensing pin	#4, #6	#3, #6	#4, #6
Frequency	L−version	L−version	L−version
DLY_EN	Low / High	Low / High	Always High
t_{INV}	320 ns	320 ns	520 ns
t_{DEAD_LBAND}	90 ns	90 ns	90 ns
t_{GRN2_ENT}	6 μs	6 μs	6 μs
f_{HFS_EN}	200 kHz	200 kHz	200 kHz
$nV_{TH\_OFF\_RST}$	2	2	3
V_{TH_HGH}	0.85 V	0.85 V	1.5 V
V_{GATE_CTRL}	2−Level (10 V, 6 V)	2−Level (10 V, 6 V)	1−Level (10 V)
t_{OFF_MIN}	2 μs	2 μs	700 ns
$V_{TH\_OFF\_MIN}$	−6 mV	−6 mV	−6 mV
$V_{TH\_OFF\_STEP}$	4 mV	4 mV	8 mV
$V_{TH\_OFF\_MAX}$	118 mV	118 mV	242 mV
$V_{TH\_OFF\_RST}$	2 mV	2 mV	10 mV
$t_{GATE\_SKIP\_L1}$	710 ns	710 ns	710 ns
$t_{GATE\_SKIP\_L2}$	510 ns	510 ns	510 ns
t_{GRN1_ENT}	60 μs	60 μs	60 μs
t_{GRN2_ENT}	6 μs	6 μs	6 μs
V_{SD_PRI}	150 mV	150 mV	200 mV
T_{OTP1}	105 °C	105 °C	130 °C
T_{OTP2}	140 °C	140 °C	Disable
t_{HFS1_EN}	5 μs	5 μs	5 μs

TYPICAL PERFORMANCE CHARACTERISTICS

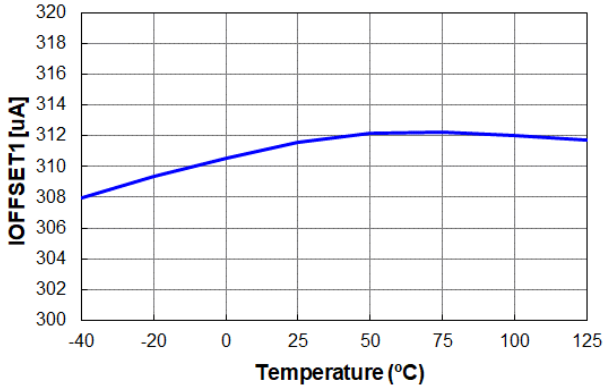


Figure 3. $I_{OFFSET1}$ vs. Temperature

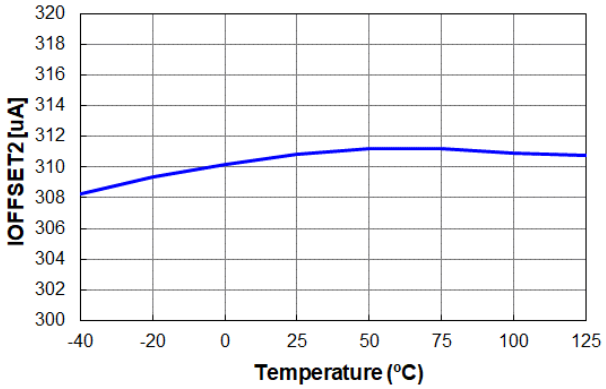


Figure 4. $I_{OFFSET2}$ vs. Temperature

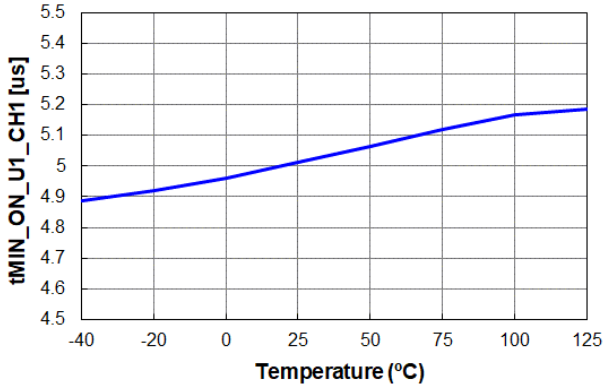


Figure 5. $t_{MIN\_ON\_U1\_CH1}$ vs. Temperature

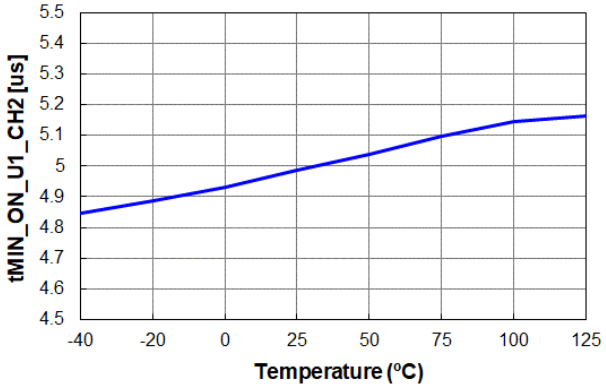


Figure 6. $t_{MIN\_ON\_U1\_CH2}$ vs. Temperature

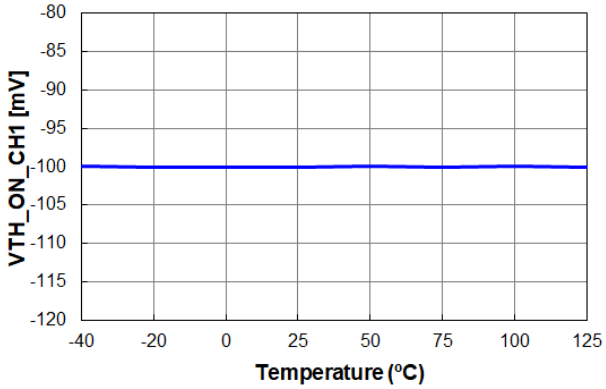


Figure 7. $V_{TH\_ON\_CH1}$ vs. Temperature

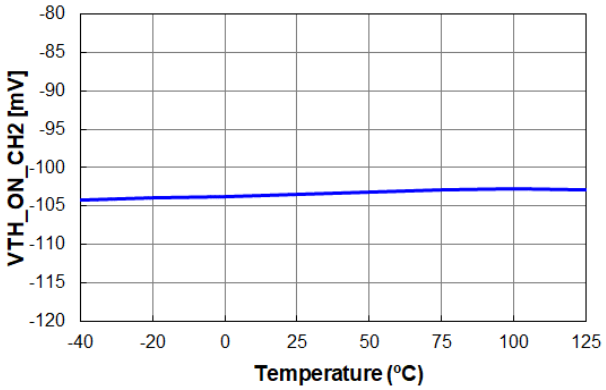


Figure 8. $V_{TH\_ON\_CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

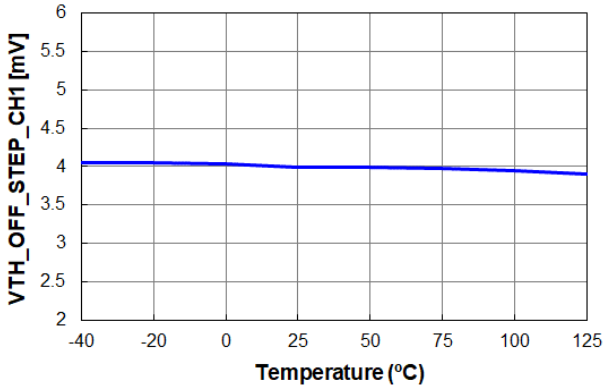


Figure 9. $V_{TH\_OFF\_STEP\_CH1}$ vs. Temperature

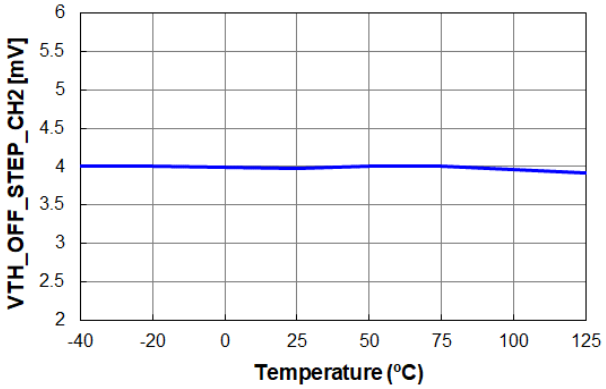


Figure 10. $V_{TH\_OFF\_STEP\_CH2}$ vs. Temperature

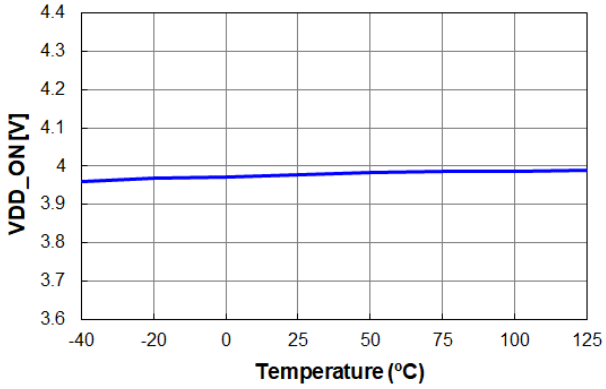


Figure 11. V_{DD_ON} vs. Temperature

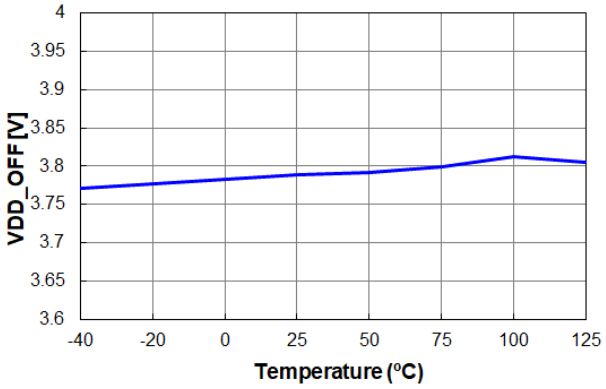


Figure 12. V_{DD_OFF} vs. Temperature

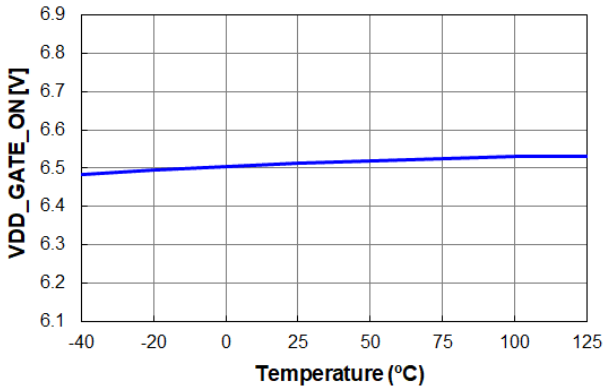


Figure 13. $V_{DD\_GATE\_ON}$ vs. Temperature

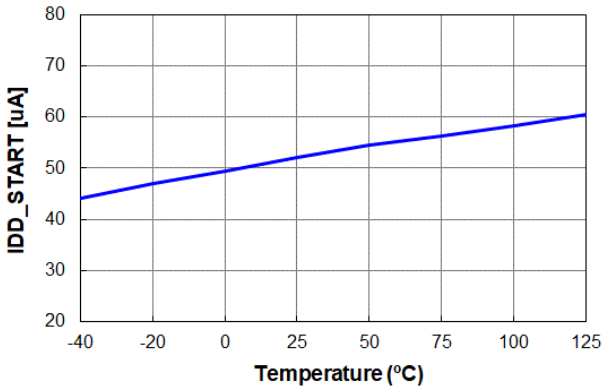


Figure 14. I_{DD_START} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

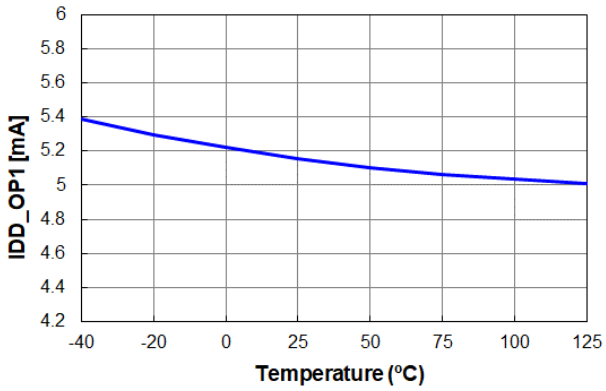


Figure 15. I_{DD_OP1} vs. Temperature

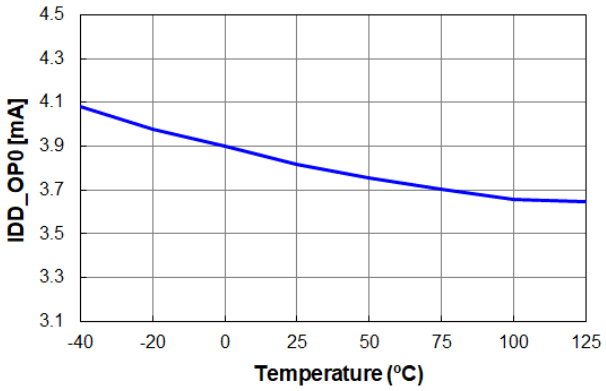


Figure 16. I_{DD_OP0} vs. Temperature

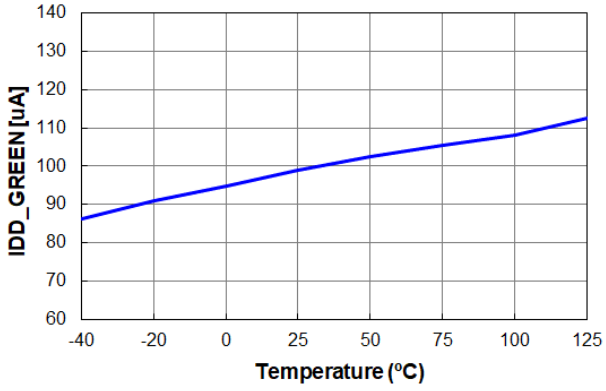


Figure 17. I_{DD_GREEN} vs. Temperature

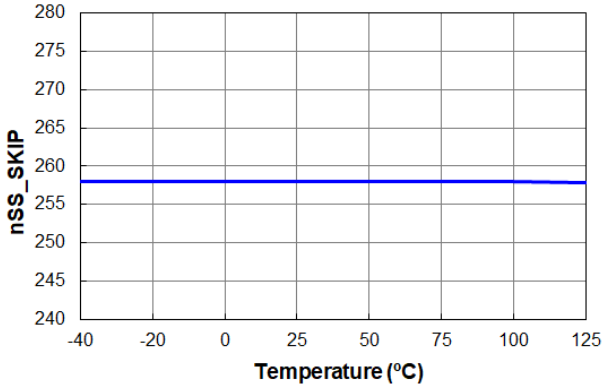


Figure 18. n_{SS_SKIP} vs. Temperature

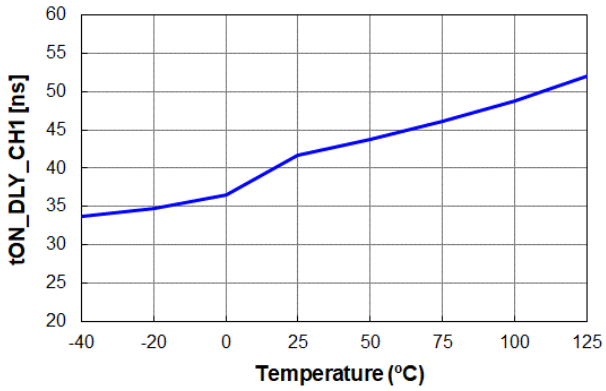


Figure 19. $t_{ON\_DLY\_CH1}$ vs. Temperature

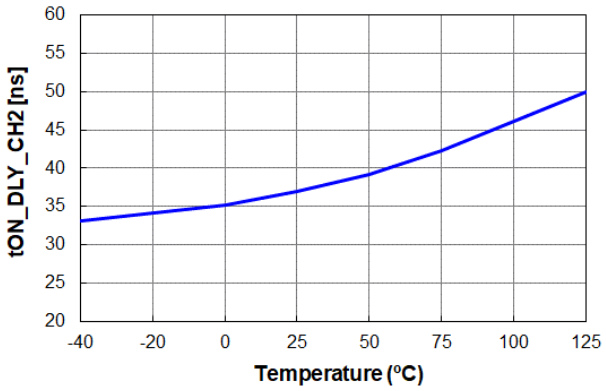


Figure 20. $t_{ON\_DLY\_CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

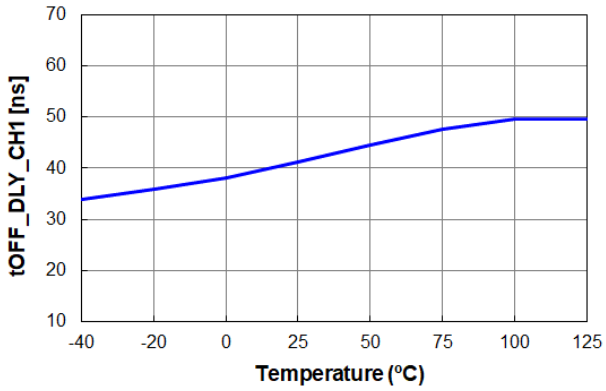


Figure 21. $t_{OFF\_DLY\_CH1}$ vs. Temperature

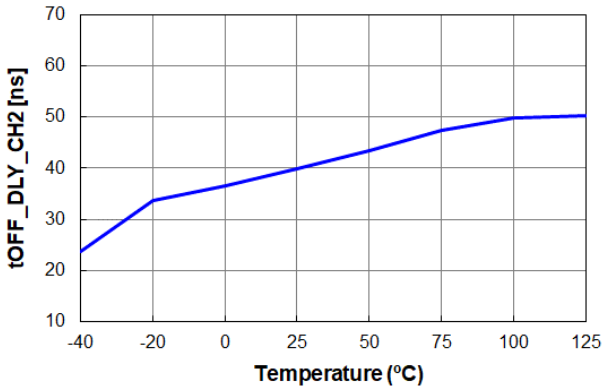


Figure 22. $t_{OFF\_DLY\_CH2}$ vs. Temperature

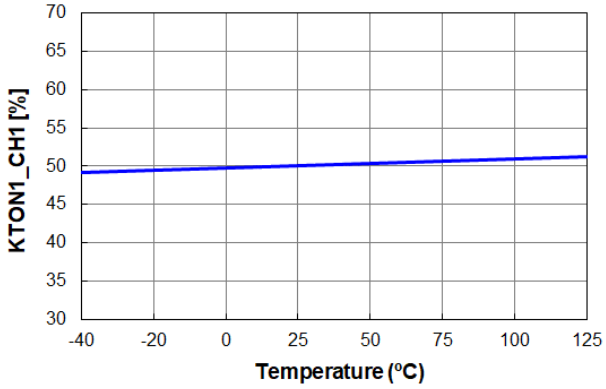


Figure 23. KTON1_CH1 vs. Temperature

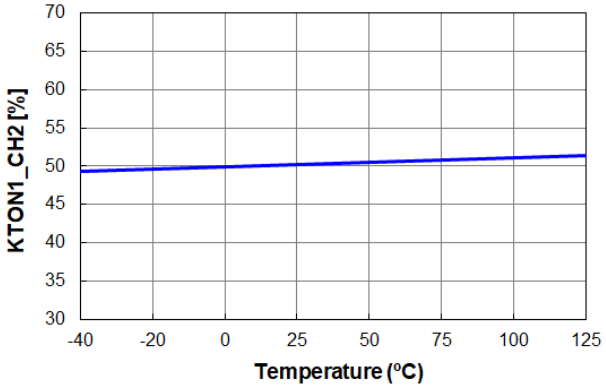


Figure 24. KTON1_CH2 vs. Temperature

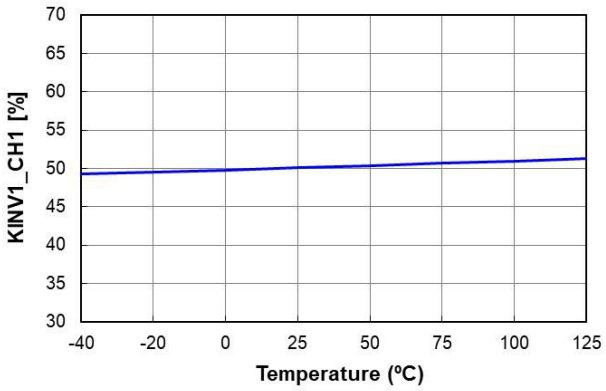


Figure 25. KINV1_CH1 vs. Temperature

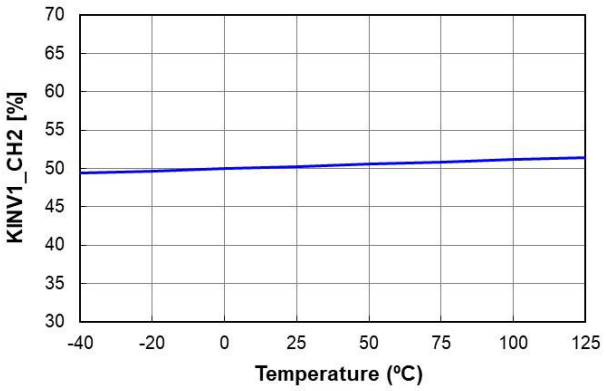


Figure 26. KINV1_CH2 vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

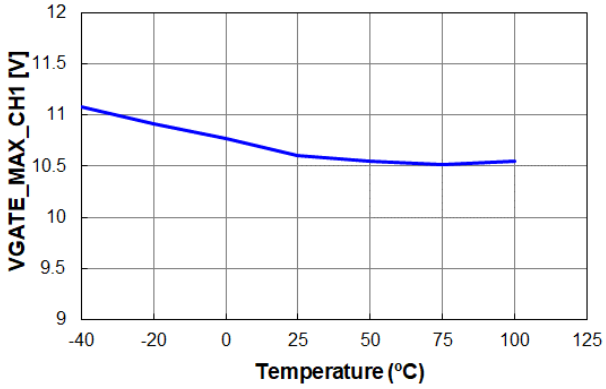


Figure 27. $V_{GATE\_MAX\_CH1}$ vs. Temperature

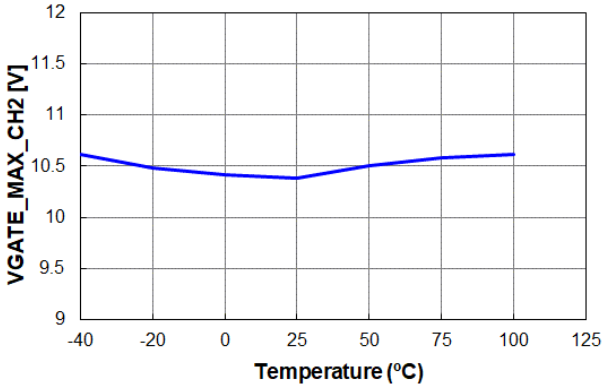


Figure 28. $V_{GATE\_MAX\_CH2}$ vs. Temperature

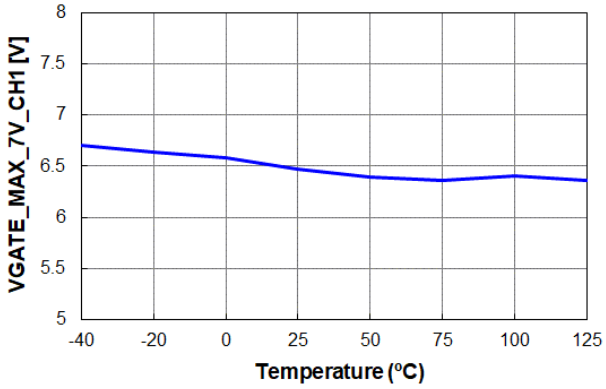


Figure 29. $V_{GATE\_MAX\_7V\_CH1}$ vs. Temperature

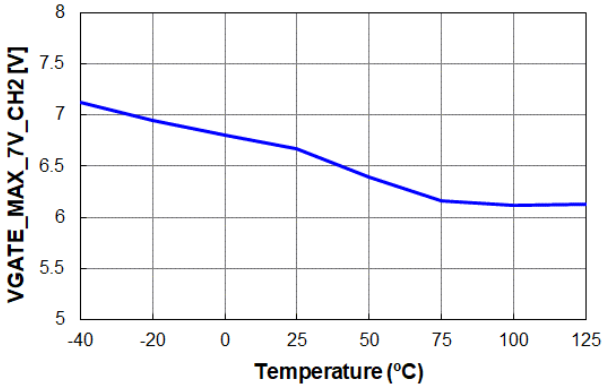


Figure 30. $V_{GATE\_MAX\_7V\_CH2}$ vs. Temperature

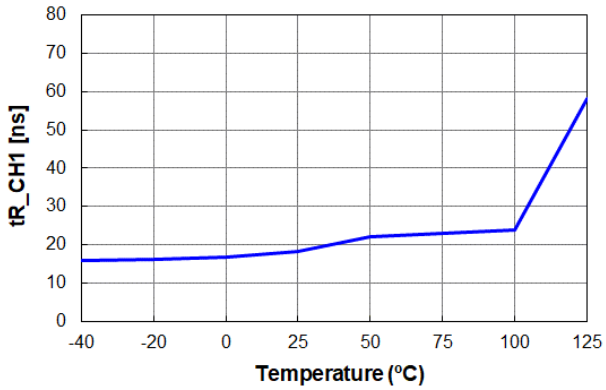


Figure 31. t_{R_CH1} vs. Temperature

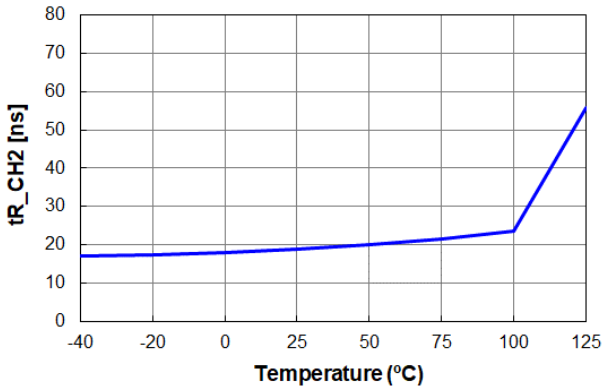


Figure 32. t_{R_CH2} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

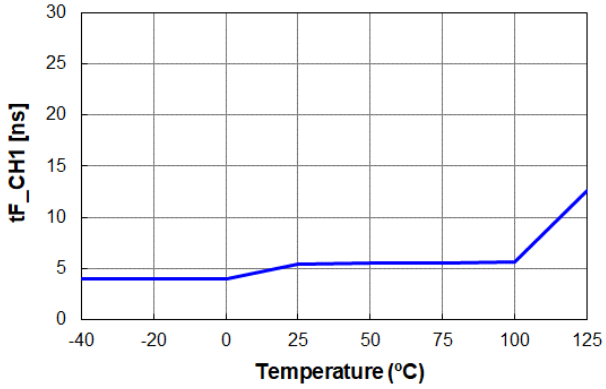


Figure 33. t_{F_CH1} vs. Temperature

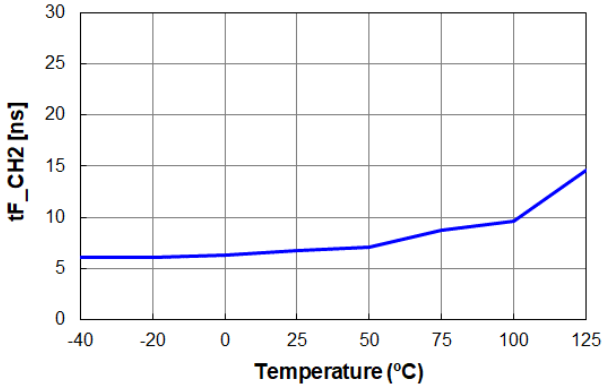


Figure 34. t_{F_CH2} vs. Temperature

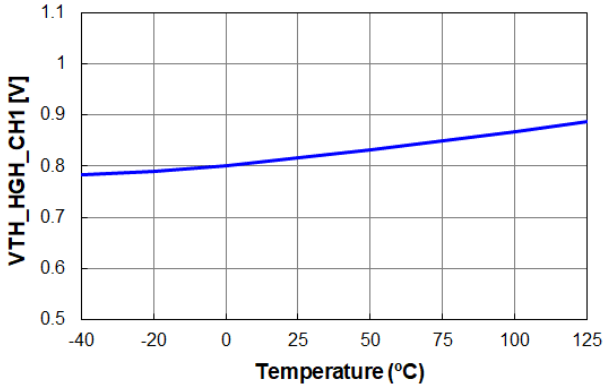


Figure 35. $V_{TH\_HIGH\_CH1}$ vs. Temperature

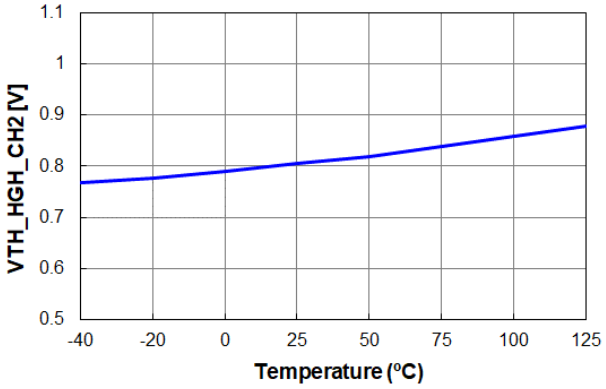


Figure 36. $V_{TH\_HIGH\_CH2}$ vs. Temperature

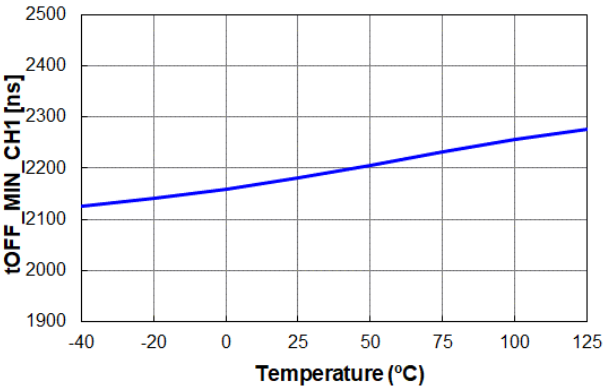


Figure 37. $t_{OFF\_MIN\_CH1}$ vs. Temperature

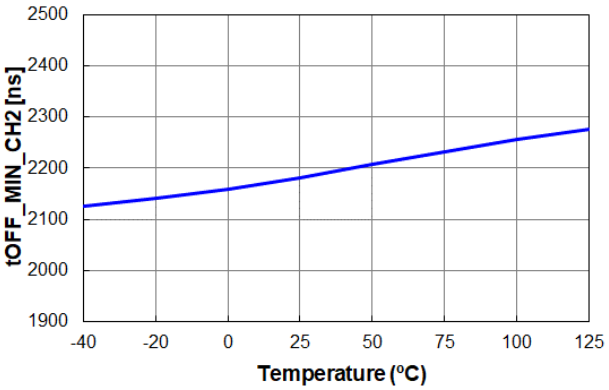


Figure 38. $t_{OFF\_MIN\_CH2}$ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

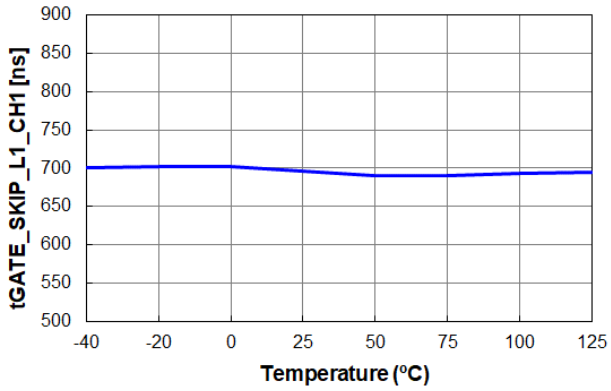


Figure 39. $t_{GATE\_SKIP\_L1\_CH1}$ vs. Temperature

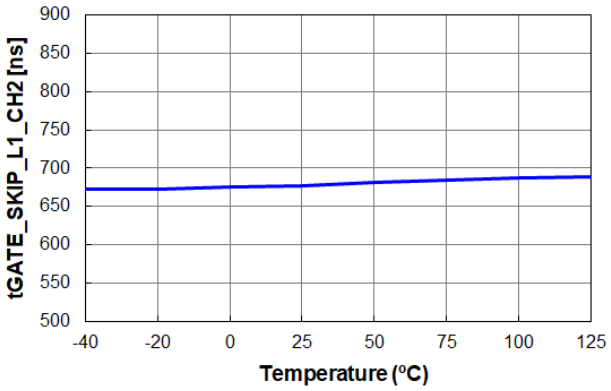


Figure 40. $t_{GATE\_SKIP\_L1\_CH2}$ vs. Temperature

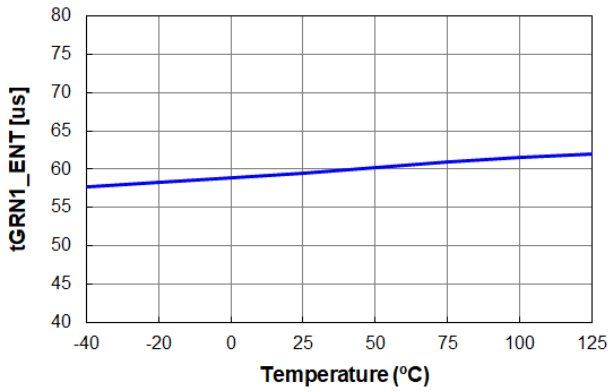


Figure 41. t_{GRN1_ENT} vs. Temperature

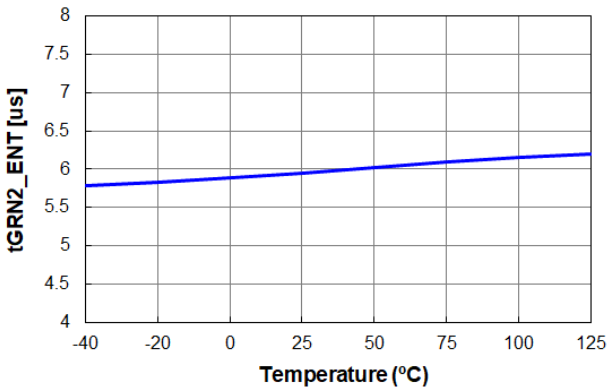


Figure 42. t_{GRN2_ENT} vs. Temperature

APPLICATION INFORMATION

Basic Operation Principle

NCP4318 controls the SR MOSFET based on the instantaneous drain−to−source voltage sensed across *DRAIN* and *SOURCE* pins. Before SR gate is turned on, SR body diode operates as the conventional diode rectifier. Once the body diode starts conducting, the drain−to−source voltage drops below the turn−on threshold voltage V_{TH_ON} which triggers the turn−on of the SR gate. Then, the drain−to−source voltage is determined by the product of turn−on resistance R_{DS_ON} of SR MOSFET and instantaneous SR current. When the drain−to−source voltage reaches the turn−off threshold voltage V_{TH_OFF}, as SR MOSFET current decreases to near zero, NCP4318 turns off the gate. If SR dead time is larger or smaller than the dead time regulation target. NCP4318 adaptively changes a virtual turn−off threshold voltage to regulate the dead time between t_{DEAD_LBAND} and t_{DEAD_HBAND} and to maximize system efficiency.

SR Turn−on Algorithm

When V_{D1} is lower than V_{TH_ON} by body diode conduction of SR MOSFET, turn−on comparator *COM1* outputs high. If an additional delay flag signal *DLY_EN1* is low, *VG1* goes high with 30 ns of t_{ON_DLY} and finally *GATE1* is charged by 1.5 A of sourcing current I_{SOURCE} of a gate driver.

On the other hand, if *DLY_EN* is turned to high by current inversion detection *SRC_INV* high or *GREEN* high, additional turn−on delay is applied by adaptive turn−on delay block. In this case, SR gate is turned on after a body diode conduction time longer than t_{ON_DLY2} is confirmed.

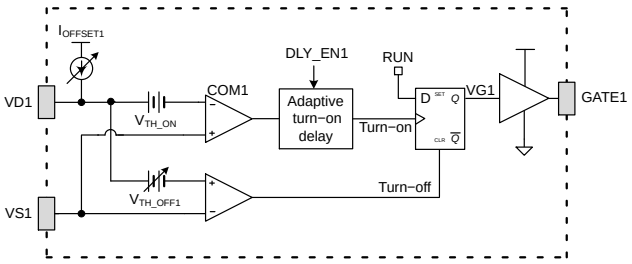


Figure 43. SR Turn−on Algorithm

SR Turn−off Algorithm

Since a SR turn−off method determines SR conduction time and stable SR operation, the SR turn−off method is one of important feature of the SR controllers. One of the conventional method uses present information by an instantaneous drain voltage. This method is widely used and easy to realize, and can prevent late turn−off. However, it frequently shows premature turn−off due to parasitic stray inductances of PCB pattern and lead frame of SR MOSFET. In another method, SR conduction time is predicted by using previous cycle drain voltage information. Since it can prevent the premature turn−off, it is good for the system with constant operating frequency and turn−on time. However, in case of the frequency varying system, it may lead to late turn−off during frequency increasing so that negative current can flow in the secondary side.

To achieve both advantages, NCP4318 adopts mixed type turn−off control method which utilizes a hysteresis band dead time control. As shown in Figure 44, the instantaneous drain voltage V_{D1} is compared with a virtual V_{TH_OFF1} to turn off SR gate. The virtual V_{TH_OFF1} is adaptively changed to compensate the stray inductance effect and regulate t_{DEAD} between t_{DEAD_LBAND} and t_{DEAD_HBAND} regardless of parasitic inductances. Therefore, NCP4318 can show robust operation with minimum dead time.

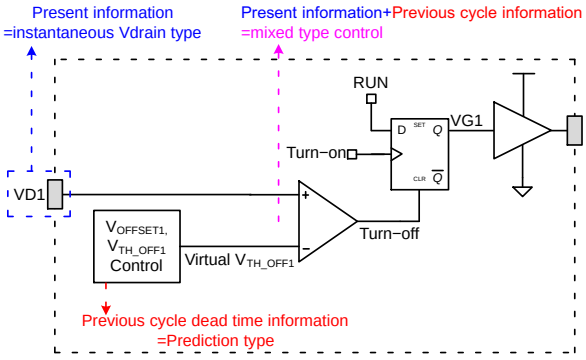


Figure 44. SR Turn−off Algorithm

Hysteresis Band Dead Time Regulation Control

The stray inductance of SR MOSFET induces a positive voltage offset across drain−to−source voltage when SR current decreases. This makes drain−to−source voltage of SR MOSFET higher than the product of R_{DS_ON} and instantaneous SR current, which results in premature SR turn−off as shown in Figure 45. Since the induced offset voltage is changed as the output load current changes, the SR dead time needs to tune with the output load variation. To compensate it, NCP4318 utilizes the virtual turn−off threshold voltage which is determined by 31 steps of internal turn−off threshold voltages $V_{TH\_OFF(n)}$ and modulated offset voltage $V_{OFFSET(n)}$ as shown in Figure 44. The virtual turn−off threshold voltage and the offset voltage can be expressed as:

$$\text{Virtual } V_{TH\_OFF1} = V_{TH\_OFF1(n)} - V_{OFFSET1(n)} \quad \text{(eq. 1)}$$

$$V_{OFFSET1(n)} = R_{OFFSET1} \times I_{OFFSET1(n)} \quad \text{(eq. 2)}$$

where, R_{OFFSET} is the external drain sensing resistance and $I_{OFFSET1}$ has 10 μA of step size. So, $V_{OFFSET1}$ is used for fine tuning of Virtual V_{TH_OFF1}. When $V_{OFFSET1}$ has saturated to maximum or minimum values, V_{TH_OFF1} changes to its next step for coarse control.

In Figure 46, if a measured dead time T_{DEAD} is larger than upper band of t_{DEAD_HBAND}, V_{OFFSET} is decreased by one

step decrease of I_{OFFSET} next switching cycle. As a result, the dead time is decreased by increase of virtual V_{TH_OFF}, and becomes closer to t_{DEAD_HBAND}, as shown in Figure 47. If the dead time is placed between lower band t_{DEAD_LBAND} and upper band t_{DEAD_HBAND} in Figure 48, V_{OFFSET} stay as is and waits until T_{DEAD} is larger than t_{DEAD_HBAND} or smaller than t_{DEAD_LBAND} Therefore, the dead time is regulated between the lower band t_{DEAD_LBAND} and the upper band t_{DEAD_HBAND} regardless of parasitic inductances. This hysteresis band dead time control provides stable operation in light load condition by minimized dead time variation.

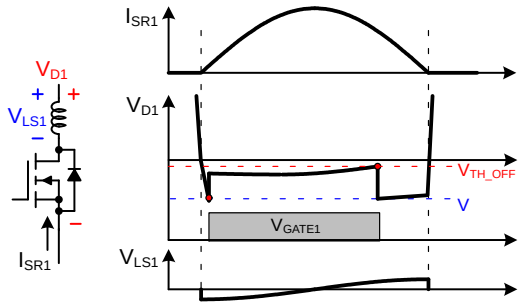


Figure 45. Premature SR Turn−off by Stray Inductor

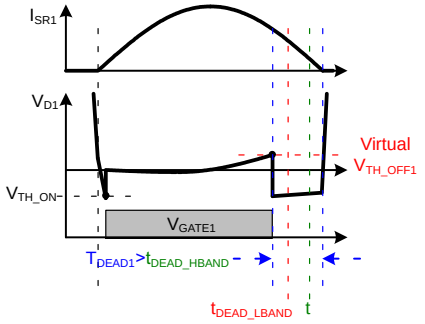


Figure 46. When T_{DEAD} > t_{DEAD_HBAND}

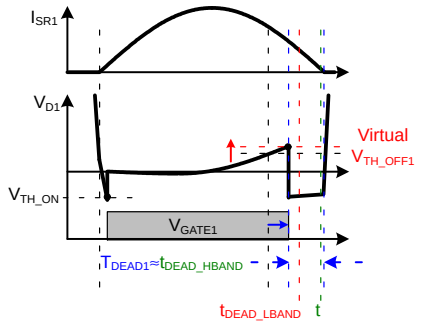


Figure 47. When T_{DEAD} = t_{DEAD_HBAND}

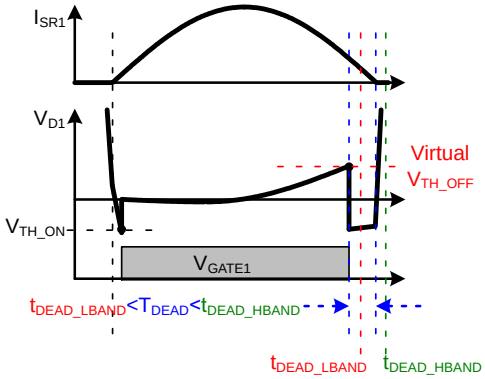


Figure 48. When t_{DEAD_LBAND} < T_{DEAD} < t_{DEAD_HBAND}

Advanced Adaptive Minimum Turn−on Time

When SR gate is turning on, there may be severe oscillation in drain−to−source voltage of SR MOSFET, which results in several turn−off mis−triggering as shown in Figure 49. To provide stable SR gate signal without short pulses, it is desirable to have large turn−off blanking time (=minimum turn−on time) until the drain voltage oscillation attenuates. However, too large blanking time results in an inversion current problem under light load condition, where the SR conduction time is shorter than the minimum turn−on time.

To solve this issue, NCP4318 has adaptive minimum turn−on time t_{MIN_ON} where the turn−off blanking time changes in accordance with the SR conduction time t_{SR_COND}(n−1) measured in previous switching cycle. The SR conduction time is measured by the time from SR gate rising edge to where the drain sensing voltage V_{D1} is higher than 0.85 V of V_{TH_HGH}. So, the adaptive minimum on−time t_{MIN_ON} is defined by 50% of $t_{SR\_COND}(n−1)$ as shown in Figure 50. During the t_{MIN_ON}, SR turn−off by Virtual V_{TH_OFF1} is prohibited to prevent abnormal turn−off by the drain sensing noise. The minimum value of t_{MIN_ON} and the maximum value of t_{MIN_ON} are defined by 200 ns and 5 μs, respectively. When the additional turn−on delay flag *DLY_EN1* is high in the light load condition, t_{MIN_ON} becomes 20% of $t_{SR\_COND}(n−1)$ as shown in Figure 51.

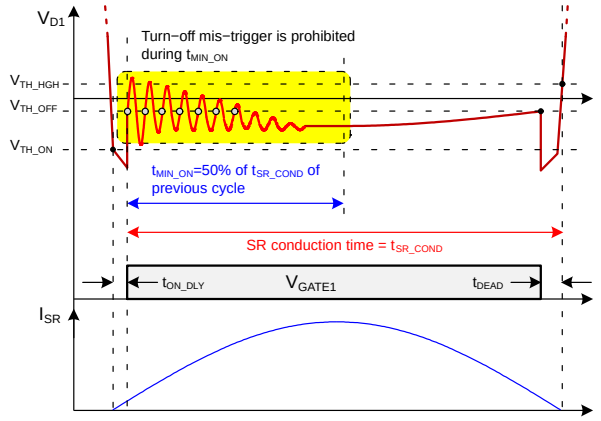


Figure 49. Minimum Turn−on Time and Turn−off Mis−triggering

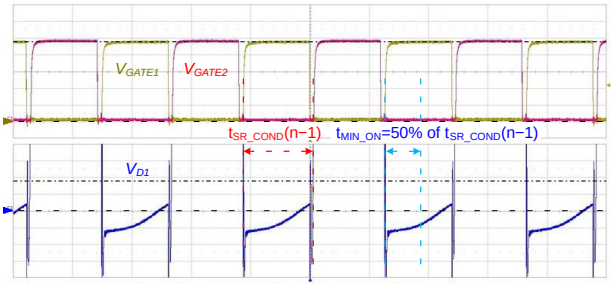


Figure 50. Minimum Turn−on Time t_{MIN_ON} when DLY_EN = 0

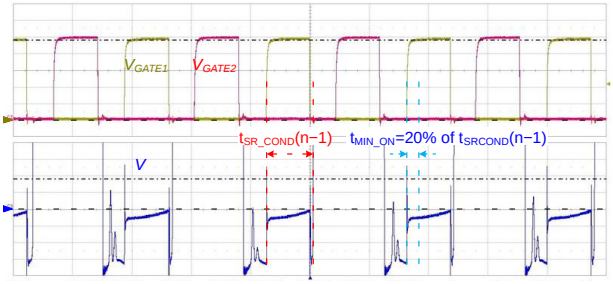


Figure 51. Minimum Turn−on Time t_{MIN_ON} when DLY_EN = 1

Current Inversion Detection

During SR operation, two types of inversion current may occur. First, leading edge inversion current is caused by the capacitive current spike in light load condition. In heavy load condition, the body diode of SR MOSFET starts conducting right after the primary side switching transition takeing place. However, when the resonance capacitor voltage amplitude is not large enough in light load condition, the voltage across the magnetizing inductance of the transformer is smaller than the reflected output voltage. Thus, the secondary side SR body diode conduction is delayed until the magnetizing inductor voltage builds up to the reflected output voltage. However, the primary side switching transition can cause capacitive current spike and turn on the body diode of SR MOSFET for a short time as shown in Figure 52, which induces SR turn−on mis−trigger. Finally, the turn−on mis−trigger makes leading edge inversion current in the secondary side.

The second inversion current is trailing edge inversion current caused by minimum on−time t_{MIN_ON}. If t_{MIN_ON} is longer than current transfer width from the primary side, trailing edge inversion current can happen as shown in Figure 53. If proper algorithm is not provided to prevent this inversion current, severe drain voltage spike may happen.

To prevent the both leading edge and trailing edge inversion currents, NCP4318 uses the current inversion detection function *SRC_INV*. When SR gate is turned on and current inversion occurs, the drain sensing voltage of SR MOSFET becomes positive value. In this condition, if V_{D1} is higher than 0mV with a light load detection flag signal *LLD*=0, or the virtual V_{TH_OFF} with *LLD* = 1 for t_{INV} of the detection debounce time, SR current inversion detection is triggered and turn−off SR gate immediately. Then, turn−on delay is increased to t_{ON_DLY2} from next turning−on.

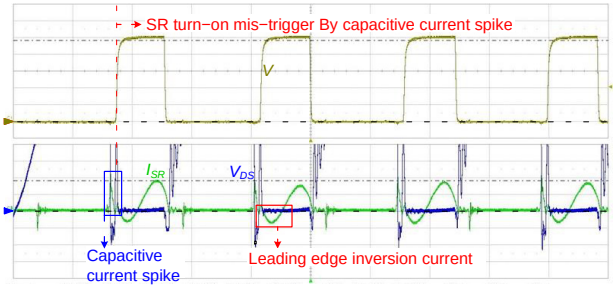


Figure 52. Leading Edge Inversion Current

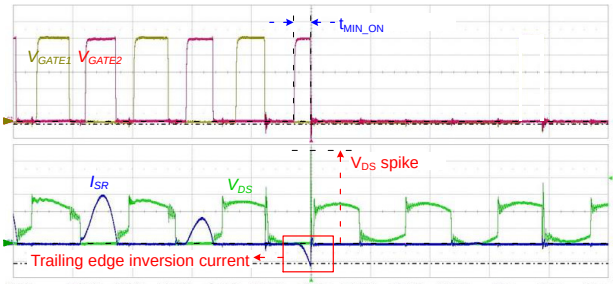


Figure 53. Trailing Edge Inversion Current

Light Load Detection (LLD)

Since NCP4318 adopts the dead time regulation control algorithm, the output load condition can be detected by the control variable V_{TH_OFF}(n). As shown in Figure 54, when the output load is increased to the heavy load condition, V_{TH_OFF}(n) is also increased. Vice versa. Therefore, V_{TH_OFF} level can represent the output load condition.

When the control variable number '*n*' is lower than '7', NCP4318 detects a light load condition. So, light load detection flag signal *LLD* goes high. If '*n*' is higher than '8', *LLD* becomes low. This *LLD* signal is used for *SRC_INV* detection threshold voltage control and adaptive V_{GATE} control.

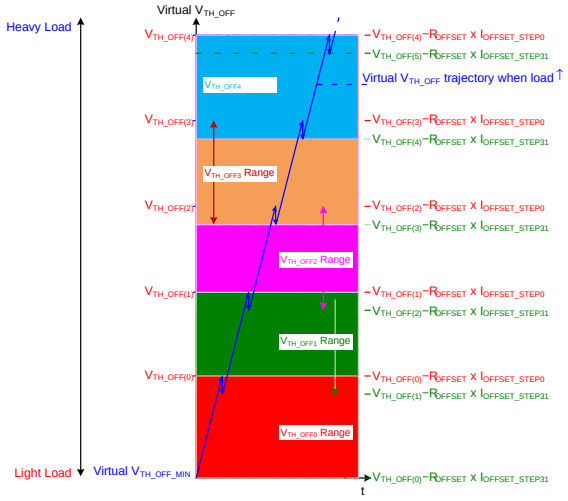


Figure 54. Virtual V_{TH_OFF} Trajectory when Iout Increases

Green Mode

In NCP4318, there are two stages to trigger *GREEN* function. *GREEN1* is for low power consumption in light load condition and *GREEN2* is for preparing *GREEN1* triggering.

When the LLC system in the primary side operates with skip mode under light load condition, NCP4318 can enter *GREEN1* mode to reduce operating current. In that condition, if V_{D1} has no switching operation for longer than t_{GRN1_ENT}, the *GREEN1* mode is activated as shown in Figure 55. Once NCP4318 is in the *GREEN1* mode, all the major functions are disabled to reduce the operating current down to 100 μA of I_{DD_GREEN}. After then, when NCP4318 exits from the *GREEN1* mode, four cycles of V_{D1} switching are required as shown in Figure 56.

Before *GREEN1* is triggered, if no switching operation of V_{D1} is longer than t_{GRN2_ENT}, 100 ns of *GREEN2* pulse is generated to reset adaptive dead time control variables including V_{TH_OFF} and I_{OFFSET}. In addition, the additional delay flag signal *DLY_EN* and the light load detection signal *LLD* become high. So, *GREEN2* prepares new SR operation start and allows soft increment of SR gate pulses next switching bundle.

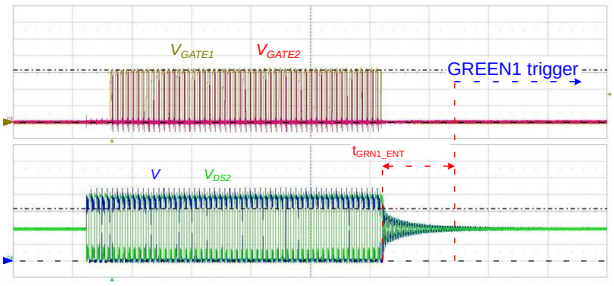


Figure 55. GREEN1 Enters

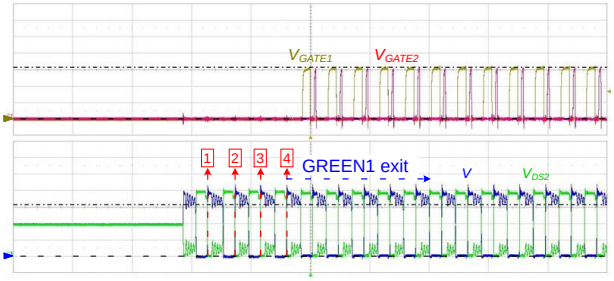


Figure 56. GREEN1 Exits

Adaptive V_{GATE} Control

In NCP4318, there are three condition to trigger adaptive V_{GATE} control. First one is the output load condition. In light load condition, to save SR gate driving current and maximize efficiency, NCP4318 adaptively changes the gate clamp voltage V_{GATE}. As shown in Figure 57, when LLD goes high, the gate clamp voltage is reduced from 10 V to 6 V. It could save 40% of gate driving power consumption. In heavy load condition, V_{GATE} comes back to 10 V for lower turn−on resistance R_{DS_ON} of SR MOSFET in Figure 58.

The second condition is the operating frequency. If the LLC operating frequency is higher than 200 kHz of f_{HFS_EN} in L−version and 250 kHz in H−version, NCP4318 reduces V_{GATE} for lower SR gate driving current.

The last condition is junction temperature T_J of IC. When T_J is higher than 105 °C of T_{OTP1}, V_{GATE} is changed to 6 V to reduce T_J. V_{GATE} comes back to 10 V, when T_J is lower than 80 °C of T_{OTP_RST}.

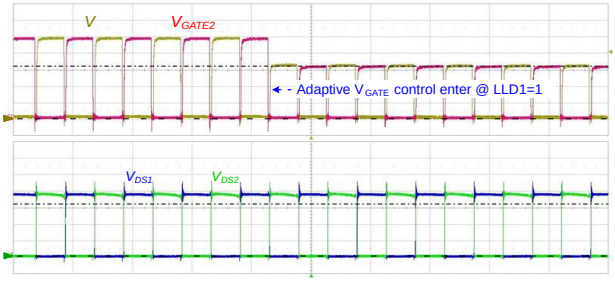


Figure 57. V_{GATE} Control Enters when LLD is High

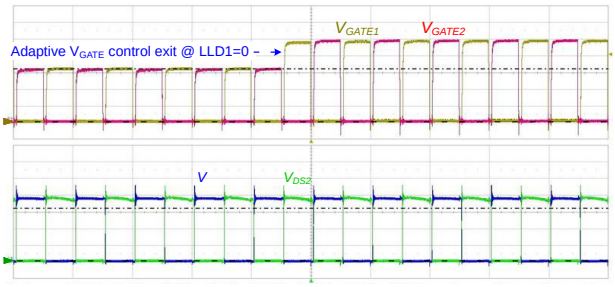


Figure 58. V_{GATE} Control Exits when LLD is Low

Soft Start

At the beginning of LLC startup, the operating frequency is severely changed and sometimes symmetrical 50% duty cycles between high−side and low−side power switches on the primary side cannot be guaranteed. It makes SR control difficult and unstable operation.

To avoid SR operation under the transition, soft−start function is utilized. In the first region of soft−start, SR gate is skipped during 256cycles to check whether LLC system is normal or not. After the first region, NCP4318 starts generating SR gate pulses with V_{GATE} = 6 V and V_{TH_OFF} = $V_{TH\_OFF\_RST}$ until *LLD* signal goes low. This allows soft−increment of SR gate pulses and gradual reduction of the SR dead time at startup.

Protection

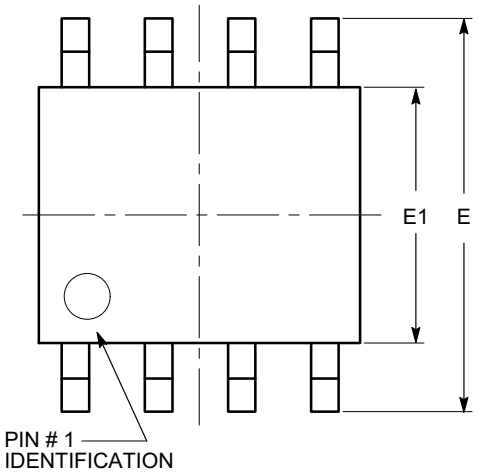
For higher system reliability, two protections are implemented in NCP4318. First one is the primary side shutdown protection. In SR controller point of view, NCP4318 cannot know directly the primary side abnormal gate off by a certain LLC protection or power−off. In that condition, SR gate should be turned off as soon as possible even in minimum on−time. Though *SRC_INV* function can turn−off SR gate at that moment, it has longer delay time for confirmation. For faster turn−off method, the primary shutdown protection is utilized.

When the LLC gate signal in the primary side is suddenly disappears, SR current shows inflection point which induces high dV/dt of drain sensing voltage. If the dV/dt is higher than a threshold level V_{SD_PRI}/t_{INV}, the protection is triggered and SR gate turns off immediately. In addition, it turns *GREEN1* high making 4 cycles gate skipping to ignore turn−on mis−trigger caused by energy bouncing in the secondary side.

The other protection is the abnormal drain sensing protection. In normal condition, when SR gate is turning on, V_{GATE} is higher than 4.5 V and the drain sensing voltage V_D should be lower than 0.85 V of V_{TH_HGH} due to the body diode conduction. However, in abnormal condition, V_D can be higher than V_{TH_HGH} even if V_{GATE} > 4.5 V due to V_D fluctuation. In that condition, NCP4318 triggers abnormal drain sensing protection and turns off SR gate and makes *GREEN1* high.

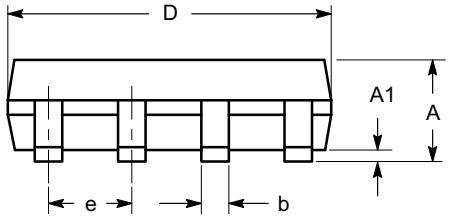
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD
ISSUE O

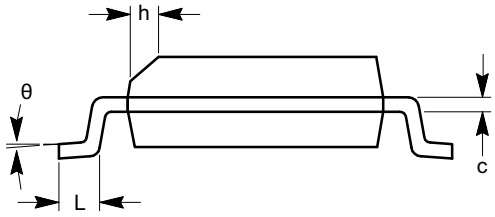


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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