Ultra Fast FET-Input Operational Amplifier

CORPORATION

LH0032 / LH0032C

FEATURES

- **500V/μs Slew Rate**
- **70MHz Bandwidth**
- **$10^{12}\Omega$ Input Impedance**
- **As Low as 2mV Max Input Offset Voltage**
- **FET Input**
- **Offset Null with Single Pot**
- **No Compensation for Gains Above 50**
- **Peak Output Current to 100mA**

GENERAL DESCRIPTION

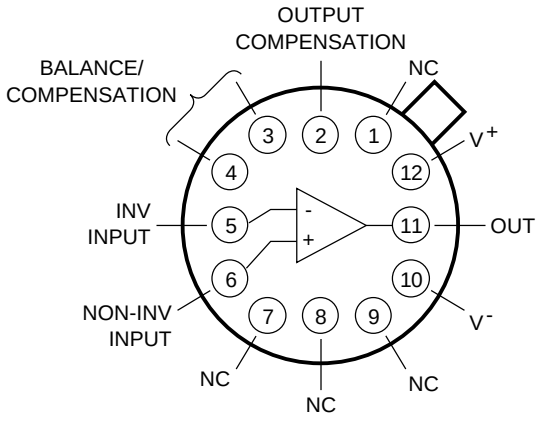
The LH0032 is a FET input, high slew rate amplifier capable of driving up to 100mA current.

With wide bandwidth, high slew rate, high input impedance and high current drive capability, LH0032 is an ideal choice for many applications that includes high speed integrator, video amplifier, summing amplifier, high speed D/A converters, etc.

ORDERING INFORMATION

Part	Package	Temperature Range
LH0032G	H12A (TO8-12 Lead)	-55^{o}C to $+125^{o}$C
LH0032CG	H12A (TO8-12 Lead)	-25^{o}C to $+85^{o}$C

CONNECTION DIAGRAMS



Top View

H12A

CALOGIC CORPORATION, 237 Whitney Place, Fremont, California 94539, Telephone: 510-656-2900, FAX: 510-651-1076

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S . . . . . ±18V
Input Voltage, V_{IN}. . . . . ±V_S
Differential Input Voltage . . . . . ±30V or± 2V_S
Power Dissipation, P_D
T_A = 25°C. . . . . 1.5W, derate 100°C/W to 125°C
T_C = 25°C. . . . . 2.2W, derate 70°C/W to 125°C

Operating Temperature Range, T_A
LH0032G . . . . . -55°C to +125°C
LH0032CG . . . . . -25°C to +85°C
Operating Junction Temperature, T_J . . . . . 175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temp. (Soldering, 10 seconds). . . . . 300°C

DC ELECTRICAL CHARACTERISTICS V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 1) ($T_A = T_j$)

SYMBOL	PARAMETER	LH0032			LH0032C			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
V_{OS}	Input Offset Voltage		2	5 10		2	15 20	mV		$T_A = T_J$ = 25°C (Note 3)
ΔVOS/ΔT	Average Offset Voltage Drift		15	50		15	50	µV/°C		(Note 4)
I_{OS}	Input Offset Current			25 250 25			50 500 5	pA pA nA	V_{IN} = 0	T_J = 25°C (Note 2) T_A = 25°C (Note 3)
I_B	Input Bias Current			100 1 50			500 5 15	pA nA nA		T_J = 25°C (Note 2) T_A = 25°C (Note 3)
V_{INCM}	Input Voltage Range	±10	±12		±10	±12		V	Note 6	
CMRR	Common Mode Rejection Ratio	50	60		50	60		dB	ΔV_{IN} = ±10V	
A_{VOL}	Open-Loop Voltage Gain	60	70		60	70		dB	V_O = ±10V, f = 1kHz R_L = 1kΩ (Note 7)	T_J = 25°C
		57			57					
V_O	Output Voltage Swing	±10	±13.5		±10	±13		V	R_L = 1kΩ	
I_S	Power Supply Current		18	20		20	22	mA	T_A = 25°C, I_O = 0 (Note 3)	
PSRR	Power Supply Rejection Ratio	50	60		50	60		dB	ΔV_S = 10V (±5 to ±15V)	

AC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25^oC$ (Note 5)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS	
S_R	Slew Rate	350	500		V/µs	A_V = +1	ΔV_{IN} = 20V
t_s	Settling Time to 1% of Final Value		100			A_V = -1	
t_s	Settling Time to 0.1% of Final Value		300		ns		
t_R	Small Signal Rise Time		8	20		A_V = +1, ΔV_{IN} = 1V	
t_D	Small Signal Delay Time		10	25			

Note 1. LH0032G/CG are 100% production tested as specified at 25^oC, Specifications at temperature extremes are verified by testing, periodic characterization, or correlation.

Note 2. Specification is at 25^oC junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25^oC$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60^oC above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 3. Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

Note 4. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25^oC and T_{MAX}, specifications at temperature are verified by testing, periodic characterization, or correlation.

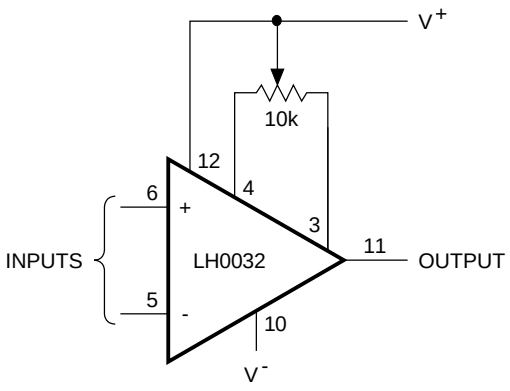
Note 5. Not 100% production tested; verified by testing, periodic characterization, or correlation.

Note 6. Guaranteed by CMRR test condition.

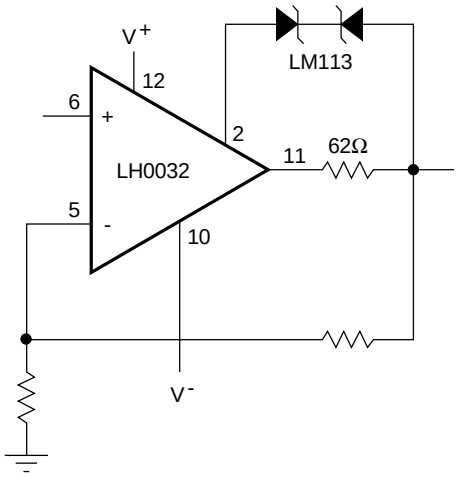
Note 7. Guaranteed thru correlated pulse testing at $T_j = 25^oC$.

AUXILIARY CIRCUITS

Offset Null

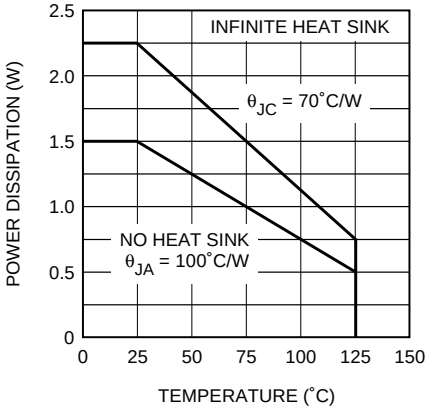


Output Short Circuit Protection

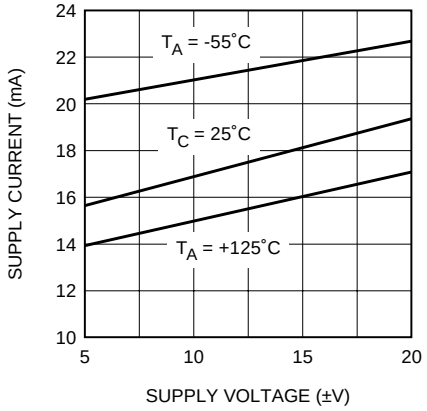


TYPICAL PERFORMANCE CHARACTERISTICS

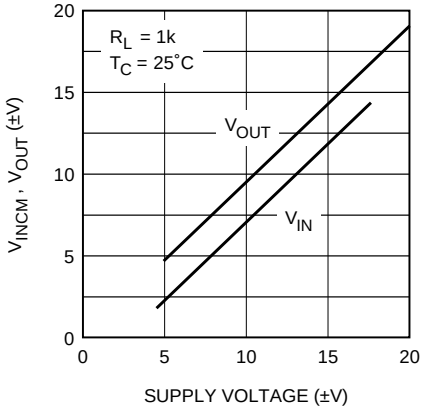
MAXIMUM POWER DISSIPATION



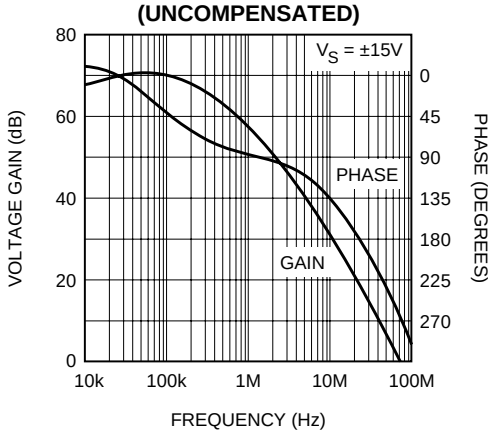
SUPPLY CURRENT vs. SUPPLY VOLTAGE



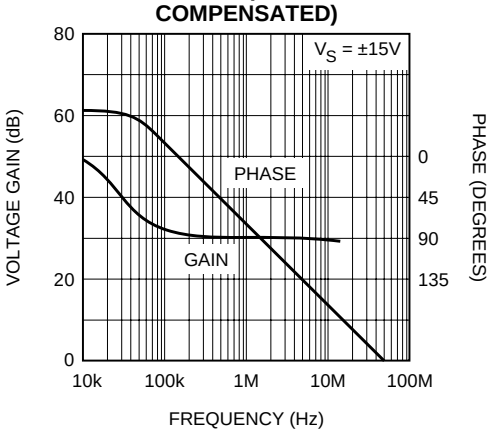
INPUT VOLTAGE RANGE AND OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



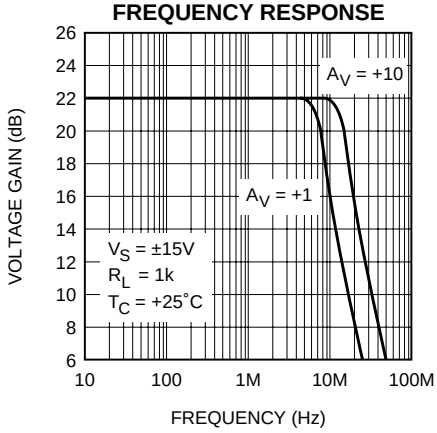
BODE PLOT (UNCOMPENSATED)



BODE PLOT (UNITY GAIN COMPENSATED)

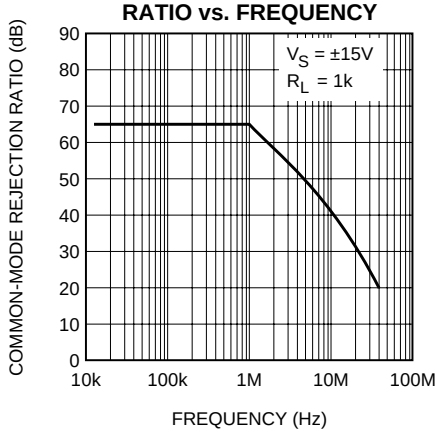


LARGE SIGNAL FREQUENCY RESPONSE

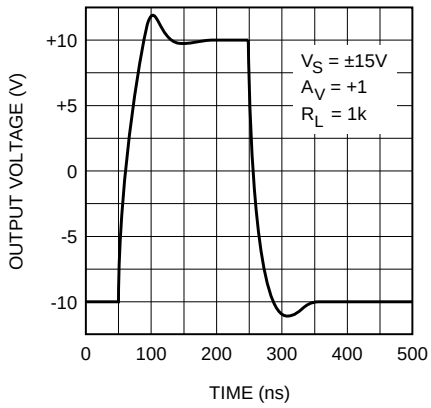


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

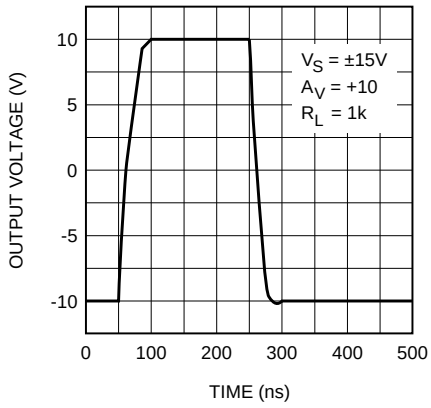
COMMON MODE REJECTION RATIO vs. FREQUENCY



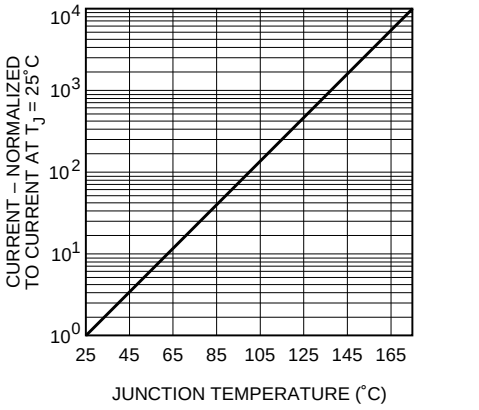
LARGE SIGNAL PULSE RESPONSE



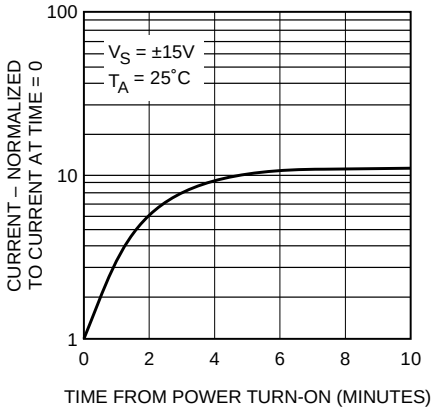
LARGE SIGNAL PULSE RESPONSE



NORMALIZED INPUT BIAS AND OFFSET CURRENT vs. JUNCTION TEMPERATURE

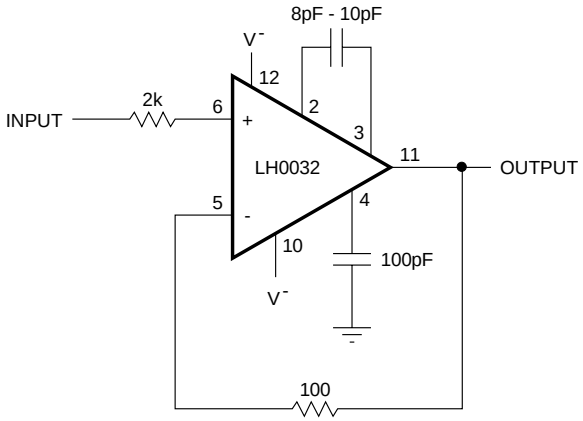


NORMALIZED INPUT BIAS CURRENT DURING WARM-UP

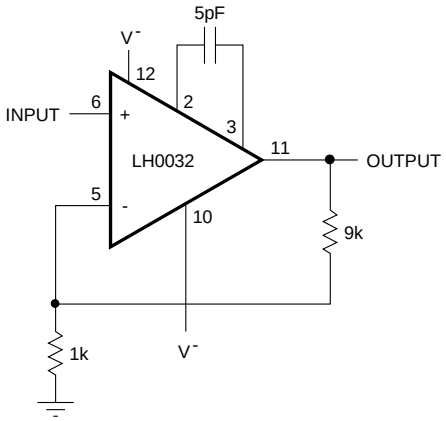


TYPICAL APPLICATIONS

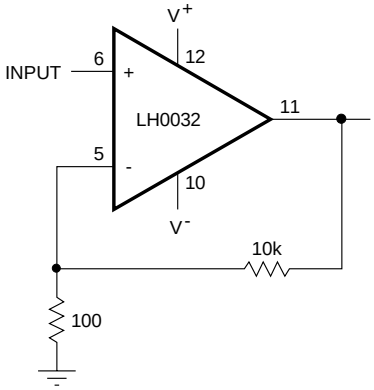
Unity Gain Amplifier



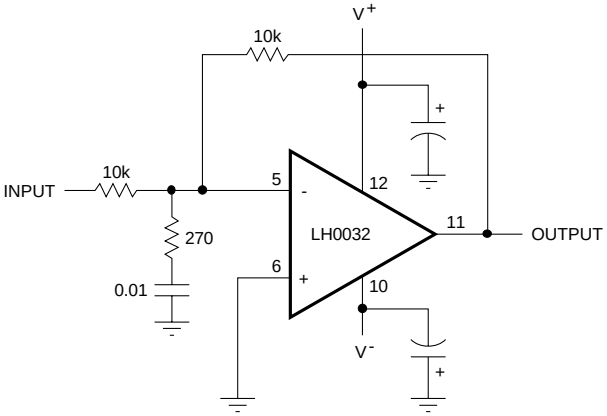
10X Buffer Amplifier



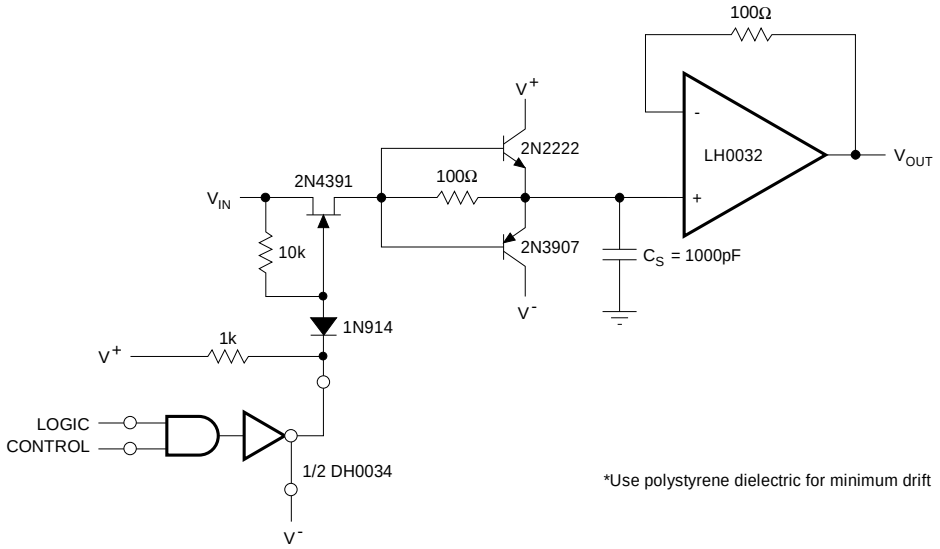
100X Buffer Amplifier



Non-Compensated Unity Gain Inverter



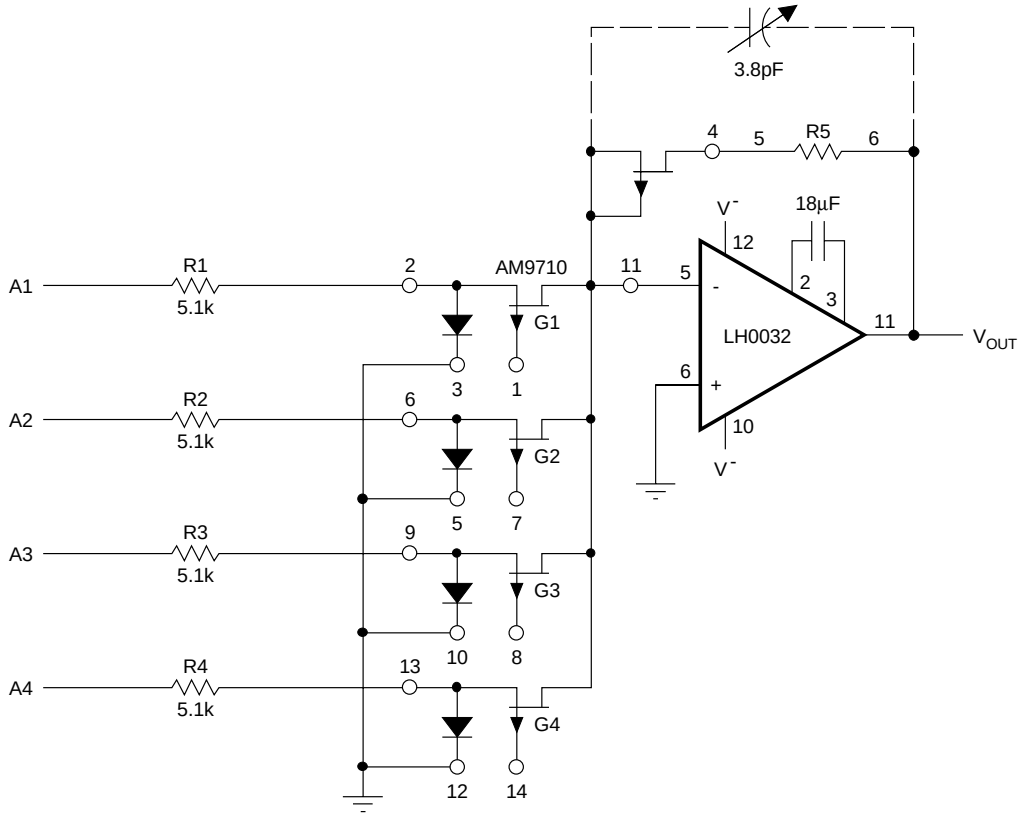
High Speed Sample and Hold



*Use polystyrene dielectric for minimum drift

TYPICAL APPLICATIONS (Continued)

High Speed Current Mode MUX



APPLICATION INFORMATION:

Power Supply Decoupling

The LH0032, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01µF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40-60°C above free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5-10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input

capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

Compensation

Two compensation schemes may be used, depending on the designer's specific needs.

The first technique is shown in *Figure 1.* It offers the best 0.1% settling time for a ±10V square wave input. The compensation capacitors C_C and C_A should be selected from *Figure 2* for various closed-loop gains. *Figure 3* shows how the LH0032 frequency response is modified for different value compensation capacitors.

Figure 1. LH0032 Frequency Compensation Circuit

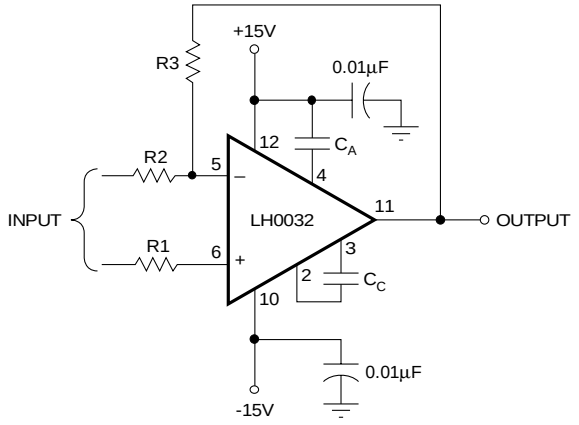


Figure 2. Recommended Value of Compensation Capacitor vs Closed-Loop Gain for Optimum Settling Time

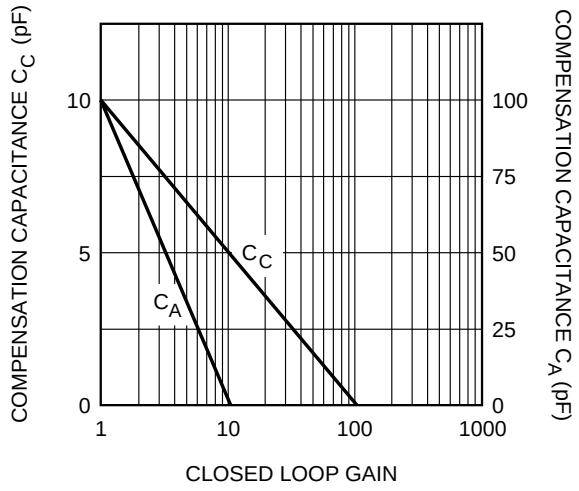


Figure 3. The Effect of Various Compensation Capacitors on LH0032 Open Loop Frequency Response

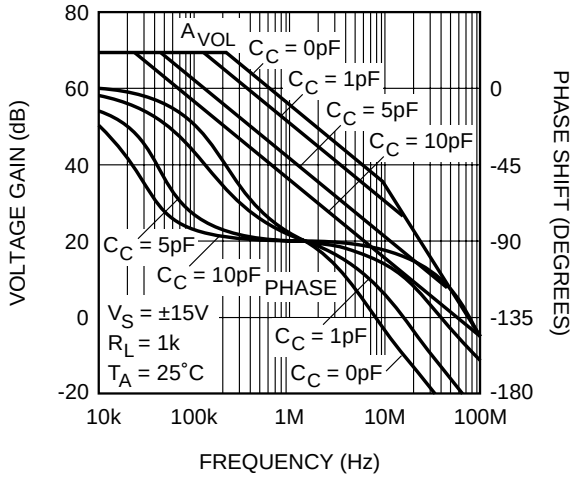
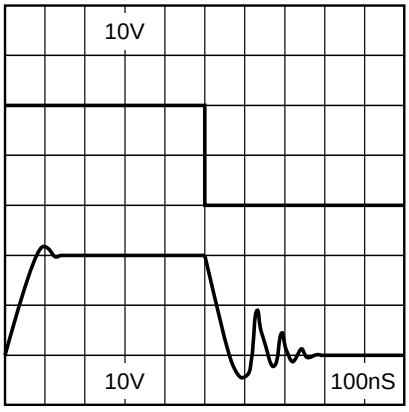


Figure 4. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: $T_A = 25^oC$, $C_C = 10pF$, $C_A = 100pF$



Although this approach offers the shortest settling time, the falling edge exhibits overshoot up to 30% lasting 200 to 300ns. *Figure 4* shows the typical pulse response.

If obtaining minimum ringing at the falling edge is the primary objective, a slight modification to the above is recommended. It is based on the same circuit as that of *Figure 1.*

The values of the unity gain compensation capacitors C_C and C_A should be modified to 5pF and 1000pF, respectively. *Figure 5* shows the suitable capacitance to use for various closed-loop gains. The resulting unity gain pulse response waveform is shown in *Figure 6.* The settling time to 1% final value is actually superior to the first method of compensation. However, the LH0032 suffers slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the previous scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slew rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required.

The second compensation scheme works well with both inverting or non-inverting modes. *Figure 7* shows the circuit schematic, in which a 270ohm resistor and a 0.01µF capacitor are shunted across the inputs of the device. This lag compensation introduces a zero in the loop modifying the response such that adequate phase margin is preserved at unity gain crossover frequency. Note that the circuit requires no additional compensation.

Figure 5. Recommended Value of Compensation Capacitor vs Closed-Loop Gain for Optimum Slew Rate

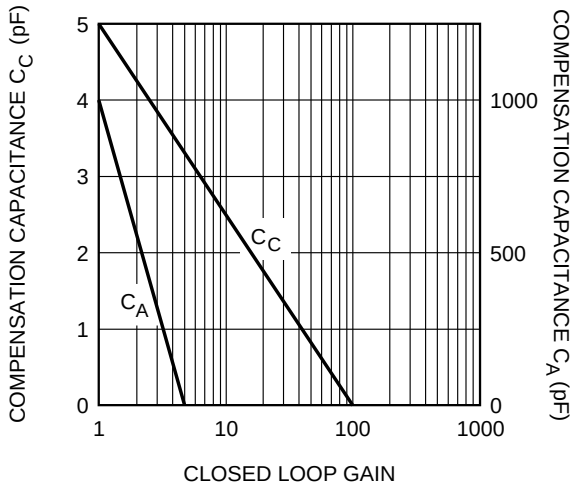


Figure 6. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: C_C = 5pF, C_A = 1000pF

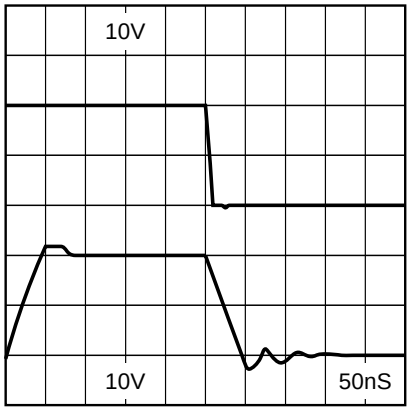
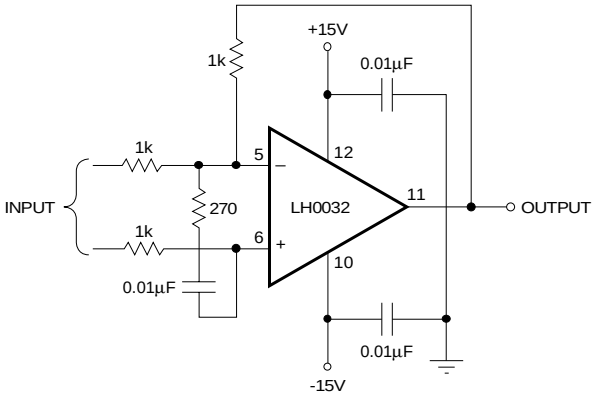


Figure 7. LH0032 Non-Compensated Unity Gain Compensation



Heat Sinking

While the LH0032 is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. However, that this will affect the stray capacitance to all pins and may thus require adjustment of circuit compensation values.