N-Channel JFET Switch

calogic CORPORATION

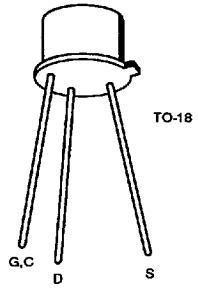
T-39-05

2N4856 – 2N4861

FEATURES

- Low $r_{DS(on)}$
- $I_{D(off)}$<250pA
- Switches ±10V Signals With ±15V Supplies (2N4858, 2N4861)

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Gate-Source or Gate-Drain Voltage	
2N4856-58	-40V
2N4859-61	-30V
Gate Current	50mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +200°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	1.8W
Derate above 25°C	10mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
2N4856	HermeticTO-18	-55°C to +200°C
X2N4856	Sorted Chips in Carriers	-55°C to +200°C
2N4857	HermeticTO-18	-55°C to +200°C
X2N4857	Sorted Chip in Carriers	-55°C to +200°C
2N4858	HermeticTO-18	-55°C to +200°C
X2N4858	Sorted Chip in Carriers	-55°C to +200°C
2N4859	HermeticTO-18	-55°C to +200°C
X2N4859	Sorted Chip in Carriers	-55°C to +200°C
2N4860	HermeticTO-18	-55°C to +200°C
X2N4860	Sorted Chip in Carriers	-55°C to +200°C
2N4861	HermeticTO-18	-55°C to +200°C
X2N4861	Sorted Chip in Carriers	-55°C to +200°C

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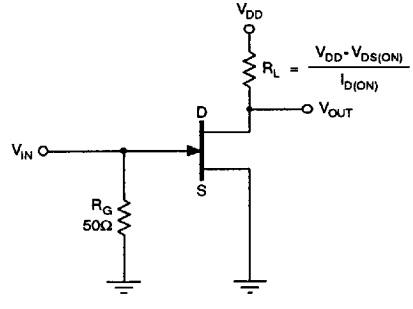
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER		2N4856		2N4857		2N4858		2N4859		2N4860		2N4861		UNITS	TEST CONDITIONS	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	-40		-40		-40		-40		-40		-40		V	I_G = -1μA, V_{DS} = 0	
		2N4859-61	-30		-30		-30		-30		-30		-30				
I_{GSS}	Gate Reverse Current			-0.25		-0.25		-0.25							nA	V_{GS} = -20V, V_{DS} = 0	
				-0.5		-0.5		-0.5							μA	V_{GS} = -20V, V_{DS} = 0 T_A = 150°C	
										-0.25		-0.25		-0.25	nA	V_{GS} = -15V, V_{DS} = 0	
										-0.5		-0.5		-0.5	nA	V_{GS} = -15V, V_{DS} = 0 T_A = 150°C	
$I_{D(off)}$	Drain Cutoff Current			250		250		250		250		250		250	pA	V_{DS} = 15V, V_{GS} = -10V	
				500		500		500		500		500		500	nA		T_A = 150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	-4	-10	-2	-6	-0.8	-4	V	V_{DS} = 15V, I_D = 0.5nA	
I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	50		20	100	8	80	mA	V_{DS} = 15V, V_{GS} = 0	
$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)		0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	V_{GS} = 0, I_D = ( )	
$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60		25		40		60	ohm	V_{GS} = 0, I_D = 0	f= 1kHz
C_{iss}	Common-Source Input Capacitance			18		18		18		18		18		18	pF	V_{DS} = 0, V_{GS} = -10V (Note 2)	f = 1MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8		8		8		8			
t_d	Turn-ON Delay Time (Note 2)			6		6		10		6		6		10	ns	464Ω (2N4856,59) V_{DD} = 10V, R_L = 953Ω (2N4857,60) $V_{GS(on)}$ = 0 1910Ω(2N4858,60) $V_{GS(off)}$ = -10V, I_D = 20mA (2N4856,9) $V_{GS(off)}$ = -6V, I_D = 10mA (2N4857,60) $V_{GS(off)}$ = -4V, I_D = 5mA (2N4858,61)	
t_r	Rise Time (Note 2)			3		4		10		3		4		10			
t_{off}	Turn-OFF Time (Note 2)			25		50		100		25		50		100			

NOTES: 1. Pulse test required, width = 100μs, duty cycle ≤10%.
2. For design reference only, not 100% tested.

SWITCHING TIMES TEST CIRCUIT



INPUT PULSE

RISE TIME 0.25ns
FALL TIME 0.75ns
PULSE WIDTH 100ns
PULSE DUTY CYCLE < 100%

SAMPLING SCOPE

RISE TIME 0.75ns
INPUT RESISTANCE 1MΩ
INPUT CAPACITANCE 2.5pF

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