Unigen Corp. Wireless Module Products

Part Number Family:
Narrowband UHF Radio Modules
UGW5S4XESM33 (ECHO-SMT-400)
UGW5S8XESM33 (ECHO-SMT-800)
UGW5S9XESM33 (ECHO-SMT-900)

Issue Date: 9-Jul-08

Revision: 0D

Revision History

Rev. No.	History	Issue Date	Remarks
0.1	Draft	8-Feb-08	Update Reference Documents, Functional Description
0.9	Initial release	25-Feb-08	FCC Data to be added after characterization
0.91	Second Draft	7-Jul-08	Improved features and content
0D	Third Draft	9-Jul-08	Corrected Pin assignments

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PRODUCT INTRODUCTION

The Unigen ECHO-SMT products are drop-in replacements for Semtech DP1205CxxxLF modules. This product is based on the Semtech XE1205 UHF transceiver. Three versions are available; 902, 868 and 433 MHz. The ECHO module is an SPI peripheral used with an external microcontroller. Echo offers best-in-class receiver sensitivity and automated packet handling. UHF links offer superior range and Non-Line-of-Sight performance compared to 2.4 GHz systems..

FEATURES AND BENEFITS

- Narrowband UHF Transceiver Module
- 433/ 868/ 915 MHz Versions
- Data Rate 152.3 kbit/s (304.7 kbPS max)
- Best Sensitivity -118 dBm @ 1.2 kBPS
- Programmable RF Power Output up to +15 dBm
- Programmable Frequency Synthesizer
- 25 kHz channel spacing
- -37 dBc ACPR @ 25 kHz/CH (RFOP3 Mode)
- 915, 868 or 433 MHz ISM Band-pass SAW filters included
- 16-Byte FIFO with Interrupts (IRQ on Full, IRQ on Empty)
- Pattern Recognition (IRQ on match)
- RSSI Window Comparator with IRQ
- Buffered FIFO and continuous streaming data modes.
- Bit-Synchronizer for clean Rx Data and Clock recovery
- User Defined 50 Ohm Antenna
- Metal Shield
- Surface Mount with tape and reel packaging
- 30.5 mm x 18.5 mm
- Supply Voltage 2.4 V – 3.6 V
- Rx Line Power 14 mA typ
- Tx Line Power 62 mA @ +15 dBm typ
- Line Power Sleep Mode 200 nA typ
- Industrial Temperature Rating -40 to +85 ºC
- RoHS 6 Compliant

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Applications

- long-range low-power point-to-point systems
- Non-Line-of-Sight radio links
- Narrowband and Wideband Security Systems
- Voice and Data over an RF Link
- Process and Building Controls
- Access Controls
- Home Automation
- Home Appliance Interconnections
- Industrial Equipment Controls
- Remote data gathering
- Telemetry
- Cable Replacement
- Phone quality audio Wireless Local Loops
- Konnex and KNX compatible systems
- EN 300-220-1 V1.3.1 systems
- Out-of-band control channel for 2.4 and 5 GHz systems.
- Automatic Meter Reading
- Alarms
- Baby monitors
- Irrigation controls

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PRODUCT DESCRIPTION

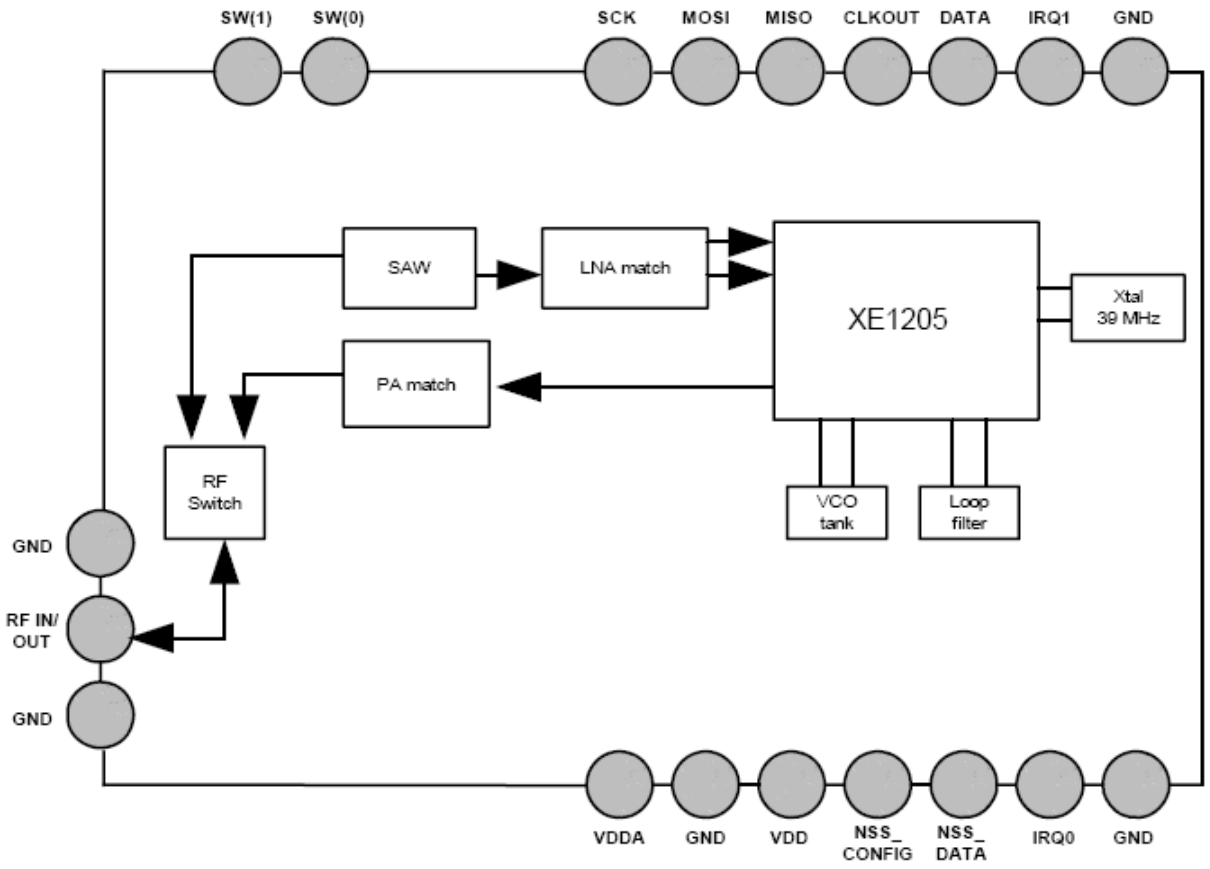
ECHO Module

The ECHO is a complete Radio Transceiver Module operating in the license free ISM (Industrial Scientific and Medical) UHF bands. The ECHO modules come pre-tuned for 433, 868, or 902 MHz. Based on the XE1205 transceiver, the ECHO offers the unique advantage of both narrow-band and wide-band communication. Offering high output power and exceptional receiver sensitivity, the radio module is suitable for applications seeking to satisfy the European (ETSI EN300-220-1 and EN301 439-3) or the North American (FCC part 15.247 and 15.249) regulatory criterion.

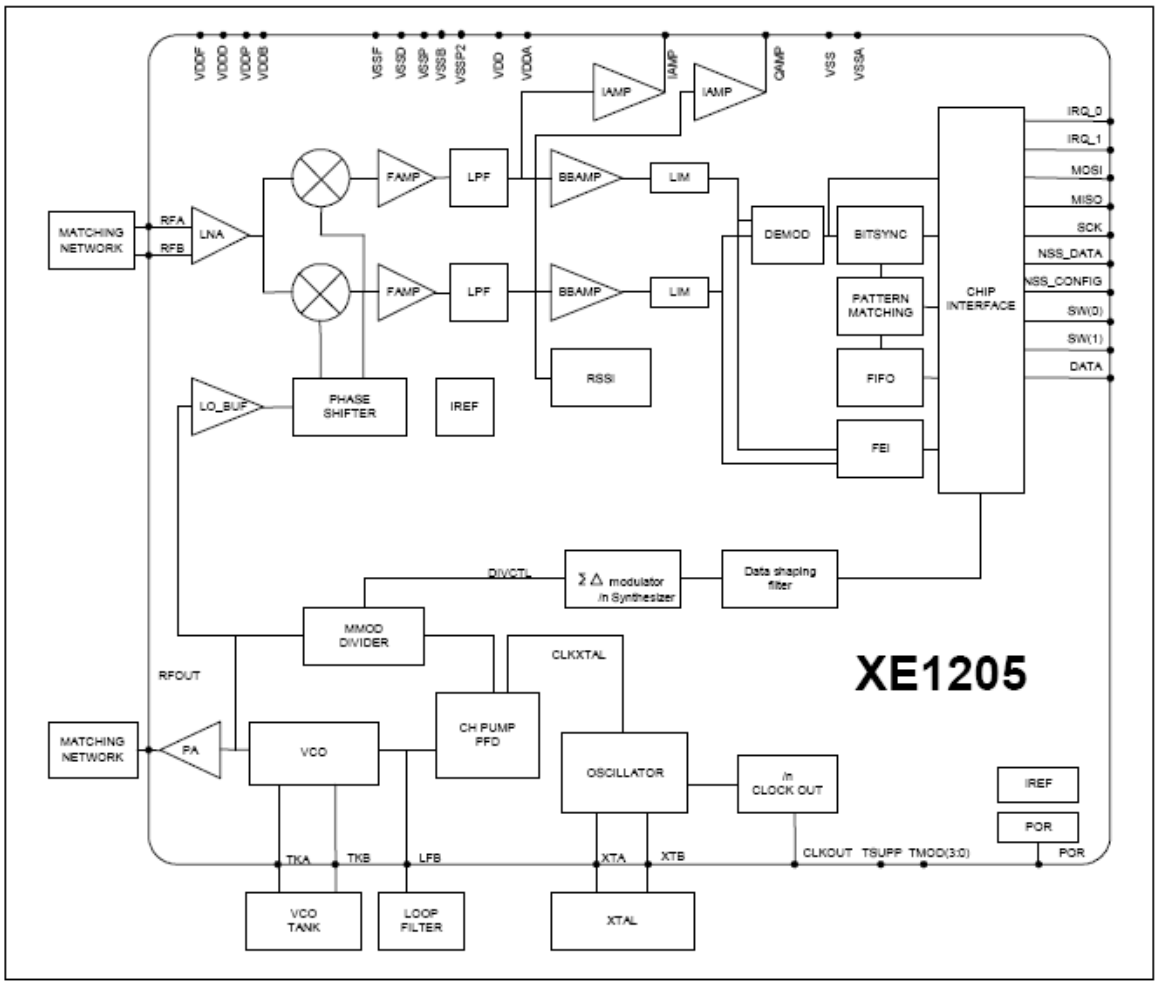
XE1205 Transceiver IC

The XE1205 single-chip solution is an integrated circuit intended for use as a low cost FSK transceiver to establish a frequency-agile, half-duplex, bi-directional RF link, with non-return to zero data coding. The device is available in a VQFN 48 package and is designed to provide a fully functional multi-channel FSK transceiver. It is intended for applications in the 433 MHz and 868 MHz European bands and the North American 915 MHz ISM band. The single chip transceiver operates down to 2.4V. Its ability to operate with 25 kHz channel spacing makes it compliant with requirements of ETSI EN300 220-1 and makes the XE1205 ideal for automatic meter reading and alarms.

Functional Block Diagrams

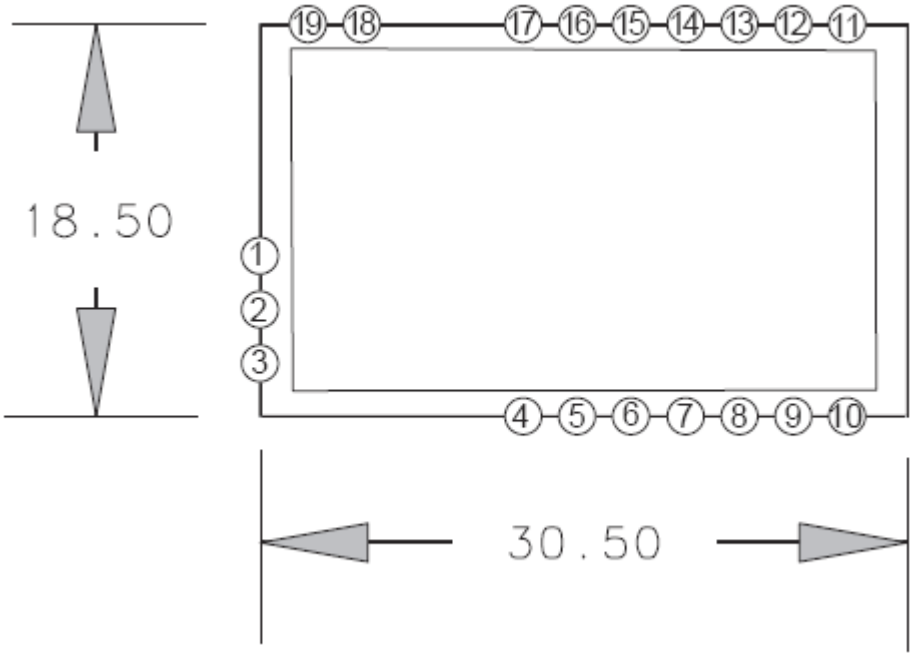


Module Block Diagram



XE1205 Block Diagram

PIN ASSIGNMENT



ECHO Module Pin Locations

PIN FUNCTIONS

PIN	NAME	I/O	DESCRIPTION
1	GND		Ground
2	RF_IN_OUT	IN/OUT	RF Input / Output terminal
3	GND		Ground
4	VDDA		Supply Voltage
5	GND		Ground
6	VDD		Supply Voltage
7	NSS_CONFIG	IN	SPI SELECT CONFIG
8	NSS_DATA	IN	SPI SELECT DATA / DATAIN
9	IRQ0	OUT	Interrupt (PATTERN/FIFOEMPTY)
10	GND		Ground
11	GND		Ground
12	IRQ1	OUT	Interrupt (DCLK/FIFOFULL)
13	DATA	IN/OUT	Data
14	CLKOUT	OUT	Output clock at reference frequency divided by 2, 4, 8, 16, 32
15	MISO	OUT	SPI Master Input Slave Output
16	MOSI	IN	SPI Master Output Slave Input
17	SCK	IN	SPI CLOCK
18	SW(0)	IN/OUT	Transmit/Receive/Stand-by/Sleep Mode Select
19	SW(1)	IN/OUT	Transmit/Receive/Stand-by/Sleep Mode Select

Pin Assignment

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
VCC	Supply Voltage – Radio SOC	-0.3	3.9	VDC
TS	Storage Temperature Range	-55	125	°C
TAP	Ambient Temperature with Power Applied	-40	85	°C
VLI	VDC to Logic Inputs	-0.3	VCC + 0.3	VDC
SDVD	Static Discharge Voltage Digital		>2000	VDC
SDVR	Static Discharge Voltage RF		>1100	VDC

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of this module. Avoid using the module outside the recommended operating conditions defined below. This module is ESD sensitive and should be handled and/or used in accordance with proper ESD mitigation.

RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Value			
		Min.	Typ.	Max	Unit
VCC	Supply Voltage	2.4	3.0	3.6	VDC
TOC	Operating Temperature Range	-40	25	85	°C
GND	Ground Voltage		0		VDC

RF AND ELECTRICAL CHARACTERISTICS

The table below gives the specifications of the ECHO modules under the following conditions: Supply voltage VDD = 3.3V, temperature = 25°C, frequency deviation Δf = 5 kHz, Bit-rate = 4.8 kbit/s, base-band filter bandwidth BWSSB = 10 kHz, carrier frequency fc = 434 MHz for the UGW5S4XESM33, fc = 869 MHz for the UGW5S8XESM33 and fc = 915 MHz for the UGW5S9XESM33, bit error rate BER = 0.1% (measured at the output of the bit synchronizer), antenna output matched at 50 Ω.

Symbol	Description	Condition(s)	MIN	TYP	MAX	UNIT
FR	Synthesizer Frequency Range	UGW5S4XESM33	433		435	MHz
		UGW5S8XESM33	868		870	MHz
		UGW5S9XESM33	902		928	MHz
IDDSL	Sleep mode supply current		-	0.2	1	µA
IDDST	Standby mode supply current	39 MHz running	-	0.85	1.1	mA
IDDR	RX mode supply current			14	16.5	mA
IDDT	TX mode supply current	P_{RF} = 5 dBm		33	40	mA
		P_{RF} = 15 dBm		62	75	
RFS	RF Sensitivity	A-Mode		-113	-110	dBm
RFS_12	RF Sensitivity @ 1.2Kb/s	A-Mode, BER = 0.1%		-118	-115	dBm
FDA	Frequency Deviation	Programmable	1	-	255	kHz
BR	Bit rate	Programmable	1.2	-	152.3	Kb/s
RFOP	RF output power	Programmable				dBm
		RFOP1	-3	0	-	
		RFOP2	2	5	-	
		RFOP3	7	10	-	
		RFOP4	12	15	-	
TS_STR	Transmitter wake up time	From oscillator enable	-	250	350	µS
TS_SRE	Receiver wake up time	From oscillator enable	-	700	850	µS
TS_OS	Quartz oscillator wake up time	Fundamental	-	1	2	mS
VIH	Digital input level high	% VDD	75	-	-	%
VIL	Digital input level low	% VDD	-	-	25	%

RF Characteristics

Name	Description	Min	Typ(25°C)	Max	Units
XO	Onboard Crystal		39.000		MHz
XO Offset	Crystal Tolerance		±10	±50	PPM
XO Drift	Crystal Drift		±5	±15	PPM/ºC
SCLK	SPI Clock	not specified		2	MHz

Clock Specifications

AGENCY CERTIFICATIONS (PRE-SCAN)

//DATA NEEDED//

REGULATORY COMPLIANCE STATEMENT

The module has been pre-scanned against the relevant requirements of standards: EN 300 328, EN 301 489-17, FCC part 15 and Industry Canada RSS-210. The module is certified by the regulatory authorities in the USA and Canada and complies with the applicable essential requirements of the Radio & Telecommunication Terminal Equipment (R&TTE) directive in the EU. The module can thus be incorporated into products sold worldwide with little or no additional testing of the module itself. The end product must meet the appropriate technical requirements that apply to that product type but re-certification of the radio module is not required in the USA and Canada.

In the EU, the integrator is responsible for evaluating their product type per the essential performance requirements of the R&TTE directive (except those associated with the module), declaring compliance and then notifying the member states prior to marketing the product (because the module uses a frequency band that is not harmonized in the EU). It is the responsibility of the module integrator to obtain the necessary approval to sell products incorporating this module in other countries outside of North America and the EU. The report of measurements performed on the module in compliance with the FCC rules and EN standards can be used in these submittal (as the requirements in many other markets around the world are based in part or in whole on the standards prevalent in North America and the EU).

FUNCTIONAL OVERVIEW

ECHO Module Functional Description

The ECHO is a complete Radio Transceiver Module operating in the license free ISM (Industrial Scientific and Medical) UHF bands. The ECHO modules come pre-tuned for 433, 868, or 902 MHz. Based on the XE1205 transceiver, the ECHO offers the unique advantage of both narrow-band and wide-band communication. Offering high output power and exceptional receiver sensitivity, the radio module is suitable for applications seeking to satisfy the European (ETSI EN300-220-1 and EN301 439-3) or the North American (FCC part 15.247 and 15.249) regulatory criterion.

The module is based on the Semtech XE1205 transceiver. The ECHO module offers best-in-class sensitivity and high power for outstanding long-range communication. The module is an SPI peripheral used with an external controller. ECHO offers a buffered data mode using the on-board 16-Byte FIFO, or Direct Digital Interface for streaming data. In buffered mode the SPI can be used for both data and control. In streaming mode XE1205 features de-multiplexed data and control paths with an RF bit-synchronizer for stable data and glitch-free clock recovery. The module is offered in an SMT for factor available in tape and reel packaging for automated assembly. Users will have to supply an external antenna via the 50 Ohm single-ended RF interface to motherboard. Echo offers designers outstanding performance for where range is critical.

XE1205 Functional Description

The XE1205 is a direct conversion (Zero-IF) half-duplex data transceiver. It includes receiver, transmitter, frequency synthesizer and control logic. The circuit is intended primarily for operation in the following three ISM frequency bands 433 MHz, 868 MHz, and 915 MHz with a same 39MHz reference crystal and uses 2-level FSK modulation.

The XE1205 is programmed by a microcontroller through the 3-wire fully-compatible SPI serial bus (MOSI, MISO, and SCK) to write to and read from the configuration registers.

The XE1205 consists of the following main functional blocks:

The receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver comprises a low-noise amplifier, down-conversion mixers, baseband filters, baseband amplifiers, limiters, demodulator and bit synchronizer. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream DATAOUT and synchronized clock DCLK. This may be easily used to sample the DATAOUT signal with minimal external processor overhead. In addition, the receiver includes a Received Signal Strength Indicator (RSSI) function and a Frequency Error Indicator (FEI) function that provides an indication of the local oscillator

frequency error. A pattern recognition function may be used to detect a user-programmable reference word in the incoming bit stream. The bandwidth of the base-band filters, the frequency deviation of the expected incoming FSK signal as well as the bit rate of the received data signal are all user-programmable. The receiver also embeds an automatic frequency offset cancellation to compensate local oscillator drifts due to XTAL.

The transmitter performs the modulation of the carrier by an input baseband data signal and the transmission of the modulated signal. The frequency synthesizer is modulated directly. The modulated signal is then amplified by the on-chip RF power amplifier. The output power is user-programmable to one of four possible values. The frequency deviation and the bit rate for the transmit signal are the same as those programmed for the receiver section. User-defined pre-filtering should be enabled to ensure compliance with the requirements of ETSI EN 300 220-1 regarding transmission at 25 kHz channel spacing.

The frequency synthesizer generates the local oscillator (LO) signal for the receiver section as well as the FSK modulated signal for the transmitter section. The core of the synthesizer is implemented with a PLL structure. The frequency is user-programmable with a frequency resolution of approximately 500 Hz in the 433 MHz, 868 MHz and 915 MHz ISM frequency bands. This section includes a crystal oscillator whose signal is the reference for the PLL. This reference frequency is divided by 2, 4, 8, 16, or 32 and is made available at the CLKOUT pin to serve as a clock signal for an external processor.

The control block generates the control signals according to the setting in its set of configuration registers.

The service block performs all the necessary functions for the circuit to work properly, including the internal voltage and current sources.

Data Operation Modes

The XE1205 is user-programmable between two modes of operation:

Continuous Mode: each bit transmitted or received is accessed directly at the DATA input/output pin.

Buffered Mode: a 16-byte FIFO is used to store each data byte transmitted or received. This data is written to/read from the FIFO via the SPI bus. It reduces processor overhead and reduces connections (the DATA input/output pin is not used in this operation mode)

In receiver mode, two lines are dedicated to interrupt information. The interrupt pins are IRQ0 and IRQ1. IRQ0 has 3 selectable sources. IRQ1 has 2 selectable sources. The two following tables summarize the interrupt management.

IRQParam_RX_irq_0	MCParam_Buffered_mode	IRQ0	IRQ0 Interrupt source
00	1	Output	No interrupt available
01	1	Output	Write_Byte
10	1	Output	/fifoempty
11	1	Output	Pattern
00	0	Output	Pattern
01	0	Output	RSSI_irq
10	0	Output	Pattern
11	0	Output	Pattern

IRQ0 Interrupt Sources in Receive Mode

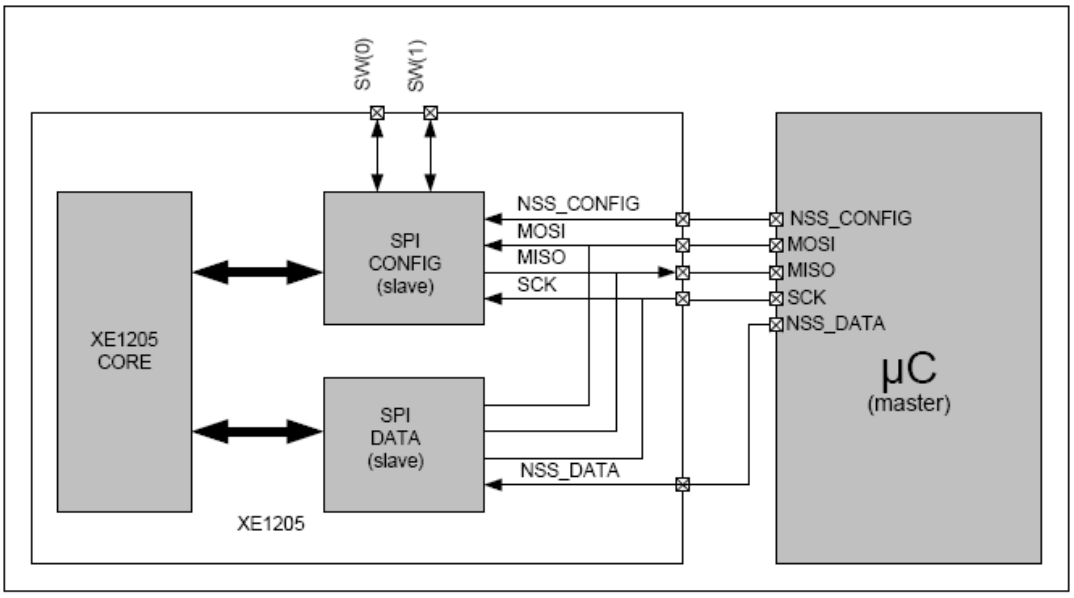
IRQParam_RX_irq_1	MCParam_Buffered_mode	IRQ1	IRQ1 Interrupt source
00	1	Output	No interrupt available
01	1	Output	Fifofull
10	1	Output	RSSI_irq
11	1	Output	RSSI_irq
00	0	Output	DCLK
01	0	Output	DCLK
10	0	Output	DCLK
11	0	Output	DCLK

IRQ1 Interrupt Sources in Receive Mode

DIGITAL INTERFACE

Serial Control Interface

The XE1205 contains two SPI-compatible serial interfaces, one to send and read the chip configuration, the other to send and receive data in buffered mode. Both interfaces are configured in slave mode and share the same pins MISO (Master In Slave Out), MOSI (Master Out Slave In), SCK (Serial Clock). Two additional pins are required to select the SPI interface: NSS_CONFIG to change or read the transceiver configuration, and NSS_DATA to send or read data. The figure below shows connections between the transceiver and a microcontroller when buffered mode is used.



Serial Control Interface

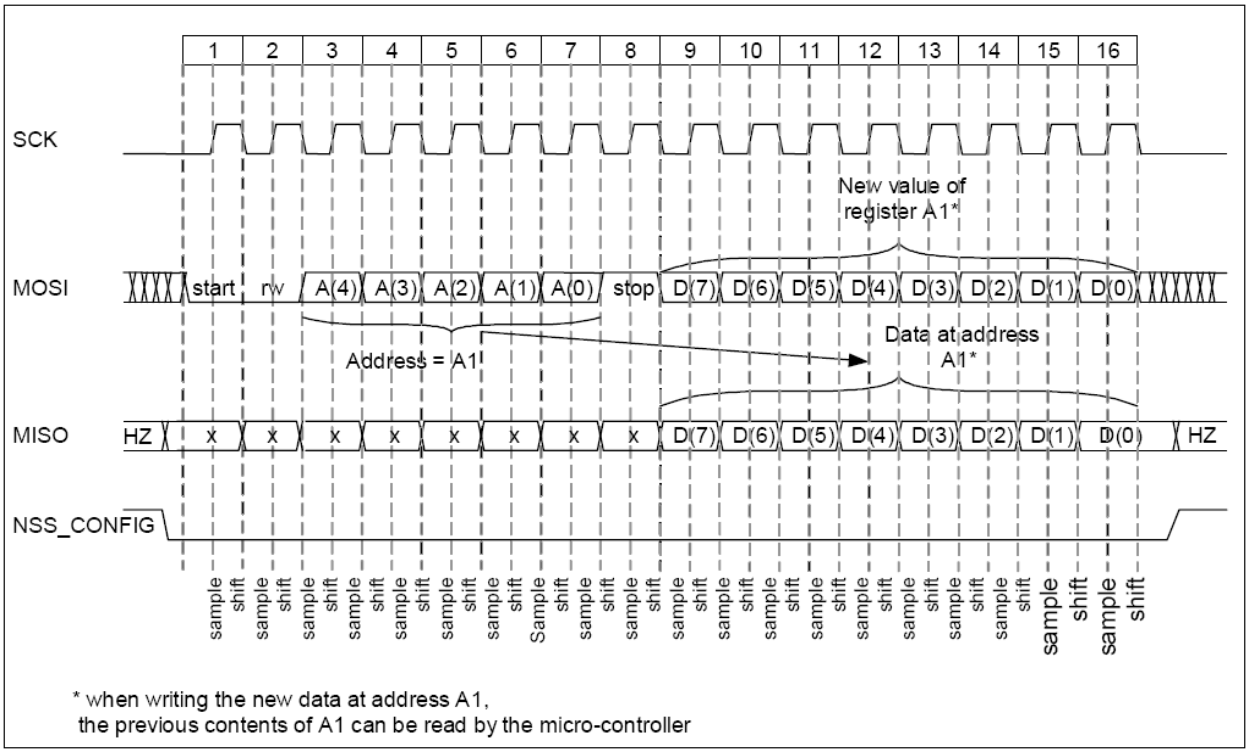
It is possible to change between the four modes (sleep, stand-by, receive, transmit) by using the two-bit signal SW(1:0). This option is enabled by setting the bit MCParam_Select_mode to '1' in the configuration register.

A byte transmission can be seen as a rotate operation between the value stored in an 8 bit shift register of the master device (the microcontroller for instance) and the value stored in an 8 bit shift register of the selected slave device (the transceiver). The SCK line is used to synchronize both SPI interfaces. Data is transferred full-duplex from master to slave through the MOSI line and from slave to master through the MISO line. The most significant bit is always sent first. In

both SPI interfaces the rising SCK edge is used to sample the received bit, and the falling SCK edge shifts the data inside the shift register. Max SCK frequency is 2MHz.
The NSS_CONFIG or NSS_DATA signal is controlled by the master device and should remain low during the byte transmission. It is not necessary to toggle the NSS_CONFIG signal back to high and back to low between each transmitted byte. However It is necessary to toggle the NSS_DATA signal back to high and back to low between each transmitted byte. The transmission is synchronized by the NSS_CONFIG or NSS_DATA signal. While the NSS_CONFIG or NSS_DATA is high, the counters controlling transmission are reset. Reception starts with the first clock cycle after the falling edge of NSS_CONFIG or NSS_DATA; if either signal goes high during a byte transmission the counters are reset and the byte has to be retransmitted.

Chip configuration via SPI_CONFIG interface

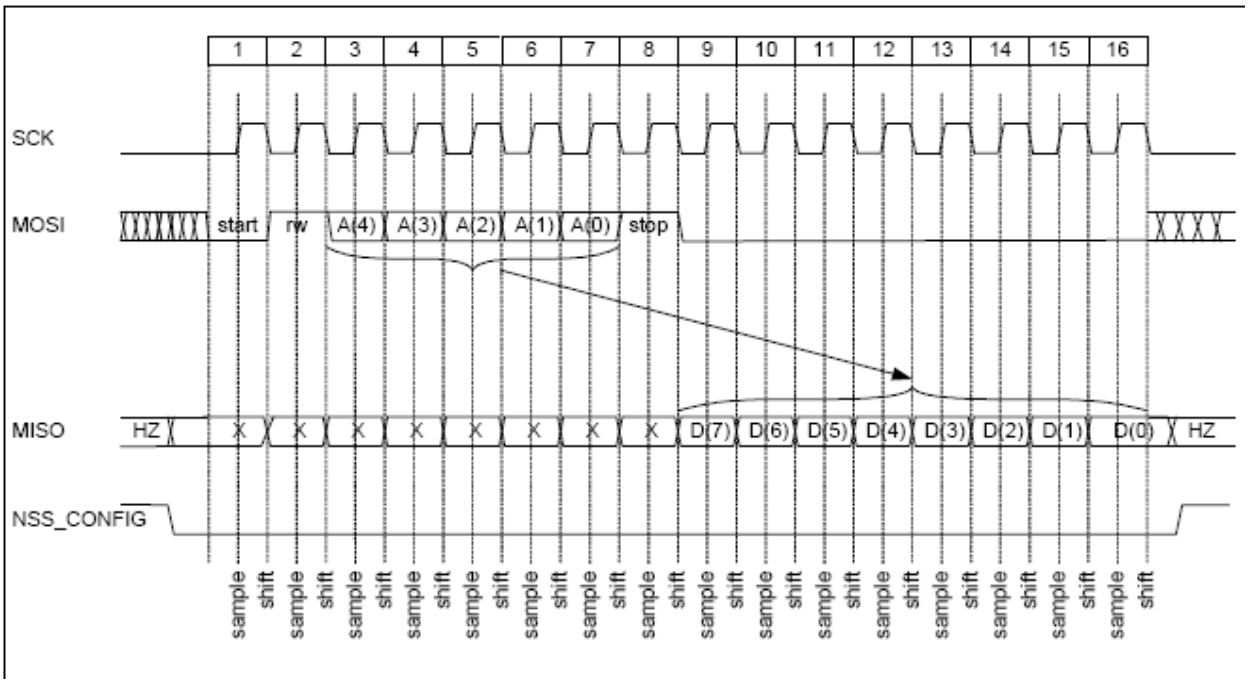
The SPI_CONFIG interface is selected if NSS_CONFIG is low even if the circuit is in buffered mode and NSS_DATA is low (SPI_CONFIG has priority). To configure the transceiver two bytes are required; the first byte contains a start bit (equal to 0), R/W information ('1' for a read operation or '0' for a write operation), 5 bits for the address of the register and finally a stop bit (equal to '1'). The second byte contains the data to be sent in write mode or the new address to read from in read mode. The figure below shows the timing diagram for a typical write sequence:



SPI Write Sequence

NSS_CONFIG must remain low during the transmission of the two bytes (address and data); if it goes high after the first byte, then the next byte will be considered as an address byte. When writing more than one register successively, NSS_CONFIG does not need to make a high to low transmission between two write sequences. The bytes are alternatively considered as an address byte followed by a data byte.

The read sequence via the SPI_CONFIG interface is similar to the write one except that the data byte contains all zeroes



SPI Read

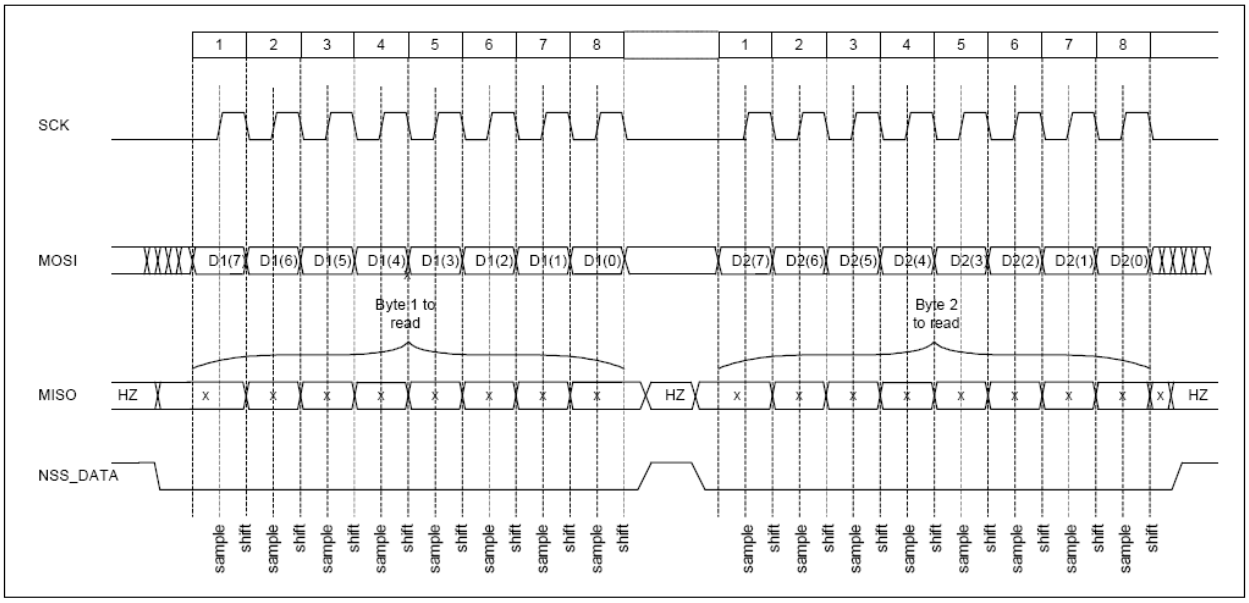
Data transmission and reception via SPI_DATA interface.

When the transceiver is used in buffered mode, the data exchange with a micro-controller is done via the SPI_DATAinterface. In transmit mode the 16 byte FIFO can be filled as long as it is not full (IRQ_1 can be used if FIFO_full is mapped). In receive mode, the FIFO may be read if one of the following events occurs:

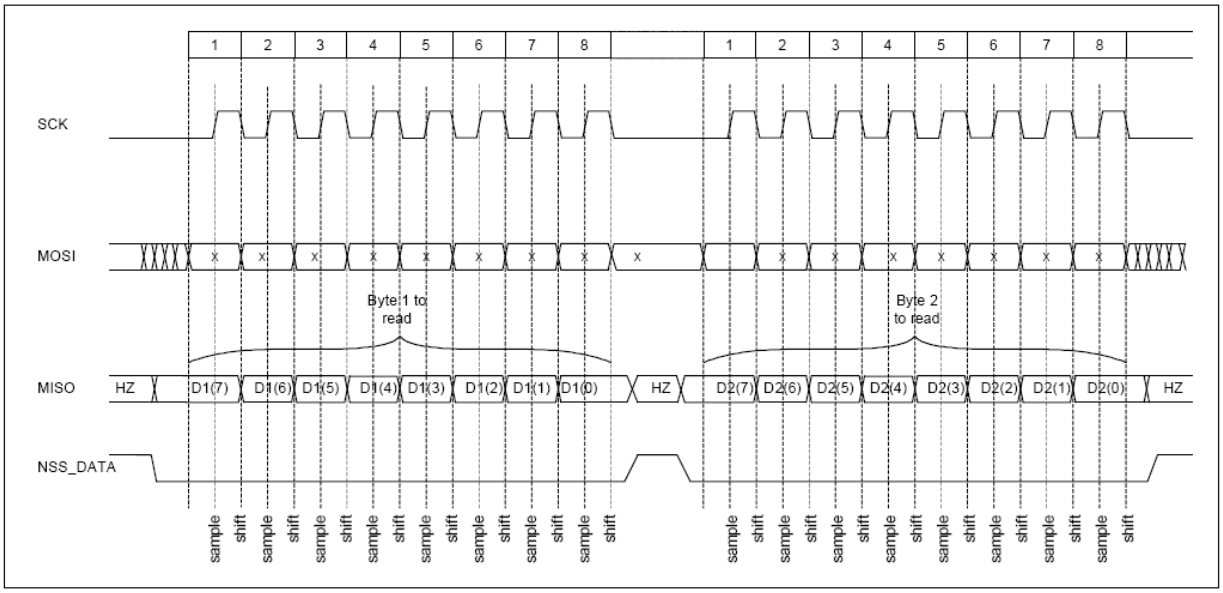
- At least one byte is present in the FIFO, i.e. a rising edge on IRQ_0 mapped to /fifoempty
- Each time a byte is written to FIFO, i.e. a rising edge on IRQ_0 mapped to WRITE_BYTE
- 16 bytes have been written to the FIFO, i.e. a rising edge on IRQ_1 mapped to RX_FIFOfull

The transceiver should be in buffered mode (MCParam_Buffered_mode = '1'). The SPI_DATA interface is then selected if NSS_DATA is low and NSS_CONFIG is high.

The operations with SPI_DATA interface are similar to those with SPI_CONFIG except that there is only a data byte (no address byte is required) and except that it is necessary to toggle the NSS_DATA signal back to high and back to low between each transmitted or received byte.



Writing 2 Bytes in transmitter mode



Reading 2 bytes in receive mode

Note that it is necessary to toggle NSS_DATA signal back to high and then back to low between each transmitted and received byte.

REGISTER DEFINITIONS

CONFIGURATION AND STATUS REGISTERS

The XE1205 has several operating modes, configuration parameters and internal status registers that may be accessed by the microcontroller via the SPI_CONFIG interface.
The switching pins SW(1:0) allows switching between one of the four operating modes (sleep, stand-by, receive, transmit) when MCParam_Select_mode is high. If MCParam_Select_mode is low, the modes are defined by the register through the SPI_CONFIG interface and SW(1:0) may be used as an output to control, for example, an antenna switch.

Configuration register: general description

All the bits that are referred to as 'reserved´ in this section should be cleared to '0´during write operations

Name	Size	Address	Description
MCParam	5 x 8	0-4	Main parameters common to transmit and receive modes
IRQParam	2 x 8	5-6	Interrupt registers
TXParam	1 x 8	7	Transmitter parameters
RXParam	9 x 8	8-16	Receiver parameters
OSCParam	2 x 8	17-18	Oscillator parameters
TParam	12 x 8	19-30	Test and special settings

Configuration Registers

Name	Bits	Address	RW	Description
Chip_mode(1:0)	7-6	0	r/w	Transceiver mode: 00 -> sleep mode 01 -> receive mode 10 -> transmit mode 11 -> stand-by mode
Select_mode	5	0	r/w	Transceiver mode selection: 0 -> mode defined by MCParam_chip_mode, SW(1:0) is an output sleep mode -> SW(1:0) = "00" receiver mode -> SW(1:0) = "01" transmitter mode -> SW(1:0) = "10" stand-by mode -> SW(1:0) = "00" 1 -> mode defined by SW(1:0) : SW(1:0) = 00 -> sleep mode SW(1:0) = 01 -> receive mode SW(1:0) = 10 -> transmit mode SW(1:0) = 11 -> stand-by mode
Buffered_mode	4	0	r/w	Enable buffered mode: 0 -> continuous mode 1 -> buffered mode
Data_unidir	3	0	r/w	Configure DATA pin 0 -> DATA is a bidirectional pin: input in transmit, output in receive mode 1 -> DATA is an output pin: output in receive mode, high-impedance in transmit mode
Band(1:0)	2-1	0	r/w	Frequency band: 01 -> 433 – 435 MHz 10 -> 863 – 870 MHz 11 -> 902 – 928 MHz
Freq_dev(8)	0	0	r/w	Frequency deviation MSB
Freq_dev(7:0)	7-0	1	r/w	Frequency deviation: Δf = int(Freq_dev(8:0)) * FSTEP Where int(x) = integer value of the binary representation of x Example 000000001 -> Δf = FSTEP 111111111 -> Δf = 511*FSTEP all these frequency deviations are available if the data shaping filter is disabled (please refer to Table 11)
Knx	7	2	r/w	Konnex mode enable 0 -> default mode -> bit rate defined by MCParam_Br(6:0) 1 -> Konnex mode-> bit rate = 32.7 kbit/s
Br(6:0)	6-0	2	r/w	Bit rate Br = 152.34e3/(int(Br) + 1) Where int(x) = integer value of the binary representation of x. Example: 0000001 -> Br = 76.1 kbit/s 1111111 -> Br = 1.19 kbit/s Note: if Konnex mode is enabled, then bit rate = 32.7 kbit/s.
Freq_lo(15:8) (7) Freq_lo(7:0)	7-0 7-0	3 4	r/w r/w	LO frequency in 2's complement: 00…0 -> Flo = middle of the range(6) 0X…X-> Flo = higher than the middle of the range 1X…X-> Flo = lower than the middle of the range Example: 00…001 -> Flo = middle of the range + FSTEP

MCParam configuration register

Name	Bits	Address	RW	Description
Rx_irq_0(1:0)	7-6	5	r/w	Select IRQ_0 source in Rx mode: If Buffered_mode = 0 00 -> IRQ_0 mapped to Pattern signal 01 -> IRQ_0 mapped to RSSI_irq signal 10 -> IRQ_0 mapped to Pattern signal 11 -> IRQ_0 mapped to Pattern signal if Buffered_mode = 1 00 -> IRQ_0 set to '0' 01 -> IRQ_0 mapped to Write_byte signal 10 -> IRQ_0 mapped to /fifoempty signal 11 -> IRQ_0 mapped to Pattern signal
Rx_irq_1(1:0)	5-4	5	r/w	Select IRQ_1 source in Rx mode If Buffered_mode = 0 00 -> IRQ_1 mapped to DCLK signal 01 -> IRQ_1 mapped to DCLK signal 10 -> IRQ_1 mapped to DCLK signal 11 -> IRQ_1 mapped to DCLK signal if Buffered_mode = 1 00 -> IRQ_1 set to '0' 01 -> IRQ_1 mapped to Fifofull signal 10 -> IRQ_1 mapped to RSSI_irq signal 11 -> IRQ_1 mapped to RSSI_irq signal
Tx_irq_1	3	5	r/w	Select IRQ_1 source in Tx mode If Buffered_mode = 0 0 or 1 -> IRQ_1 is mapped to DCLK 0 or 1 -> IRQ_0 is set to low if Buffered_mode = 1 0 -> IRQ_1 is mapped to Fifofull signal 1 -> IRQ_1 is mapped to TX_stopped signal (IRQ_0 is mapped to /Fifoempty in Buffered mode)
Fifofull	2	5	r	FIFO full (IRQ source)
/fifoempty	1	5	r	FIFO empty (IRQ source)
Fifooverrun	0	5	r/w/c	FIFO overrun error : Write '1' clear FIFO after Overrun occurred
Start_fill	7	6	r/w	FIFO filling selection mode 0 -> The FIFO is filled if a pattern is detected 1 -> The FIFO is filled as long as Start_detect is high
Start_detect	6	6	r/w/c	Start of FIFO filling If start_fill = '0' goes high when a start sequence is detected writing a '1' clears the bit and wait for a new start sequence If start_fill = '1', 1 -> start to fill the FIFO, 0 -> stop to fill the FIFO.
Tx_stopped	5	6	r	Transmission stopped (IRQ source)
Start_full	4	6	r/w	0 -> Start transmission when the FIFO is full 1 -> Start transmission when FIFO is not empty (/fifoempty = '1')
RSSI_int	3	6	r/w	Enable interrupt RSSI_irq when RSSI_thr is reached: 0 -> no interrupt generated 1 -> interrupt allowed
RSSI_signal_detect	2	6	r/w/c	Detection of a signal above RSSI_thr (IRQ source) 0 -> signal power lower than the threshold defined by RSSI_thr. 1 -> signal power equal or greater than the threshold defined by RSSI_thr Writing '1' clear RSSI_signal_detect
RSSI_thr	1-0	6	r/w	RSSI threshold for interrupt 00 -> input power ≥ VTHR1 01 -> input power ≥ VTHR2 10 -> input power ≥ VTHR3 11 -> input power ≥ VTHR3

IRQParam configuration register

Name	Bits	Address	RW	Description
Power(1:0)	7-6	7	r/w	Transmitter output power: 00 -> 0 dBm 01 -> 5 dBm 10 -> 10 dBm 11 -> 15 dBm
/Modul	5	7	r/w	Inhibition of the modulation in transmitter mode: 0 -> modulation 1 -> no modulation
Filter	4	7	r/w	Pre-filtering of the bit stream in transmitter mode: 0 -> no filtering 1-> data shaping filter enabled all bit rates defined by Br are available frequency deviations given in Table 11 are available
RESERVED	3-2	7	r/w	RESERVED
Fix_bsync	1	7	r/w	0 -> bit sync in normal environment 1-> bit sync in noisy environment
RESERVED	0	7	r/w	RESERVED

TXParam configuration register

Name	Bits	Address	RW	Description
Disable_bitsync	7	8	r/w	Bit synchronizer on/off: 0 -> ON 1 -> OFF
BW(1:0)	6-5	8	r/w	Bandwidth of the base band filter(SSB): must be ≥ Freq_dev + Br/2 00 -> 10 kHz 01 -> 20 kHz 10 -> 40 kHz 11 -> 200 kHz
Max_BW	4	8	r/w	Forces the bandwidth of the base band filter to its maximum value

RXParam part I

				(about 400 kHz SSB) and disables calibration: 0 -> bandwidth defined by BW(1:0) 1 -> bandwidth forced to its maximal value
Reg_BW(1:0)	3-2	8	r/w	Calibration of the bandwidth of the base band filter: 00 -> calibration at start up 01 -> no calibration 10 -> calibration when the bandwidth of the base band filter changes 11 -> calibration is forced each time 11 is written
Init_filter(1:0)	1-0	8	r/w	Base band filter initialization: 00 -> default initialize at start up 01 -> RESERVED 10 -> initialize each time the bandwidth change 11 -> force re-initialization
RSSI	7	9	r/w	RSSI off/on: 0 -> off 1 -> on
RSSI_range	6	9	r/w	Range of the RSSI: 0 -> low range 1 -> high range
RSSI_out	5-4	9	r	00 -> input power ≤ VTHR1 01 -> VTHR1 ≤ input power ≤ VTHR2 10 -> VTHR2 ≤ input power ≤ VTHR3 11 -> VTHR3 ≤ input power
FEI	3	9	r/w	Frequency Error Indicator off/on: 0 -> off 1 -> on
AFC_start	2	9	r/w	0 -> AFC not running process 1 -> AFC running Writing 0 will start the AFC process. At the end of the AFC process, the bit goes automatically back low.
AFC_OK	1	9	r/w	Result of the AFC 0 -> AFC operation successful 1 -> AFC operation unsuccessful
AFC_disable	0	9	r/w	Disabling the AFC 0 -> the error cancelation is automatically applied on the LO frequency 1 -> the error cancelation is not applied on the LO frequency
AFC_overflow	7	10	r/w	AFC overflow indicator 0 -> no overflow 1 -> the integrator of the frequency error is too high writing 1 to this bit will reset the integrator
IQAMP	6	10	r/w	IQ amplifier off/on: 0 -> off 1 -> on
Rmode	5	10	r/w	Linearity/sensitivity mode 0 -> Mode A (high sensitivity) 1 -> Mode B (high linearity)
Pattern	4	10	r/w	Pattern recognition off/on: 0 -> off 1 -> on
Psize(1:0)	3-2	10	r/w	Size of the reference Pattern: 00 -> 8 bits 01 -> 16 bits 10 -> 24 bits 11 -> 32 bits

RXParam part II

Name	Bits	Address	RW	Description
Ptol(1:0)	1-0	10	r/w	Number of tolerated errors for the pattern recognition: 00 -> 0 error 01 -> 1 error 10 -> 2 errors 11 -> 3 errors
FEI_out(15:8) FEI_out(7:0)	7-0 7-0	11 12	r r	FEI output in a 2's complement representation

RXPAram part III

Name	Bits	Address	RW	Description
Reg_pattern(31:24)	7-0	13	r/w	1st byte of the reference pattern
Reg_pattern(23:16)	7-0	14		2nd byte of the reference pattern
Reg_pattern(15:8)	7-0	15		3rd byte of the reference pattern
Reg_pattern(7:0)	7-0	16		4th byte of the reference pattern

Pattern register

Pattern Register

This register holds the user supplied reference pattern of 8, 16, 24, or 32 bits (see the RXParam_Psize(1:0) parameter). The first byte of this pattern is always stored in the byte at address 13. If used, the 2nd byte is stored at address 14, the 3rd byte at address 15 and finally the 4th byte at 16. The MSB bit of the reference pattern is always bit 7 of address 13.

Comparing the demodulated data, the first bit received is compared with bit 7 (the MSB) of byte address 13. The last bit received is compared with bit 0 (the LSB) in the Pattern register.

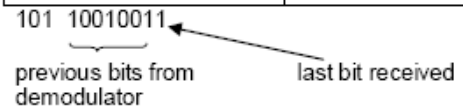
Byte Address 13 Bit 7 Bit 0	Byte Address 14 Bit 7 Bit 0	Byte Address 15 Bit 7 Bit 0	Byte Address 16 Bit 7 Bit 0
10010011	10101010	10010011	10101010
101 10010011	10101010	10010011	10101010

previous bits from demodulator

last bit received

Patter register 32 bit example

Byte Address 13 Bit 7 Bit 0	Byte Address 14 Bit 7 Bit 0	Byte Address 15 Bit 7 Bit 0	Byte Address 16 Bit 7 Bit 0
10010011	Xxxxxxxx	Xxxxxxxx	Xxxxxxxx



Pattern register 8 bit example

ADParam configuration register (additional settings)

Most of the parameters of this category are for test purposes. Some of them can be used to supersede settings that are described in previous sections to optimize special applications. These last parameters are described in the table below.

Name	Bits	Address	RW	Description
Add_BW	1	19	r/w	Change of RXParam_BW(1:0) decoding, allowing additional bandwidths for the base-band filter to be selected: Add_BW = 0 -> default values of RXParam_BW(1:0): RXParam_BW(1:0) = 00 => 10 kHz RXParam_BW(1:0) = 01 => 20 kHz RXParam_BW(1:0) = 10 => 40 kHz RXParam_BW(1:0) = 11 => 200 kHz Add_BW = 1 -> new bandwidth values: RXParam_BW(1:0) = 00 => 14.3 kHz RXParam_BW(1:0) = 01 => 28.5 kHz RXParam_BW(1:0) = 10 => 66.7 kHz RXParam_BW(1:0) = 11 => 100 kHz
Low_BW	2	19	r/w	Flag allowing selection of base-band filter bandwidths lower than 10 kHz: 0 -> default values given by RXParam_BW(1:0) and TParam_Add_BW 1-> bandwidths defined by TParam_Code_BW(8:0)
Code_BW(8:0)	6-0 7-6	21 22	r/w	Low base-band filter bandwidths, when TParam_Low_BW = 1: Code_BW(8:0) = 139 => 9 kHz Code_BW(8:0) = 160 => 8 kHz Code_BW(8:0) = 185 => 7 kHz MSB Code_BW(8) = bit 6 of address 21
Add_HPF(2:0)	5-3	22	r/w	Cut-off frequency of the HPF stages allowing cancellation of the DC and low-frequency offsets in the baseband circuit: 0 0 0 -> 660 Hz (default value) 0 0 1 -> 1.48 kHz 0 1 0 -> 1.75 kHz 0 1 1 -> 1.96 kHz 1 0 0 -> 2.55 kHz 1 0 1 -> 3.34 kHz 1 1 0 -> 5.11 kHz 1 1 1 -> 10.2 kHz
Chg_OSR	4	27	r/w	Flag allowing the over-sampling ratio of the bit synchronizer to be changed: 0 -> default OSR (32) 1 -> OSR defined by TParam_OSR(7:0)
OSR	7-0	28	r/w	Over-sampling ratio of the bit synchronizer when TParam_Chg_OSR = 1 Actual OSR = TParam_OSR(7:0) + 1

Useful Settings from TPram register

OSCParam Register

Reference frequency

The ECHO modules come with 39 MHz XO and RF transmission lines tuned for 433 MHz or 868 MHz or 902 MHz depending on the model ordered. Modifications of the OSCParam registers are limited by these system constraints the table below is provided for reference.

Name	Bits	Address	RW	Description
Osc	7	17	r/w	Sources of reference frequency 0 -> internal quartz oscillator (for XTAL or TCXO) 1 -> external signal applied on pin XTA (CMOS type signal, external clock)
Clkout	6	17	r/w	Enable clkout 0 -> no signal provided on pin CLKOUT 1 -> Signal at reference frequency divided by 2, 4, 8,16, 32 provided on CLKOUT (19.5 MHz down to 1.22 MHz)
Clkout_freq(2:0)	5-3	17	r/w	Frequency of signal provided on CLKOUT: 000 -> 1.22 MHz 001 -> 2.44 MHz 010 -> 4.87 MHz 011 -> 9.75 MHz others -> 19.5 MHz
RESERVED	2-0	17	r/w	RESERVED
Resxosc	7-4	18	r/w	Select the value of the resistor placed between TKA and TKB in order to use the transceiver with a crystal operating on its third overtone 0000 -> no resistor (3.8 MΩ) 0001 -> 1.48 kΩ 0010 -> 1.56 kΩ 0011 -> 1.66 kΩ 0100 -> 1.78 kΩ 0101 -> 1.91 kΩ 0110 -> 2.07 kΩ 0111 -> 2.26 kΩ 1000 -> 2.55 kΩ 1001 -> 2.81 kΩ 1010 -> 3.22 kΩ 1011 -> 3.79 kΩ 1100 -> 4.65 kΩ 1101 -> 6.04 kΩ 1110 -> 8.79 kΩ 1111 -> 16.55 kΩ
304 kbit/s_filter	3	18	r/w	304.7 kbit/s Tx filter 0 -> disabled 1 -> enabled
RESERVED	2-0	18	r/w	RESERVED

Clock output interface

When OSCParam_Clkout is set high, a CLKOUT clock frequency is provided for a microcontroller or external circuitry. A user-programmable frequency divider ratio of 2, 4, 8, 16, 32 is selectable

depending on OSCParam_Clkout_freq(2:0). The input frequency of this divider is the 39.0 MHz reference clock; the possible output frequencies are listed in the table below

OSC_Param_Clkout_freq (1:0)	CLKOUT frequency
000	1.22 MHz
001	2.44 MHz
010	4.87 MHz
011	9.75 MHz
Others	19.5 MHz

Frequency divider output

When the XE1205 is in sleep mode, CLKOUT is inactive even if bit OSCParam_Clkout remains high

Default settings at power up

The internally generated power on reset signal sets the MCParam, RXParam, and TXParam registers to '1'. The only exception is the CLKOUT generation: though OSCParam_Clkout is set to low (i.e. disabled) the XE1205 provides a signal at 1.22 MHz on the pin CLKOUT.

The first rising edge on the NSS_CONFIG pin causes the registers to be updated and this will result in CLKOUT being disabled. For this reason the first programming sequence should be to enable CLKOUT by setting OSCParam_Clkout to high for applications using CLKOUT. It is recommended to initialize the XE1205 registers immediately after power-up.

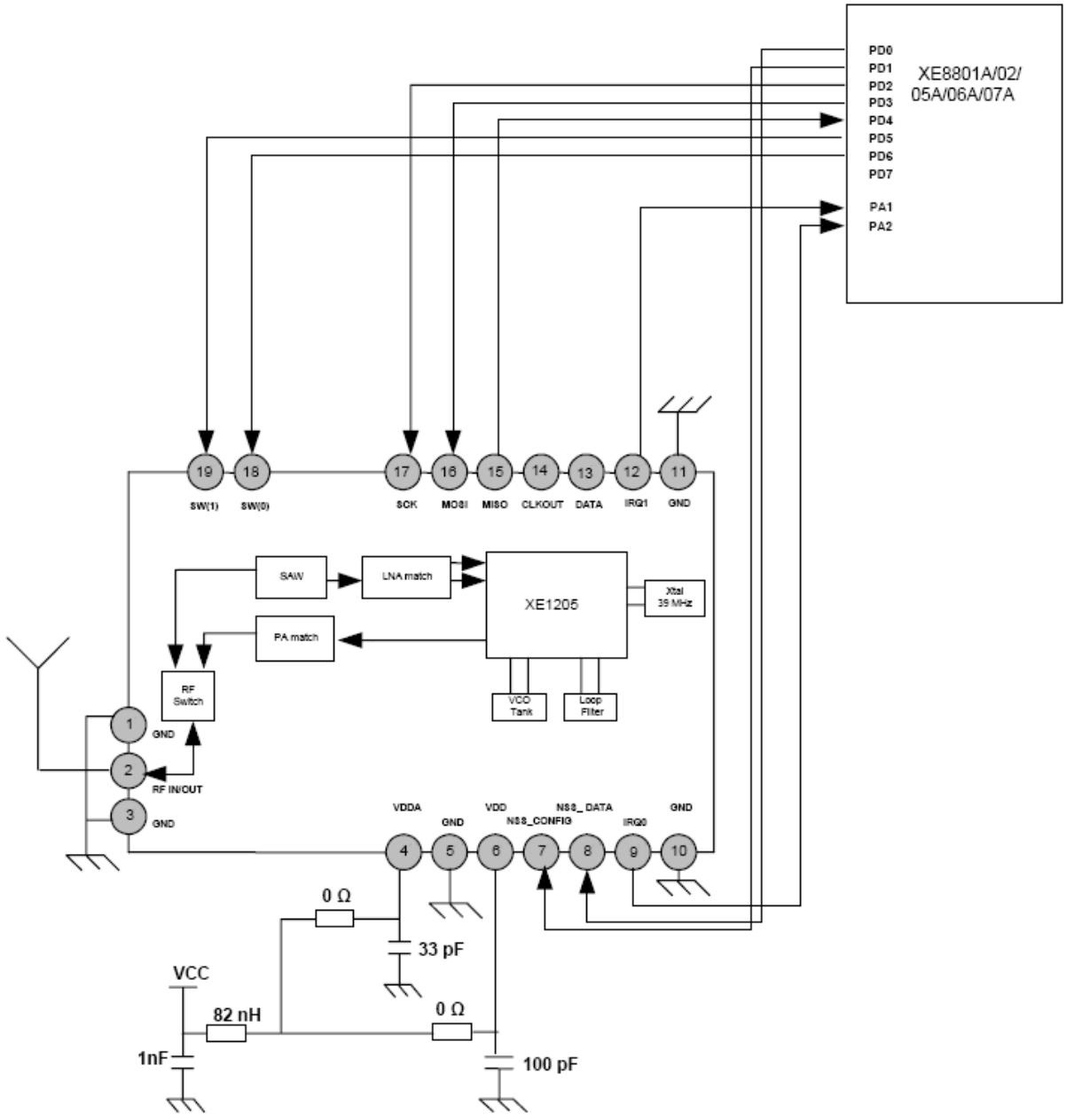
XE1205 Operating Modes

The XE1205 has four main operating modes illustrated in the table below. These modes are defined by register MCParam_Chip_mode(1:0) when bit MCParam_Select_mode is low and defined by SW(1:0) pins when MCParam_Select_mode is high. Please note that in both cases the changes will be applied to the transceiver upon the rising edge of the NSS_CONFIG signal (ie NSS_CONFIG must be set low even when using SW(1:0) as inputs)

MCParam_Select_ mode	MCParam_Chip_mode (1:0)	SW(1 :0) mode	SW(1 :0) value	Operatin g Mode	Enable blocks of the transceiver
0	00	Outpu t	00	Sleep	-
0	01	Output	01	Receive	Quartz oscillator, Frequency synthesizer, Receiver
0	10	Output	10	Transmit	Quartz oscillator, Frequency synthesizer, Transmitter
0	11	Output	11	Standby	Quartz Oscillator
1	00	Input	00	Sleep	-
1	01	Input	01	Receive	Quartz oscillator, Frequency synthesizer, Receiver
1	10	Input	10	Transmit	Quartz oscillator, Frequency synthesizer, Transmitter
1	11	Input	11	Standby	Quartz Oscillator

Operating Modes

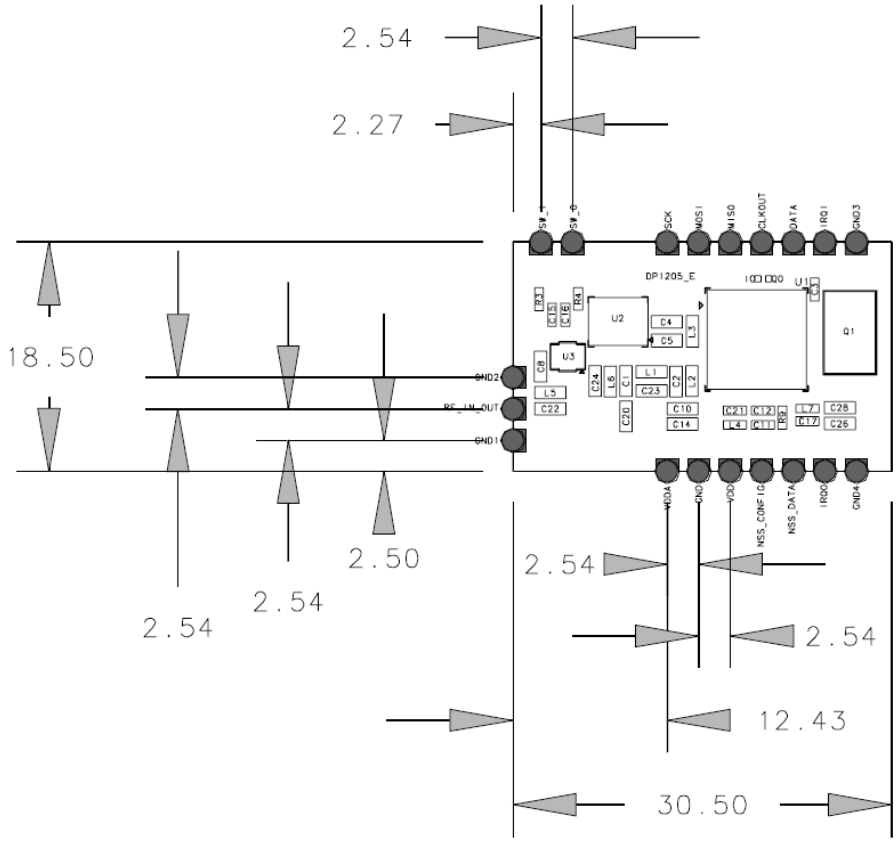
Typical Application



Typical microcontroller interface

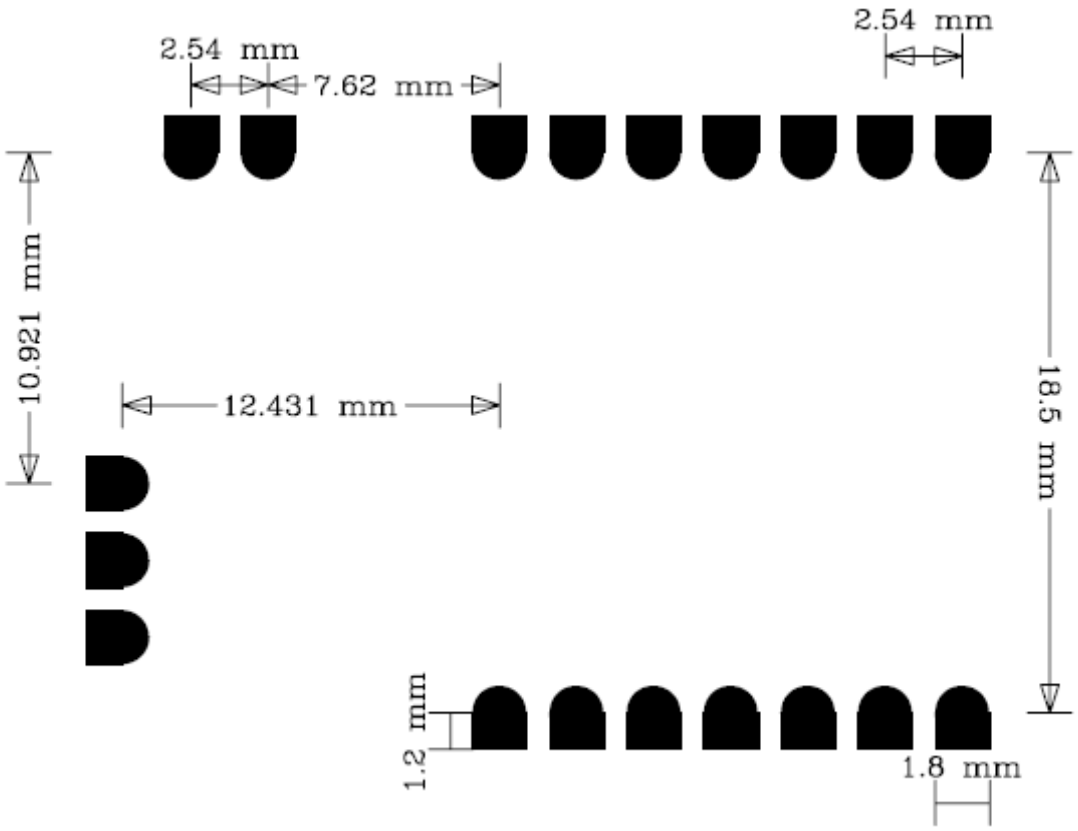
MECHANICAL DRAWINGS

Module Dimensions

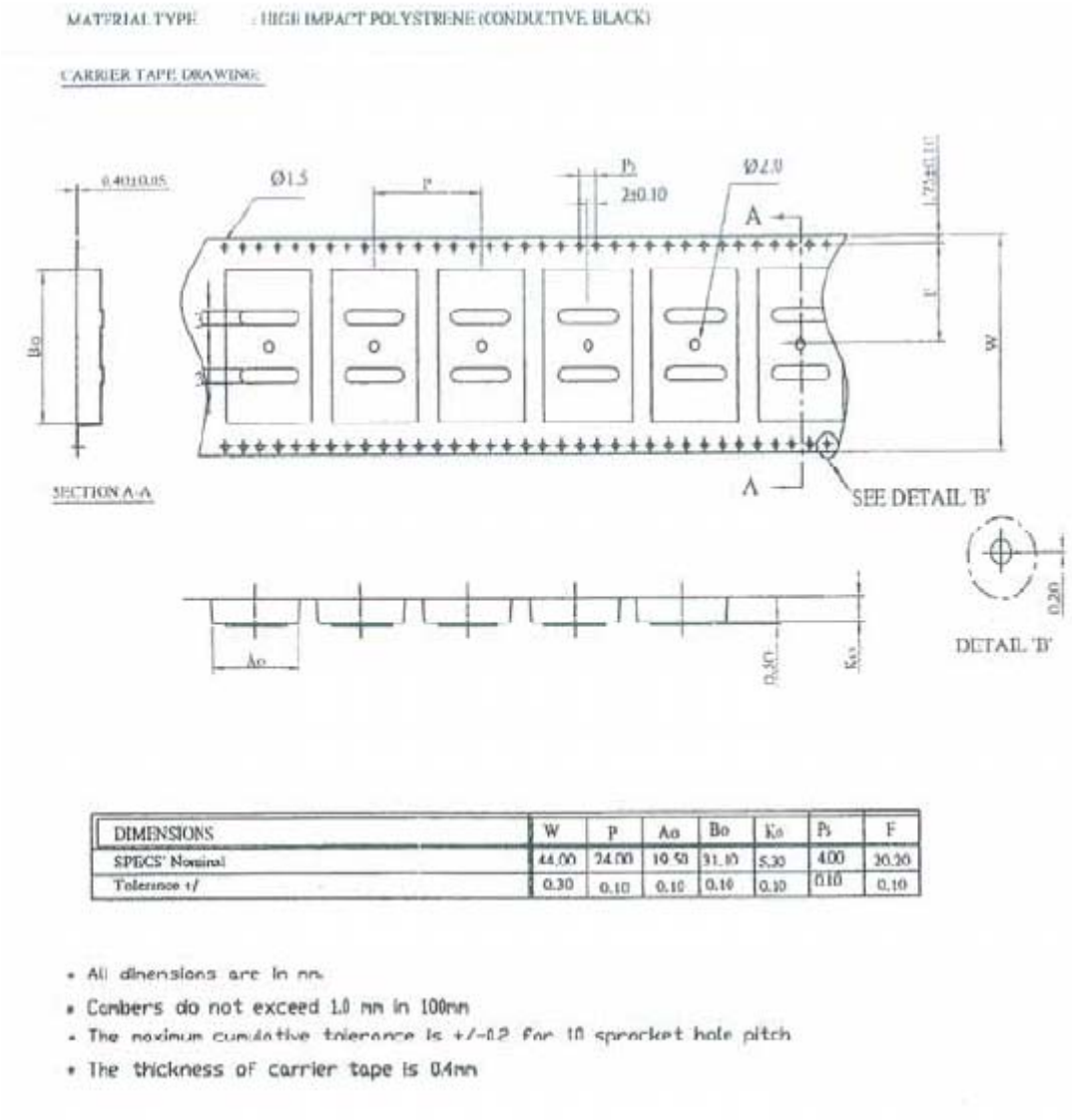


Module Dimensions and Pin Location
X=30.5 Y=18.5 Z=4.6 mm

Recommended PCB Layout



Tape and Reel Dimensions



DIMENSIONS	W	P	Ao	Bo	Ko	P1	F
SPECS' Nominal	44.00	24.00	10.50	31.10	5.30	4.00	20.20
Tolerance +/-	0.30	0.10	0.10	0.10	0.10	0.10	0.10

- All dimensions are in mm
- Cambers do not exceed 1.0 mm in 100mm
- The maximum cumulative tolerance is +/-0.2 for 10 sprocket hole pitch
- The thickness of carrier tape is 0.4mm

PRODUCTION GUIDELINES

- PAN modules that are formed into a hybrid surface mount package which allows both manual and automated placement.
- PAN modules contain discrete components, therefore the assembly procedures utilized by automated or manual techniques are critical for the performance after installation on the end users product.
- Unigen recommends proper ESD procedures.

Manual Assembly

- The primary mounting surface for the module is located on the bottom pad surface.
- Castellations have been provided that run perpendicular to the pad surface beneath. This design allows for proper heat transfer and solder wicking to the bottom side.
- It is recommended that the user carefully align and tack one corner of the module then move sequentially around the module.
- The end user layout pads should extend out slightly from the module to allow a fine tip soldering iron to heat the pad and castellation simultaneously.
- Use a fine point conical tip to heat the modules castellation and board pad simultaneously.
- Apply .020 solder wire to the pad where the castellation contacts. The solder will wick properly to the underlying surface providing a secure electrical connection.

Automated Assembly

- Modules have been designed to be compatible with techniques utilized in an automated process.
- Due to the complexity of the module, additional attention is required in comparison to other component types.
- The reflow temperature profile is a critical point for creating a consistent solder connection.
- Any shock that may be applied during the reflow movement process should be avoided.
- If a shock is applied during the liquefied state of reflow, the components may shift causing malfunction of the module.

Washing

- If modules are assembled with a water soluble process special attention to cleaning will be necessary.
- All flux residue should be removed with deionized water to ensure performance, as well as reduce the potential of ionic contamination and corrosive activity.
- Modules which have been washed must be completely dry before power-up or testing. Overnight bake is recommended.
- Ultrasonic cleaning systems should not be used.
- Proper support during wash is necessary to eliminate any mechanical stress which could damage components on the module.

SOLDER PROFILES

Recommended Soldering Parameters (RoHS Compliant)		
Printing/Dispensing	Reflow Profile	Note
• Stencil: 0.006 inch (6 mil) • Squeegee: Metal (recommended)	• Ramp @ 1.0 – 2.0ºC/sec to 130ºC • Slow ramp from 130ºC to 180ºC for 90- 120 seconds • Ramp @ 0.5- 2ºC /sec to peak temperature 230ºC to 250ºC TAL for 40- 80 seconds • Ramp down to R.T. @ 1- 3ºC/sec	Please note that the reflow profiles listed are guidelines only and adjustments may be necessary to ensure proper wetting of the solder.

Recommended Soldering Parameters (non-RoHS Compliant)		
Printing/Dispensing	Reflow Profile	Note
• Stencil: 0.006 inch (6 mil) • Squeegee: Metal (recommended)	• Straight ramp up profile preferred • Ramp up from ambient temp. to peak temp. of 210ºC to 225ºC @ 1ºC /sec • TAL (Time Above Liquidus) = 45 to 75 seconds • Ramp down to R.T. @ 1- 3ºC/sec	Please note that the reflow profiles listed are guidelines only and adjustments may be necessary to ensure proper wetting of the solder.

REFERENCE DOCUMENTATION

Semtech DP1205 Datasheet Rev 4 May 2006
Semtech XE1205 Datasheet Rev 8 June 2007

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