Unigen Corp. Flash Media Products

Part Number Family: UGB30STX

Issue Date: Sept. 10, 2009
Revision: 1.2

Revision History

Rev. No.	History	Issue Date	Remarks
0.9	Preliminary Release	Dec. 17, 2008	
1.0	Updated CHS table	Feb 10,2009	
1.1	Corrected typo on table 2.4, data transfer rates	June 8, 2009	
1.2	Updated Firmware	Sept 10, 2009	

Datasheet
Unigen Corporation
CompactFlash® Card

FEATURES

- CompactFlash, PCMCIA and ATA specification standard
- Compliance:
  - PCMCIA version 2.1
  - PC Card ATA
  - CF specification version 3.0
- Interface: CompactFlash, PC Card ATA and true ATA/IDE
- Compatible with all PC Card Services and Socket Services.
- Compatible with host ATA disk I/O BIOS, DOS/Windows/Linux file system.
- High Performance Throughput:
  - Typical Read: 40 MB/s
  - Typical Write: 20 MB/s
- Available Storage Capacities:
  - Type I: 256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB
- Support for 3.3 Volt and 5Volt Power Supply
- Access modes:
  - PC Card Memory Mode
  - PC Card I/O Mode
  - True-IDE Mode (supports up to PIO Mode 6, Multiword DMA mode 4 and UDMA mode 4 in True-IDE mode)
- Hardware Data Protection
- Firmware Upgradeable
- Auto Sleep Mode
- Power Consumption (3.3V/ 5.0V).
  - Active mode (typical): 50 mA
  - Sleep mode (typical): 600 uA
- High reliability and long life
  - Internal ECC (Error Correcting Code) results in high data reliability
  - Advanced wear leveling algorithm
- Temperature Range: 0 to 70 ^{o}C (C - TEMP), -40 ^{o}C to 85 ^{o}C (I – TEMP)
- RoHS Compliant

PRODUCT DESCRIPTION

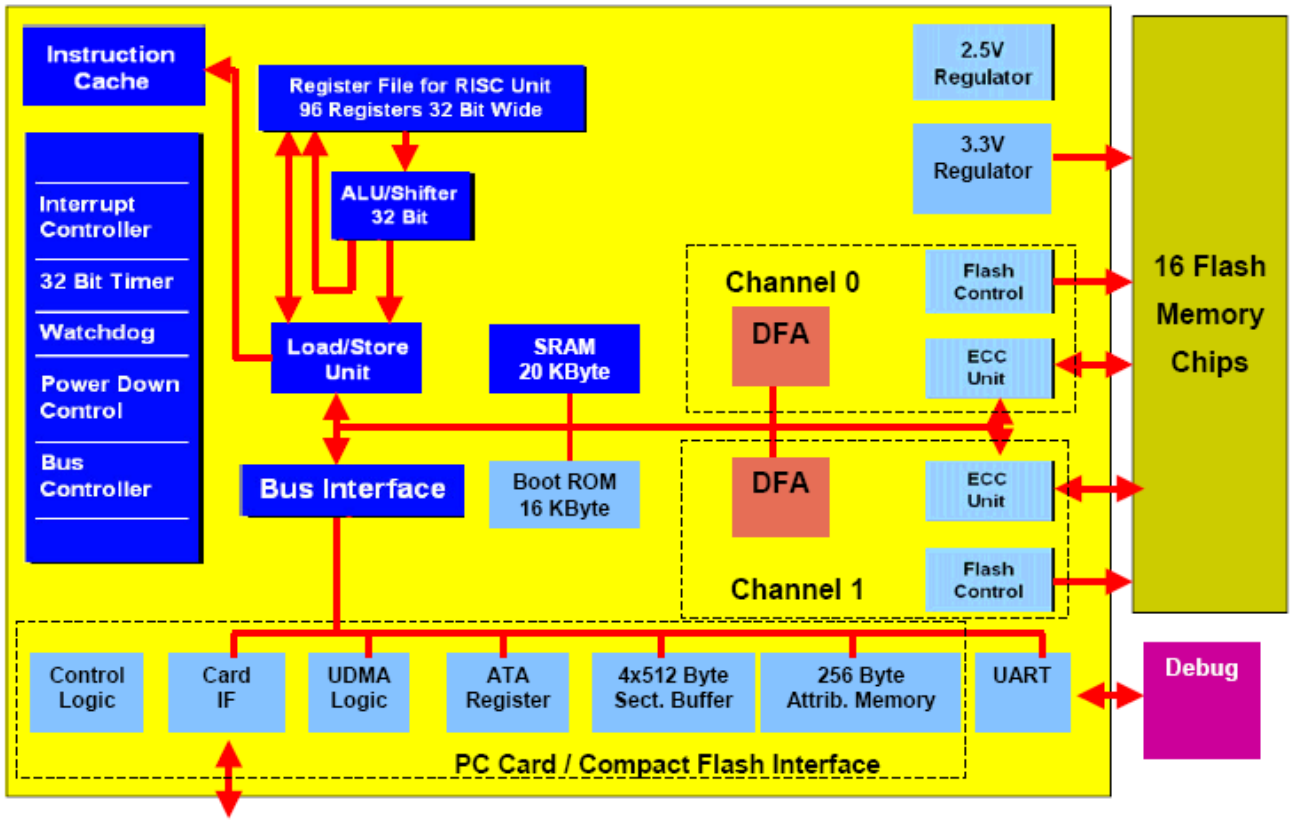
Unigen's UGB30STX CompactFlash cards are storage devices that use solid-state SLC flash technology as the storage media. This ultrahigh speed, rugged, storage media are ideal for consumer products and variety of embedded and industrial applications. Up to 16 GByte cards can be built using a Type I CompactFlash form-factor. With a PC Card adapter, UGB30STX CompactFlash cards can be used in any Type II or Type III PCMCIA slot.
All UGB30STX are configured as CF cards unless specified otherwise specified by the customer.

Table of Contents:

1 General Description

The Unigen Corporation CompactFlash card contains a Hyperstone Media designed Flash controller, programmable firmware and flash memory module(s). The proprietary space manager architecture in the controller maximizes read/write data rate performance to and from the host and flash memory, eliminating firmware delays during sector read and write operations. The Hyperstone Media Flash controller, combined with tailored firmware, provides complete ATA disk emulation, which ensures complete compatibility with a wide range of operating systems.

Figure 1-1: Block Diagram



2 PRODUCT SPECIFICATION

2.1 CompactFlash Card Setup Parameters

Model Number	Form Factor	Capacity in Bytes	Sectors/Card	Cylinders	Heads	Sectors/Track
UGB30STX0256	Type 1	260,571,136	508,928	994	16	32
UGB30STX0512		512,483,28	1,00,944	993	16	63
UGB30STX1000		1,023,934,464	1,999,872	1984	16	63
UGB30STX2000		2,097,414,144	4,096,512	4064	16	63
UGB30STX4000		4,113,285,120	8,033,760	7970	16	63
UGB30STX8000		8,231,215,104	16,076,592	15,949	16	63
UGB30STX16H0		16,494,428,160	32,215,680	31,960	16	63

NOTE: To calculate the "Capacity in Bytes", use the following formula:

- Capacity in Bytes = Cylinders * Heads * Sectors * 512 bytes per sector.
  Unigen defines 1MBytes = 10^6 bytes. The capacities of all Unigen CompactFlash cards are in decimal values. Available user capacity may varies

Parameters in the above table are subject to change without advanced notice.

2.2 Electrical Interface

This section provides information on the Electrical Interface Descriptions, the Bus Timing, PC Card ATA Interface compliant Register set, ATA Task File Register set, and the Host Commands for both CompactFlash cards.

2.2.1 CompactFlash Electrical Interface

UGB30STX CompactFlash card is fully compliant with the CompactFlash specifications. This interface standard electrically complies with the PC Card ATA specifications, functioning in the I/O mode, the Memory mode, True IDE mode.

2.2.2 Interface Connector

The Host is connected to the CompactFlash card using a standard 50-pin connector, consisting of two rows of 25 female contacts on 1.27 mm (50 mils) centers. In addition, the CompactFlash card can be used with a PCMCIA Type II passive adaptor, which converts the CompactFlash card to a Type II PCMCIA PC card.

2.2.3 Connector Pin Assignments

Table 2-1 below lists the signal/pin assignments for the CompactFlash card. Active low signals have a "-" prefix.

The superscript[1] after Pin Numbers indicate that the functionality of that pin changes between I/O mode, Memory mode and/or True IDE mode operation.

The following abbreviations are used for signal types: (I) indicates input to CompactFlash; (O) indicates output from CompactFlash; (I/O) indicates a bi-directional signal; (TS) indicates three-state; (OC) indicates open collector.

Table 2-1: 50-pin CompactFlash Connector Pin Assignments and Type

Pin No.	Signal	Signal Types	Function
1	GND	DC	Ground
2	D03	I/O	Data bit 3
3	D04	I/O	Data bit 4
4	D05	I/O	Data bit 5
5	D06	I/O	Data bit 6
6	D07	I/O	Data bit 7
7[1]	-CE1/-CS0	I	Card Enable 1/ Chip Select 0
8	A10	I	Address bit 10
9[1]	-OE/-ATA SEL	I	Output Enable/ ATA Select
10	A09	I	Address bit 9
11	A08	I	Address bit 8
12	A07	I	Address bit 7
13	VCC	DC in	Supply Voltage
14	A06	I	Address bit 6
15	A05	I	Address bit 5
16	A04	I	Address bit 4
17	A03	I	Address bit 3
18	A02	I	Address bit 2
19	A01	I	Address bit 1
20	A00	I	Address bit 0
21	D00	I/O	Data bit 0
22	D01	I/O	Data bit 1
23	D02	I/O	Data bit 2
24[1]	WP/-IOIS16/-IOCS16	O	Write Protect / I/O port is 16-bit
25	-CD2	O	Card Detect 2
26	-CD1	O	Card Detect 1
27	D11	I/O	Data bit 11
28	D12	I/O	Data bit 12
29	D13	I/O	Data bit 13
30	D14	I/O	Data bit 14
31	D15	I/O	Data bit 15
32[1]	-CE2/-CS1	I	Card Enable 2/ Chip Select 1
33	-VS1	O	Voltage Sense 1
34[1]	-IORD/HSTROBE/ HDMARDY/-HDMARDY	I	I/O Read / Host Strobe / Host Ready
35[1]	-IOWR / STOP	I	I/O Write / Termination of data burst
36	-WE	I	Write Enable

Table 2-1: 50-pin CompactFlash Connector Pin Assignments and Type

Pin No.	Signal	Signal Types	Function
37[1]	READY/-IREQ/INTRQ	O	Ready/Interrupt Request/Host Interrupt
38	VCC	DC in	Supply Voltage
39[1]	-CSEL	I	Card Select (in True IDE mode)
40	-VS2	O	Voltage Sense 2
41[1]	RESET/-RESET	I	Host Reset
42[1]	-WAIT/IORDY	O	Extend Bus Cycle/ I/O Ready
43[1]	-INPACK/DREQ/ -DDMARDY/DSTROBE	O	Input Acknowledge / DMA Request / DMA READY / DMA Strobe
44[1]	-REG / DMACK / -DMACK	I	Register (Attribute Memory) Select / DMA Acknowledge
45[1]	BVD2/-SPKR /-DASP	I/O	Battery Voltage Detect2/Speaker/Device Active or Slave Present
46[1]	BVD1/-STSCHG/-PDIAG	I/O	Battery Voltage Detect1/ Card Status Change/Passed Diagnostics
47	D08	I/O	Data bit 8
48	D09	I/O	Data bit 9
49	D10	I/O	Data bit 10
50	GND	DC	Ground

2.2.4 CompactFlash Signal Definitions

Table below defines the CompactFlash signals that interface with the Host.

Table 2-2: 50-Pin CompactFlash Connector Signal Definitions

Name	Pin No.	Type	Description
BVD1/ STSCHG PDIAG	46[1]	I/O	**BATTERY VOLTAGE DETECT 1**: In Memory mode, this output signal is always asserted (high), as BVD1 is not supported. **STATUS CHANGED:** In I/O mode, this signal is used to indicate a change in RDY/BSY or Write Protect states. **PASSED DIAGNOSTICS:** In True IDE mode this signal is used between two drives to indicate that the drive in Slave mode has passed diagnostics.
BVD2/ -SPKR/ -DASP	45[1]	I/O	**BATTERY VOLTAGE DETECT 2**: In Memory mode, this output signal is always asserted (high), as BVD2 is not supported. **SPEAKER**: In I/O mode, this output signal is always de-asserted (low), since the CompactFlash does not support audio functions. **DEVICE ACTIVE/SLAVE PRESENT**: In True IDE mode, this is the Device Active/Slave Present signal.
-CD1 –CD2	26 25	O	**CARD DETECT**: These outputs are directly connected to ground on the Compact Flash. By sensing these signals, the Host determines that the card is fully inserted into the socket.
-CE1/CS0 – CE2/CS1	7[1] 32[1]	I	**CARD ENABLE:** These inputs select the card and indicate to the CompactFlash whether a byte or word operation is being performed. –CE2 always accesses the odd byte of the word; CE1 accesses the even or odd byte of the word depending on the status of A0 and –CE2. **CHIP SELECT:** In True IDE mode, CS0 selects the ATA Command Block Registers, while CS1 selects the ATA Control Block Registers.

Table 2-2: 50-Pin CompactFlash Connector Signal Definitions

Name	Pin No.	Type	Description
-CSEL	39[1]	I	**CARD SELECT**: This signal is not used in the Memory or I/O modes. In True IDE mode, this signal configures the drive as a Master or Slave. If the signal is de-asserted (low), the drive is configured as a Master. If the pin is open, the drive is configured as a slave.
A10 – A00	8 10 11 12 14 15 16 17 18 19 20	I	**ADDRESS[10:0]**: In I/O and Memory mode, these are the Host Address lines that select the I/O port address registers or the memory mapped port address registers, and the control and status registers. In True IDE mode, only A[2:0] are used to select the control, status and data register; A[10:3] are not used in this mode.
D15 – D00	31 30 29 28 27 49 48 47 6 5 4 3 2 23 22 21	I/O	**DATA [15:0]:** These bi-directional signals carry the data, commands, and status information between the Host and the controller.
-INPACK/ -DMARQ	43[1]	O	**INPUT PORT ACKNOWLEDGE:** In I/O mode, this input signal is asserted when the card is selected and can respond to an I/O cycle at the address on the address bus. This signal is used by the Host to control the enable of any input data buffer between the card and Host system data bus. This signal is not used in Memory mode. **DMA REQUEST:** In True IDE mode, this signal is used as the DMA Request signal. This signal is not used in the Memory mode.
-IORD/ HSTROBE/ -HDMARDY/ HDMARDY	34[1]	I	**I/O READ**: In I/O mode, and True IDE mode, this input pulse clocks I/O data from the internal controller to the card bus. This signal is not used in Memory mode. **HOST STROBE :** When UDMA mode DMA write is active, this signal is the data out strobe generated by the host. **HOST DMA READY :** When UDMA mode DMA read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts.
-IOWR/ STOP	35[1]	I	**I/O WRITE**: In I/O mode, and True IDE mode, this input pulse clocks I/O data from the card bus to the internal controller. This signal is not used in Memory mode. **STOP** : While UDMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
-OE/ -ATA SEL	9[1]	I	**OUTPUT ENABLE**: In I/O and Memory modes his input signal is used to gate Memory Read data from the memory card. In Memory mode it is used to read both data and the CIS and Configuration registers. In I/O mode, this signal is used to read the CIS and Configuration registers only. **ATA SELECT:** This signal should be grounded to enable True IDE mode.

Table 2-2: 50-Pin CompactFlash Connector Signal Definitions

Name	Pin No.	Type	Description
RDY/-BSY /IREQ /INTRQ	37[1]	O	**READY/BUSY**: In Memory mode, this input is set high to indicate that the CompactFlash is ready to accept a new data transfer operation. This signal is held low when the card is busy. A pull-up resistor must be provided on the Host memory card socket. During Power Up and at Reset, this signal must be held low, and no access should be made to the CompactFlash until the Power Up or Reset sequence is complete. The only exception is if the CompactFlash is being Powered Up with the RESET signal disconnected or asserted; in this case the RDY/BSY signal is held high (RDY signal). **INTERRUPT REQUEST**: In I/O mode, this input is strobed low to generate a pulse-mode interrupt or held low for a level-mode interrupt. **HOST INTERRUPT:** In True IDE mode this is the Interrupt Request to the Host (active high).
-REG/ DMACK/ -DMACK	44[1]	I	**REGISTER (ATTRIBUTE) MEMORY SELECT**: In Memory mode, this input signal distinguishes the register (attribute) memory from the common memory. In I/O mode, this signal must be asserted (low) when the I/O address is on the bus. In True IDE mode, this signal is used as the DMA Acknowledge signal. **DMA ACKNOWLEDGE** : This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers.
RESET/ -RESET	58	I	**RESET:** The CompactFlash is reset when this signal is set, initializing the control and status registers and aborting any command in progress. In PC card mode, this signal is active high; in True IDE mode, it is active low.
-WE	36[1]	I	**WRITE ENABLE**: In Memory mode, this input signal is used for strobing Memory Write data into the CompactFlash. In both Memory mode and I/O mode, this signal is used for writing the configuration register, in conjunction with the REG signal. In True IDE mode, this signal is not used and should be connected to Vcc.
WP/ -IOIS16 / -IOCS16	24[1]	O	**WRITE PROTECT**: In Memory mode this signal is used to reflect the status of the cards write protect switch. At this time the CompactFlash is not configured with a write protect switch. **I/O PORT IS 16 BITS**: In I/O operation, this output selects the 16-bit port. A low signal indicates that a 16-bit port is being addressed or an odd byte only operation can be performed at the addressed port. In True IDE mode, this signal is IOCS16. A low signal indicates that a 16-bit transfer is in progress on the Host bus. This open collector line is only driven on assertion (low).
-WAIT/ IORDY/ -DDMARDY/ DSTROBE	42[1]	O	**WAIT:** In Memory mode, and I/O mode, this output is driven by the CompactFlash to signal the Host to insert a delay before completing a memory or I/O cycle. **IORDY:** In True IDE mode, except in UDMA mode, this output signal may be used as IORDY. **-DDMARDY :** In all modes, when UDMA mode DMA write is active, this signal is asserted by the host to indicate that the device is ready to receive UDMA data-in bursts. **DSTROBE :** In all modes, when UDMA mode DMA write is active, this signal is the data out strobe generated by the device.
GND	1 50	DC	**GROUND**: These two pins supply ground for the CompactFlash.
VCC	13 38	DC in	**+ 3.3v or + 5 VOLTS:** These pins supply 3.3v or 5 V to the CompactFlash.

Table 2-2: 50-Pin CompactFlash Connector Signal Definitions

Name	Pin No.	Type	Description
-VS1	33	O	**VOLTAGE SENSE 1**: This signal is grounded, so that the CompactFlash CIS can be read at 3.3 volts.
-VS2	40	O	**VOLTAGE SENSE 2**: This pin is reserved for a secondary voltage.
[1] Functionality of Pin changes between Memory mode, I/O mode, and True IDE mode operation			

2.3 Environmental and Reliability Characteristics

Shock	2,000 G max. (operating/non-operating)
Vibration	15 G peak to peak max. (operating/non-operating)
Acoustic Noise	0 dB
Humidity	5% to 95%, non-condensing
Altitude	80,000 ft max.
MTBF	1,000,000 power-on hours
Data Reliability	1 in 10^{14} bits, read
Endurance	>3,000,000 erase/program cycles

2.4 Data Transfer Rates

Speed Rate	Sequential Read Speed (Typ.)
250 X	37 MB/S
Speed Rate	**Sequential Write Speed (Typ.)**
120 X	18 MB/s

2.5 Product Speed Availability

The UGB30STXXXXXXX CompactFlash cards are available in one choices of speed; 133X where X denotes a write performance of 150Kbytes per second.

3 EIECTRICAL SPECIFICATION

3.1 Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Storage Temperature	Tstg	-40	+85	°C
Input Power	Vcc	-0.3	6.5	V
Voltage on any pin except Vcc with respect to GND	V	0.5	Vcc+0.5	V

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Input Power

Voltage	Maximum Average RMS Current	Measurement Method
3.3V ± 5%	75 mA	3.3V at 25°C
5.0V ± 10%	100 mA	5.0V at 25°C

NOTE: Current measurement is accomplished by connecting an amp meter (set to the 2 amp scale range) with a fast current probe with an RC filter in series with the Vcc supply to the CompactFlash card. Current measurements are to be taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specifiied in the above table.

3.3 Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit	Test Condition
Operating Temperature	Ta	0	70	°C	C - Temp
	Ta	-40	85	°C	I - Temp
Supply Voltage	Vcc	3.15	3.45	V	
Supply Voltage	Vcc	4.5	5.5	V	

3.4 Input Leakage Current

Parameters	Type	Symbol	Min	Max	Unit	Test Condition
Input Leakage Current	IxZ	IL	-10	10	μA	Vil = GND; Vih = Vcc
Pull Up Resistor	IxU	RPU1	50k	500k	Ohm	Vcc = 5.0V
Pull Down Resistor	IxD	RPD1	50k	500k	Ohm	Vcc = 5.0V

NOTE: In the table above, x refers to the characteristics described in section 3.5 below. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

3.5 DC Characteristics (TA = 0 TO +60°C, VCC = 5.0V ± 10% OR 3.3V ± 5%)

Parameters	Symbol	Min	Max	Unit	Test Condition
Input Low Voltage CMOS	Vil	-	Vcc x 0.3V	V	
Input High Voltage CMOS	Vih	Vcc x 0.7V	-	V	
Output Low Voltage CMOS	Vol	GND	GND + 0.4V	V	Iol = 4mA
Output High Voltage CMOS	Voh	Vcc – 0.8	Vcc	V	Ioh = -4mA
Read Current	Irc		100	mA	
Write Current	Iwr		100	mA	
Sleep Current	Isc		1	mA	

3.6 AC Characteristics (Ta = 0 to +60°C, Vcc = 5.0V ± 10% or 3.3V ± 5%)

This bus timings for Unigen Corporation's UGB30STXXXXXXX CompactFlash card supports timing modes 5 & 6 as specified in the CompactFlash Specification 3.0 for timing information, please refer to the CompactFlash Specification.

Unigen Corporation CompactFlash card contains 256 bytes of fully static RAM to be used to hold the Card Information Structure (CIS). This starts at Attribute Memory Address 000H and continues through Attribute Memory Address 1FEH. Only even locations are accessible within attribute memory space. The base address of the card configuration registers is 200h. This SRAM can be read or written by both the Host and the local micro controller.

3.6.1 Attribute Memory Read

Table 3-1: Attribute Memory Read Access

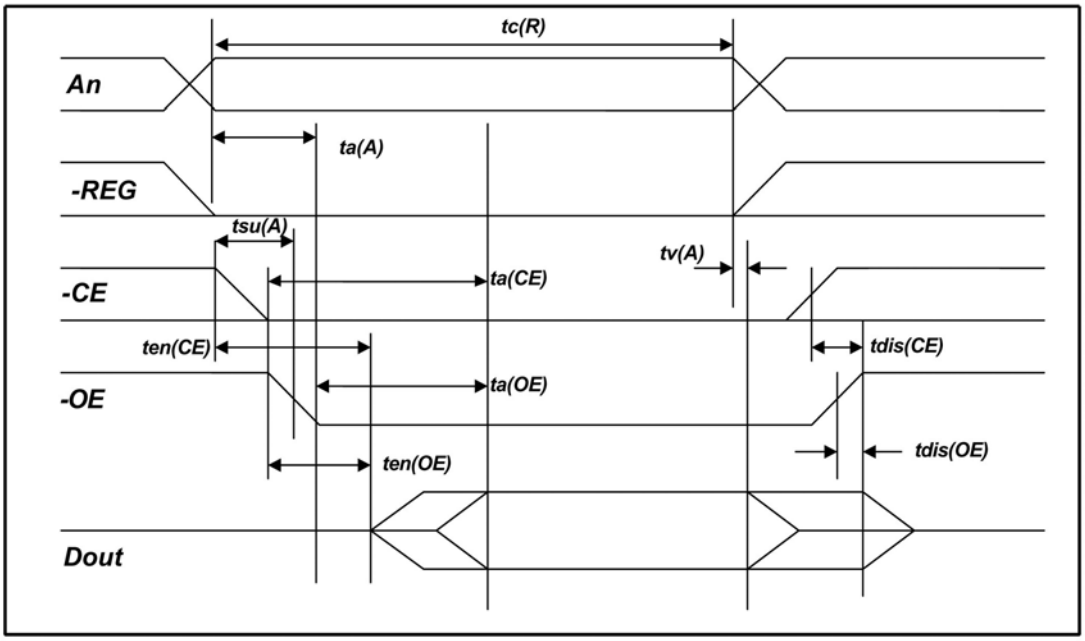
Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby mode (no access)	X	1	1	X	X	X	X	X	High-Z	High-Z
CIS Byte Access	0	1	0	0	0	0	0	1	High-Z	Even byte
Configuration Byte Access	0	1	0	0	1	0	0	1	High-Z	Even byte
CIS Word Access	0	0	0	0	0	X	0	1	Not Valid	Even Byte
Configuration Word Access	0	0	0	0	1	X	0	1	Not Valid	Even byte

Table 3-2: Attribute Memory Read Timing

Speed Version			300ns	
Parameters	**Symbol**	**IEEE Symbol**	**Min**	**Max**
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tEHQZ		150
Output Disable Time form CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVQL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enabled Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Note: All times are in nanoseconds. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

Figure 3-1: Attribute Memory Read Timing Diagram



3.6.2 Attribute Memory Write

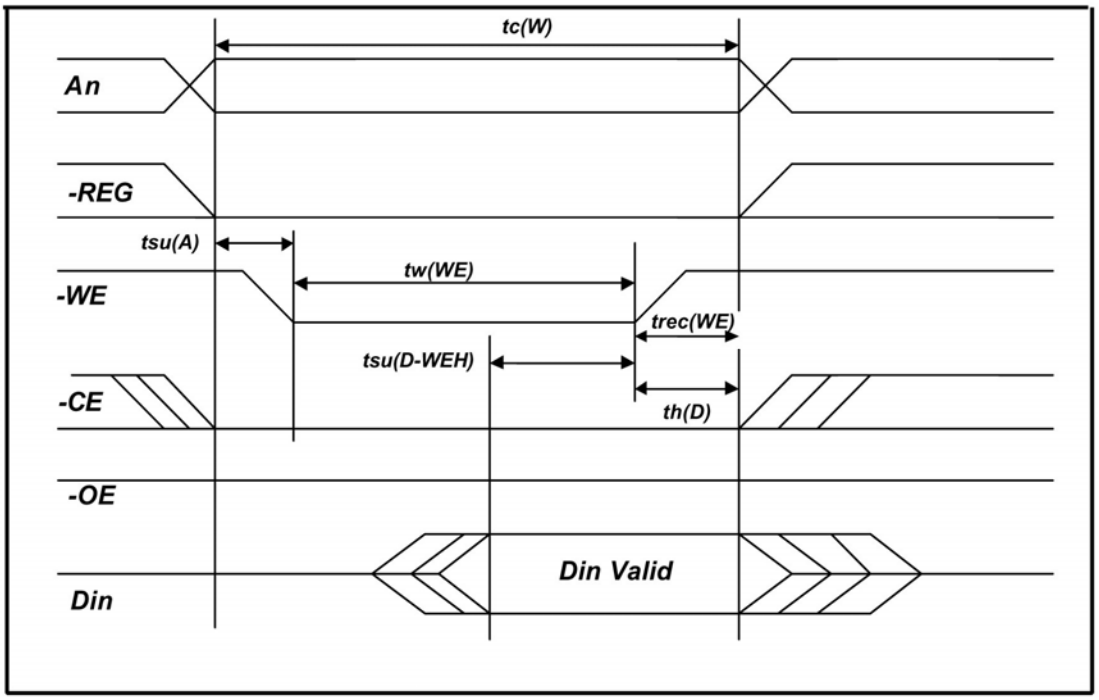
Table 3-3: Attribute Memory Write Access

Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby mode (no access)	X	1	1	X	X	X	X	X	High-Z	High-Z
CIS Byte Access (Invalid)	0	1	0	0	0	0	1	0	Don't Care	Even byte
Configuration Byte Access	0	1	0	0	1	0	1	0	Don't Care	Even byte
CIS Word Access (Invalid)	0	0	0	0	0	X	1	0	Don't Care	Even Byte
Configuration Word Access	0	0	0	0	1	X	1	0	Don't Care	Even byte

Table 3-4: Attribute Memory Write Timing

Speed Version			250ns	
Parameters	**Symbol**	**IEEE Symbol**	**Min (ns)**	**Max (ns)**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Figure 3-2: Attribute Memory Write Timing Diagram



3.6.3 Common Memory Read

Table 3-5: Common Memory Read Access

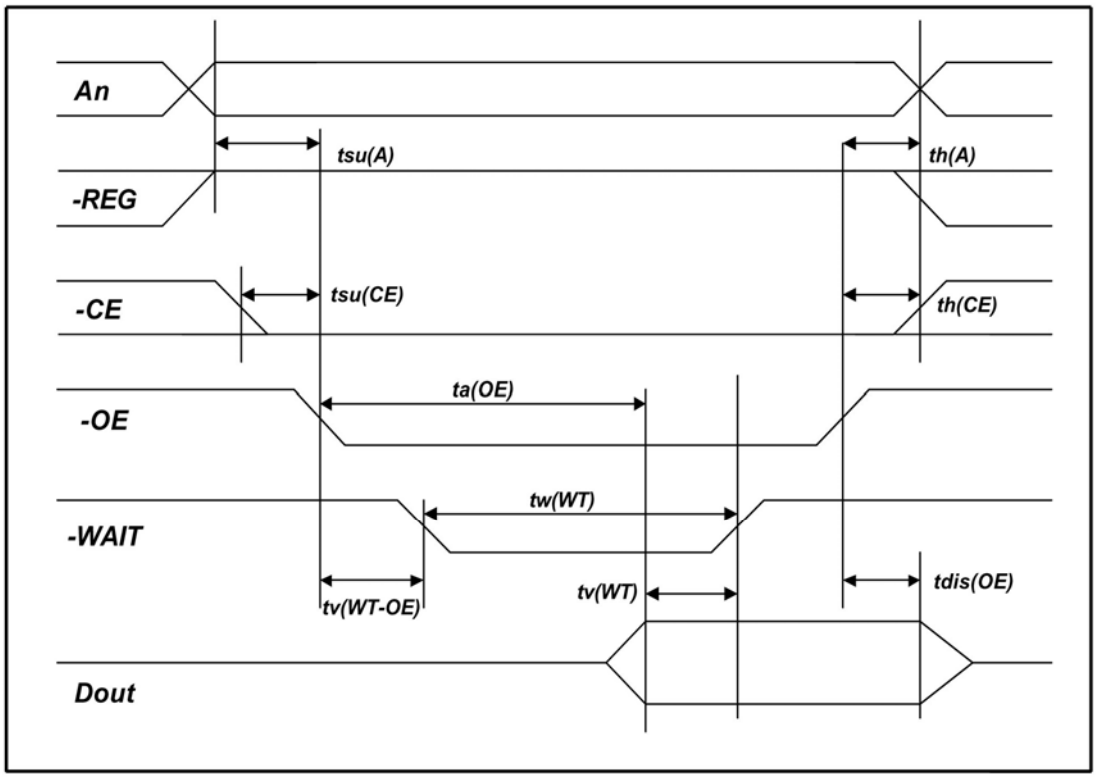
Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D15-D8	D7-D0
Standby mode (no access)	X	1	1	X	X	X	X	X	High-Z	High-Z
8/16-bit mode (even byte)	1	1	0	0	0	1	1	1	High-Z	Even byte
8-bit mode (odd byte)	1	1	0	1	0	1	1	1	High-Z	Odd byte
16-bit mode (odd byte only)	1	0	1	0	0	1	1	1	Odd byte	High-Z
16-bit mode (even & odd byte)	1	0	0	0	0	1	1	1	Odd byte	Even byte

Table 3-6: Common Memory Read Timing

Parameters	Symbol	IEEE Symbol	250 ns Cycle Mode		120 ns Cycle Mode		100 ns Cycle Mode		80 ns Cycle Mode	
			Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		NA[1]
Data Setup for Wait Release	tv(WT)	tQWTH		0		0		0		NA[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350		350		350		NA[1]

Note: 1) WAIT is not supported in this mode. 2) The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120ns Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the UGB30STXXXXXXX Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS).

Figure 3-3: Common Memory Read Timing Diagram



3.6.4 Common Memory Write

Table 3-7: Common Memory Write Access

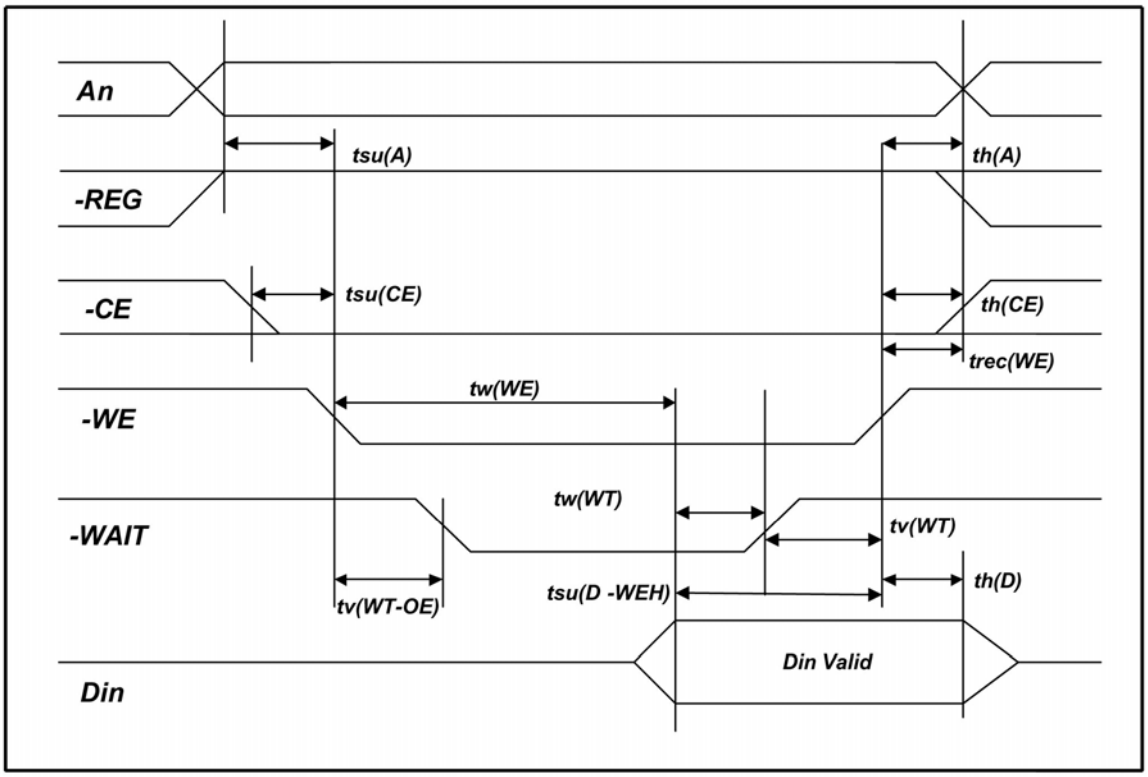
Mode	-REG	-CE1	-CE2	A0	-OE	-WE	-IORD	-IOWR	D15-D8	D7-D0
Standby mode (no access)	X	1	1	X	X	X	X	1	High-Z	High-Z
8/16-bit mode (even byte)	1	0	1	0	1	0	X	1	High-Z	Even byte
8-bit mode (odd byte)	1	0	1	1	1	0	X	1	High-Z	Odd byte
16-bit mode (odd byte only)	1	1	0	0	1	0	X	1	Odd byte	High-Z
16-bit mode (even & odd byte)	1	0	0	0	1	0	X	1	Odd byte	Even byte

Table 3-8: Common Memory Write Timing

Parameters	Symbol	IEEE Symbol	250 ns Cycle Mode		120 ns Cycle Mode		100 ns Cycle Mode		80 ns Cycle Mode	
			Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		15	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35		35	10	NA[1]
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		NA[1]	
Wait Width Time	tw(WT)	tWTLWTH		350		350		350		NA[1]

Note: 1) WAIT is not supported in this mode. 2) The maximum load on –WAIT is 1 LSTTL with 50pF (40pF below 120ns Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the UGB30STXXXXXXX Card to the system. The –WAIT signal may be ignored if the –OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure (CIS).

Figure 3-4: Common Memory Write Timing Diagram



3.6.5 I/O Memory Read

Table 3-9: I/O Memory Read Access

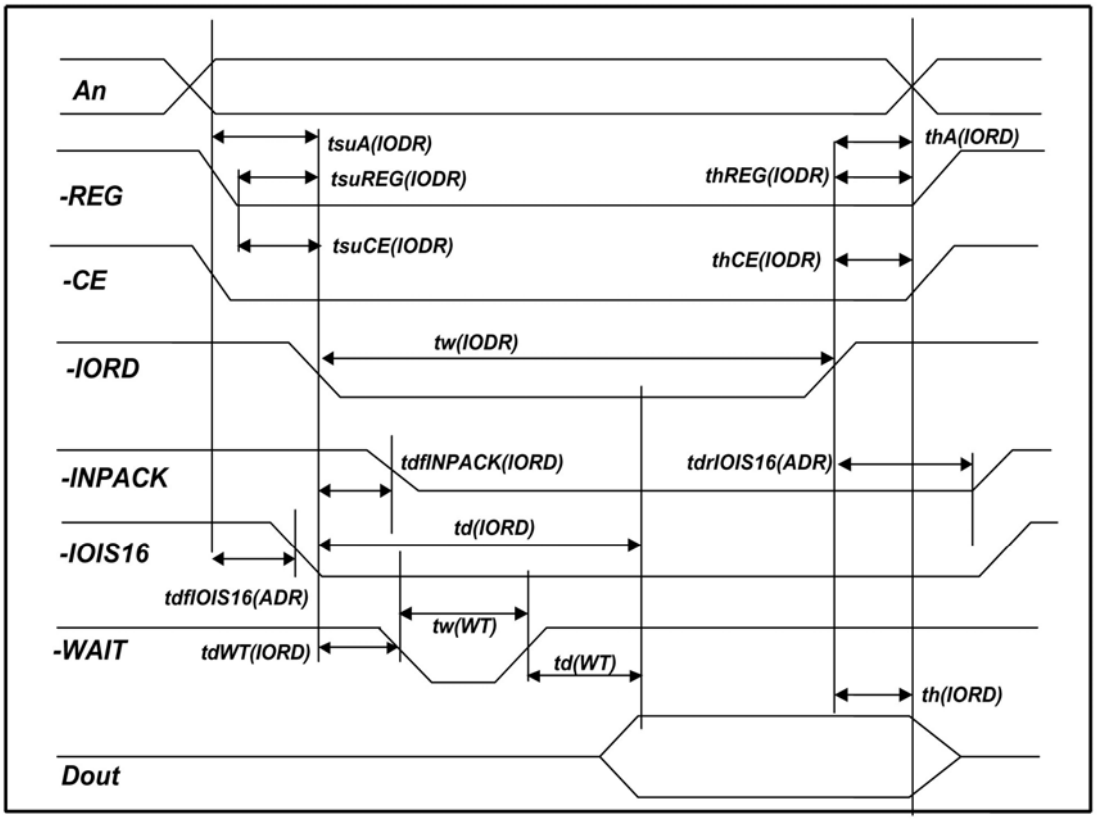
Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D15-D8	D7-D0
Standby mode (no access)	X	1	1	X	X	X	X	X	High-Z	High-Z
8/16-bit mode (even byte)	0	1	0	0	1	1	0	1	High-Z	Even byte
8-bit mode (odd byte)	0	1	0	1	1	1	0	1	High-Z	Odd byte
16-bit mode (odd byte only)	0	0	1	0	1	1	0	1	Odd byte	High-Z
16-bit mode (even & odd byte)	0	0	0	0	1	1	0	1	Odd byte	Even byte

Table 3-10: I/O Memory Read Timing

Parameters	Symbol	IEEE Symbol	250 ns Cycle Mode		120 ns Cycle Mode		100 ns Cycle Mode		80 ns Cycle Mode	
			Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdINPACK(IORD)	tIGLIAL	0	45	0	NA[1]	0	NA[1]	0	NA[1]
INPACK Delay Rising from IORD[3]	tdrINPACK(IORD)	tIGHIAH		45		NA[1]		NA[1]		NA[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16(ADR)	tAVISL		35		NA[1]		NA[1]		NA[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16(ADR)	tAVISH		35		NA[1]		NA[1]		NA[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		NA[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		NA[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350		350		350		NA[2]

Note: 1) -IOIS16 and –INPACK are not supported in this mode. 2) WAIT is not supported in this mode. 3) The maximum load on –WAIT, -INPACK and –IOIS16 is 1 LSTTL with 50pF (40pF below 120ns Cycle Time) total load. All times are in nanoseconds. Minimum time from –WAIT high to –IORD high is 0ns, but minimum –IORD width shall be met. Dout signifies data provided by the UGB30STXXXXXXX Card to the system.

Figure 3-5: I/O Memory Read Timing Diagram



3.6.6 I/O Memory Write

Table 3-11: I/O Memory Write Access

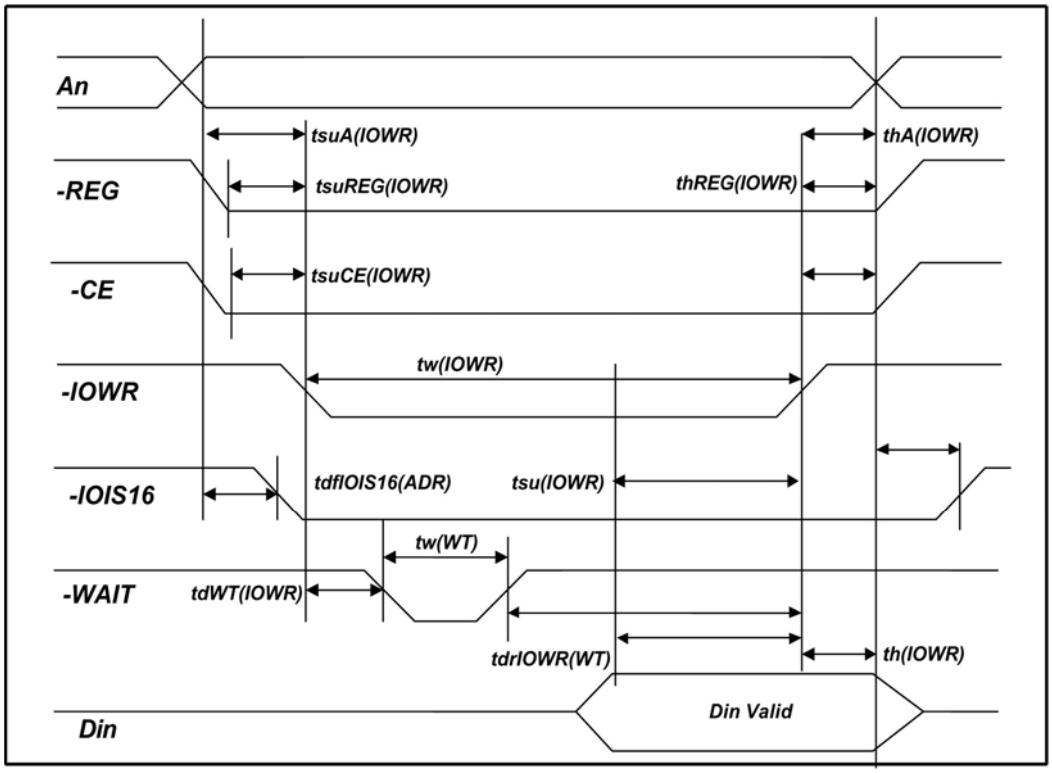
Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D15-D8	D7-D0
Standby mode (no access)	X	1	1	X	X	X	X	X	High-Z	High-Z
8/16-bit mode (even byte)	0	1	0	0	1	1	1	0	High-Z	Even byte
8-bit mode (odd byte)	0	1	0	1	1	1	1	0	High-Z	Odd byte
16-bit mode (odd byte only)	0	0	1	0	1	1	1	0	Odd byte	High-Z
16-bit mode (even & odd byte)	0	0	0	0	1	1	1	0	Odd byte	Even byte

Table 3-12: I/O Memory Write Timing

Parameters	Symbol	IEEE Symbol	250 ns Cycle Mode		120 ns Cycle Mode		100 ns Cycle Mode		80 ns Cycle Mode	
			Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35		NA[1]		NA[1]		NA[1]
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35		NA[1]		NA[1]		NA[1]
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35		35		35		NA[2]
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0		0		0		NA[2]	
Wait Width Time	tw(WT)	tWTLWTH		350		350		350		NA[2]

Note: 1) -IOIS16 and –INPACK are not supported in this mode. 2) WAIT is not supported in this mode. 3) The maximum load on –WAIT, -INPACK and –IOIS16 is 1 LSTTL with 50pF (40pF below 120ns Cycle Time) total load. All times are in nanoseconds. Minimum time from –WAIT high to –IORD high is 0ns, but minimum –IORD width shall be met. Din signifies data provided by the UGB30STXXXXXXX Card to the system.

Figure 3-6: I/O Memory Write Timing Diagram



3.6.7 True IDE PIO Mode Read Access

Table 3-13: True IDE Read Access

Mode	-CE2	-CE1	A2-A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid mode	0	0	X	X	X	High-Z	High-Z
Standby mode	1	1	X	X	X	High-Z	High-Z
Task file read	1	0	1-7h	0	1	High-Z	Data Out
Data Register read	1	0	0	0	1	Odd byte Out	Even byte Out
Alt Status read	0	1	6h	0	1	High-Z	Data Out

3.6.8 True IDE PIO Mode Write Access

Table 3-14: True IDE Write Access

Mode	-CE2	-CE1	A2-A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid mode	0	0	X	X	X	High-Z	High-Z
Standby mode	1	1	X	X	X	High-Z	High-Z
Task file write	1	0	1-7h	1	0	X	Data In
Device Control write	0	1	6h	1	0	x	Data In
Data Register write	1	0	0h	1	0	Odd Byte In	Even Byte In

Table 3-15: True IDE PIO Read/Write Timing

Parameters	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
Cycle time (min)	t0	600	383	240	180	120	100	80	1
Address Valid to –IORD/IOWR setup (min)	t1	70	50	30	30	25	15	10	
-IORD/-IOWR (min)	t2	165	125	100	80	70	65	55	1
-IORD/-IOWR (min) Register (8-bit)	t2	290	290	290	80	70	65	55	1
-IORD/-IOWR recovery time (min)	t2i	-	-	-	70	25	25	20	
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	
-IORD data setup (min)	t5	50	35	20	20	20	15	10	
-IORD data hold (min)	t6	5	5	5	5	5	5	5	
-IORD data tristate (max)	t6Z	30	30	30	30	30	20	20	2
Address valid to –IOCS16 assertion (max)	t7	90	50	40	N/A	N/A	N/A	N/A	4
Address valid to –IOCS16 released (max)	t8	60	45	30	N/A	N/A	N/A	N/A	4
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	
Read Data Valid to IORDY active (min) (if IORDY initially low after tA)	tRD	0	0	0	0	0	0	0	
IORDY Setup time	tA	35	35	35	35	35	N/A[5]	N/A[5]	3
IORDY Pulse Width (max)	tB	1250	1250	1250	1250	1250	N/A[5]	N/A[5]	
IORDY assertion to release (max)	tC	5	5	5	5	5	N/A[5]	N/A[5]	

Note: All timings are in nanoseconds. The maximum load on –IOCS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from IORDY high to –IORD high is 0 ns, but minimum –IORD width must be still met.

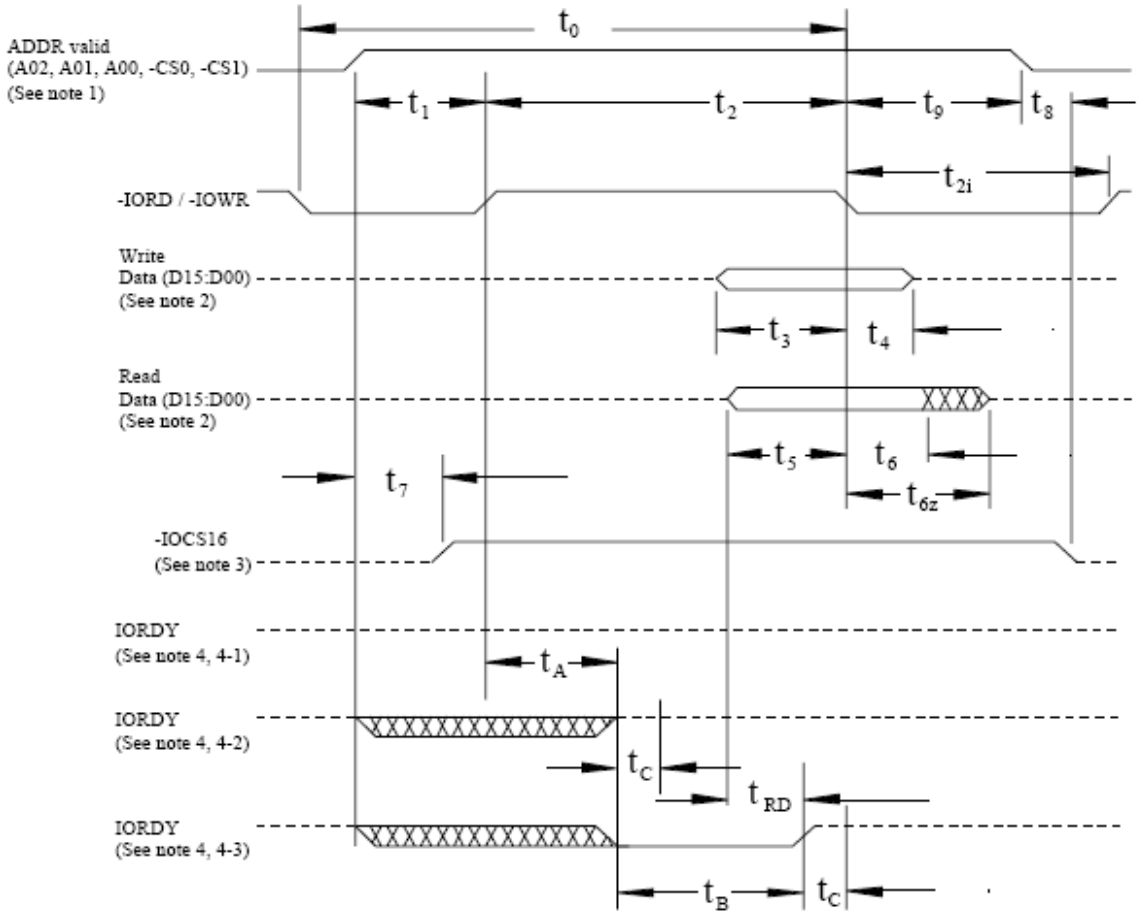
1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle a time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify drive data. A CF Card implementation shall support any legal host implementation.

2) This parameter specifies the time from the negation edge of –IORD to the time that the CF Card (tri-state) no longer drives the data bus.

3) The delay from the activation of –IORD or –IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CF Card is not driving IORDY negated at the tA after the activation of IOR or –IOW, then t5 shall be met and tRD is not applicable. If the CF Card is driving IORDY negated at the time tA after the activation of –IOR or –IOW, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1, and 2. For other modes, this signal is not valid.

Figure 3-8: True IDE Read/Write Timing Diagram



Note : 1) Device Address consists of signals –CS0, -CS1 and A(2:0)

2) Data consists of D(16:0) (16-bit) or D(7:0) (8-bit)

3) –IOCS16 shown for PIO modes 0, 1, and 2. For other modes, this signal is not valid

4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of –IORD or –IOWR. The assertion and negation of IORDY are described in the following three cases:

5) Device never negates IORDY: no wait is generated.

6) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: no wait generated.

7) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and –IR is asserted, the device shall place read data on D(15:0) for tRD before causing IORDY to be asserted.

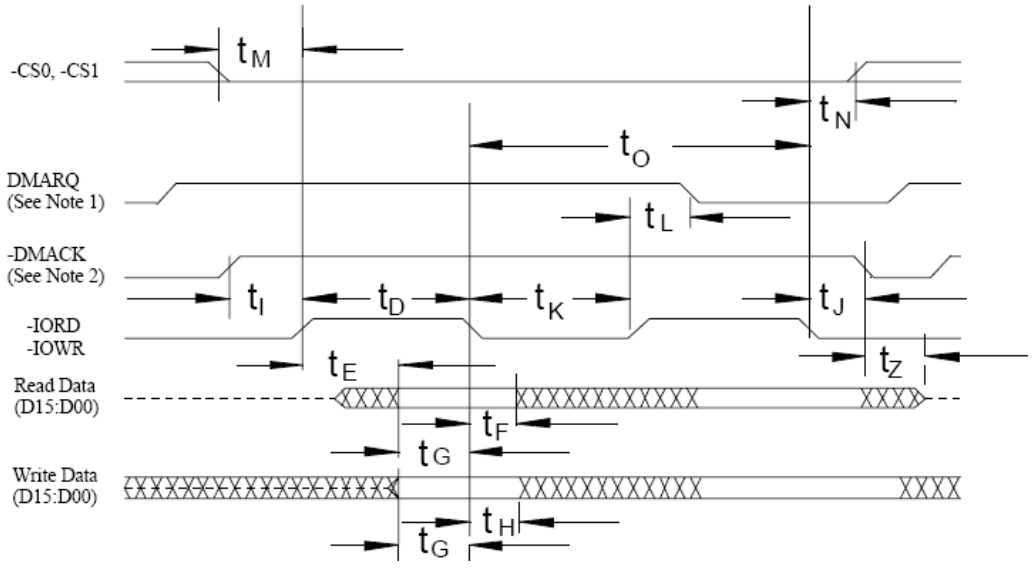
3.6.9 True IDE Mode Multiword DMA

Table 3-15: True IDE Mode Multiword DMA Read/Write Timing

Parameters	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note
Cycle time (min)	to	480	150	120	100	80			1
-IORD / -IOWR asserted width (min)	t_D	215	80	70	65	55			1
-IORD data access (max)	t_E	150	60	50	50	45			
-IORD data hold (min)	t_F	5	5	5	5	5			
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10			
-IOWR data hold (min)	t_H	20	15	10	5	5			
DMACK to –IORD/-IOWR setup (min)	t_I	0	0	0	0	0			
-IORD / -IOWR to -DMACK hold (min)	t_J	20	5	5	5	5			
-IORD negated width (min)	t_{KR}	50	50	25	25	20			1
-IOWR negated width (min)	t_{KW}	215	50	25	25	20			1
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35			
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35			
CS(1:0) valid to –IORD / -IOWR	t_M	50	30	25	10	5			
CS(1:0) hold	t_N	15	10	10	10	10			
-DMACK	t_Z	20	25	25	25	25			

Notes: 1) t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW}.for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

Figure 3-9: True IDE Multiword DMA Mode Read/Write Timing Diagram



Notes: (1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
(2) This signal may be negated by the host to suspend the DMA transfer in progress.

3.6.10 True IDE Mode Ultra DMA

Table 3-16: True IDE UDMA Read/Write Timing

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode 4 (ns)		Measurement location (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note 3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note 4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes: 1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V. 2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and -DMARDY transitions are measured at the sender connector. 3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender. 4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector. 5)The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

Table 3-17: True IDE UDMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Table 3-18: True IDE UDMA Sender and Recipient IC Timing Requirements

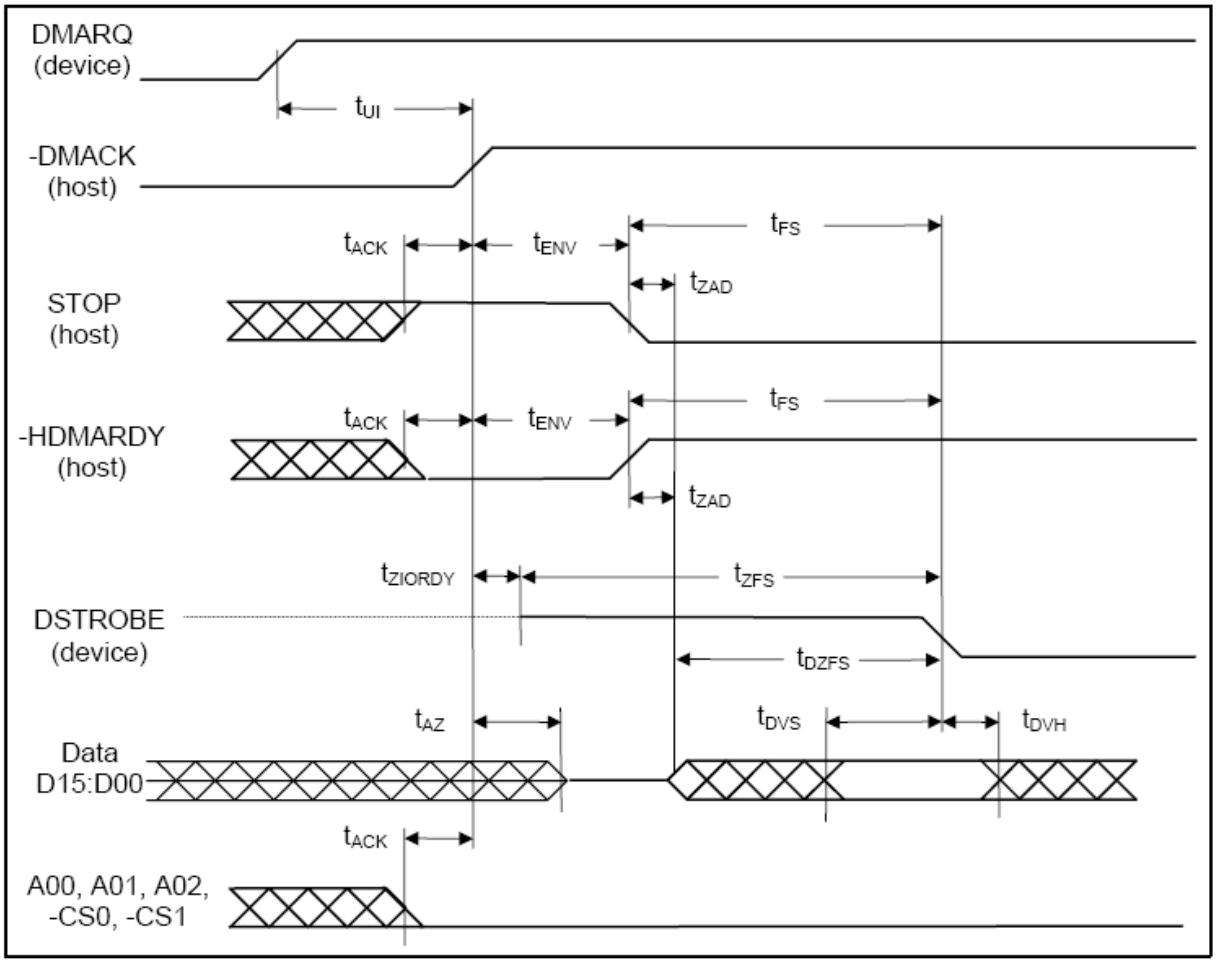
Name	Comments	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8		4.8		4.8	
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0		9.0		9.0	

Notes: 1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V. 2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V). 3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 3-19: True IDE UDMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Figure 3-10: True IDE Mode UDMA Data-In Burst Initiation Timing



Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted.

Figure 3-11: True IDE Mode Sustained UDMA Data-In Burst Timing

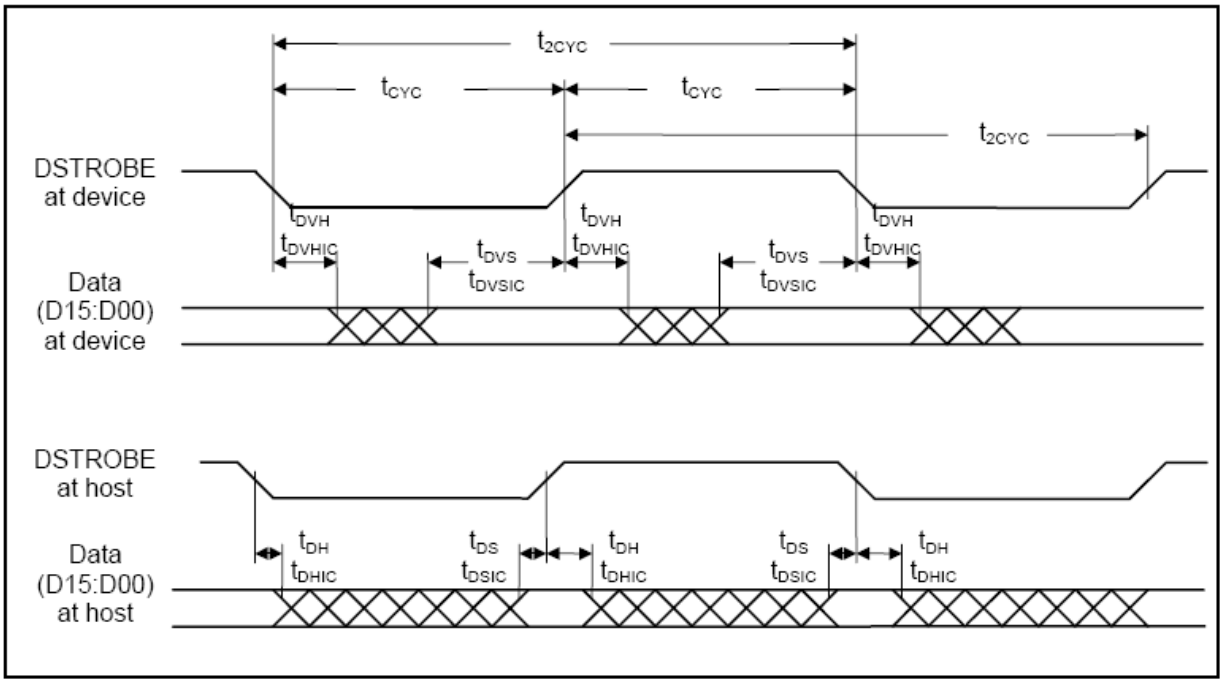


Figure 3-12: True IDE Mode UDMA Data-In Burst Host Pause Timing

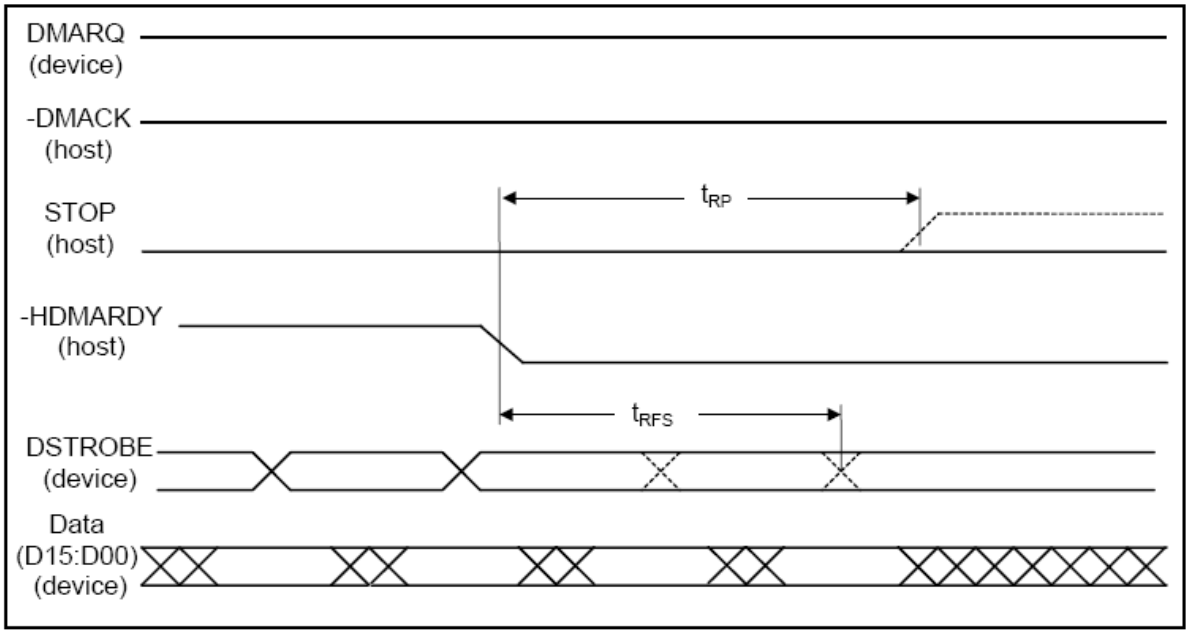


Figure 3-13: True IDE Mode UDMA Data-In Burst Device Termination Timing

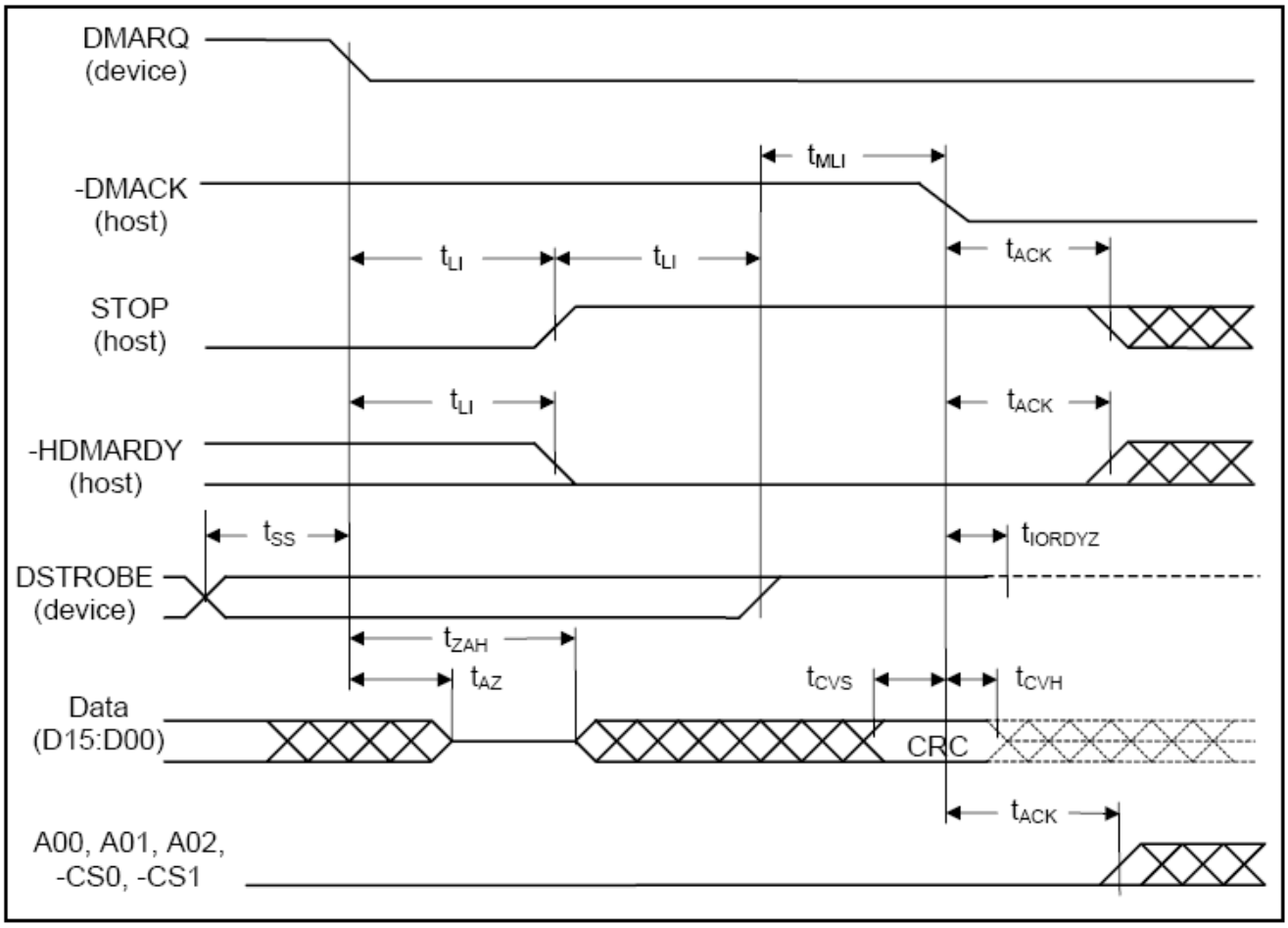


Figure 3-14: True IDE Mode UDMA Data-In Burst Host Termination Timing

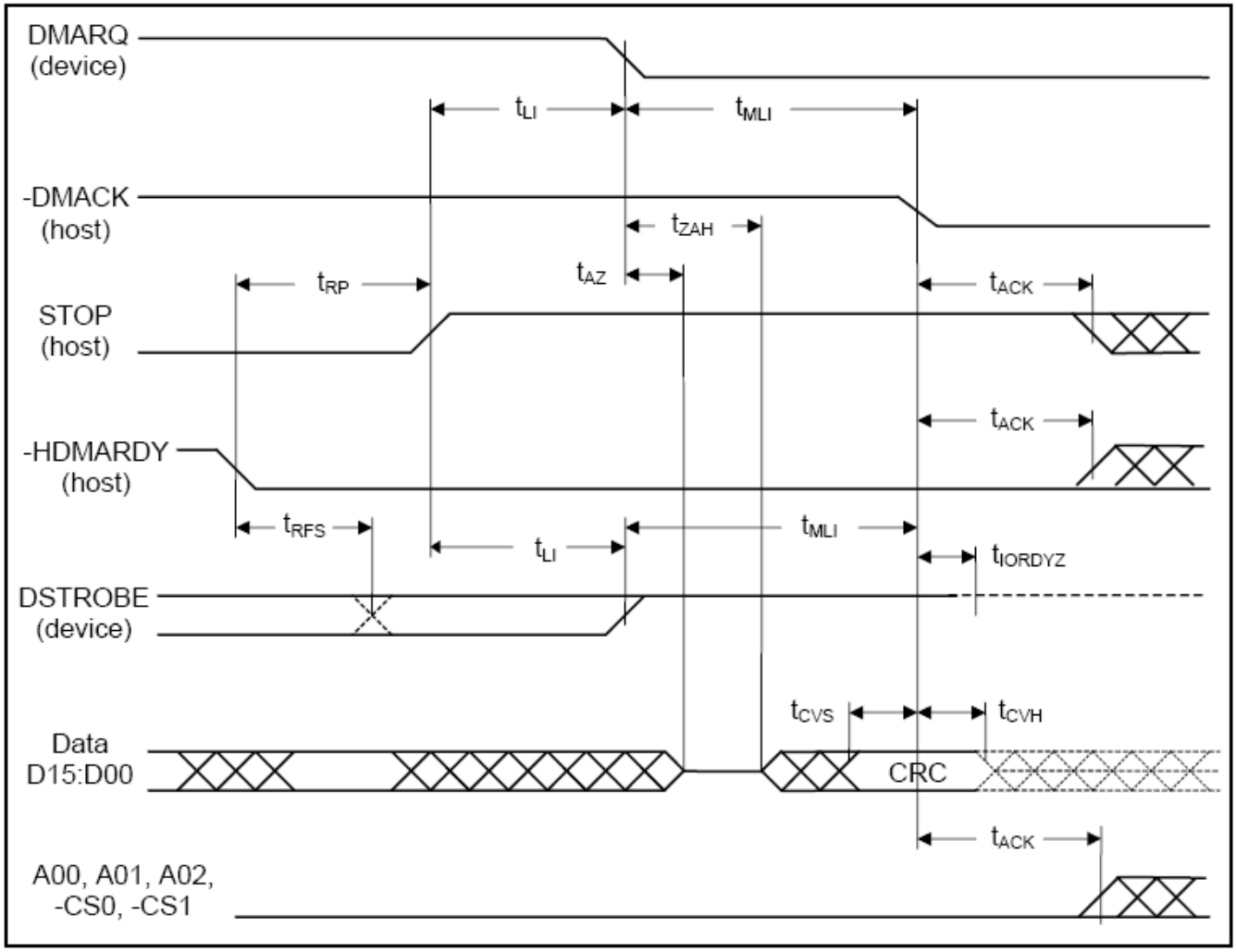


Figure 3-15: True IDE Mode UDMA Data-Out Burst Initiation Timing

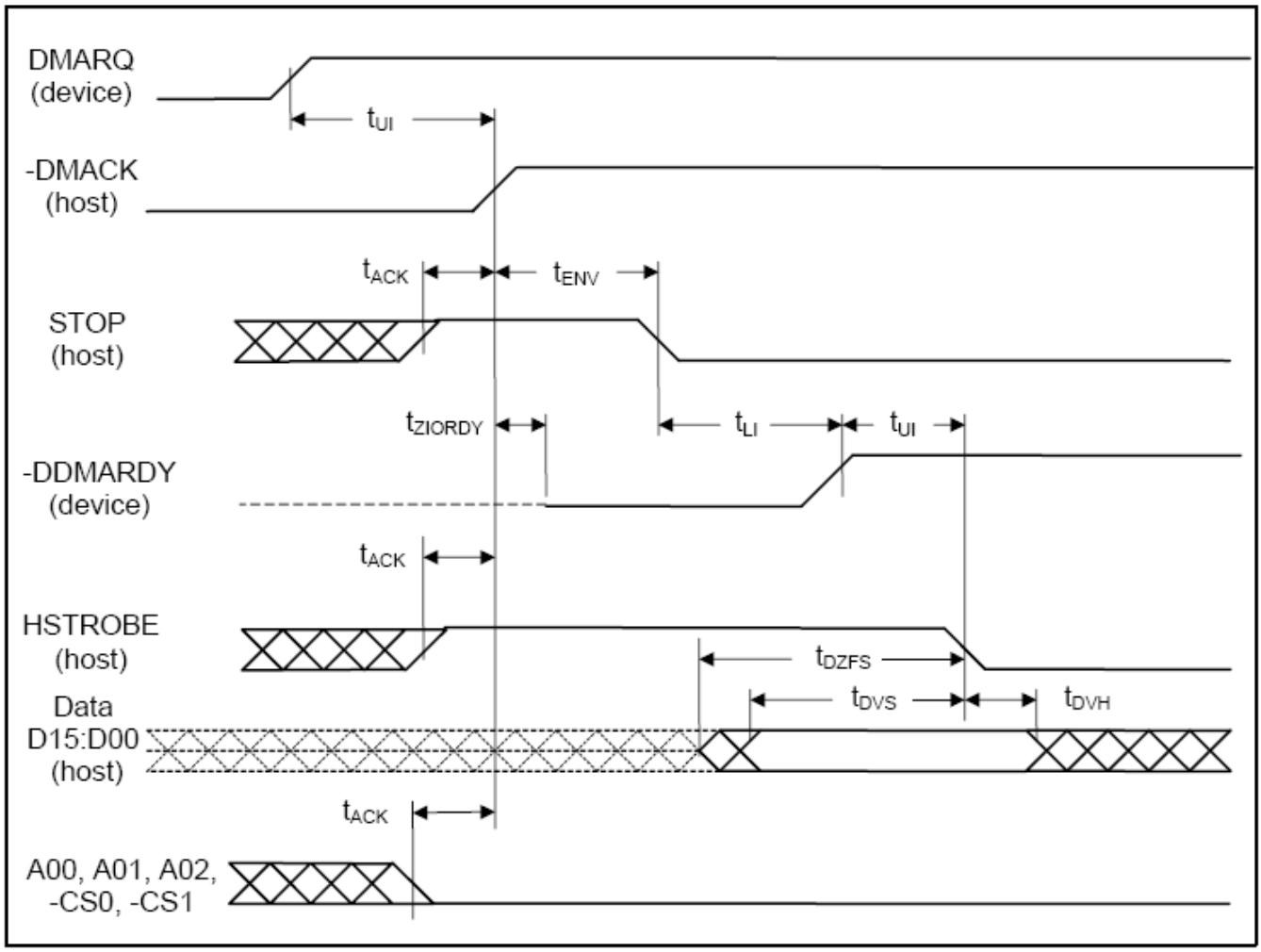


Figure 3-16: True IDE Mode UDMA Data-Out Burst Initiation Timing

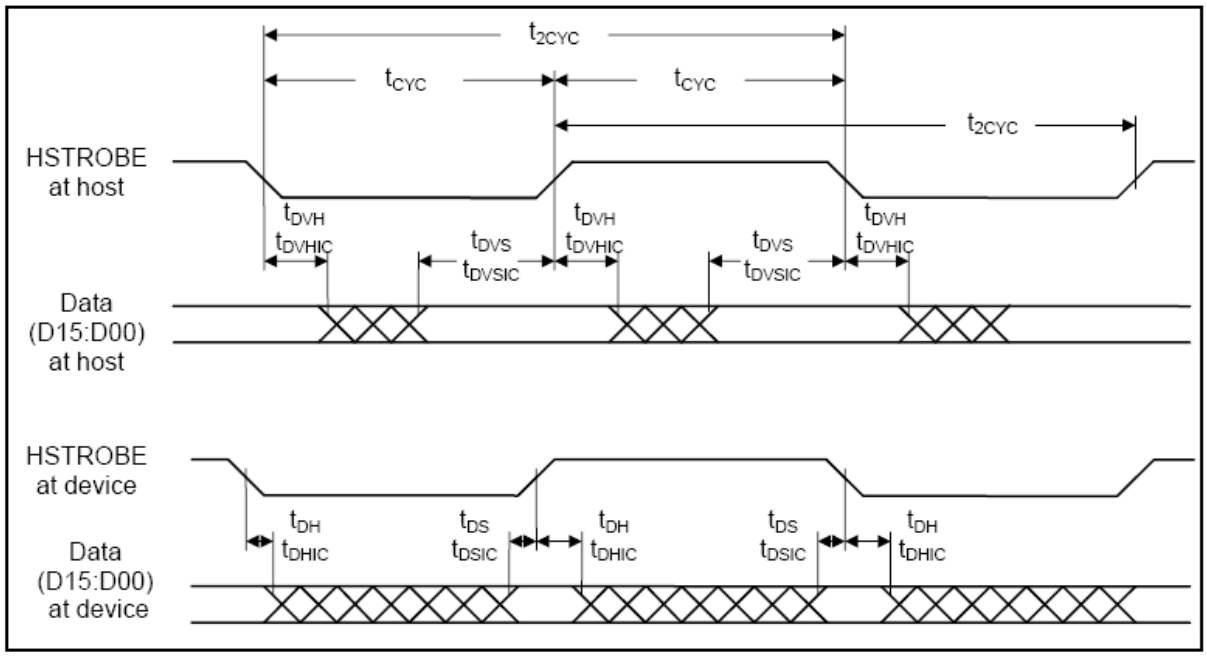


Figure 3-17: True IDE Mode Sustained UDMA Data-Out Burst Timing

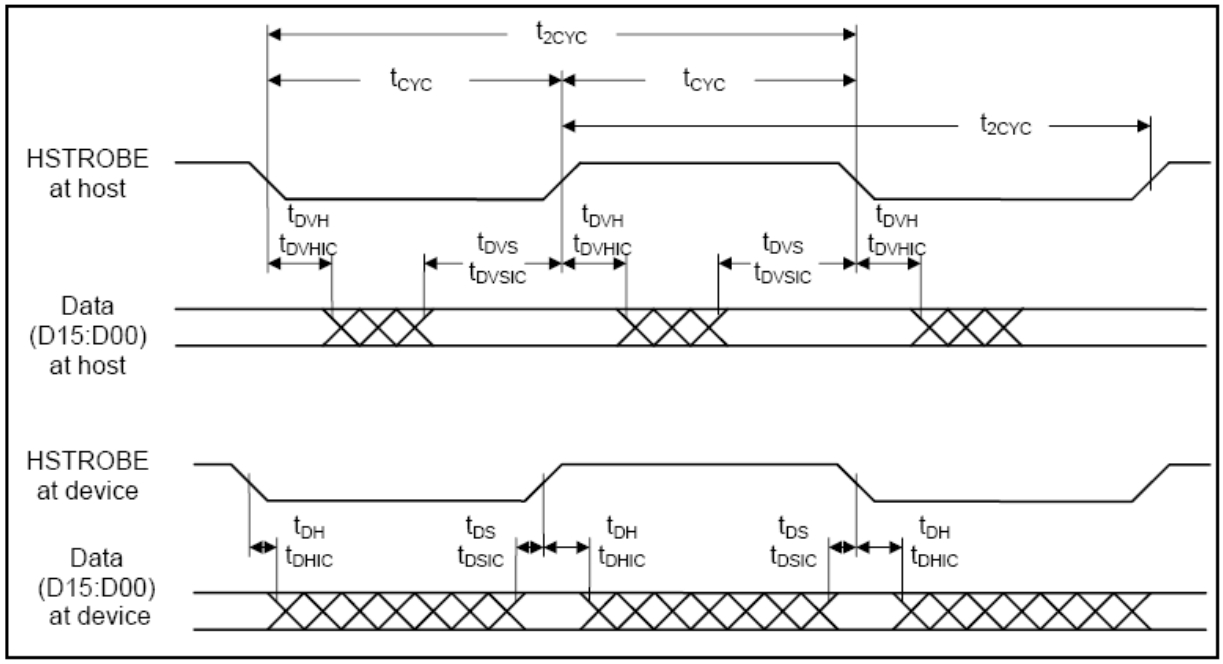


Figure 3-18: True IDE Mode UDMA Data-Out Burst Device Pause Timing

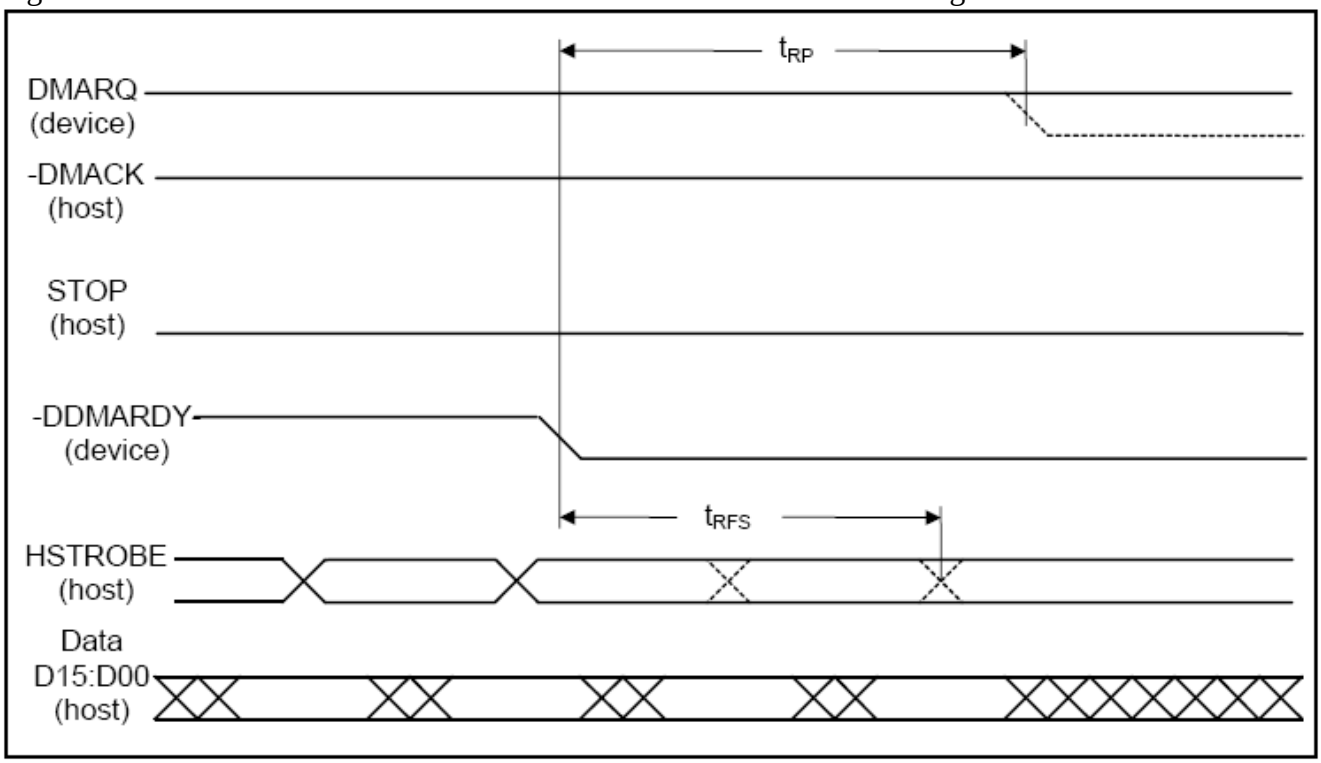
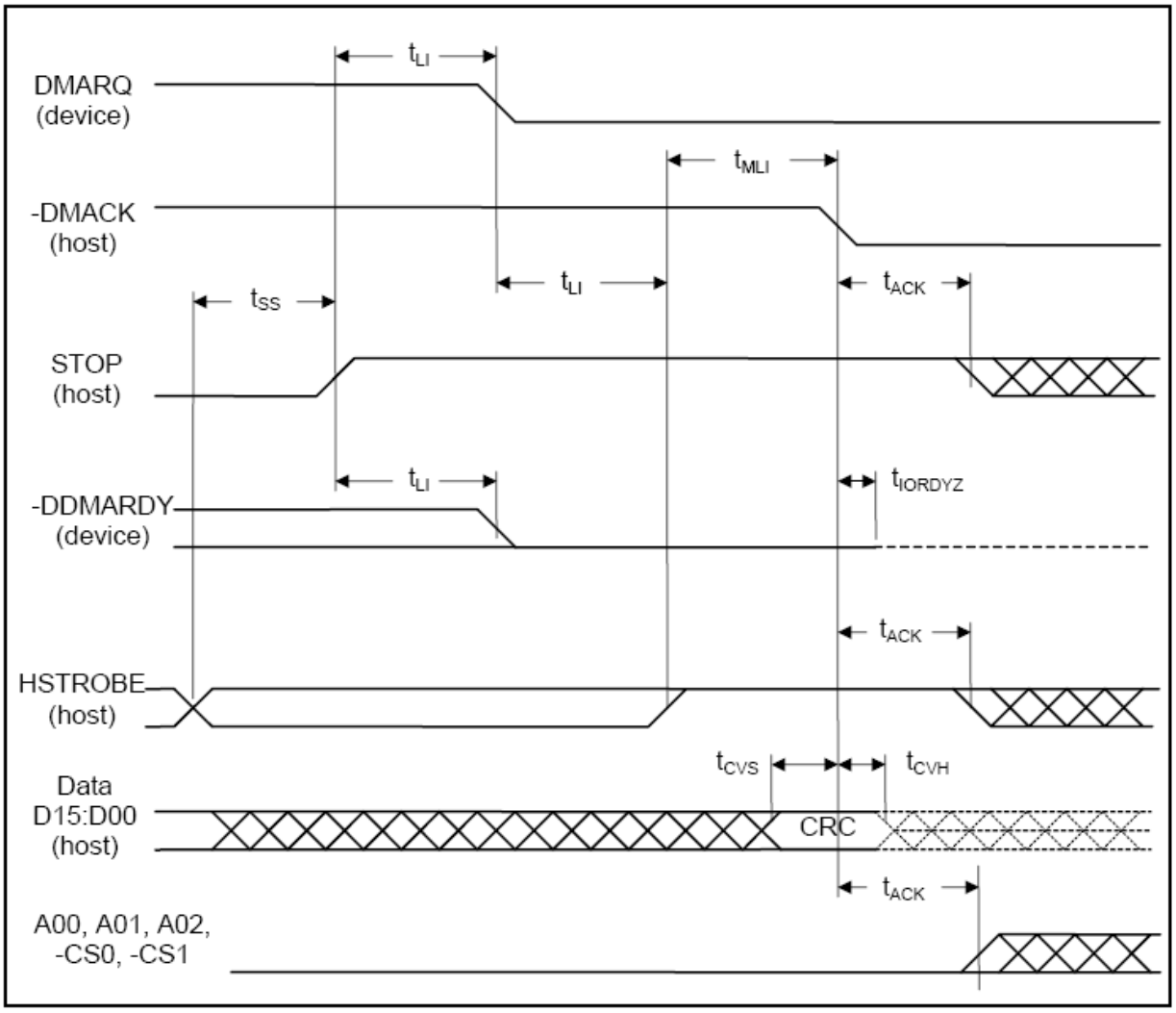


Figure 3-19: True IDE Mode UDMA Data-Out Burst Device Termination Timing



4 HOST INTERFACE AND REGISTERS

This section provides the Host interface and registers for Unigen Corporation's CompactFlash card.

Unigen Corporation's CompactFlash card supports two Host modes:

- PC Card ATA Mode
- True IDE Mode

The CompactFlash card automatically senses its environment and configures itself on power-up to either the PC Card ATA Mode or the True IDE Mode. The local processor can override the configuration. In both the PC Card ATA Mode and the True IDE Modes the CompactFlash is electrically compliant with the CompactFlash specifications.

4.1 PC Card ATA Configuration Registers

The Card Configuration Registers described in the following sections are addressable by the Host.

4.1.1 Configuration Option Register

Attribute Memory Address 200H (Read/Write)

The Configuration Option register is used by the Host System to configure the CompactFlash card and to issue soft resets to the CompactFlash. This register is reset at system Power On and by the HRESET signal (after the CompactFlash is configured in PC Card ATA or True IDE extension mode).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRESET	LevIREQ	Configuration Index. See Decode Table below					

Bit 7	R/W	**Soft Reset:** When this bit is set to a logic one, the Host Interface is in the reset state. This reset condition is the same as a hardware or power-on reset state with the exception that this bit stays set. This software reset condition is removed when this bit is reset to a logic zero. Following a power-on or hardware reset this bit is cleared.
Bit 6	R/W	**Level Mode/Pulsed Mode Interrupt Request:** Level Mode Interrupts are selected when this bit is one. Pulse Mode Interrupts are selected when this bit is zero. A pulsed-mode interrupt is asserted by placing an active-going (low) pulse on the interrupt line. The pulse width is at least 0.5 microseconds. A level-mode interrupt is asserted by placing the interrupt line in an active (low) state until the interrupt has been serviced by the system. The interrupt is driven in the inactive state.
Bits 5:0	R/W	**Configuration Index:** This 6-bit field comprises the configuration index. These 6-bits are initialized after a power-on, hardware or software reset to a field of six zeroes. This places the controller in a mode to accept attribute memory accesses only. The Host system should load a non-null value into this register after scanning and parsing the tuples in the CIS. This index points to the I/O configuration this Host system requires. Certain nonzero values in this field switch the CompactFlash from Common Memory mode to I/O mode. Bits 1:0 of this register are used to directly decode the addressing option chosen by the Host system. This provides the Host with immediate access to the CompactFlash Task File after writing the Configuration Option register.

Configuration Index Decode Table			
Bit 1	**Bit 0**	**Selected Decode Mode**	**See Table**
0	0	Common Memory Linear Address AT Decode	Table 7-1
0	1	I/O Independent Linear Address AT Decode	Table 7-1
1	0	I/O Standard Primary AT Decode	Table 7-1
1	1	I/O Standard Secondary AT Decode	Table 7-1

Table 4-1: Common Memory Linear Address AT Decode: Configuration Index

Register-Enable Address						Register(s) Enabled when - OE=0 (Read)	Register(s) Enabled when - WE=0 (Write)
-CE1	**-CE2**	**-REG**	**A10**	**A9–A4**	**A3–A0**		
0	0	1	0	Don't Care	000X	16-bit Data (D15:D0)	16-bit Data (D15:D0)
0	1	1	0	Don't Care	0H	Even/Odd Data (D7:D0)	Even/Odd Data (D7:D0)
1	0	1	0	Don't Care	000X	Error register (D15:D8)	Features (D15-:D8)
0	1	1	0	Don't Care	1H	Error register (D7:D0)	Features (D7:D0)
0	0	1	0	Don't Care	001X	Sector Count (D7:D0) Sector Number (D15:D8)	Sector Count (D7:D0) Sector Number (D15:D8)
0	1	1	0	Don't Care	2H	Sector Count (D7:D0)	Sector Count (D7:D0)
0	1	1	0	Don't Care	3H	Sector Number (D7:D0)	Sector Number (D7:D0)
1	0	1	0	Don't Care	3H	Sector Number (D15:D8)	Sector Number (D15:D8)
0	0	1	0	Don't Care	010X	Cylinder Low (D7:D0) Cylinder High (D15:D8)	Cylinder Low (D7:D0) Cylinder High (D15:D8)
0	1	1	0	Don't Care	4H	Cylinder Low (D7:D0)	Cylinder Low (D7:D0)
0	1	1	0	Don't Care	5H	Cylinder High (D7:D0)	Cylinder High (D7:D0)
1	0	1	0	Don't Care	5H	Cylinder High (D15:D8)	Cylinder High (D15:D8)
0	0	1	0	Don't Care	011X	Drive/Head (D7:D0) Status (D15:D8)	Drive/Head (D7:D0) Command (D15:D8)
0	1	1	0	Don't Care	6H	Drive/Head (D7:D0)	Drive/Head (D7:D0)
0	1	1	0	Don't Care	7H	Status (D7:D0)	Command (D7:D0)
1	0	1	0	Don't Care	7H	Status (D15:D8)	Command (D15:D7)
0	0	1	0	Don't Care	100X	Duplicate Data (D15:D0)	Duplicate Data (D15:D0)
0	1	1	0	Don't Care	8H	Duplicate Even Data (D7:D0)	Duplicate Even Data (D7:D0)
1	0	1	0	Don't Care	9H	Duplicate Odd Data (D15:D8)	Duplicate Odd Data (D15:D8)
0	1	1	0	Don't Care	9H	Duplicate Odd Data (D7:D0)	Duplicate Odd Data (D7:D0)
0	0	1	0	Don't Care	110X	Undefined (D7:D0) Duplicate Error (D15:D8)	Undefined (D7:D0) Duplicate Error (D15:D8)
0	1	1	0	Don't Care	DH	Duplicate Error (D7:D0)	Duplicate Feature (D7:D0)
0	0	1	0	Don't Care	111X	Alternate Status (D7:D0) Drive Address (D15:D8)	Device Control (D7:D0) Undefined (D15:D8)
0	1	1	0	Don't Care	EH	Alternate Status (D7:D0)	Device Control (D7:D0)
0	1	1	0	Don't Care	FH	Drive Address (D7:D0)	Not Used

Table 4-1: Common Memory Linear Address AT Decode: Configuration Index

Register-Enable Address						Register(s) Enabled when - OE=0 (Read)	Register(s) Enabled when - WE=0 (Write)
-CE1	-CE2	-REG	A10	A9–A4	A3–A0		
1	0	1	0	Don't Care	FH	Drive Address (D15:D8)	Not Used
0	0	1	1	Don't Care	Don't Care	16-bit Data (D15:D0)	16-bit Data (D15:D0)
0	1	1	1	Don't Care	XXX0	Even Data (D7:D0)	Even Data (D7:D0)
0	1	1	1	Don't Care	XXX1	Odd Data (D7:D0)	Odd Data (D7:D0)
1	0	1	1	Don't Care	XXX0	Odd Data (D15:D8)	Odd Data (D15:D8)
1	0	1	1	Don't Care	XXX1	Odd Data (D15:D8)	Odd Data (D15:D8)

4.1.2 Configuration and Status Register

Attribute Memory Address 202H (Read/Write)

The configuration and status register is implemented in the CompactFlash to ensure that the Host interface has all status available to it on signal pins or bits in this register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Changed	SigChg	I/Ois8	Rsvd 0	Audio	PwrDwn	Intr	Rsvd 0

Bit 7	R	Changed: This bit indicates that one or more of the Pin Replacement register bits CRdy/-Bsy (Register 204H, bit 5) or CWProt (Register 204H, bit 4) is set to one.
Bit 6	R/W	Signal Changed Enable: This bit is set and reset by the Host to control the Signal Changed signal output (bit 7 above and -STSCHG, Pin 46 in the I/O mode). If no state change signal is required, this bit should be set to 0 and -STSCHG signal will be held high in the I/O mode.
Bit 5	R/W	I/O is 8: This bit is used to tell a memory card that the system only accesses data using an 8-bit data path. The control for an 8-bit data access is built into the ATA command set, and still must be used.
Bit 4	–	Reserved: The power-on state of this bit is a zero. This bit is not used and should be left as a zero.
Bit 3	R/W	Audio/DASP: This bit is used to enable the output of the DASP* signal onto the PCMCIA Audio pin. When bit 3 is set, this signal is enabled. When bit 3 is reset, the output of this signal is disabled, and the pin is held at high-impedance. Note: In the Compact Card Interface, the bit is always set to 0, since the Compact Card does not support audio functions
Bit 2	R/W	Power Down: This bit is used to tell a drive card to enter a Power Down mode. For storage, the Storage-Specific Power Down modes are also controlled through the ATA command set.
Bit 1	R	Interrupt: This bit reflects the real time status of the Host Interrupt Signal pin. If interrupts are disabled by the -IEn bit in the Device Control Register.
Bit 0	–	Reserved: This bit is reserved. This bit must be set to 0 when this register is written.

4.1.3 Pin Replacement Register

Attribute Memory Address 204H (Read/Write)

The Pin Replacement register provides status for signals on the PC Card ATA interface that are used in Memory access mode but assume a different meaning or use in I/O mode. The register may be read and

written; however, when written, the lower four bits act as a mask for changing the corresponding upper four bits.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED		CRdy/Bsy	CWProt	RESERVED		Rdy	WProt

Bits 7:6	–	**Reserved:** These bits are reserved. These bits must be set to 0 when this register is written. In the Release 2.0 PCMCIA specification, these bits are the change notification for battery voltage.
Bit 5	R/W	**Changed Rdy/—Bsy:** This bit is set to one when the Rdy bit (bit 1 below) changes state. The Host must clear this bit.
Bit 4	R/W	**Changed Write Protect State:** This bit is set to one when the RWProt bit (bit 0) changes state. The Host must clear this bit.
Bits 3:2	–	**Reserved:** These bits are reserved. These bits must be set to 0 when this register is written. In the Release 2.0 PCMCIA specification, these bits provide the battery voltage status.
Bit 1	R/W	**Rdy/-Bsy:** This bit reflects the real time status of the Rdy/—Bsy signal. This bit may be used to determine the state of the Rdy/—Bsy signal when the pin has the Interrupt function in the PC Card ATA I/O mode. When written, this bit acts as a mask or enable to allow the corresponding bit, Changed Rdy/-Bsy to be written.
Bit 0	R	**Write Protect:** This bit reflects the real time status of the WProt signal. This bit may be used to determine the state of the Wprot signal when the pin has the IOis16 function in the PC Card ATA I/O mode. When written, this bit acts as a mask or enable to allow the corresponding bit Changed CWProt to be written. This bit is always clear.

4.1.4 Socket and Copy Register

Attribute Memory Address 206H (Read/Write)

This Read-Write register may be used by the Host System to implement a substitute for the True IDE Master/Slave functionality. This register, if used, must be written by the system before the CompactFlash's Configuration Option register (Attribute Memory Address 200H).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSVD	Copy Number			Socket Number			

Bit 7	–	This bit is reserved for future PCMCIA standardization. This bit must be set to 0 when this byte is written.
Bits 6-4	R/W	**Copy Number**: **Flash Drive**'s which indicate in their CIS that they support more than one copy of identically configured drive-cards, should have a copy number (0 to MAX twin cards, MAX = n-1, for the ATA protocol, n = 2) written back to this field. This feature can be used to emulate ATA Master/Slave functionality. Only 0 or 1 should be loaded into this field.
Bits 3-0	R/W	**Socket Number:** This field indicates to the CompactFlash that it is located in the nth socket. The first socket is numbered 0.

4.1.5 Summary of Host Commands

Table 4-2 ATA Host Commands support list

Command	Command Code	FR	SC	SN	CY	DR	HD	LBA
Check Power Mode	E5H, 98H	-	-	-	-	Y	-	-
Erase Sectors	C0H	-	Y	Y	Y	Y	Y	Y
Execute Drive Diagnostic	90H	-	-	-	-	-	-	-
Flush Cache	E7H	-	-	-	-	Y	-	-
Format Track	50H	-	Y	-	Y	Y	Y	Y
Identify Drive	ECH	-	-	-	-	Y	-	-
Identify Device DMA	EEH	-	-	-	-	Y	-	-
Idle	E3H,97H	-	Y	-	-	Y	-	-
Idle Immediate	E1H,95H	-	-	-	-	Y	-	-
Initialize Drive Parameters	91h	-	Y	-	-	Y	Y	-
Media Lock	DEH	-	-	-	-	Y	-	-
Media Unlock	DEH	-	-	-	-	Y	-	-
NOP	00H	-	-	-	-	Y	-	-
Read Buffer	E4H	-	-	-	-	Y	-	-
Read DMA	C8H,C9H	-	Y	Y	Y	Y	Y	Y
Read Long Sector	22H, 23H	-	-	Y	Y	Y	Y	Y
Read Multiple	C4h	-	Y	Y	Y	Y	Y	Y
Read Long	22H,23H	-	-	Y	Y	Y	Y	Y
Read Native Max Address	F8H	-	-	-	-	Y	-	-
Read Sectors	20H, 21H	-	Y	Y	Y	Y	Y	Y
Read Verify Sectors	40H, 41H	-	Y	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	Y	-	-
Request Sense	03H	-	-	-	-	Y	-	-
Seek	7XH	-	-	Y	Y	Y	Y	Y
Set Features	EFH	Y	-	-	-	Y	-	-
Set Max Address	F9H	-	Y	Y	Y	Y	Y	Y
Set Multiple Mode	C6H	-	Y	-	-	Y	-	-
Set Sleep Mode	E6H, 99H	-	-	-	-	Y	-	-
Standby	E2H, 96H	-	Y	-	-	Y	-	-
Standby Immediate	E0H, 94H	-	-	-	-	Y	-	-
Translate Sector	87h	-	Y	Y	Y	Y	Y	Y
Wear Leveling	F5H	-	-	-	-	Y	Y	-
Write Buffer	E8H	-	-	-	-	Y	-	-
Write Long Sector	32H, 33H	-	-	Y	Y	Y	Y	Y
Write Multiple	C5H	-	Y	Y	Y	Y	Y	Y
Write Multiple (w/o erase)	CDH	-	Y	Y	Y	Y	Y	Y
Write Sectors	30H, 31H	-	Y	Y	Y	Y	Y	Y
Write Sectors (w/o erase)	38H	-	Y	Y	Y	Y	Y	Y
Write Verify	3CH	-	Y	Y	Y	Y	Y	Y

Notes:
FR: Feature Register
SC: Sector Count register (00H to FFH, 00H means 256 sectors)
SN: Sector Number register
CY: Cylinder Low/High register
DR: Drive bit of Drive/Head register
HD: Head No. (0 to 15) of Drive/Head register
Y: Used for the command —: Not used for the command

4.1.6 Detailed Description of Commands

This section details the functionality of commands supported by the CompactFlash. For each command, the Command Block register contents for the command invoked by the Host, and the Command Block registers updated by the CompactFlash after command completion, are shown. Following is an example of the command description, showing the conventions used for each command description. Throughout this document, the terms 'Task File' and \Command Block' are used interchangeably to refer to the ATA I/O registers.

A detailed description of the execution of the command is provided. This is followed by two tables, the first showing the requirements of the Command Block registers at the time that the Host issues the command to the CompactFlash, and the second showing the contents of the Command Block after completion or termination on error of the command.

Command Block specified by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	Command Code							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	Set Features Code							

The preceding table represents the contents of the Command Block registers when the Host issues the command. Where applicable, the Host first writes the appropriate data into the Features, Sector Count, Sector Number, Cylinder Hi/Low, and Drive/Head registers, and lastly, writes the command code into the Command register. The act of writing to the command register causes the CompactFlash to execute the command based on the contents of the Command Block at that instance.

Note that bits 7 and 5 of the Drive/Head register are denoted as 'nu.' Although the Host is expected to always set these bits to 1 when the command is issued, the CompactFlash ignores the value of these bits.

Command Block specified by CompactFlash upon completion/termination of 'Sample' command								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							

Command Block specified by CompactFlash upon completion/termination of 'Sample' command								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	0	V	0	V	0	0

The above table represents the contents of the Command Block registers upon completion of the command by the CompactFlash.

At the completion of every command, specific bits in the Status register is as follows: the BuSY, DriveWriteFault, DataReQuest, and InDeX bits are always deasserted, while the DriveReaDY, and DriveSeekComplete bits are always asserted. The CORRected ECC bit and the ERRor bit are set or cleared as appropriate.

The contents of the Error register are always set to zero when a command is received, and are only valid if the ERR bit in the Status register is set to '1' at the completion of a command. In addition, the MediaChange, MediaChangeRequest, TracK0NotFound, and AddressMarkNotFound bits are always cleared, regardless of the state of the ERR bit in the Status register.

For the Command Block tables, explanations for each possible code are shown below:

L (LBA Mode bit) — This bit is used to specify whether the requested sector is addressed in the LBA mode or in the Cylinder-Head-Sector, CHS, mode. When set, the LBA mode is specified. The LBA is comprised of the lower significant nibble in the Drive/Head register, LBA [27:24], concatenated with the contents of the Cylinder Hi/Lo, and the Sector registers, LBA [23:0], respectively. If L=0, the sector is addressed in the classic Cylinder/Head/Sector CHS mode.

D (Drive Select bit) — This bit is used to select card 0 or 1, allowing up to two cards to share a single Task File. If two PC Card ATA cards are present in the system, one of the cards may be assigned as copy 0, and the second card may be assigned as copy 1, using the Copy field of the PCMCIA Socket & Copy card configuration register. In this case, the card designated as Copy 0 is selected when D=0. Conversely, the card designated as Copy 1 is selected when D=1.

1 (Bit is Set) — When referring to the Command Block registers when the Host issues a command, this bit must be set to a 1 by the Host before command invocation.

When referring to the Command Block contents read by the Host after completion of a command, the CompactFlash upon command completion sets this bit.

0 (Bit is Cleared) — When referring to the Command Block registers when the Host issues a command, this bit must be cleared to 0 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, the CompactFlash upon command completion clears this bit.

nu (Not Used) — Although the Host may specify this register/bit when invoking the command, the value for this command block register or bit is ignored by the card.

V (Valid Data) — When referring to the Command Block contents read by the Host after completion of a command, the value for the applicable bit is specified by the card.

na (Not Affected) — The value for this bit, or register, is neither set nor cleared by the card; i.e., it is unchanged by the card after command completion.

4.1.7 Check Power Mode

Although this command is supported for backward compatibility, it has no actual function. The card always returns the In Idle mode code 'FFh' in the Sector Count register, in response to this command. Command completion status always indicates command completed with no error.

Check Power Mode Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	98h/E5h							
DRIVE/HEAD	Nu	nu	nu	D	Nu			
CYLINDER HI	Nu							
CYLINDER LOW	Nu							
SECTOR NUM	Nu							
SECTOR COUNT	Nu							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion / termination of Check Power Mode command (98h / E5h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	Na	na	na	na	Na			
CYLINDER HI	Na							
CYLINDER LOW	Na							
SECTOR NUM	Na							
SECTOR COUNT	Power Mode Code is always FFh							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.8 Erase Sectors

This command erases the number of sectors specified in the Sector Count register, starting at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File.

Erase Sectors Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[[27:24] of the starting sector/LBA			

Erase Sectors Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to eraser							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to eraser							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	Nu							

Command Block specified by Flash upon completion/termination of Erase Sectors command (C0h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	V	1	0	0	0	V
DRIVE/HEAD	na	L	na	Na	H[3:0] or LBA[27:24] last good sector erased			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector erased							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector erased							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector erased							
SECTOR COUNT	The number of sectors that were not erased if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

4.1.9 Execute Drive Diagnostic

This command performs self-diagnostics on various internal components of the CompactFlash. Results of the test are reported in the Error register. Note that the bit definitions for the Error register do not apply in this command; rather, the value in the Error register is a diagnostic code, defined in the Table below.

Execute Drive Diagnostics Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	90h							
DRIVE/HEAD	Nu	Nu	nu	D	Nu			
CYLINDER HI	Nu							
CYLINDER LOW	Nu							
SECTOR NUM	Nu							
SECTOR COUNT	Nu							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion/termination of Execute Drive Diagnostics command (90h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Command Block specified by CompactFlash upon completion/termination of Execute Drive Diagnostics command (90h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STATUS	0	1	0	1	V	V	0	V
DRIVE/ HEAD	na	na	na	na	na			
CYLINDER HI	Na							
CYLINDER LOW	Na							
SECTOR NUM	Na							
SECTOR COUNT	Na							
ERROR	Diagnostic Code. See Table below							

Execute Drive Diagnostic Return Codes	
Code	**Description**
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC logic error
05h	Controller microprocessor error
8xh	Slave Error1

4.1.10 Format Track

This command erases 32 sectors starting at the sector specified by the Cylinder, Head, and Sector Number parameters in the task file. If the sector is not valid, an IDNF (ID Not Found) bit is set in the Error register and the command terminates.

In CHS mode, the number of sectors to format per track is set to the number of Current Sectors per Track in the Identify Drive data, by default 20h. Otherwise, it is set to the number of sectors per track by the Initialize Drive Parameters command.

In LBA mode, the number of sectors to format per track is specified by the Host in the Sector Count register. For backward compatibility, the CompactFlash accepts one sector of data from the Host. This data is not used.

Format Track Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							

1 Valid only if CompactFlash is in True IDE Mode.

Format Track Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECTOR COUNT	[LBA mode only] The number of sectors to be formatted on the track.							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion/termination of Format Track command (50h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	Na			
CYLINDER HI	Na							
CYLINDER LOW	Na							
SECTOR NUM	Na							
SECTOR COUNT	Na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

4.1.11 Identify Drive

This command passes to the Host one sector of data describing the CompactFlash's parameters. See Table below for a detailed description of the Identify Drive data.

Identify Drive Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Identify Drive command (ECh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	0
DRIVE/HEAD	na	na	na	Na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							

Command Block specified by CompactFlash upon completion/termination of Identify Drive command (ECh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.12 Identify Drive Information

Table 4-3 Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	045Ah	2	General configuration bit
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Number of unformatted bytes per track
5	0200h	2	Number of unformatted bytes per sector
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (word 7 = MSW, Word 8 = LSW)
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number in ASCII
20	0002h	2	Buffer type
21	000Xh	2	Buffer size in 512 byte increments
22	0004h	2	# of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	800Xh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double Word not supported
49	0F00h	2	Capabilities: DMA, LBA, IORDY supported
50	0000h	2	Capabilities
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	DMA data transfer cycle timing mode not supported
53	0001h	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010Xh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Single Word DMA transfer not implemented
63	0X0Xh	2	Multiword DMA transfer mode
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time
66	0078h	2	Recommended Multiword DMA transfer cycle time

Word Address	Default Value	Total Bytes	Data Field Type Information
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer time with IORDY flow control
69-79	0000h	22	Reserved
80	0020h	2	Major version number
81	0000h	2	Minor version number
82	7408h	2	Command set: NOP, READ BUFFER, WRITE BUFFER, Host protected area, power management feature set
83	5004h	2	Command set: FLUSH CACHE
84	4000h	2	Command set/feature supported extension
85	7408h	2	Command set: NOP, READ BUFFER, WRITE BUFFER, Host protected area, power management feature set
86	1004h	2	Command set: FLUSH CACHE
87	4000h	2	Command set/feature default
88	XXXXh	2	Ultra DMA Mode
89-129	0000h	82	Reserved
130-133	XXXXh	8	Firmware data string
134	848Ah	2	General Configuration word
135	045Ah	2	General Configuration word
136-141	XXXXh	12	Firmware file name
142-147	XXXXh	12	Preformat file name
148-153	XXXXh	12	Anchor program file name
154-254	0000h	202	Reserved
255	XXA5h	2	Integrity Word

4.1.13 Idle

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Idle Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	97h/E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Time-out Parameter. This parameter is ignored by the card.							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion/termination of Idle command (97h/E3h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.14 Idle Immediate

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Idle Immediate Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	95h/E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Idle Immediate command (95h/E1h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.15 Initialize Drive Parameters

This command allows the Host to alter the number of sectors per track and the number of heads per cylinder. This enables Translation Mode, which maps the flash storage using the altered parameters. On Host Reset, the default is 32 Sectors per Track and 8 Heads per Cylinder. The current values used for mapping are returned in the Identify Drive command as Number of Current Sectors per Track, and Number of Current Heads.

Initialize Drive Parameters Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads per Cyl minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	The Number of Sectors per Track							
FEATURES	nu							

Command Block specified by CompactFlash upon completion / termination of Initialize Drive Parameters command (91h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.16 Read Buffer

This command transfers the current contents of the first page of the data buffer (512 bytes) to the Host.

Read Buffer Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	E4h							
DRIVE/HEAD	Nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Read Buffer command (E4h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.17 Read Long Sector

This command is similar to the Read Sectors command except the contents of the Sector Count register are ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer (with no ECC correction) and then transferred to the Host.

Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	22h (retries enabled) -or- 23h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/LBA to trans fer			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. This should be set to 01 for compatibility							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion/termination of Read Long command (22h/23h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] of the sector requested			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector requested							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector requested							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the sector requested							
SECTOR COUNT	00 if the command proceeded without error. 01 if an error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

4.1.18 Read Multiple

The R/W Multiple commands have to be enabled by a previous valid Set Multiple command. Once enabled, the Read Multiple command is identical to Read Sectors operation, except that the number of sectors as specified in the most recent Set Multiple command is transferred as a block to the Host without intervening Host handshaking. This number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one.

If Read Multiple has not been enabled, the ABRT (Aborted Command) bit is set in the Error register and the command terminates.

Read Multiple Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	C4h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion / termination of Read Multiple command (C4h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred. Zero otherwise.							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

4.1.19 Read Sectors

This command transfers data from the CompactFlash to the Host. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register.

Read Sectors Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	20h (retries enabled) -or- 21h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Read Sectors command (20h/21h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

4.1.20 Read Verify Sectors

The Read Verify Sectors command verifies one or more sectors on the card by transferring data from the Flash media to the data buffer in the card and verifying that the ECC is correct. It is performed identically to the Read Sectors command, except that DRQ is not asserted, and no data is transferred to the Host. If an uncorrectable error occurs, the read verify is terminated at the failing sector. The Command Block registers contain the CHS, or LBA of the sector in which the error occurred.

Read Verify Sectors Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	40h (retries enabled) -or- 41h (retries disabled)							
DRIVE/HEAD	Nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to verify							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to verify							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to verify							
SECTOR COUNT	The number of sectors/logical blocks to verify							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Read Verify Sectors command (40h/41h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last sector verified, or sector where an unrecoverable error occurred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector verified, or sector where an unrecoverable error occurred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR NUM	Sector or LBA[7:0] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR COUNT	The number of sectors that were not yet verified if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

4.1.21 Recalibrate

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Recalibrate Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	1xh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Recalibrate command (1xh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF

Command Block specified by CompactFlash upon completion/termination of Recalibrate command (1xh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	0	0	0	0	0	0	0	0

4.1.22 Request Sense

This command returns an extended error code for the previous command, which ended with an error. Table below defines and describes the contents of the Error register on completion of the Request Sense command.

Request Sense Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	03h							
DRIVE/HEAD	Nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Request Sense command 03h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	Na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	See Table below							

Extended Error Codes	
Extended Error Code	**Description**
00h	No error detected
01h	Self test OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (Requested Head or Sector invalid)

Extended Error Codes	
Extended Error Code	**Description**
2Fh	Address overflow (Address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30-34h, 37h, 3Eh	Self test or diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/Aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted media format
03h	Write/Erase failed

4.1.23 Seek

This command is supported for backward compatibility. Although this command has no actual function, it does perform a range check of valid track, and posts an IDNF error if the Head or Cylinder specified are out of bounds.

Seek Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	7xh							
DRIVE/HEAD	Nu	L	nu	D	H[3:0] or LBA[27:24] of the track			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the track							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the track							
SECTOR NUM	(Valid in LBA mode only) LBA[7:0] of the track							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion / termination of Seek command (7xh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	Na	na	na	na	na			

Command Block specified by CompactFlash upon completion/termination of Seek command (7xh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

4.1.24 Set Features

This command allows the Host to control various card features. Each feature is selected by passing its feature code in the Features register. Certain features use additional information passed in the Sector Count register. If the Feature register contains a feature code that is not supported, the drive will respond by setting the Error bit in the Status register and the Abort bit in the Error register.

Set Features Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	EFh							
DRIVE/HEAD	Nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu (additional info if features code is 97h or 9Ah)							
FEATURES	Feature Code. See Table on page [...]							

Command Block specified by CompactFlash upon completion/termination of Set Features command (EFh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	V
DRIVE/HEAD	Na	na	na	na	na			
CYLINDER HI	na (8: maximum current divided by 4 if feature code is 9Ah)							
CYLINDER LOW	na (2: minimum current divided by 4 if feature code is 9Ah)							

Command Block specified by CompactFlash upon completion / termination of Set Features command (EFh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SECTOR	Na							
SECTOR COUNT	Na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

Valid Feature Codes	
Code	Feature
01h	Enable 8-bit data transfers
44h	NOP; accepted for backward compatibility
55h	NOP; accepted for backward compatibility
66h	Disable restoration of default features with Soft Reset
69h	NOP; accepted for backward compatibility
81h	Disable 8-bit data transfer
96h	NOP; accepted for backward compatibility
97h	Control clock using value in Sector Count register
9Ah	Control current using value in Sector Count register
Aah	NOP; accepted for backward compatibility
BBh	NOP; accepted for backward compatibility
CCh	Enable restoration of default features with Soft Reset

NOTES

Feature codes 01h and 81h controls Host transfer data width. By default, 8-bit transfers are disabled.

Feature codes 44h, 55h, 69h, 96h, AAh, and BBh are supported for backward compatibility and have no function.

Feature codes 66h and CCh control whether or not a Soft Reset restores any feature codes to their Power On default value. The features effected are 81h (8-bit transfer), 97h (clock control), and 9A (current control). By default, a Soft Reset will restore the default features.

Feature codes 97h and 9Ah are used to control the card's power and performance. They are mutually exclusive; each feature code will overwrite the power/performance features set by the other command.

Feature codes 97h controls the card's internal clock using the value set in the Sector Count register. See Table below. The default value is 0Fh.

Sector Count Code Specifying CompactFlash's Internal Clock Rate	
Sector Count Register Value	**Function**
00h	Lowest power/slowest performance
0Ah	Intermediate power and performance
0Bh	Intermediate power and performance
0Eh	Highest power/fastest performance
0Fh	Highest power/fastest performance

Feature code 9Ah enables the card to self-configure to best meet the Host system's power requirements. The Host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register is set to 6, the card will self-configure to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the Host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The card will accept values outside this programmable range, but will operate either at the lowest power or highest performance as appropriate.

4.1.25 Set Multiple

This command is used either to set the block count (number of sectors per block), simultaneously enabling R/W Multiple command support, or to disable support of R/W Multiple commands. Although setting, reading, and writing blocks are supported, the only valid block count is one. If the block count specified by the Host is greater than one, the command is aborted. The ERR bit in the Status register is set, and the ABRT bit in the Error register is set. In addition, Read Multiple and Write Multiple commands are disabled.

If the content of the Sector Count register is '1', Read Multiple and Write Multiple commands are enabled until the next Host RESET. Invoking this command with Sector Count = 0 disables R/W Multiple commands. In this case, the CompactFlash card aborts all subsequent R/W Multiple commands issued by the Host.

Set Multiple Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	C6h							
DRIVE/HEAD	Nu	nu	nu	D	nu			
CYLINDER HI	Nu							
CYLINDER LOW	Nu							
SECTOR NUM	Nu							
SECTOR COUNT	01: R/W Multiple command transfer enabled, 00: R/W Multiple command transfer disabled							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion / termination of Set Multiple command (C6h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	V
DRIVE/HEAD	Na	Na	na	na	na			
CYLINDER HI	Na							
CYLINDER LOW	Na							
SECTOR NUM	Na							
SECTOR COUNT	Na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

4.1.26 Sleep

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Sleep Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	99h/E6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Sleep command (99h/E6h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	Na	na	Na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.27 Standby

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Standby Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	96h/E2h							
DRIVE/HEAD	nu	nu	Nu	D	nu			
CYLINDER HI	nu							

Standby Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Time-out Parameter. This is ignored by the CompactFlash							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Standby command (96h/E2h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	Na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.28 Standby Immediate

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Standby Immediate Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	94H/E0h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Standby Immediate command (94H/E0h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	Na	na			
CYLINDER HI	Na							
CYLINDER LOW	Na							
SECTOR NUM	Na							
SECTOR COUNT	Na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.29 Translate Sector

This command transfers one block of data to the Host relating to the sector specified in the Task File. See Table below for a detailed description of this data.

Translate Sector Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	87h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA							
SECTOR COUNT	Nu							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion/termination of Translate Sector command (87h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

Translate Sector Data Description	
Byte Address	Description
00h	00h
01h	Cylinder LSB
02h	Head
03h	Sector
04h-06h	LBA
07h-12h	00h
13h	Erased flag
14h-17h	00h
18h-1Ah	Hot Count (not supported)
1Bh-1FFh	00h

4.1.30 Wear Leveling

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Wear Leveling Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	F5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Wear Leveling command (F5h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	00							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.31 Write Buffer

This command transfers 512 bytes of data from the Host to the first page of the data buffer.

Write Buffer Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	E8h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Write Buffer command (E8h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.1.32 Write Long (with and without retry)

This command is similar to the Write Sectors command except the contents of the Sector Count register are ignored and only one sector is written. The 512 data bytes and 4 ECC bytes are transferred from the Host and then written from the buffer to the flash.

Write Long Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	32h (retries enabled) -or- 33h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. Should be set to 1 for compatibility.							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Write Long command (32h/33h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	1 if an unrecoverable error occurred, 0 if the command proceeded successfully							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	V0

4.1.33 Write Multiple

The R/W Multiple commands have to be enabled by a previous valid Set Multiple command. Once enabled, the Write Multiple command is identical to Write Sectors operation, except that the number of sectors as specified in the most recent Set Multiple command is transferred as a block from the Host without intervening Host handshaking. This number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple and R/W Multiple commands are supported, the only valid block count is one. If Write Multiple has not been enabled, the ABRT (Command Aborted) bit is set in the Error register and the command terminates.

Write Multiple Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	C5h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	Nu							

Command Block specified by CompactFlash upon completion / termination of Write Multiple command (C5h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.1.34 Write Multiple without Erase

This command is supported for backward compatibility. The actual function performed is identical to the Write Multiple command.

Write Multiple without Erase Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	CDh							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by CompactFlash upon completion / termination of Write Multiple without Erase command (CDh)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	Na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.1.35 Write Sectors (with and without retry)

This command transfers data from the Host to the CompactFlash. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register. If the address of the starting sector is not within the range of addresses supported by this card, the IDNF (ID Not Found)) bit is set in the Error register and the command terminates.

Write Sectors Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	30h (retries enabled) -or- 31h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Write Sectors command (30h/31h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.1.36 Write Sectors without Erase

This command is supported for backward compatibility. The actual function performed is identical to the Write Sectors (with retry) command.

Write Sectors w/o Erase Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	C8h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by CompactFlash upon completion/termination of Write Sectors w/o Erase command (C8h)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.1.37 Write Verify

This command is similar to the write sectors (without retry) command except that each sector is verified after being written.

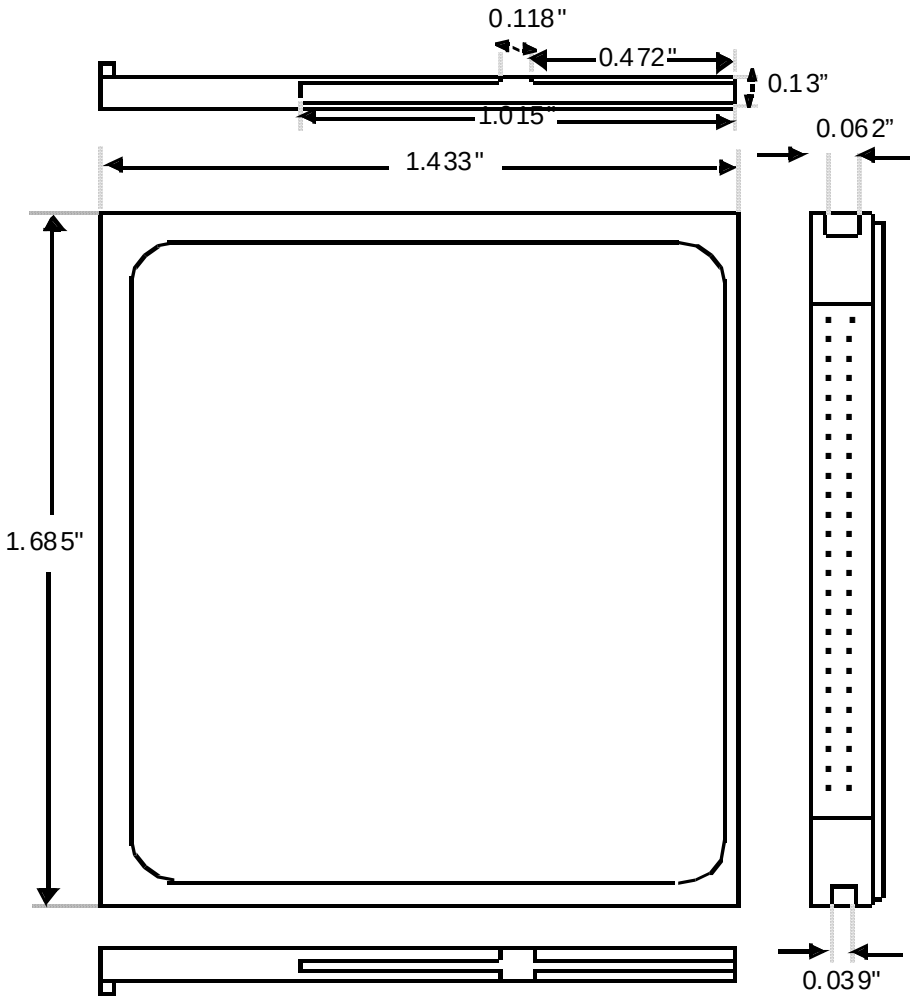
Write Verify Command Issued by Host								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
COMMAND	3Ch							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by CompactFlash upon completion / termination of Write Verify command (3Ch)								
Task File Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

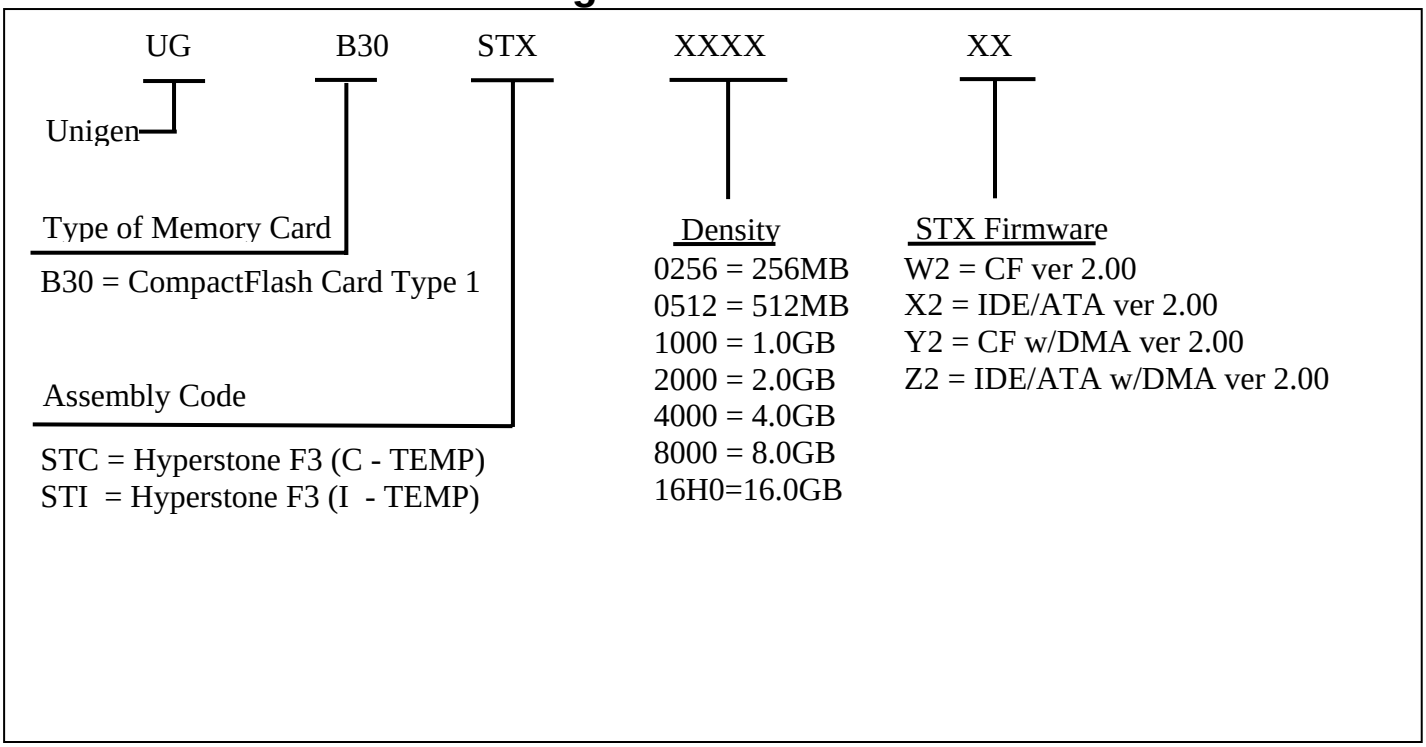
5 PHYSICAL DIMENSIONS

Length	1.433 in. (36.4 mm)
Width	1.685 in. (42.8 mm)
Thickness	0.130 in. (3.3 mm)

5.1 PACKAGE DIMENSIONS



6. Part Number and Ordering Information



7. CONTACT INFORMATION

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