Toradex
Swiss. Embedded. Computing.

Verdin iMX8M Mini

Datasheet

Revision History

Date	Doc. Rev.	Module Version	Changes
20-Feb-2020	Rev. 0.90	V1.0	Initial Release
21-Feb-2020	Rev. 0.91	V1.0	Fixes
21-Feb-2020	Rev. 0.92	V1.0	Marked SE050 Secure Element as experimental feature
17-Mar-2020	Rev. 0.93	V1.0	Layout corrections Update Figure 6 Add section 5.1.1 Minor changes
8-Apr-2020	Rev. 0.94	V1.0	Minor cosmetic improvements
17-Jun-2020	Rev. 0.95	V1.1	Update Document for version 1.1 module Replace PMIC with PCA9450 Replace ADC with TLA2024 Update specification and behavior of CTRL_FORCE_OFF_MOCI# Update specifications of SD_1 signals Update JTAG description Add TPM 2.0 information Update PCIe clock source Update module SKUs Update GPIO naming Update module drawings Change pin names from TSP to MSP Minor changes
05-Oct-2020	Rev. 0.96	V1.1	Update section 1.1 with benefits of wide input voltage range and 1.8V I/O voltage Updating Verdin Signal Name for pin 17 and 21 Update link to errata page (section 7)
23-Oct-2020	Rev. 0.97	V1.1	Correction of CTRL_SLEEP_MOCI# signal type from open drain to CMOS Section 1.4.4: Update document links for Wi-Fi module Minor changes
5-Jan-2021	Rev. 0.98	V1.1	Section 2.1: Update block diagram with correct RTC clock path Section 8.5: Clarify tolerances in drawing
14-Jun-2021	Rev. 1.0	V1.1	Updated the PHY status LED signal names according to the 1.3 version of the Verdin Family Specification throughout the whole document

Contents

1. Introduction

1.1 Hardware

The Verdin iMX8M Mini is a System on Module based on the NXP® i.MX 8M Mini family of embedded System on Chips (SoCs). The i.MX 8M Mini family consists of the i.MX 8M Mini Quad, i.MX 8M Mini QuadLite, i.MX 8M Mini Dual, i.MX 8M Mini DualLite, i.MX 8M Mini Solo, and i.MX 8M Mini SoloLite. The top-tier i.MX 8M Mini Quad features four Cortex-A53 cores as the main processor cluster. The cores provide complete 64-bit Armv8-A support while maintaining seamless backwards compatibility with 32-bit Armv7-A software. The main cores run at up to 1.8 GHz for commercial graded products and 1.6 GHz for industrial temperature range products.

In addition to the main CPU complex, the i.MX 8M Mini features a Cortex-M4F processor which peaks up to 400 MHz. This processor is independent of the main complex and features its own dedicated interfaces while still being able to access the regular interfaces. This heterogeneous multicore system allows for the running of additional real-time operating systems on the M4 cores for time- and security-critical tasks.

The i.MX 8M Mini Quad features the GC Nano Ultra 3D Graphics Processing Unit (GPU) from Vivante®. The GPU provides a single four vector (Vec-4) shader core which peaks up to 6.4 GFLOPS and supports OpenGL® ES 2.0 and OpenVG® 1.1. In addition to the GPU, the SoC features the GC 320 Composition Processing Core (CPC) from Vivante®.

The Verdin iMX8M Mini incorporates DVFS (Dynamic Voltage and Frequency Switching) and thermal throttling, which enables the system to continuously adjust both the operating frequency and the voltage in response to changes in workload and temperature thus achieving the best performance with the lowest power consumption.

The Verdin iMX8M Mini is available with an optional a Dual-Band (2.4/5 GHz) Wi-Fi ac/a/b/g/n and Bluetooth 5/BLE interface. The Wi-Fi module features MHF4 compatible connectors for external antennas. The module is pre-certified for FCC (US), CE (Europa), IC (Canada), TELEC (Japan), and WPC (India).

The Verdin family of SoMs features a wide input voltage range that allows those SoMs to be powered from a broad range of power sources (e.g. directly from a USB power supply or a single lithium cell). Due to increasing transistor density and the need for more power-efficient devices, the I/O voltage level is trending to decrease from 3.3V to 1.8V. For this reason, the Verdin family of SoMs supports 1.8V I/O voltage level only. Both the wide input voltage range and the 1.8V I/O voltage make the power supply designs for a Verdin carrier board simple, easy and cost-efficient. These features altogether make the Verdin family of SoMs perfectly suited for battery-powered applications as well.

The module targets a wide range of applications, including Industrial Automation, Medical, Transportation, Smart Cities, Test and Measurement and many more.

It offers a wide range of interfaces ranging from simple GPIOs, industry standard I2C, SPI, CAN, and UART buses to PCI Express interfaces. The Verdin iMX8M Mini module features a Gigabit Ethernet PHY with IEEE1588 support on the module.

The Verdin iMX8M Mini module eliminates much of the complexity associated with modern-day electronic design. Complicated circuitry such as high-speed impedance-controlled layouts with high component density utilizing blind and buried via technology is encapsulated on the SoM. This allows the customer to create a carrier board that focuses solely on application-specific electronics, making the project substantially less complex. The Verdin iMX8M Mini module takes this one step further and implements an interface pinout which allows direct connection of real-world I/O ports without the need to cross traces or traverse layers, referred to as Direct Breakout™. This becomes increasingly important for customers as more interfaces move toward high-speed serial

technologies that require impedance controlled differential pairs. Direct Breakout™ allows them to easily route such interfaces to common connectors in a simple, robust fashion.

1.2 Main Features

1.2.1 CPU

	Verdin iMX8M Mini DualLite 1GB	Verdin iMX8M Mini DualLite 1GB WB IT	Verdin iMX8M Mini Quad 2GB IT	Verdin iMX8M Mini Quad 2GB WB IT
i.MX 8MM Family SoC	MIMX8MM3DVTLZAx	MIMX8MM3CVTKZAx	MIMX8MM6CVTKZAx	MIMX8MM6CVTKZAx
Arm Cortex-A53 CPU Cores	2	2	4	4
Arm Cortex-M4F CPU Cores	1	1	1	1
L1 Instruction Cache (each core)	32 KB (A53) 16 KB (M4)	32 KB (A53) 16 KB (M4)	32 KB (A53) 16 KB (M4)	32 KB (A53) 16 KB (M4)
L1 Data Cache (each core)	32 KB (A53) 16 KB (M4)	32 KB (A53) 16 KB (M4)	32 KB (A53) 16 KB (M4)	32 KB (A53) 16 KB (M4)
L2 Cache (shared by all A35 cores)	512 KB (A53)	512 KB (A53)	512 KB (A53)	512 KB (A53)
Tightly Coupled Memory	256 KB (M4)	256 KB (M4)	256 KB (M4)	256 KB (M4)
Maximum CPU frequency	1.8 GHz (A53) 400 MHz (M4)	1.6 GHz (A53) 400 MHz (M4)	1.6 GHz (A53) 400 MHz (M4)	1.6 GHz (A53) 400 MHz (M4)
NEON MPE	Yes	Yes	Yes	Yes
Arm TrustZone	Yes	Yes	Yes	Yes
High Assurance Boot	Yes	Yes	Yes	Yes
Cryptographic Acceleration and Assurance Module	Yes	Yes	Yes	Yes
Secure Real-Time Clock	Yes	Yes	Yes	Yes
Secure JTAG Controller	Yes	Yes	Yes	Yes
Secure Non-Volatile Storage*	Yes	Yes	Yes	Yes

* Secure Non-Volatile Storage (SNVS) runs from main VCC, not VCC_BACKUP. Therefore, it can only be used if VCC is permanently applied to the module.

1.2.2 Memory

	Verdin iMX8M Mini DualLite 1GB	Verdin iMX8M Mini DualLite 1GB WB IT	Verdin iMX8M Mini Quad 2GB IT	Verdin iMX8M Mini Quad 2GB WB IT
LPDDR4 RAM Size	1 GB	1 GB	2 GB	2 GB
LPDDR4 RAM Speed	3000 MT/s (1.5 GHz)	3000 MT/s (1.5 GHz)	3000 MT/s (1.5 GHz)	3000 MT/s (1.5 GHz)
LPDDR4 RAM Memory Width	1x32 bit	1x32 bit	1x32 bit	1x32 bit
eMMC NAND Flash (8-bit) V5.0 *	4 GB	8 GB	16 GB	16 GB
I^2C EEPROM	2 Kb	2 Kb	2 Kb	2 Kb

*eMMC is based on MLC NAND flash memory. As with all flash memories, the write endurance is limited. Extensive writing to the memory can wear out the memory cell. The wear leveling in the eMMC controller helps to ensure that cells are getting worn out evenly. More information can be found here http://developer.toradex.com/knowledge-base/flash-memory and here https://en.wikipedia.org/wiki/Flash_memory#Write_endurance.

1.2.3 Interfaces

	Verdin iMX8M Mini DualLite 1GB	Verdin iMX8M Mini DualLite 1GB WB IT	Verdin iMX8M Mini Quad 2GB IT	Verdin iMX8M Mini Quad 2GB WB IT
Wi-Fi IEEE 802.11 ac/a/b/g/n Dual-Band (2.4/5 GHz)	-	1	-	1
Bluetooth 5/BLE	-	1	-	1
MIPI DSI	1x 4 Data Lanes	1x 4 Data Lanes	1x 4 Data Lanes	1x 4 Data Lanes
HDMI	-	-	-	-
USB 2.0 OTG	1	1	1	1
USB 2.0 host	1	1	1	1
USB 3.1 Gen 1 host	-	-	-	-
Gigabit Ethernet	1	1	1	1
RGMII	-	-	-	-
PCIe (Gen 2)	1	1	1	1
MIPI CSI-2	1x 4 Data Lanes	1x 4 Data Lanes	1x 4 Data Lanes	1x 4 Data Lanes
SPI	1+2*	1+2*	1+1*	1+1*
QSPI	1+1*	1	1+1*	1
UART	4	4	4	4
I^2C	3	3	3	3
I^2S	2+3*	2+2*	2+3*	2+2*
PWM	3+1*	3+1*	3+1*	3+1*
SD/SDIO/MMC	1+1*	1	1+1*	1
GPIO	8+90*	8+80*	8+86*	8+76*
CAN	-	-	1	1
ADC	4	4	4	4
JTAG	1	1	1	1
S/PDIF (RX and TX)	1*	1*	1*	1*
Secure Element SE050 (experimental)	-	-	-	-
TPM 2.0 Module	-	-	-	-

*These interfaces are available on pins that are not defined as *"Always Compatible"* or *"Reserved"* interfaces in the Verdin architecture. The pins are either located in the *"Module-specific"* area or are alternate functions of other pins. There are restrictions on using different interfaces simultaneously. Please check the available alternate functions to understand any constraints. See section 1.3 for more information.

1.2.4 Graphics Processing Unit

	Verdin iMX8M Mini DualLite 1GB	Verdin iMX8M Mini DualLite 1GB WB IT	Verdin iMX8M Mini Quad 2GB IT	Verdin iMX8M Mini Quad 2GB WB IT
Vivante GCNanoUltra GPU Units	1	1	1	1
Vec-4 Shaders (per unit)	1	1	1	1
OpenGL® ES 2.0, 1.1	Yes	Yes	Yes	Yes
OpenVG 1.1	Yes	Yes	Yes	Yes
Vivante GC 320 CPC Units	1	1	1	1

1.2.5 HD Video Decode

	Verdin iMX8M Mini DualLite 1GB	Verdin iMX8M Mini DualLite 1GB WB IT	Verdin iMX8M Mini Quad 2GB IT	Verdin iMX8M Mini Quad 2GB WB IT
H.265 HEVC 1080p60	-	-	Yes	Yes
H.264 AVC Baseline, Main and High profile 1080p60	-	-	Yes	Yes
VP8 1080p60	-	-	Yes	Yes

1.2.6 HD Video Encode

	Verdin iMX8M Mini DualLite 1GB	Verdin iMX8M Mini DualLite 1GB WB IT	Verdin iMX8M Mini Quad 2GB IT	Verdin iMX8M Mini Quad 2GB WB IT
H.264 1080p60	-	-	Yes	Yes
VP8 1080p60	-	-	Yes	Yes
VP9 1080p60	-	-	Yes	Yes

1.2.7 Supported Operating Systems

- ✓ Toradex Reference Images (Yocto Project BSP layers)
- ✓ TorizonCore
- ✓ Android
- ✓ For other operating systems, please contact Toradex

1.3 Interface Overview

Features of the Verdin module are split into three distinct categories: *"Always Compatible"*, *"Reserved"* and *"Module-specific"*. The *"Always Compatible"* and *"Reserved"* pins are also referred to as the "Verdin Standard" pins.

Additionally, to this definition the i.MX 8M Mini SoC allows for alternate functions. As an example, many pins can apart from their primary function also work as GPIOs.

"Always Compatible" interfaces are features that shall be present on each SoM in the Verdin Family. Customers can count on upgradeability and maximum scalability regarding these interfaces.

"Reserved" interfaces are features that are defined and reserved, but possibly missing on some SoM models due to lack of availability. It could be that a certain SoC does not provide a specific interface or that there is an assembly option that omits certain interfaces for cost optimization. Replacement pins must be electrically compatible with the specified functionality. This means any

Verdin SoM can be reliably inserted into any Verdin carrier board without causing damage due to incompatible *"Reserved"* pins.

A *"Module-specific"* feature is a feature that is not guaranteed to be functionally or electrically compatible between modules. If a carrier board design uses such features, it is possible that other modules in the Verdin module family do not provide these features and instead provide other features on the associated pins. In this case, Verdin modules which are suitable for use in the carrier board design may be restricted. An incompatible SoM/carrier board combination may disable all functionality or even damage the SoM and/or the carrier board. Use of these pins could make upgrades impossible.

The alternate functions group means that an interface is provided as an additional function on an *"Always Compatible"*, *"Reserved"*, or *"Module-specific"* pin. These functions can only be used if the primary function of the pin is not used.

The table in Figure 1 shows the interfaces that are supported on the Verdin iMX8M Mini module along with the group in which that feature is provided: *"Always Compatible"*, *"Reserved"*, *"Module-specific"* or *alternate function*. The PWM interface is an example of an interface feature that makes use of standard and alternate function pins; one PWM interface is available as *"Always Compatible"*, two as *"Reserved"*, and a fourth one is available as an alternate function of the USB_2_OC#, CSI_1_MCLK, and I2C_4_CSI_SCL signals. Check section 4.4 for a list of all alternate functions of the SODIMM pins. The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin iMX8M Mini Module. The tool allows us to compare the interfaces of different Verdin modules. More information on this tool can be found here: http://developer.toradex.com/knowledge-base/pinout-designer

Feature	Total	*"Always Compatible"*	*"Reserved"*	*"Module-specific"*	Alternate Function
MIPI DSI	1		1		
HDMI	-				
USB 2.0 OTG	1	1			
USB 2.0 host	1	1			
USB 3.1 Gen 1 host (Requires USB 2.0 Host)	-				
Gigabit Ethernet	1	1			
RGMII	-				
PCIe (Gen 2)	1		1		
MIPI CSI-2	1		1		
SPI	3*	1			2*
QSPI	2*		1	1*	
UART	4	3	1		
I^2C	3	1	2		
I^2S	5*		2	2*	1
PWM	4	1	2		1
SD/SDIO/MMC	2*	1		1*	
GPIO	98*	8		26*	64*
CAN	1*		1*		
ADC	4		4		
JTAG	1		1		
S/PDIF (RX and TX)	1				1

Figure 1: Verdin iMX8M Mini Module Interfaces

*These interfaces are not available on all the Verdin iMX8M Mini module versions. Please compare the available interfaces in section 1.2.3 or use the Toradex Pinout Designer.

1.4 Reference Documents

1.4.1 NXP i.MX 8M Mini

You will find additional details about the i.MX 8M Mini SoC in the Datasheet and Reference Manual provided by NXP.
https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i.mx-applications-processors/i.mx-8-processors/i.mx-8m-mini-arm-cortex-a53-cortex-m4-audio-voice-video:i.MX8MMINI

1.4.2 Ethernet Transceiver

Verdin iMX8M Mini utilizes a Microchip KSZ9131RNX Gigabit Ethernet Transceiver (PHY).
https://www.microchip.com/wwwproducts/en/KSZ9131

1.4.3 ADC

Verdin iMX8M Mini utilizes a Texas Instrument TLA2024 four-channel ADC with 12-bit and I²C.
https://www.ti.com/lit/gpn/tla2024

1.4.4 Wi-Fi and Bluetooth Module

Some Verdin iMX8M Plus models utilize an AzureWave AW-CM276NF wireless module. The AW-CM276NF datasheet is available from AzureWave:
https://www.azurewave.com/wireless-modules-nxp.html
Information on pre-certified antennas and cables can be found here:
https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products
Certification documents are available on the Toradex website:
https://developer.toradex.com/knowledge-base/certification-documents-for-azurewave-aw-cm276nf-wi-fi-bluetooth-module

1.4.5 Secure Element

Some Verdin iMX8M Mini models utilize an NXP Plug & Trust Secure Element SE050. Please note that this feature is experimental.
https://www.nxp.com/products/security-and-authentication/authentication/edgelock-se050-plug-trust-secure-element-family-enhanced-iot-security-with-maximum-flexibility:SE050

1.4.6 TPM 2.0 Module

The Verdin iMX8M Mini can be assembled with a Trusted Platform Module (TPM 2.0), the ATTPM20P from Microchip. There is only a summary datasheet available online. The complete datasheet is only available under NDA.
http://ww1.microchip.com/downloads/en/DeviceDoc/ATTPM20P-Trusted-Platform-Module-TPM-2.0-SPI-Interface-Summary-Data-Sheet-DS40002082A.pdf

1.4.7 EEPROM

The Verdin iMX8M Mini has an on-module I²C EEPROM, the M24C02 from ST.
https://www.st.com/en/memories/m24c02-r.html

1.4.8 RTC

The Verdin iMX8M Mini has a low power RX8130CE real-time clock from Epson.
https://www5.epsondevice.com/en/products/rtc/rx8130ce.html

1.4.9 CAN Controller

The Verdin iMX8M Mini has up to two MCP2518FD CAN FD controllers from Microchip.
https://www.microchip.com/wwwproducts/en/MCP2518FD

1.4.10 Verdin Carrier Board Design Guide

This document provides additional information about the Verdin form factor. A custom carrier board should follow the Verdin Carrier Board Design Guide to make the board compatible within the Verdin module family. Please study this document in detail prior to starting your carrier board design. The document will be available soon on the Toradex website.

1.4.11 Verdin Family Specification

This document outlines the specification which defines the Verdin Computer on Module family. It defines the interfaces in terms of functional and electrical characteristics, signal definitions and pin assignments. It also defines the mechanical form factor, including key dimensions and possible thermal solutions. The document will be available soon on the Toradex website.

1.4.12 Layout Design Guide

This document contains information about high-speed layout design and additional factors that help get the carrier board layout right the first time.
http://docs.toradex.com/102492-layout-design-guide.pdf

1.4.13 Toradex Developer Center

The Toradex Developer Center is updated with the latest product support information on a regular basis. You can find an abundance of additional information there.

Please note that the Developer Center is common to all Toradex products. You should always check to ensure if the information provided is valid or relevant for the Verdin iMX8M Mini.
http://www.developer.toradex.com

1.4.14 Verdin Carrier Board Schematics

We provide complete schematics plus an Altium project file which includes library symbols and IPC-7351 compliant footprints for the Verdin Software Development Board, as well as other carrier boards, free of charge. This resource is of great help when designing your own carrier board.
http://developer.toradex.com/hardware-resources/arm-family/carrier-board-design

1.4.15 Toradex Pinout Designer

The Toradex Pinout Designer is a powerful tool for configuring the pin multiplexing of the Verdin, Apalis, and Colibri Modules. The tool allows comparing the interfaces across different modules.
http://developer.toradex.com/knowledge-base/pinout-designer

1.5 Naming Conventions

The naming of i.MX 8M Mini based products can be confusing. In this document, a consistent naming convention is used. It is important to notice the punctuation and spaces in the names. Do not confuse the i.MX 8M Mini with the i.MX 8 or the i.MX 8M. These are 3 different SoC families with different features.

1.5.1 Naming of NXP System on Chip

i.MX 8 Series	A series of different SoC families which consist of the i.MX 8, i.MX 8M, i.MX 8M Mini, i.MX 8M Nano, as well as the i.MX 8X families. This document only contains information on the Verdin module which uses an i.MX 8M Mini family SoC. For information on other i.MX 8 Series based modules, please visit the Toradex website.
i.MX 8M Mini	The NXP i.MX 8M Mini SoC family which consists of the i.MX 8M Mini Quad, i.MX 8M Mini QuadLite, i.MX 8M Mini Dual, i.MX 8M Mini DualLite, i.MX 8M Mini Solo, and i.MX 8M Mini SoloLite. Whenever this document uses the term i.MX 8M Mini, all versions of the i.MX 8M Mini SoC family are meant.
i.MX 8MM	Short name for the i.MX 8M Mini SoC family.
i.MX 8M Mini Quad	The top-tier SoC of the i.MX 8M Mini family. It features a quad core Cortex-A53 main CPU.
i.MX 8MMQ	Short name for the i.MX 8M Mini Quad.
i.MX 8M Mini QuadLite	Quad core SoC of the i.MX 8M Mini family which does not include the VPU.
i.MX 8MMQL	Short name for the i.MX 8M Mini QuadLite.
i.MX 8M Mini Dual	Dual core SoC of the i.MX 8M Mini family.
i.MX 8MMD	Short name for the i.MX 8M Mini Dual.
i.MX 8M Mini DualLite	Dual core SoC of the i.MX 8M Mini family which does not include the VPU.
i.MX 8MMDL	Short name for the i.MX 8M Mini DualLite.
i.MX 8M Mini Solo	Single core SoC of the i.MX 8M Mini family.
i.MX 8MMS	Short name for the i.MX 8M Mini Solo.
i.MX 8M Mini SoloLite	Single core SoC of the i.MX 8M Mini family which does not include the VPU.
i.MX 8MMSL	Short name for the i.MX 8M Mini SoloLite.

1.5.2 Naming of Toradex Verdin Modules

Verdin iMX8M Mini	Verdin module based on the i.MX 8M Mini family SoC. Whenever this document uses the term Verdin iMX8M Mini, all versions of the Verdin iMX8MM are meant.
Verdin iMX8MM	Short name for the Verdin iMX8M Mini. Whenever this document uses the term Verdin iMX8MM, all versions of the Verdin iMX8M Mini are meant.
Verdin iMX8M Mini Quad 2GB WB IT	Verdin module based on the i.MX 8M Mini Quad processor with 2GB memory, Wi-Fi and Bluetooth function, and IT temperature range.
Verdin iMX8MM Q 2GB WB IT	Short name for the Verdin iMX8M Mini Quad 2GB WB IT.
Verdin iMX8M Mini Quad 2GB IT	Verdin module based on the i.MX 8M Mini Quad processor with 2GB memory, no Wi-Fi and Bluetooth function, and IT temperature range.
Verdin iMX8MM Q 2GB IT	Short name for the Verdin iMX8M Mini Quad 2GB IT.

Verdin iMX8M Mini DualLite 1GB WB IT	Verdin module based on the i.MX 8M Mini DualLite processor with 1GB memory, Wi-Fi and Bluetooth function, and IT temperature range.
Verdin iMX8MM DL 1GB WB IT	Short name for the Verdin iMX8M Mini DualLite 1GB WB IT.
Verdin iMX8M Mini DualLite 1GB	Verdin module based on the i.MX 8M Mini DualLite processor with 1GB memory, no Wi-Fi and Bluetooth function, and standard temperature range.
Verdin iMX8MM DL 1GB	Short name for the Verdin iMX8M Mini DualLite 1GB.

1.6 Build-to-Order Options

The Verdin iMX8M Mini module is available in different variants (see section 1.2). In addition to these stock keeping units (SKU), it is possible to order customized versions of the module. These versions are built-to-order (BTO). This means the lead time is longer since they are not kept in stock. Additional setup costs may apply for such versions. Please get in touch with your local Toradex sales team to discuss a BTO version of the Verdin iMX8M Mini module. More information can be found here: https://developer.toradex.com/knowledge-base/customized-computer-on-modules.

The following customization options are technically possible for the Verdin iMX8M Mini:

- SoC versions:
  - i.MX 8M Mini Quad
  - i.MX 8M Mini QuadLite
  - i.MX 8M Mini Dual
  - i.MX 8M Mini DualLite
  - i.MX 8M Mini Solo
  - i.MX 8M Mini SoloLite
- RAM size
- eMMC size
- I²C EEPROM size
- Industrial or commercial temperature range
- With or without Wi-Fi and Bluetooth module
- With or without on-module Ethernet PHY. The RGMII interface signals can then be made available on the *"Reserved"* pins of the module edge connector. This allows having the RGMII interface available on the module edge connector for an Ethernet PHYs with special features on the carrier board.
- With or without PCIe (including clock generator)
- With one, two, or without CAN controller
- With or without Secure Element (SE50)
- With or without Trusted Platform Module (TPM 2.0)
- With or without ADC

2. Architecture Overview

2.1 Block Diagram

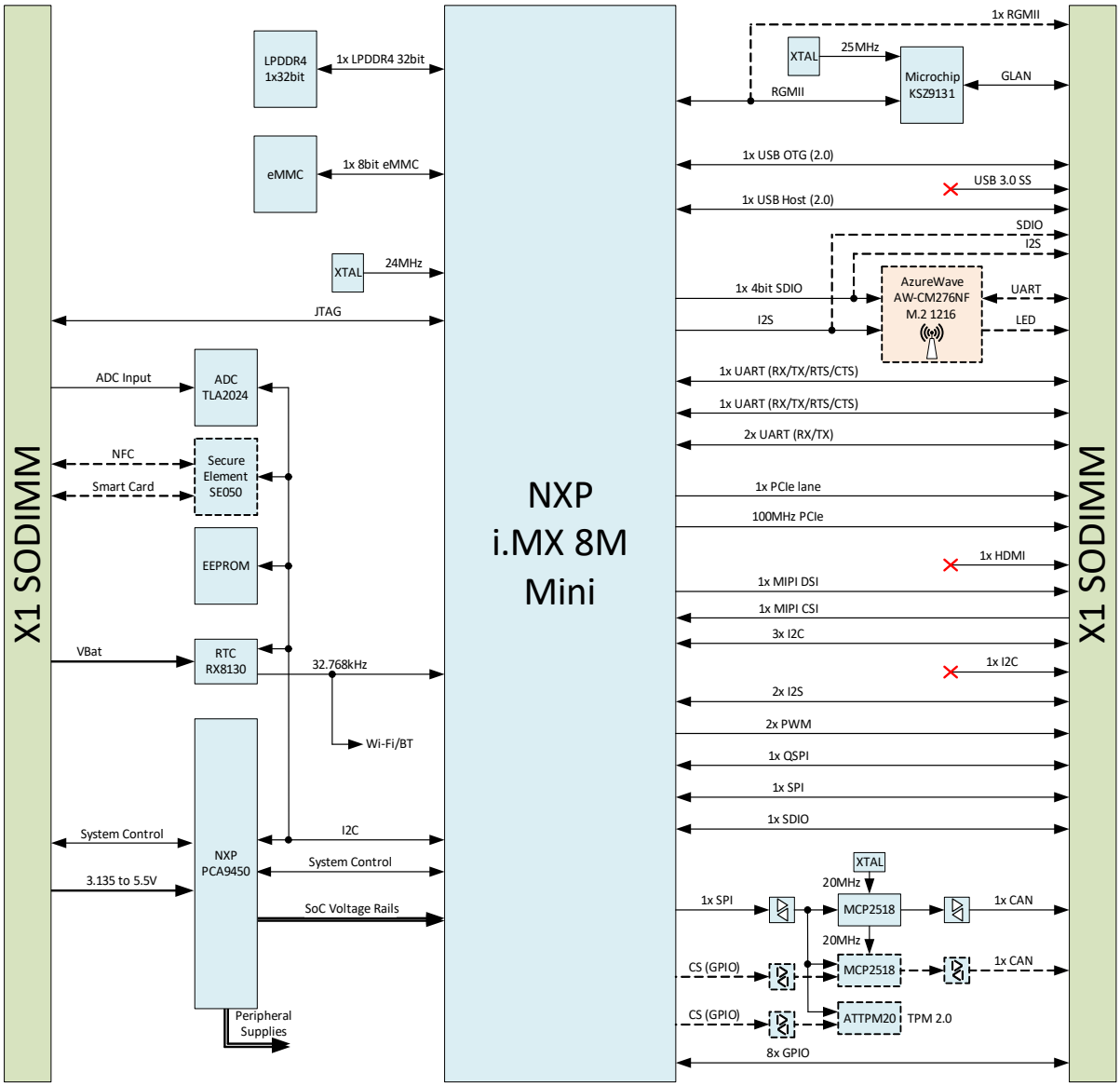

Figure 2 Verdin iMX8M Mini Block Diagram

Dashed lines indicate assembly options. See also section 1.6 for more information on build-to-order options.

3. Verdin iMX8M Mini Connector

3.1 Pin Numbering

The Verdin module follows the same pin numbering scheme as the SODIMM DDR4 standard. Pins on the top side of the module have an odd number while the pins on the bottom side have an even number.

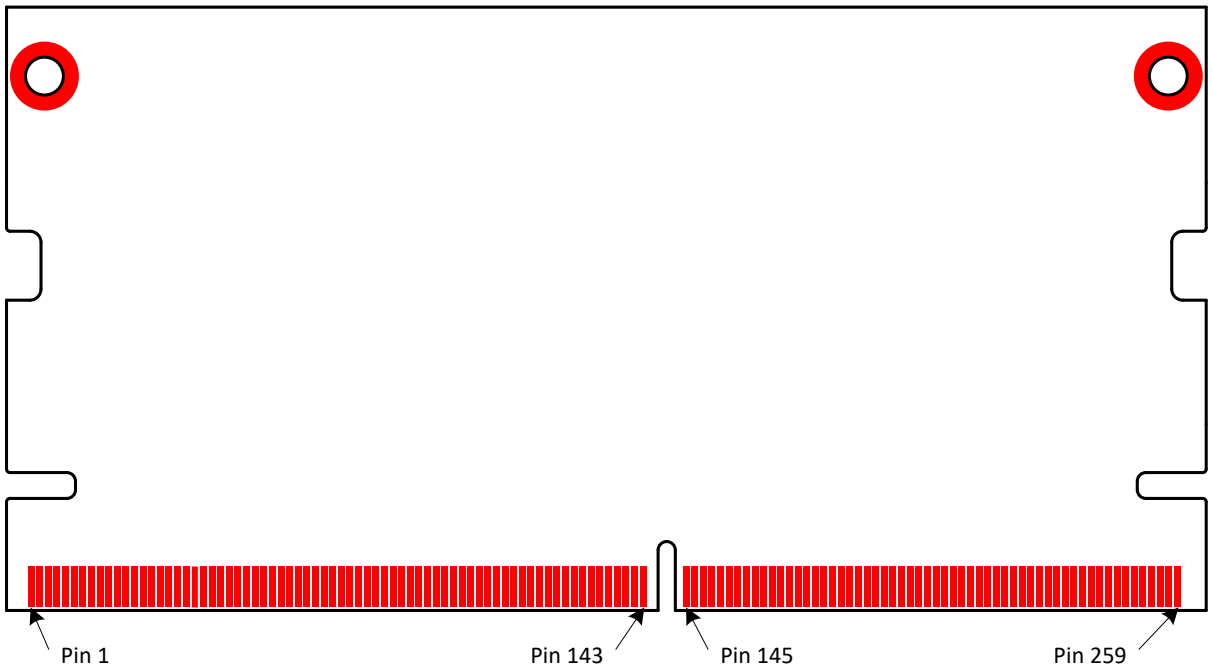

Figure 3: Pin numbering schema on the top side of the module

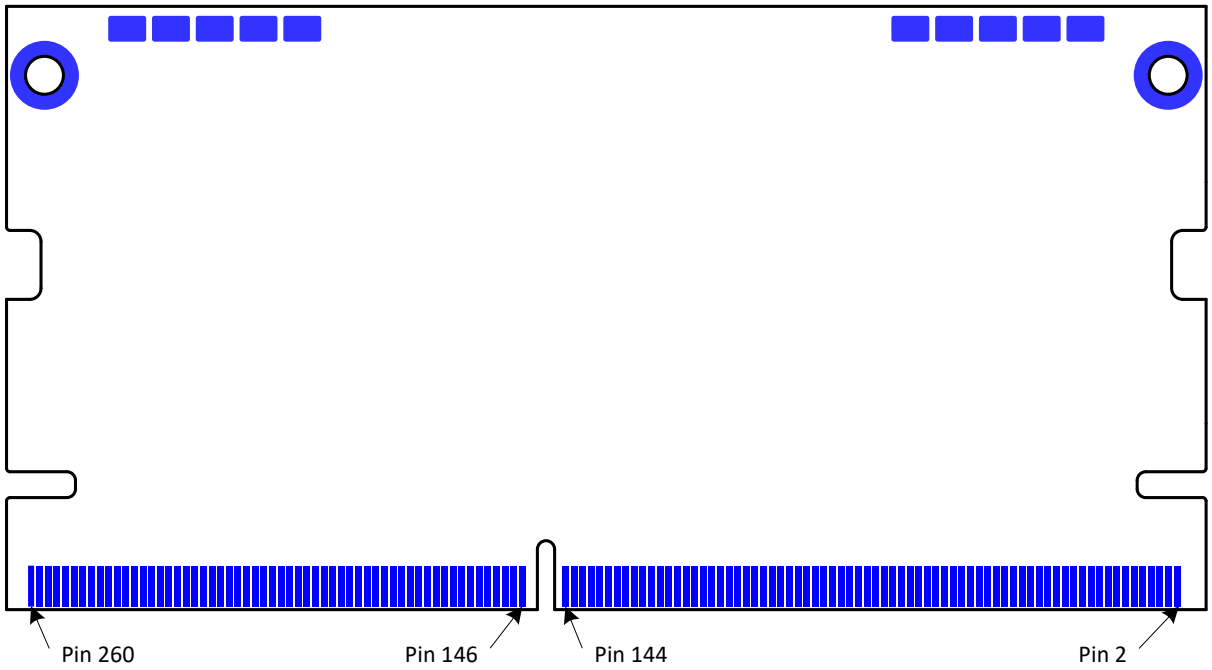

Figure 4: Pin numbering schema on the bottom side of the module (bottom view)

3.1 Assignment

The following table describes the SODIMM connector pinout. Some pins are shaded dark grey as *"Module-specific"* interfaces. These pins might not be compatible with other modules in the Verdin family. Please be aware that you might lose compatibility when using other Verdin modules on your carrier board if you make use of these interfaces. It should be noted that *"Module-specific"* interfaces will be kept common across modules that share such interfaces wherever possible. For example, if both modules A and module B have a LVDS interface which is available in the same configurations as a *"Module-specific"* interface, then they shall be assigned to the same pins in the *"Module-specific"* area of the connector. Hence, both module A and module B shall share compatibility between these parts of the *"Module-specific"* interface.

- X1: Pin number on the SODIMM edge connector (X1).
- Verdin Signal Name: The name of the signal according to the Verdin form factor definition. This name corresponds to the default usage of the pin. Some of the pins also have an alternate function. However, in order to be compatible with other Verdin modules, only the default function should be used, and the carrier board should be implemented according to the Verdin Carrier Board Design Guide.
- i.MX 8MM Ball Name: The name of the pin of the i.MX 8M Mini SoC.

Table 3-1 X1 Connector

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
1	JTAG_1_TDI	JTAG_TDI		
3	JTAG_1_TRST#	JTAG_TRST_B		
5	JTAG_1_TDO	JTAG_TDO		
7	JTAG_1_VREF		1.8V	Reference output (max 10mA)
9	JTAG_1_TCK	JTAG_TCK		
11	GND		GND	
13	JTAG_1_TMS	JTAG_TMS		
15	PWM_1	SPDIF_RX		
17	GPIO_9_DSI	NAND_RE_B		
19	PWM_3_DSI	GPIO1_IO01		
21	GPIO_10_DSI	NAND_CE2_B		
23	DSI_1_D3_N	MIPI_DSI_D3_N		
25	DSI_1_D3_P	MIPI_DSI_D3_P		
27	GND		GND	
29	DSI_1_D2_N	MIPI_DSI_D2_N		
31	DSI_1_D2_P	MIPI_DSI_D2_P		
33	GND		GND	
35	DSI_1_CLK_N	MIPI_DSI_CLK_N		
37	DSI_1_CLK_P	MIPI_DSI_CLK_P		
39	GND		GND	
41	DSI_1_D1_N	MIPI_DSI_D1_N		
43	DSI_1_D1_P	MIPI_DSI_D1_P		
45	GND		GND	
47	DSI_1_D0_N	MIPI_DSI_D0_N		
49	DSI_1_D0_P	MIPI_DSI_D0_P		
51	GND		GND	
53	I2C_2_DSI_SDA	I2C2_SDA		

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
55	I2C_2_DSI_SCL	I2C2_SCL		
57	I2C_3_HDMI_SDA			no connection
59	I2C_3_HDMI_SCL			no connection
61	HDMI_1_HPD			no connection
63	HDMI_1_CEC			no connection
65	GND		GND	
67	HDMI_1_TXC_N			no connection
69	HDMI_1_TXC_P			no connection
71	GND		GND	
73	HDMI_1_TXD0_N			no connection
75	HDMI_1_TXD0_P			no connection
77	GND		GND	
79	HDMI_1_TXD1_N			no connection
81	HDMI_1_TXD1_P			no connection
83	GND		GND	
85	HDMI_1_TXD2_N			no connection
87	HDMI_1_TXD2_P			no connection
89	GND		GND	
91	CSI_1_MCLK	SAI3_MCLK		
93	I2C_4_CSI_SDA	I2C3_SDA		
95	I2C_4_CSI_SCL	I2C3_SCL		
97	GND		GND	
99	CSI_1_D3_P	MIPI_CSI_D3_N		
101	CSI_1_D3_N	MIPI_CSI_D3_P		
103	GND		GND	
105	CSI_1_D2_P	MIPI_CSI_D2_N		
107	CSI_1_D2_N	MIPI_CSI_D2_P		
109	GND		GND	
111	CSI_1_CLK_P	MIPI_CSI_CLK_N		
113	CSI_1_CLK_N	MIPI_CSI_CLK_P		
115	GND		GND	
117	CSI_1_D1_P	MIPI_CSI_D1_N		
119	CSI_1_D1_N	MIPI_CSI_D1_P		
121	GND		GND	
123	CSI_1_D0_P	MIPI_CSI_D0_N		
125	CSI_1_D0_N	MIPI_CSI_D0_P		
127	GND		GND	
129	UART_1_RXD	SAI3_TXFS		
131	UART_1_TXD	SAI3_TXC		
133	UART_1_RTS	SAI3_RXC		
135	UART_1_CTS	SAI3_RXD		
137	UART_2_RXD	ECSPI1_SCLK		
139	UART_2_TXD	ECSPI1_MOSI		
141	UART_2_RTS	ECSPI1_MISO		
143	UART_2_CTS	ECSPI1_SS0		
145	GND		GND	

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
147	UART_3_RXD	SAI2_RXC		
149	UART_3_TXD	SAI2_RXFS		
151	UART_4_RXD	UART4_RXD		
153	UART_4_TXD	UART4_TXD		
155	USB_1_EN	GPIO1_IO12		
157	USB_1_OC#	GPIO1_IO13		
159	USB_1_VBUS	USB1_VBUS		
161	USB_1_ID	USB1_ID		
163	USB_1_D_N	USB1_DN		
165	USB_1_D_P	USB1_DP		
167	GND		GND	
169	USB_2_SSTX_N			no connection
171	USB_2_SSTX_P			no connection
173	GND		GND	
175	USB_2_SSRX_N			no connection
177	USB_2_SSRX_P			no connection
179	GND		GND	
181	USB_2_D_N	USB2_DN		
183	USB_2_D_P	USB2_DP		
185	USB_2_EN			
187	USB_2_OC#			
189	ETH_2_RGMII_INT#			no connection
191	ETH_2_RGMII_MDIO			no connection
193	ETH_2_RGMII_MDC			no connection
195	GND		GND	
197	ETH_2_RGMII_RXC			no connection
199	ETH_2_RGMII_RX_CTL			no connection
201	ETH_2_RGMII_RXD_0			no connection
203	ETH_2_RGMII_RXD_1			no connection
205	ETH_2_RGMII_RXD_2			no connection
207	ETH_2_RGMII_RXD_3			no connection
209	GND		GND	
211	ETH_2_RGMII_TX_CTL			no connection
213	ETH_2_RGMII_TXC			no connection
215	ETH_2_RGMII_TXD_3			no connection
217	ETH_2_RGMII_TXD_2			no connection
219	ETH_2_RGMII_TXD_1			no connection
221	ETH_2_RGMII_TXD_0			no connection
223	GND		GND	
225	ETH_1_MDI0_P		TXRXP_A	KSZ9131 Pin 2
227	ETH_1_MDI0_N		TXRXM_A	KSZ9131 Pin 3
229	GND		GND	
231	ETH_1_MDI1_N		TXRXM_B	KSZ9131 Pin6
233	ETH_1_MDI1_P		TXRXP_B	KSZ9131 Pin5

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
235	ETH_1_LED_1		LED1	KSZ9131Pin17 (buffered)
237	ETH_1_LED_2		LED2	KSZ9131Pin15 (buffered)
239	ETH_1_MDI2_P		TXRXP_C	KSZ9131 Pin 7
241	ETH_1_MDI2_N		TXRXM_C	KSZ9131 Pin 8
243	GND		GND	
245	ETH_1_MDI3_N		TXRXM_D	KSZ9131 Pin 11
247	ETH_1_MDI3_P		TXRXP_D	KSZ9131 Pin 10
249	VCC_BACKUP		VBAT	RX8130 Pin 10
251	VCC		VCC	3.135 to 5.5V input
253	VCC		VCC	3.135 to 5.5V input
255	VCC		VCC	3.135 to 5.5V input
257	VCC		VCC	3.135 to 5.5V input
259	VCC		VCC	3.135 to 5.5V input
2	ADC_1		AIN3	TLA2024 Pin 7
4	ADC_2		AIN2	TLA2024 Pin 6
6	ADC_3		AIN1	TLA2024 Pin 5
8	ADC_4		AIN0	TLA2024 Pin 4
10	GND		GND	
12	I2C_1_SDA	I2C4_SDA		
14	I2C_1_SCL	I2C4_SCL		
16	PWM_2	SPDIF_TX		
18	GND		GND	
20	CAN_1_TX		TXCAN	MCP2518 (modules with CAN) Pin 1 (level shifted to 1.8V)
		UART2_RXD		Only on modules without CAN
22	CAN_1_RX		RXCAN	MCP2518 (modules with CAN) Pin 2 (level shifted to 1.8V)
		UART1_RXD		Only on modules without CAN
24	CAN_2_TX			no connection on modules with CAN
		UART2_TXD		Only on modules without CAN
26	CAN_2_RX			no connection on modules with CAN
		UART1_TXD		Only on modules without CAN
28	GND		GND	
30	I2S_1_BCLK	SAI2_TXC		
32	I2S_1_SYNC	SAI2_TXFS		
34	I2S_1_D_OUT	SAI2_TXD0		
36	I2S_1_D_IN	SAI2_RXD0		
38	I2S_1_MCLK	SAI2_MCLK		
40	GND		GND	
42	I2S_2_BCLK	SAI5_RXD2		

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
44	I2S_2_SYNC	SAI5_RXD1		
46	I2S_2_D_OUT	SAI5_RXD3		
48	I2S_2_D_IN	SAI5_RXD0		
50	GND		GND	
52	QSPI_1_CLK	NAND_ALE		
54	QSPI_1_CS#	NAND_CE0_B		
56	QSPI_1_IO0	NAND_DATA00		
58	QSPI_1_IO1	NAND_DATA01		
60	QSPI_1_IO2	NAND_DATA02		
62	QSPI_1_IO3	NAND_DATA03		
64	QSPI_1_CS2#	NAND_CE1_B		
66	QSPI_1_DQS	NAND_DQS		
68	GND		GND	
70	SD_1_D2	SD2_DATA2 [1)]		Switchable output voltage, 47kΩ pull-up resistor on module
72	SD_1_D3	SD2_DATA3 [1)]		Switchable output voltage, 47kΩ pull-up resistor on module
74	SD_1_CMD	SD2_CMD [1)]		Switchable output voltage, 47kΩ pull-up resistor on module
76	SD_1_PWR_EN	NAND_CLE		
78	SD_1_CLK	SD2_CLK [1)]		Switchable output voltage
80	SD_1_D0	SD2_DATA0 [1)]		Switchable output voltage, 47kΩ pull-up resistor on module
82	SD_1_D1	SD2_DATA1 [1)]		Switchable output voltage, 47kΩ pull-up resistor on module
84	SD_1_CD#	SD2_CD_B [1)]		Switchable output voltage, 10kΩ pull-up resistor on module
86	GND		GND	
88	MSP_1	SAI1_MCLK		Not available on Verdin iMX8MN (modules based on i.MX 8M Nano)
90	MSP_2	SAI1_RXC		
92	MSP_3	SAI1_RXD0		
94	MSP_4	SAI1_RXD1		
96	MSP_5	SAI1_RXD2		
98	GND		GND	
100	MSP_6	SAI1_RXD3		Not available on Verdin iMX8MN (modules based on i.MX 8M Nano)
102	MSP_7	SAI1_RXFS		
104	MSP_8	SAI1_TXC		
106	MSP_9	SAI1_TXD0		
108	MSP_10	SAI1_TXD1		
110	GND		GND	
112	MSP_11	SAI1_TXD2		Not available on Verdin iMX8MN (modules based on i.MX 8M Nano)
114	MSP_12	SAI1_TXD3		
116	MSP_13	SAI1_TXD4		
118	MSP_14	SAI1_TXD6		
120	MSP_15	SAI1_TXFS		
122	GND		GND	
124	MSP_16		ISO 7816 CLK	SE050 card interface Pin 13
126	MSP_17		ISO 7816 IO1	SE050 card interface Pin 3

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
128	MSP_18			
130	MSP_19		ISO 7816 IO2	SE050 card interface Pin 16
132	MSP_20		ISO 7816 RST_N	SE050 card interface Pin 14
134	GND		GND	
136	MSP_21		ISO 14443 LA	SE050 NFC Antenna Pin 17
138	MSP_22		ISO 14443 LB	SE050 NFC Antenna Pin 1
140	MSP_23		IRQ#	RX8130 Pin 6
142	MSP_24		GPIO[22]/ PCIE_W_DISABLEn	AW-CM276NF Pin 63, **Only on module with Wi-Fi**
144	MSP_25		CONFIG_HOST[0]	AW-CM276NF Pin 8, **Only on module with Wi-Fi, Maximum voltage 1.8V**, leave unconnected
146	GND		GND	
148	MSP_26	SAI1_RXD4 [2)]		**Not Available on modules with Wi-Fi**
150	MSP_27	SAI1_TXD5 [2)]		**Not Available on modules with Wi-Fi**
152	MSP_28	SAI1_RXD5 [2)]		**Not Available on modules with Wi-Fi**
154	MSP_29	SAI1_RXD6 [2)]		**Not Available on modules with Wi-Fi**
156	MSP_30	NAND_WE_B [2)]		**Not Available on modules with Wi-Fi**
158	GND		GND	
160	MSP_31	NAND_WP_B [2)]		**Not Available on modules with Wi-Fi**
162	MSP_32	NAND_DATA04 [2)]		**Not Available on modules with Wi-Fi**
164	MSP_33	NAND_DATA05 [2)]		**Not Available on modules with Wi-Fi**
166	MSP_34	NAND_DATA06 [2)]		**Not Available on modules with Wi-Fi**
168	MSP_35	NAND_DATA07 [2)]		**Not Available on modules with Wi-Fi**
170	GND		GND	
172	MSP_36		GPIO[13]/ BT Wake Host	AW-CM276NF Pin 28, **Only on module with Wi-Fi**
174	MSP_37	SAI1_RXD7	GPIO[14]/TCK/ WLAN Wake Host	AW-CM276NF Pin 46, **Only on module with Wi-Fi, Also connected to SoC Pin**
176	MSP_38		GPIO[3]/ BT_LED	AW-CM276NF Pin 65, **Only on module with Wi-Fi**
178	MSP_39		GPIO[16]/ LTE Coex In	AW-CM276NF Pin 12, **Only on module with Wi-Fi**
180	MSP_40		GPIO[17]/ LTE Coex Out	AW-CM276NF Pin 11, **Only on module with Wi-Fi**
182	GND		GND	
184	MSP_41		GPIO[10]/ UART_CTS	AW-CM276NF Pin 54, **Only on module with Wi-Fi**
186	MSP_42		GPIO[11]/ UART_RTS	AW-CM276NF Pin 57, **Only on module with Wi-Fi**

X1 Pin	Verdin Signal Name	i.MX 8MM Ball Name	Non i.MX 8MM Ball	Note
188	MSP_43		GPIO[2]/ WLAN_LED	AW-CM276NF Pin 64, **Only on module with Wi-Fi**
190	MSP_44		GPIO[9]/ UART_SIN	AW-CM276NF Pin 56, **Only on module with Wi-Fi**
192	MSP_45		GPIO[8]/ UART_SOUT	AW-CM276NF Pin 55, **Only on module with Wi-Fi**
194	GND		GND	
196	SPI_1_CLK	ECSPI2_SCLK		
198	SPI_1_MISO	ECSPI2_MISO		
200	SPI_1_MOSI	ECSPI2_MOSI		
202	SPI_1_CS	ECSPI2_SS0		
204	GND		GND	
206	GPIO_1	NAND_CE3_B		
208	GPIO_2	SPDIF_EXT_CLK		
210	GPIO_3	UART3_RXD		
212	GPIO_4	UART3_TXD		
214	PWR_1V8_MOCI		1.8V Output	Max. 250mA
216	GPIO_5_CSI	GPIO1_IO00		
218	GPIO_6_CSI	GPIO1_IO11		
220	GPIO_7_CSI	GPIO1_IO08		
222	GPIO_8_CSI	GPIO1_IO09		
224	GND		GND	
226	PCIE_1_CLK_N	PCIE_CLK_N		
228	PCIE_1_CLK_P	PCIE_CLK_P		
230	GND		GND	
232	PCIE_1_L0_RX_N	PCIE_RXN_N		
234	PCIE_1_L0_RX_P	PCIE_RXN_P		
236	GND		GND	
238	PCIE_1_L0_TX_N	PCIE_TXN_N		
240	PCIE_1_L0_TX_P	PCIE_TXN_P		
242	GND		GND	
244	PCIE_1_RESET#	SAI5_RXFS		
246	CTRL_RECOVERY_MICO#	BOOT_MODE0#		Inverted signal, open-drain
248	CTRL_PWR_BTN_MICO#	ONOFF		Open-drain
250	CTRL_FORCE_OFF_MOCI#		Power Management	Open-drain, 5V tolerant
252	CTRL_WAKE1_MICO#	SAI3_RXFS		
254	CTRL_PWR_EN_MOCI		Power Management	
256	CTRL_SLEEP_MOCI#	SAI3_TXD		10kΩ pull-down resistor on module
258	CTRL_RESET_MOCI#		Power Management	Open-drain, 3.3V tolerant
260	CTRL_RESET_MICO#		Power Management	

[1] It is possible to change the IO voltage of the main SD interface from 3.3V (default) to 1.8V. This may be used by the SD card driver to switch to 1.8V for higher speed modes (SD UHS-I). Please note that the voltage can only be changed for all pins simultaneously, and not individually. Therefore, use these pins with care.

[2] This SoC pin is not available on modules with Wi-Fi and Bluetooth.

4. I/O Pins

4.1 Function Multiplexing

Low-speed I/O pins of the NXP i.MX 8M Mini SoC can be configured for any of the (and up to) eight alternate functions. Most of the pins can also be used as GPIOs (General Purpose I/O, sometimes also referred to as Digital I/O). As an example: The i.MX 8M Mini signal pin on the SODIMM finger pin 131 has the primary function uart2.TX (Verdin standard function UART_1_RXD). Besides this UART function, the pin can also be configured as sai3_TX_BCLK (digital audio bit clock), gpt1_COMPARE2 (timer compare input), sai5.RX_DATA[2] (digital audio input data), and gpio5.IO[0] (GPIO).

The default setting for this pin is the primary function uart2.TX. It is strongly recommended, whenever possible, to use a pin for a function that is compatible with all Verdin modules. This guarantees the best compatibility with the standard software and with other modules in the Verdin family.

Some of the alternate functions are available on more than one pin. Care should be taken to ensure that two pins are not configured with the same function. This could lead to system instability and undefined behavior.

In the table listed in chapter 4.4, you will find a list of all pins which have alternate functions. There you can find which alternate functions are available for each individual pin.

4.2 Pin Control

The alternate function of each pin can be changed independently. Every pin has a Pad Mux Register in which the following settings can be configured (some settings might not be available for certain pins). The register is called IOMUXC_SW_MUX_CTL_PAD_x where x is the name of the i.MX 8M Mini pin. More information about the available register settings can be found in the i.MX 8M Mini Reference Manual.

Table 4-1 Pad Mux Register

Bit	Field	Description	Remarks
31-5	Reserved		
4	SION	0 Software Input On Field disabled 1 Software Input On Field enabled	Force the selected mux mode input path
3	Reserved		
2-0	MUX_MODE	000 Select mux mode: ALT0 mux port 001 Select mux mode: ALT1 mux port 010 Select mux mode: ALT2 mux port 011 Select mux mode: ALT3 mux port 100 Select mux mode: ALT4 mux port 101 Select mux mode: ALT5 mux port (GPIO) 110 Select mux mode: ALT6 mux port 111 Select mux mode: ALT7 mux port	Check section 4.4 for the available alternate function of the pin

The pins have an additional register which allows configuration of pull up/down resistors, drive strength, and other settings. The register is called IOMUXC_SW_PAD_CTL_PAD_x where x is the name of the i.MX 8M Mini pin. Some settings might not be available on certain pins. More information about the available register settings can be found in the i.MX 8M Mini Reference Manual.

Table 4-2 Pad Control Register

Bit	Field	Description	Remarks
31-9	Reserved		
8	PE	0 Pull resistor disabled 1 Pull resistor enable	
7	HYS	0 CMOS input 1 Schmitt trigger input	
6	PUE	0 Select pull-down resistor 1 Select pull-up resistor	Typical pull-up value 22kΩ Typical pull-down value 23kΩ
5	ODE	0 Output is CMOS 1 Output is open-drain	
4-3	FSE	0x Slow Slew Rate 1x Fast Slew Rate	Use slow slew rate, if possible for reducing EMC problems
2-0	DSE	00x Drive strength X1 01x Drive strength X2 10x Drive strength X4 11x Drive strength X6	If possible, decrease the drive strength in order to reduce EMC problems

Input functions that are available at more than one physical pin require an additional input multiplexer. This multiplexer is configured by a register called IOMUXC_x_SELECT_INPUT where x is the name of the input function. More information about this register can be found in the i.MX 8M Mini Reference Manual.

4.3 Pin Reset Status

After a reset, the i.MX 8M Mini pins can be in different modes. Most of them are pulled low. A few are, high impedance, or pulled up. Please check the table in chapter 4.4 for a list of reset states for each of the pins. As soon as the bootloader is running, it is possible to reconfigure the pins and their states.

Please be aware, the pin reset status is only guaranteed during the release of the reset signal. During the power-up sequence, the states of the pins might be undefined until the related IO bank voltage is enabled on the module.

Reset Status Description

PD: Pull-down (input)
PU: Pull-up (input)
Z: High impedance (input)
Z/PU: High impedance during reset, afterwards pull-up (input)

4.4 SoC Functions List

Below is a list of all the i.MX 8M Mini pins that are available on the SODIMM connector. It shows the alternate functions that are available for each pin. The GPIO functionality is normally defined as the ALT5 function. The alternate functions used to provide the primary interfaces, done to ensure the best compatibility with other Verdin modules, are highlighted.

Function Short Forms

ADC:	Analog Digital Convert input
CAAM:	Cryptographic Acceleration and Assurance Module
CAN:	Controller Area Network
CCM:	Clock Control Module
CSI:	Camera Serial Interface
CSU:	Central Security Unit
ECSPI:	Enhanced Configurable SPI
ENET:	Ethernet MAC interface
GPIO:	General Purpose Input Output
GPC:	General Power Controller
GPT:	General Purpose Timer
I2C:	Inter-Integrated Circuit
MIPI_CSI:	MIPI CSI Subsystem
MIPI_DSI:	MIPI DSI Subsystem
PCIE:	PCI Express
PDM:	Pulse-Density Modulation Microphone Input
PWM:	Pulse Width Modulation output
QSPI:	Quad Serial Peripheral Interface
RAWNAND:	Interface for NAND Flash
SAI:	Serial Interface for Audio (I2S and AC97)
SDMA:	Smart Direct Memory Access Controller
SJC:	System JTAG Controller
SNVS:	Secure Non-Volatile Storage
SPDIF:	Sony/Philips Digital Interface
SPI:	Serial Peripheral Interface Bus
SRC:	System Reset Controller
UART:	Universal Asynchronous Receiver/Transmitter
USB:	Universal Serial Bus
USDHC:	Ultra-Secured Digital Host Controller (interface for SD and MMC cards)

X1 Pin	i.MX 8M Mini Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Default Mode	Reset State	Power Block
1	JTAG_TDI	E27	cjtag_wrapper.TDI								ALT0	PU	NVCC_JTAG
3	JTAG_TRST_B	C27	cjtag_wrapper.TRST_B								ALT0	PU	NVCC_JTAG
5	JTAG_TDO	E26	cjtag_wrapper.TDO								ALT0	PU	NVCC_JTAG
9	JTAG_TCK	F26	cjtag_wrapper.TCK								ALT0	PU	NVCC_JTAG
13	JTAG_TMS	F27	cjtag_wrapper.TMS								ALT0	PU	NVCC_JTAG
15	SPDIF_RX	AG9	spdif1.IN	pwm2.OUT				gpio5.IO[4]		tpsmp.HDATA[6]	ALT5	PD	NVCC_SAI3
17	NAND_RE_B	N27	rawnand.RE_B	qspi.B_DQS	usdhc3.DATA4			gpio3.IO[15]		sim_m.HADDR[11]	ALT5	PU	NVCC_NAND
19	GPIO1_IO01	AF14	gpio1.IO[1]	pwm1.OUT				anamix.REF_CLK_24M	ccmsrcgpcmix.EXT_CLK2	sjc.ACTIVE	ALT0	Z/PU	NVCC_GPIO1
21	NAND_CE2_B	M27	rawnand.CE2_B	qspi.B_SS0_B	usdhc3.DATA5			gpio3.IO[3]		sim_m.HPROT[3]	ALT5	PD	NVCC_NAND
53	I2C2_SDA	D9	i2c2.SDA	enet1.1588_EVENT1_OUT	usdhc3.WP			gpio5.IO[17]		tpsmp.HDATA[19]	ALT5	PD	NVCC_I2C
55	I2C2_SCL	D10	i2c2.SCL	enet1.1588_EVENT1_IN	usdhc3.CD_B			gpio5.IO[16]		tpsmp.HDATA[18]	ALT5	PD	NVCC_I2C
91	SAI3_MCLK	AD6	sai3.MCLK	pwm4.OUT	sai5.MCLK			gpio5.IO[2]		tpsmp.HDATA[4]	ALT5	PD	NVCC_SAI3
93	I2C3_SDA	F10	i2c3.SDA	pwm3.OUT	gpt3.CLK			gpio5.IO[19]		tpsmp.HDATA[21]	ALT5	PD	NVCC_I2C
95	I2C3_SCL	E10	i2c3.SCL	pwm4.OUT	gpt2.CLK			gpio5.IO[18]		tpsmp.HDATA[20]	ALT5	PD	NVCC_I2C
129	SAI3_TXFS	AC6	sai3.TX_SYNC	gpt1.CAPTURE2	sai5.RX_DATA[1]	sai3.TX_DATA[1]	uart2.RX	gpio4.IO[31]		tpsmp.HDATA[1]	ALT5	PD	NVCC_SAI3
131	SAI3_TXC	AG6	sai3.TX_BCLK	gpt1.COMPARE2	sai5.RX_DATA[2]		uart2.TX	gpio5.IO[0]		tpsmp.HDATA[2]	ALT5	PD	NVCC_SAI3
133	SAI3_RXC	AG7	sai3.RX_BCLK	gpt1.CLK	sai5.RX_BCLK		uart2.CTS_B	gpio4.IO[29]		tpsmp.HTRANS[1]	ALT5	PD	NVCC_SAI3
135	SAI3_RXD	AF7	sai3.RX_DATA[0]	gpt1.COMPARE1	sai5.RX_DATA[0]		uart2.RTS_B	gpio4.IO[30]		tpsmp.HDATA[0]	ALT5	PD	NVCC_SAI3
137	ECSPI1_SCLK	D6	ecspi1.SCLK	uart3.RX				gpio5.IO[6]		tpsmp.HDATA[8]	ALT5	PD	NVCC_ECSPI
139	ECSPI1_MOSI	B7	ecspi1.MOSI	uart3.TX				gpio5.IO[7]		tpsmp.HDATA[9]	ALT5	PD	NVCC_ECSPI
141	ECSPI1_MISO	A7	ecspi1.MISO	uart3.CTS_B				gpio5.IO[8]		tpsmp.HDATA[10]	ALT5	PD	NVCC_ECSPI
143	ECSPI1_SS0	B6	ecspi1.SS0	uart3.RTS_B				gpio5.IO[9]		tpsmp.HDATA[11]	ALT5	PD	NVCC_ECSPI
147	SAI2_RXC	AB22	sai2.RX_BCLK	sai5.TX_BCLK			uart1.RX	gpio4.IO[22]		sim_m.HSIZE[1]	ALT5	PD	NVCC_SAI2
149	SAI2_RXFS	AC19	sai2.RX_SYNC	sai5.TX_SYNC	sai5.TX_DATA[1]	sai2.RX_DATA[1]	uart1.TX	gpio4.IO[21]		sim_m.HSIZE[0]	ALT5	PD	NVCC_SAI2
151	UART4_RXD	F19	uart4.RX	uart2.CTS_B	pcie1.CLKREQ_B			gpio5.IO[28]		tpsmp.HDATA[30]	ALT5	PD	NVCC_UART
153	UART4_TXD	F18	uart4.TX	uart2.RTS_B				gpio5.IO[29]		tpsmp.HDATA[31]	ALT5	PD	NVCC_UART
155	GPIO1_IO12	AB10	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]	ccmsrcgpcmix.OUT1	csu.CSU_ALARM_AUT[0]	ALT0	PD	NVCC_GPIO1
157	GPIO1_IO13	AD9	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT	ccmsrcgpcmix.OUT2	csu.CSU_ALARM_AUT[1]	ALT0	PD	NVCC_GPIO1
185	GPIO1_IO14	AC9	gpio1.IO[14]	usb2.OTG_PWR			usdhc3.CD_B	pwm3.OUT	ccmsrcgpcmix.CLKO1	csu.CSU_ALARM_AUT[2]	ALT0	PD	NVCC_GPIO1
187	GPIO1_IO15	AB9	gpio1.IO[15]	usb2.OTG_OC			usdhc3.WP	pwm4.OUT	ccmsrcgpcmix.CLKO2	csu.CSU_INT_DEB	ALT0	PD	NVCC_GPIO1
12	I2C4_SDA	E13	i2c4.SDA	pwm1.OUT				gpio5.IO[21]		tpsmp.HDATA[23]	ALT5	PD	NVCC_I2C
14	I2C4_SCL	D13	i2c4.SCL	pwm2.OUT	pcie1.CLKREQ_B			gpio5.IO[20]		tpsmp.HDATA[22]	ALT5	PD	NVCC_I2C
16	SPDIF_TX	AF9	spdif1.OUT	pwm3.OUT				gpio5.IO[3]		tpsmp.HDATA[5]	ALT5	PD	NVCC_SAI3
20	UART2_RXD [4]	F15	uart2.RX	ecspi3.MISO				gpio5.IO[24]		tpsmp.HDATA[26]	ALT5	PD	NVCC_UART
22	UART1_RXD [4]	E14	uart1.RX	ecspi3.SCLK				gpio5.IO[22]		tpsmp.HDATA[24]	ALT5	PD	NVCC_UART
24	UART2_TXD [4]	E15	uart2.TX	ecspi3.SS0				gpio5.IO[25]		tpsmp.HDATA[27]	ALT5	PD	NVCC_UART
26	UART1_TXD [4]	F13	uart1.TX	ecspi3.MOSI				gpio5.IO[23]		tpsmp.HDATA[25]	ALT5	PD	NVCC_UART
30	SAI2_TXC	AD22	sai2.TX_BCLK	sai5.TX_DATA[2]				gpio4.IO[25]		sim_m.HREADYOUT	ALT5	PD	NVCC_SAI2
32	SAI2_TXFS	AD23	sai2.TX_SYNC	sai5.TX_DATA[1]		sai2.TX_DATA[1]	uart1.CTS_B	gpio4.IO[24]		sim_m.HWRITE	ALT5	PD	NVCC_SAI2
34	SAI2_TXD0	AC22	sai2.TX_DATA[0]	sai5.TX_DATA[3]				gpio4.IO[26]		tpsmp.CLK	ALT5	PD	NVCC_SAI2
36	SAI2_RXD0	AC24	sai2.RX_DATA[0]	sai5.TX_DATA[0]			uart1.RTS_B	gpio4.IO[23]		sim_m.HSIZE[2]	ALT5	PD	NVCC_SAI2
38	SAI2_MCLK	AD19	sai2.MCLK	sai5.MCLK				gpio4.IO[27]		tpsmp.HDATA_DIR	ALT5	PD	NVCC_SAI2
42	SAI5_RXD2	AD13	sai5.RX_DATA[2]	sai1.TX_DATA[4]	sai1.TX_SYNC	sai5.TX_BCLK	pdm.BIT_STREAM[2]	gpio3.IO[23]			ALT5	PD	NVCC_SAI5

X1 Pin	i.MX 8M Mini Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Default Mode	Reset State	Power Block
44	SAI5_RXD1	AC14	sai5.RX_DATA[1]	sai1.TX_DATA[3]	sai1.TX_SYNC	sai5.TX_SYNC	pdm.BIT_STREAM[1]	gpio3.IO[22]			ALT5	PD	NVCC_SAI5
46	SAI5_RXD3	AC13	sai5.RX_DATA[3]	sai1.TX_DATA[5]	sai1.TX_SYNC	sai5.TX_DATA[0]	pdm.BIT_STREAM[3]	gpio3.IO[24]			ALT5	PD	NVCC_SAI5
48	SAI5_RXD0	AD18	sai5.RX_DATA[0]	sai1.TX_DATA[2]			pdm.BIT_STREAM[0]	gpio3.IO[21]			ALT5	PD	NVCC_SAI5
52	NAND_ALE	N22	rawnand.ALE	qspi.A_SCLK				gpio3.IO[0]		sim_m.HPROT[0]	ALT5	PD	NVCC_NAND
54	NAND_CE0_B	N24	rawnand.CE0_B	qspi.A_SS0_B				gpio3.IO[1]		sim_m.HPROT[1]	ALT5	PU	NVCC_NAND
56	NAND_DATA00	P23	rawnand.DATA00	qspi.A_DATA[0]				gpio3.IO[6]		sim_m.HADDR[2]	ALT5	PD	NVCC_NAND
58	NAND_DATA01	K24	rawnand.DATA01	qspi.A_DATA[1]				gpio3.IO[7]		sim_m.HADDR[3]	ALT5	PD	NVCC_NAND
60	NAND_DATA02	K23	rawnand.DATA02	qspi.A_DATA[2]	usdhc3.CD_B			gpio3.IO[8]		sim_m.HADDR[4]	ALT5	PD	NVCC_NAND
62	NAND_DATA03	N23	rawnand.DATA03	qspi.A_DATA[3]	usdhc3.WP			gpio3.IO[9]		sim_m.HADDR[5]	ALT5	PD	NVCC_NAND
64	NAND_CE1_B	P27	rawnand.CE1_B	qspi.A_SS1_B	usdhc3.STROBE			gpio3.IO[2]		sim_m.HPROT[2]	ALT5	PD	NVCC_NAND
66	NAND_DQS	R22	rawnand.DQS	qspi.A_DQS				gpio3.IO[14]		sim_m.HADDR[10]	ALT5	PD	NVCC_NAND
70	SD2_DATA2	V24	usdhc2.DATA2					gpio2.IO[17]	ccmsrcgpcmix.STOP	observe_mux.OUT[4]	ALT5	PD	NVCC_SD2
72	SD2_DATA3	V23	usdhc2.DATA3					gpio2.IO[18]	ccmsrcgpcmix.EARLY_RESET		ALT5	PD	NVCC_SD2
74	SD2_CMD	W24	usdhc2.CMD					gpio2.IO[14]	ccmsrcgpcmix.OBSERVE1	observe_mux.OUT[1]	ALT5	PD	NVCC_SD2
76	NAND_CLE	K27	rawnand.CLE	qspi.B_SCLK	usdhc3.DATA7			gpio3.IO[5]		sim_m.HADDR[1]	ALT5	PD	NVCC_NAND
78	SD2_CLK	W23	usdhc2.CLK					gpio2.IO[13]	ccmsrcgpcmix.OBSERVE0	observe_mux.OUT[0]	ALT5	PD	NVCC_SD2
80	SD2_DATA0	AB23	usdhc2.DATA0					gpio2.IO[15]	ccmsrcgpcmix.OBSERVE2	observe_mux.OUT[2]	ALT5	PD	NVCC_SD2
82	SD2_DATA1	AB24	usdhc2.DATA1					gpio2.IO[16]	ccmsrcgpcmix.WAIT	observe_mux.OUT[3]	ALT5	PD	NVCC_SD2
84	SD2_CD_B	AA26	usdhc2.CD_B					gpio2.IO[12]			ALT5	PD	NVCC_SD2
88	SAI1_MCLK	AB18	sai1.MCLK	sai5.MCLK	sai1.TX_BCLK	pdm.CLK		gpio4.IO[20]		sim_m.HRESP	ALT5	PD	NVCC_SAI1
90	SAI1_RXC	AF16	sai1.RX_BCLK	sai5.RX_BCLK			coresight.TRACE_CTL	gpio4.IO[1]		sim_m.HADDR[16]	ALT5	PD	NVCC_SAI1
92	SAI1_RXD0	AG15	sai1.RX_DATA[0]	sai5.RX_DATA[0]	sai1.TX_DATA[1]	pdm.BIT_STREAM[0]	coresight.TRACE[0]	gpio4.IO[2]	ccmsrcgpcmix.BOOT_CFG[0]	sim_m.HADDR[17]	ALT5	PD	NVCC_SAI1
94	SAI1_RXD1	AF15	sai1.RX_DATA[1]	sai5.RX_DATA[1]		pdm.BIT_STREAM[1]	coresight.TRACE[1]	gpio4.IO[3]	ccmsrcgpcmix.BOOT_CFG[1]	sim_m.HADDR[18]	ALT5	PD	NVCC_SAI1
96	SAI1_RXD2	AG17	sai1.RX_DATA[2]	sai5.RX_DATA[2]		pdm.BIT_STREAM[2]	coresight.TRACE[2]	gpio4.IO[4]	ccmsrcgpcmix.BOOT_CFG[2]	sim_m.HADDR[19]	ALT5	PD	NVCC_SAI1
100	SAI1_RXD3	AF17	sai1.RX_DATA[3]	sai5.RX_DATA[3]		pdm.BIT_STREAM[3]	coresight.TRACE[3]	gpio4.IO[5]	ccmsrcgpcmix.BOOT_CFG[3]	sim_m.HADDR[20]	ALT5	PD	NVCC_SAI1
102	SAI1_RXFS	AG16	sai1.RX_SYNC	sai5.RX_SYNC			coresight.TRACE_CLK	gpio4.IO[0]		sim_m.HADDR[15]	ALT5	PD	NVCC_SAI1
104	SAI1_TXC	AC18	sai1.TX_BCLK	sai5.TX_BCLK			coresight.EVENTI	gpio4.IO[11]		sim_m.HADDR[26]	ALT5	PD	NVCC_SAI1
106	SAI1_TXD0	AG20	sai1.TX_DATA[0]	sai5.TX_DATA[0]			coresight.TRACE[8]	gpio4.IO[12]	ccmsrcgpcmix.BOOT_CFG[8]	sim_m.HADDR[27]	ALT5	PD	NVCC_SAI1
108	SAI1_TXD1	AF20	sai1.TX_DATA[1]	sai5.TX_DATA[1]			coresight.TRACE[9]	gpio4.IO[13]	ccmsrcgpcmix.BOOT_CFG[9]	sim_m.HADDR[28]	ALT5	PD	NVCC_SAI1
112	SAI1_TXD2	AG21	sai1.TX_DATA[2]	sai5.TX_DATA[2]			coresight.TRACE[10]	gpio4.IO[14]	ccmsrcgpcmix.BOOT_CFG[10]	sim_m.HADDR[29]	ALT5	PD	NVCC_SAI1
114	SAI1_TXD3	AF21	sai1.TX_DATA[3]	sai5.TX_DATA[3]			coresight.TRACE[11]	gpio4.IO[15]	ccmsrcgpcmix.BOOT_CFG[11]	sim_m.HADDR[30]	ALT5	PD	NVCC_SAI1
116	SAI1_TXD4	AG22	sai1.TX_DATA[4]	sai6.RX_BCLK	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]	ccmsrcgpcmix.BOOT_CFG[12]	sim_m.HADDR[31]	ALT5	PD	NVCC_SAI1
118	SAI1_TXD6	AG23	sai1.TX_DATA[6]	sai6.RX_SYNC	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]	ccmsrcgpcmix.BOOT_CFG[14]	sim_m.HBURST[1]	ALT5	PD	NVCC_SAI1
120	SAI1_TXFS	AB19	sai1.TX_SYNC	sai5.TX_SYNC			coresight.EVENTO	gpio4.IO[10]		sim_m.HADDR[25]	ALT5	PD	NVCC_SAI1
148	SAI1_RXD4 [1)]	AG18	sai1.RX_DATA[4]	sai6.TX_BCLK	sai6.RX_BCLK		coresight.TRACE[4]	gpio4.IO[6]	ccmsrcgpcmix.BOOT_CFG[4]	sim_m.HADDR[21]	ALT5	PD	NVCC_SAI1

X1 Pin	i.MX 8M Mini Ball Name	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Default Mode	Reset State	Power Block
150	SAI1_TXD5 [1]	AF22	sai1.TX_DATA[5]	sai6.RX_DATA[0]	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]	ccmsrcgpcmix.BOOT_CFG[13]	sim_m.HBURST[0]	ALT5	PD	NVCC_SAI1
152	SAI1_RXD5 [1]	AF18	sai1.RX_DATA[5]	sai6.TX_DATA[0]	sai6.RX_DATA[0]	sai1.RX_SYNC	coresight.TRACE[5]	gpio4.IO[7]	ccmsrcgpcmix.BOOT_CFG[5]	sim_m.HADDR[22]	ALT5	PD	NVCC_SAI1
154	SAI1_RXD6 [1]	AG19	sai1.RX_DATA[6]	sai6.TX_SYNC	sai6.RX_SYNC		coresight.TRACE[6]	gpio4.IO[8]	ccmsrcgpcmix.BOOT_CFG[6]	sim_m.HADDR[23]	ALT5	PD	NVCC_SAI1
156	NAND_WE_B [1]	R26	rawnand.WE_B		usdhc3.CLK			gpio3.IO[17]		sim_m.HADDR[13]	ALT5	PD	NVCC_NAND
160	NAND_WP_B [1]	R27	rawnand.WP_B		usdhc3.CMD			gpio3.IO[18]		sim_m.HADDR[14]	ALT5	PD	NVCC_NAND
162	NAND_DATA04 [1]	M26	rawnand.DATA04	qspi.B_DATA[0]	usdhc3.DATA0			gpio3.IO[10]		sim_m.HADDR[6]	ALT5	PD	NVCC_NAND
164	NAND_DATA05 [1]	L26	rawnand.DATA05	qspi.B_DATA[1]	usdhc3.DATA1			gpio3.IO[11]		sim_m.HADDR[7]	ALT5	PD	NVCC_NAND
166	NAND_DATA06 [1]	K26	rawnand.DATA06	qspi.B_DATA[2]	usdhc3.DATA2			gpio3.IO[12]		sim_m.HADDR[8]	ALT5	PD	NVCC_NAND
168	NAND_DATA07 [1]	N26	rawnand.DATA07	qspi.B_DATA[3]	usdhc3.DATA3			gpio3.IO[13]		sim_m.HADDR[9]	ALT5	PD	NVCC_NAND
174	SAI1_RXD7 [3]	AF19	sai1.RX_DATA[7]	sai6.MCLK	sai1.TX_SYNC	sai1.TX_DATA[4]	coresight.TRACE[7]	gpio4.IO[9]	ccmsrcgpcmix.BOOT_CFG[7]	sim_m.HADDR[24]	ALT5	PD	NVCC_SAI1
196	ECSPI2_SCLK	E6	ecspi2.SCLK	uart4.RX				gpio5.IO[10]		tpsmp.HDATA[12]	ALT5	PD	NVCC_ECSPI
198	ECSPI2_MISO	A8	ecspi2.MISO	uart4.CTS_B				gpio5.IO[12]		tpsmp.HDATA[14]	ALT5	PD	NVCC_ECSPI
200	ECSPI2_MOSI	B8	ecspi2.MOSI	uart4.TX				gpio5.IO[11]		tpsmp.HDATA[13]	ALT5	PD	NVCC_ECSPI
202	ECSPI2_SS0	A6	ecspi2.SS0	uart4.RTS_B				gpio5.IO[13]		tpsmp.HDATA[15]	ALT5	PD	NVCC_ECSPI
206	NAND_CE3_B	L27	rawnand.CE3_B	qspi.B_SS1_B	usdhc3.DATA6			gpio3.IO[4]		sim_m.HADDR[0]	ALT5	PD	NVCC_NAND
208	SPDIF_EXT_CLK	AF8	spdif1.EXT_CLK	pwm1.OUT				gpio5.IO[5]		tpsmp.HDATA[7]	ALT5	PD	NVCC_SAI3
210	UART3_RXD	E18	uart3.RX	uart1.CTS_B	usdhc3.RESET_B			gpio5.IO[26]		tpsmp.HDATA[28]	ALT5	PD	NVCC_UART
212	UART3_TXD	D18	uart3.TX	uart1.RTS_B	usdhc3.VSELECT			gpio5.IO[27]		tpsmp.HDATA[29]	ALT5	PD	NVCC_UART
216	GPIO1_IO00	AG14	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT				anamix.REF_CLK_32K	ccmsrcgpcmix.EXT_CLK1	sjc.FAIL	ALT0	PD	NVCC_GPIO1
218	GPIO1_IO11	AC10	gpio1.IO[11]	usb2.OTG_ID			usdhc3.VSELECT	ccmsrcgpcmix.PMIC_READY	ccmsrcgpcmix.OUT0	caam_wrapper.RNG_OSC_OBS	ALT0	PD	NVCC_GPIO1
220	GPIO1_IO08	AG10	gpio1.IO[8]	enet1.1588_EVENT0_IN				usdhc2.RESET_B	ccmsrcgpcmix.WAIT	qspi.TEST_TRIG	ALT0	PD	NVCC_GPIO1
222	GPIO1_IO09	AF10	gpio1.IO[9]	enet1.1588_EVENT0_OUT			usdhc3.RESET_B	sdma2.EXT_EVENT[0]	ccmsrcgpcmix.STOP	rawnand.TEST_TRIG	ALT0	PD	NVCC_GPIO1
244	SAI5_RXFS	AB15	sai5.RX_SYNC	sai1.TX_DATA[0]				gpio3.IO[19]		ecspi3.TEST_TRIG	ALT5	PD	NVCC_SAI5
248	ONOFF	A25	snvsmix.ONOFF								ALT0	Z [2]	NVCC_SNVS_1P8
252	SAI3_RXFS	AG8	sai3.RX_SYNC	gpt1.CAPTURE1	sai5.RX_SYNC	sai3.RX_DATA[1]		gpio4.IO[28]		tpsmp.HTRANS[0]	ALT5	PD	NVCC_SAI3
256	SAI3_TXD	AF6	sai3.TX_DATA[0]	gpt1.COMPARE3	sai5.RX_DATA[3]			gpio5.IO[1]		tpsmp.HDATA[3]	ALT5	PD	NVCC_SAI3

[1] These signals are only available on modules without Wi-Fi/Bluetooth
[2] 100k pull-up resistor on the module
[3] On modules with Wi-Fi/Bluetooth, this pin is shared with the WLAN Wake Host signal of the Wi-Fi module
[4] These signals are only available on modules without a CAN interface

5. Interface Description

5.1 Power Signals

Table 5-1 Power Supply Pins

X1 Pin #	Verdin Signal Name	I/O	Description	Remarks
251, 253, 255, 257, 259	VCC	I	3.135V to 5.5V main power supply	Use decoupling capacitors on the carrier board
10, 11, 18, 27, 28, 33, 39, 40, 45, 50, 51, 65, 68, 71, 77, 83, 86, 89, 97, 98, 103, 109, 110, 115, 121, 122, 127, 134, 145, 146, 158, 167, 170, 173, 179, 182, 194, 195, 204, 209, 223, 224, 229, 230, 236, 242, 243	GND	I	Digital Ground	
249	VCC_BACKUP	I	RTC Power supply can be connected to a backup battery.	Can be left unconnected if the internal RTC is not used. The SNVS supplies of the SoC are powered by VCC, not VCC_BACKUP.

Table 5-2 Power Management Pins

X1 Pin #	Verdin Signal Name	I/O	Type	Remarks
258	CTRL_RESET_MOCI#	O	OD 3.3V	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and/or after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. Can be left floating on carrier board.
254	CTRL_PWR_EN_MOCI	O	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	1.8V	Enable signal for the power rails on the carrier board peripherals which need to be turned off during sleep mode. It is only high during running mode. The signal is standard GPIO with an on-module 10k pull-down resistors. The signal is defined during the power up sequence. The signal can be left floating on carrier board.
260	CTRL_RESET_MICO#	I	OD 1.8V	Open-drain input which resets the module if shorted to ground on carrier board. There is a 100k on-module pull-up to the 1.8V SNVS rail present. This means it can be left floating on carrier board.
248	CTRL_PWR_BTN_MICO#	I	OD 1.8V	Long pulling down is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with 100k pull-up resistor to the 1.8V SNVS rail is on the module. Can be left floating on carrier board.
246	CTRL_RECOVERY_MICO#	I	OD 1.8V	Shorting to ground during power-up is setting module into recovery mode. There is a 10k pull-up on the module. Can be left floating on carrier board.
252	CTRL_WAKE1_MICO#	I	1.8V	Wake-capable pin which allows resuming from sleep mode. There are no pull resistors on the carrier board. Can be left floating on carrier board if the wake feature is disabled in software. Is a regular SoC GPIO.
250	CTRL_FORCE_OFF_MOCI#	O	OD 5V	Output for forcing the turning-off of the main power rail. This signal needs to be ignored for the first 400ms during power-up sequence. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. Can be left floating on carrier board.

The Verdin iMX8M Mini features the NXP PCA9450A power management IC (PMIC). In addition to managing the power-up and down sequence, this IC also enables controlling the voltage level of certain power rails. When applying the main power to the Verdin module the PMIC will ramp up all rails, then release the POR_B signal at the end. This reset is used for the SoC and some of the on-module peripherals. It is available as a buffered output on pin 258 of the SODIMM module edge connector. This CTRL_RESET_MOCI# signal is an open-drain signal without pull up resistors on the module. Since the pin is 3.3V tolerant, the carrier board can pull it up to 1.8V or 3.3V.

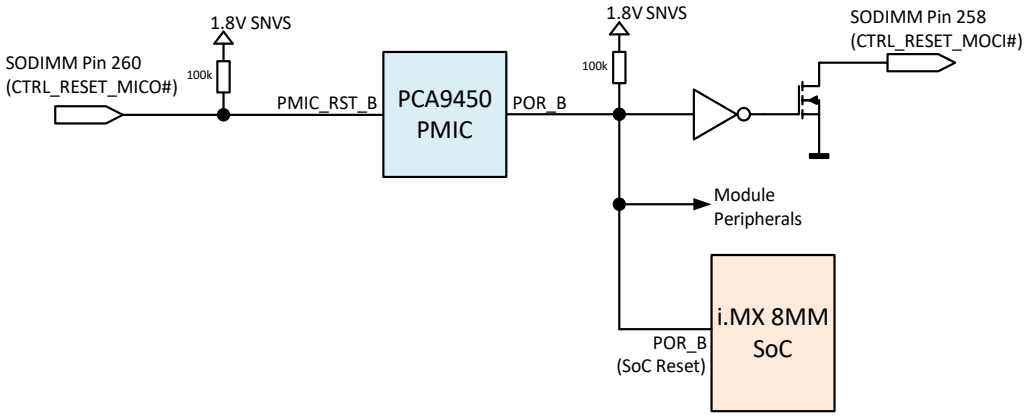

Figure 5 RESET_MOCI# circuit

The Verdin standard features a reset input (CTRL_RESET_MICO#, pin 260). This input is connected to the PMIC_RST_B input of the PCA9450A PMIC. The PMIC is programmed to do a power-down sequence when the PMIC_RST_B signal is set low. The power-down sequence is followed by a power-up sequence if the CTRL_RESET_MICO# is released. The CTRL_RESET_MICO# pin can be left floating if not needed.

The Verdin iMX8M Mini features a power button input signal (CTRL_PWR_BTN_MICO#, pin 248). This input signal is connected directly to the ONOFF input of the i.MX 8M Mini SoC. A short press (<5s) starts the power-up sequence if the module is shut down. If the module is running, a short press (<5s) will create an interrupt. It depends on the settings in the operating system whether this interrupt will initiate a power-down sequence or some other reaction. A long press (>5s) of the CTRL_PWR_BTN_MICO# will initiate the power-down sequence of the PMIC, independent of the operating system (force off). Since the Verdin standard defines that a module always starts booting when the main power rail is applied, there is a pulse generator circuit on the module which generates a short power button press signal after the main input rail is attached to the module.

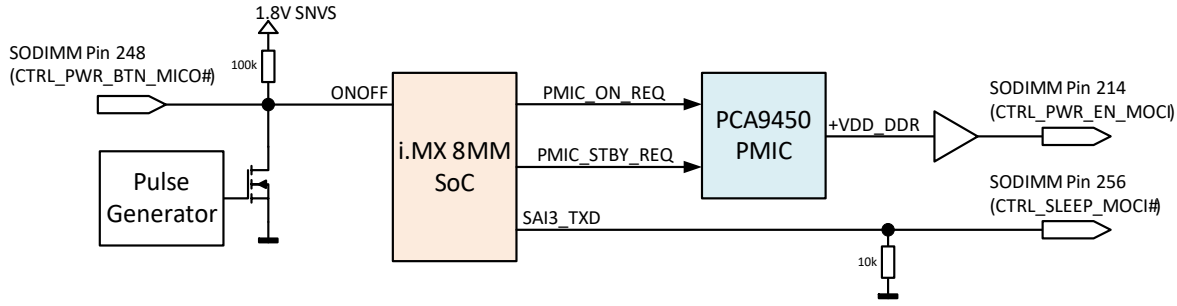

Figure 6 Power enable circuit

To be able to save power, several peripheral devices on the Verdin iMX8M Mini module have dedicated power rails which can be switched off. The Wi-Fi (and Bluetooth) module power rails can be controlled by the GPIO3.IO[25]. The Wi-Fi module features a power on reset, no external reset is required. However, the firmware needs to be downloaded to the Wi-Fi module every time the power rail is turned on. The power rails of the Ethernet PHY can be controlled by using the

GPIO2.IO[20]. The Ethernet PHY circuit features a reset circuit that resets the device if the Ethernet power rail is turned off. All the GPIO controls for the on-module peripheral rail switches are active on. This means setting the GPIO high will enable the rail while setting it low will disable it.

Table 5-3 On-Module Peripheral Power Control

GPIO	i.MX 8MM Ball Name	Peripheral Power Rail
GPIO3.IO[25]	SAI5_MCLK	Wi-Fi and Bluetooth Module
GPIO2.IO[20]	SD2_WP	Ethernet PHY

The Verdin iMX8M Mini features a CTRL_FORCE_OFF_MOCI# signal which is intended to be used for killing the main power rail. This signal is generated from the PMIC. For preventing the signals is triggered during a reset cycle, the CTRL_FORCE_OFF_MOCI# is delayed. This means the CTRL_FORCE_OFF_MOCI# is asserted around 1.5s after the PMIC has been powered off. The 1.5 seconds is a typical value. The actual delay can vary between modules and temperatures.

5.1.1 Power Supply Use Case Examples

The power control pins of the Verdin module are very flexible and allow different use cases for the power supply on the carrier board. The following block diagrams are just examples. There are other options possible.

Verdin Development Board Use Case

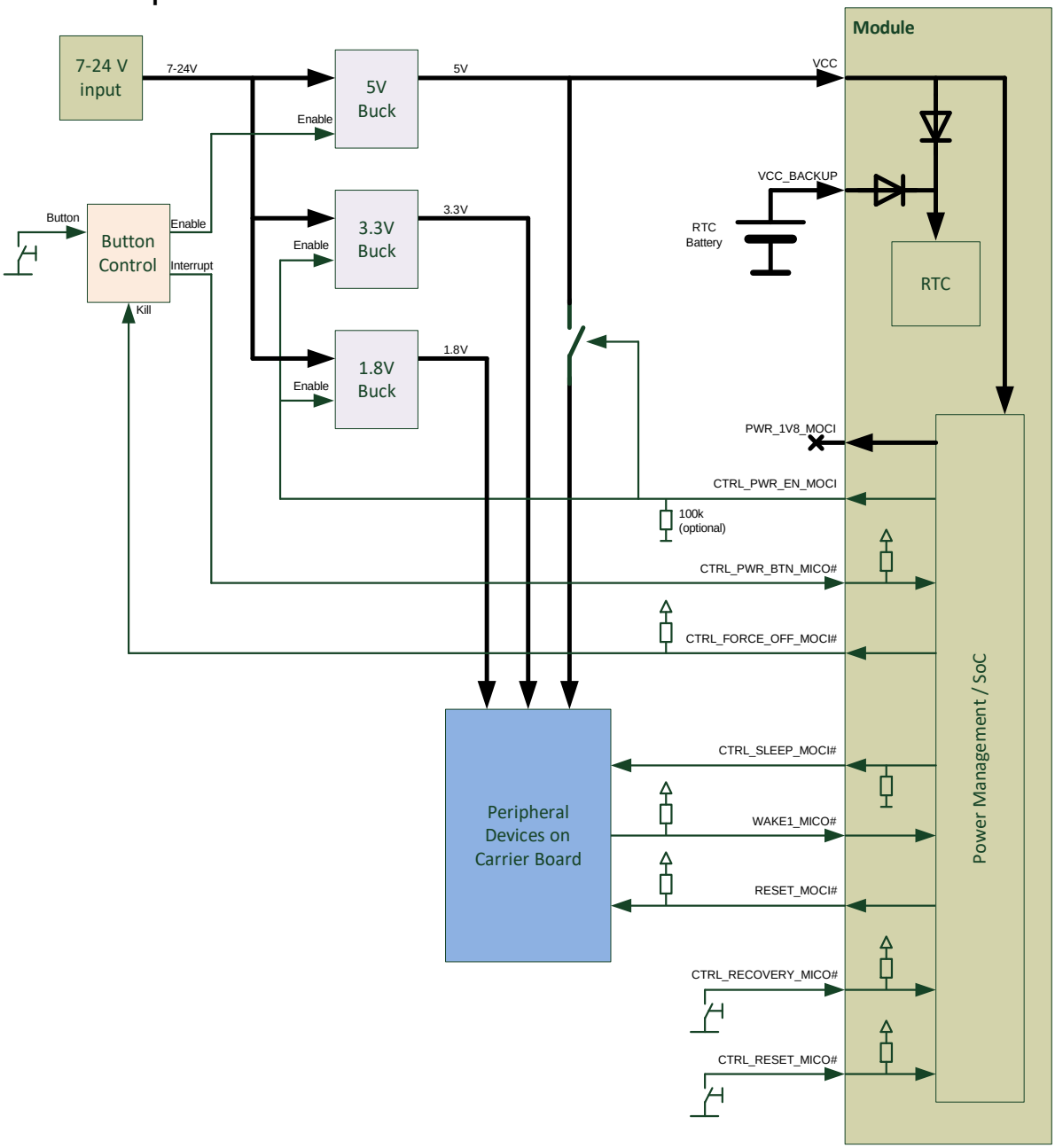

Figure 7 Verdin Development Power Supply Block Diagram

On the Verdin Development Board, the module gets powered from a 5V buck regulator. This regulator is enabled by a button control IC. Short pressing the power button will enable the 5V buck regulator which powers up the Verdin module. The Verdin module is then enabling the peripheral power rails on the carrier board by asserting the CTRL_PWR_EN_MOCI signal.

If the module is running, a short pressing of the power button will generate an interrupt output at the power button control IC. This interrupt is connected to the CTRL_PWR_BTN_MICO# input of the module. A falling edge on this input will cause a software interrupt. Depending on the configuration, the OS will then start shutting down the software and ramping down power rails on the module. The module is asserting the CTRL_FORCE_OFF_MOCI# signal which kills the enable output of the power button control IC. This disables the main 5V rail.

If the module is running, a long pressing of the power button (>5s) is generating an emergency power shutdown of the system. The power button control IC is forwarding the long press event to the CTRL_PWR_BTN_MICO# input of the module PMIC. The PMIC is shutting down all power rails

without software interaction. In the end, the CTRL_FORCE_OFF# is asserted which turns off the main 5V regulator.

Minimalistic Carrier Board Power Supply Use Case

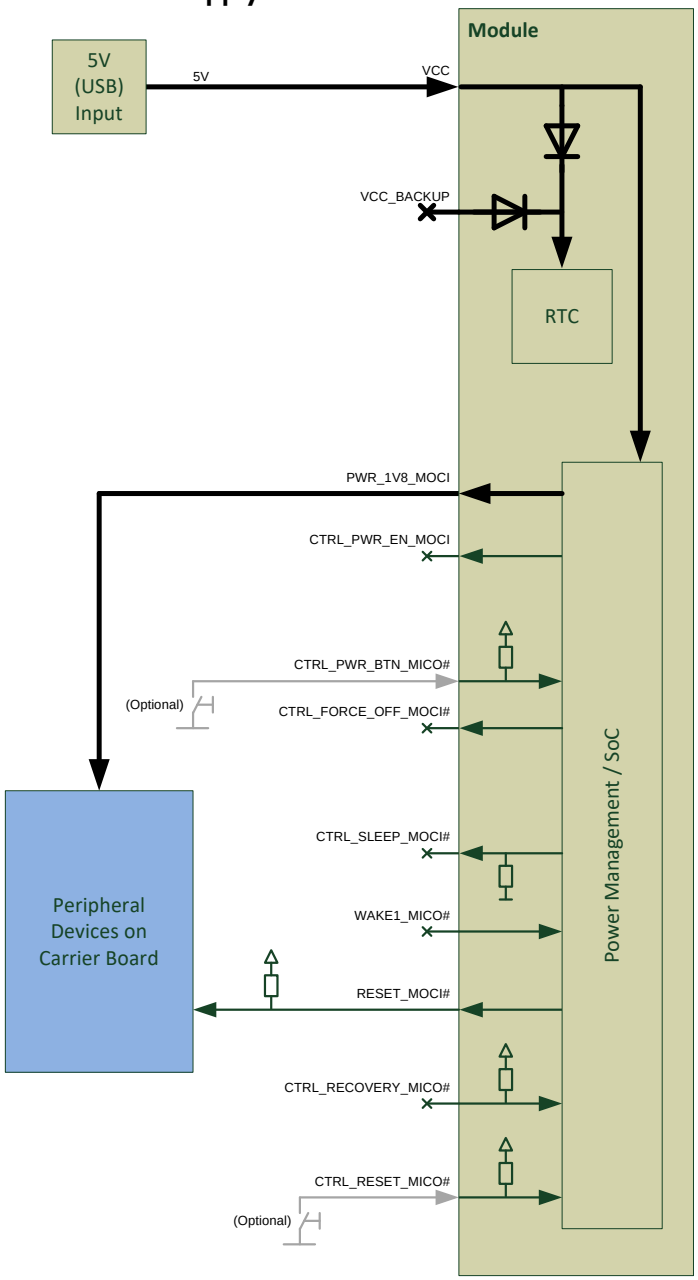

Figure 8 Minimalistic Power Supply Block Diagram

The Verdin module can run directly from any power source between 3.135V and 5.5V. This means the module can run directly from a 5V USB power port. As soon as the main power is plugged in, the module starts to ramp up all the voltages and boots. The PWR_1V8_MOCI can deliver up to 250mA for peripherals on the carrier board.

Optional, a simple push button can be added to the CTRL_PWR_BTN_MICO# and the CTRL_RESET_MICO# input. Short pressing the power button when the system is booted, a software interrupt is generated. Depending on the configuration, the OS will then start shutting down the software and ramping down power rails on the module (including the PWR_1V8_MOCI). In this off-state, the system can be turned on by pressing again the power button.

A long pressing on the power button (>5s) initiates an emergency power shutdown. All power rails will be turned off. The module can be turned back on by using the power button.

Single Cell Battery Powered Use Case

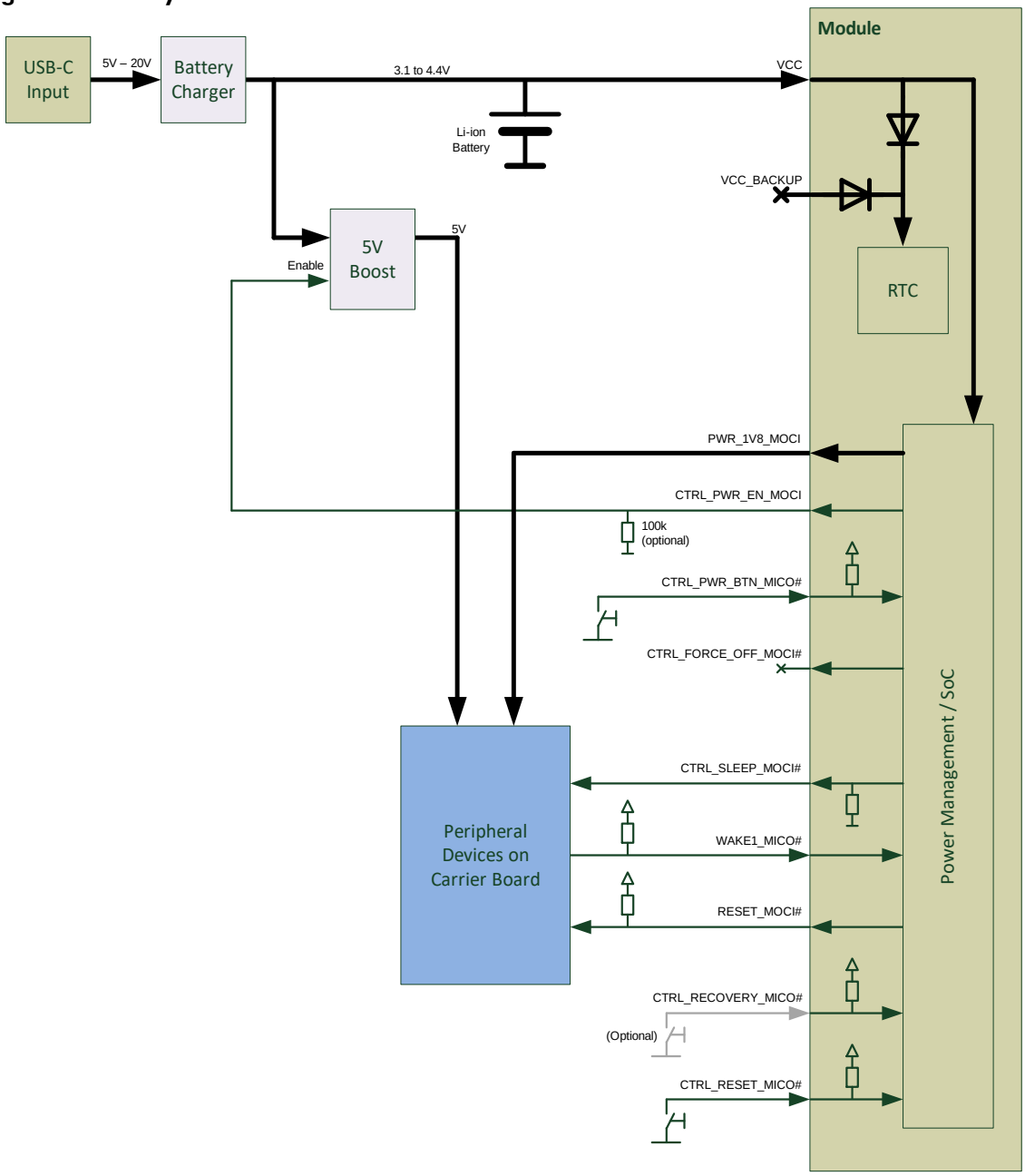

Figure 9 Single Cell Battery Power Supply Block Diagram

The wide input voltage range of the Verdin module allows it to run directly from a single cell Li-ion battery. If any buck or boost regulators are required for the peripherals on the carrier board, make sure they can also run from the voltage range of the battery system. The external regulators can be enabled by using the CTRL_PWR_EN_MOC signal.

The simple push button on the CTRL_PWRBTN_MICO# input can be used for turning on the module, creating software interrupts (short pressing), or initiating an emergency power-off (long pressing).

The CTRL_SLEEP_MOCI# signal can be used to turn off peripheral rails that are not used while the system is in low power mode in order to save battery. The WAKE1_MICO# input can be used for

waking up the system from sleep modes. Alternatively, the power button can also be used for generating a wake event.

5.2 GPIOs

The Verdin form factor features 10 dedicated general-purpose input-output (GPIO) pins. Four of them are reserved for the MIPI CSI camera interface and two for the MIPI DSI display interface. Besides these 10 GPIOs, several pins can be used as GPIO if their primary function is not in use. For compatibility reasons, it is recommended to use the 10 dedicated GPIOs first.

Table 5-4 Dedicated GPIO signals

X1 Pin#	Verdin Standard Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
206	GPIO_1	NAND_CE3_B	gpio3.IO[4]	I/O	
208	GPIO_2	SPDIF_EXT_CLK	gpio5.IO[5]	I/O	
210	GPIO_3	UART3_RXD	gpio5.IO[26]	I/O	
212	GPIO_4	UART3_TXD	gpio5.IO[27]	I/O	
216	GPIO_5_CSI	GPIO1_IO00	gpio1.IO[0]	I/O	Reserved general-purpose IO for MIPI CSI camera interface
218	GPIO_6_CSI	GPIO1_IO11	gpio1.IO[11]	I/O	
220	GPIO_7_CSI	GPIO1_IO08	gpio1.IO[8]	I/O	
222	GPIO_8_CSI	GPIO1_IO09	gpio1.IO[9]	I/O	
17	GPIO_9_DSI	NAND_RE_B	gpio3.IO[15]	I/O	Reserved general-purpose IO for MIPI DSI display interface
21	GPIO_10_DSI	NAND_CE2_B	gpio3.IO[3]	I/O	

5.2.1 Wakeup Source

In principle, all GPIOs can be used to wake up the Verdin iMX8M Mini module from a suspend state. In the Verdin module standard, pin 252 is the default wakeup source. Only this pin is guaranteed to be wakeup compatible with other Verdin modules. Please use only this pin to wake up the module if the carrier board needs to be compatible with other Verdin modules.

Table 5-5 Verdin Wakeup Source

X1 Pin#	Verdin Standard Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
252	CTRL_WAKE1_MICO#	SAI3_RXFS	gpio4.IO[28]	I/O	Standard external wake signal

5.3 Ethernet

In the Verdin module standard, there are two Ethernet ports. One port is a 10/100/1000 Mbit media-dependent interface. This interface has the Ethernet PHY on the module. The second port is a gigabit media independent interface (RGMII). Since the i.MX 8M Mini SoC features only a single Ethernet MAC, only one or the other Verdin Ethernet is available on a module. The standard SKU versions of the Verdin feature an on-module Microchip KSZ9131 Gigabit Ethernet PHY and therefore provide the media dependent interface. Modules with RGMII output are available as build-to-order assembly variants.

Table 5-6 Media Dependent Ethernet Pins

X1 Pin #	Verdin Signal Name	KSZ9131 Signal Name	I/O	Description	Remarks
225	ETH_1_MDI0_P	TXRXP_A	I/O	Media Dependent Interface	
227	ETH_1_MDI0_N	TXRXM_A	I/O	Media Dependent Interface	
233	ETH_1_MDI1_P	TXRXP_B	I/O	Media Dependent Interface	
231	ETH_1_MDI1_N	TXRXM_B	I/O	Media Dependent Interface	
239	ETH_1_MDI2_P	TXRXP_C	I/O	Media Dependent Interface	
241	ETH_1_MDI2_N	TXRXM_C	I/O	Media Dependent Interface	
247	ETH_1_MDI3_P	TXRXP_D	I/O	Media Dependent Interface	
245	ETH_1_MDI3_N	TXRXM_D	I/O	Media Dependent Interface	
237	ETH_1_LED_2	LED2	O	LED indication output	Is low if a link (any speed) is established
235	ETH_1_LED_1	LED1	O	LED indication output	Toggles during RX/TX activity

If only fast Ethernet is required, 10/100Mbit magnetics providing only 2 lanes are sufficient. In this case, MDI2 and MDI3 can be left unconnected. Please follow the carrier board design guide.

The Gigabit Ethernet MAC in the SoC integrates an accurate IEEE 1588 compliant timer for clock synchronization for distributed control nodes used in industrial automation applications. The interface features up to four external IEEE 1588 synchronization pins on alternate functions. The Ethernet interface supports Audio Video Bridging (AVB) and Time-Sensitive Networking (TSN).

The KSZ9131 INT# signal (pin 38) is connected to the GPIO1_IO10 ball of the i.MX 8M Mini SoC.

Table 5-7 IEEE 1588 Signals (alternate functions, not compatible with other Verdin modules)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
220	GPIO_7	GPIO1_IO08	enet1.1588_EVENT0_IN	I	IEEE 1588 input capture signal
55	I2C_2_DSI_SCL	I2C2_SCL	enet1.1588_EVENT1_IN	I	
222	GPIO_8	GPIO1_IO09	enet1.1588_EVENT0_OUT	O	IEEE 1588 output compare
53	I2C_2_DSI_SDA	I2C2_SDA	enet1.1588_EVENT1_OUT	O	

As a built-to-order version, the Verdin is available with a media independent interface (RGMII) instead of the media dependent Ethernet port. Such assembly variants have no on-module Ethernet PHY and make the RGMII signals available on the module edge connector. This allows placing a specialized PHY on the carrier board which fits special needs for automotive or industrial applications. The RGMII signals are available on the *"Reserved"* Verdin pins.

Table 5-8 RGMII signals (not available on standard SKU)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
199	ETH_2_RGMII_RX_CTL	ENET_RX_CTL	enet1.RGMII_RX_CTL	I	RGMII_RX_CTL
197	ETH_2_RGMII_RXC	ENET_RXC	enet1.RGMII_RXC	I	RGMII_RXC
201	ETH_2_RGMII_RXD_0	ENET_RD0	enet1.RGMII_RD0	I	RGMII_RXD0
203	ETH_2_RGMII_RXD_1	ENET_RD1	enet1.RGMII_RD1	I	RGMII_RXD1
205	ETH_2_RGMII_RXD_2	ENET_RD2	enet1.RGMII_RD2	I	RGMII_RXD2
207	ETH_2_RGMII_RXD_3	ENET_RD3	enet1.RGMII_RD3	I	RGMII_RXD3
211	ETH_2_RGMII_TX_CTL	ENET_TX_CTL	enet1.RGMII_TX_CTL	O	RGMII_TX_CTL
213	ETH_2_RGMII_TXC	ENET_TXC	enet1.RGMII_TXC	O	RGMII_TXC
221	ETH_2_RGMII_TXD_0	ENET_TD0	enet1.RGMII_TD0	O	RGMII_TXD0
219	ETH_2_RGMII_TXD_1	ENET_TD1	enet1.RGMII_TD1	O	RGMII_TXD1
217	ETH_2_RGMII_TXD_2	ENET_TD2	enet1.RGMII_TD2	O	RGMII_TXD2
215	ETH_2_RGMII_TXD_3	ENET_TD3	enet1.RGMII_TD3	O	RGMII_TXD3
193	ETH_2_RGMII_MDC	ENET_MDC	enet1.MDC	O	RGMII_MDC
191	ETH_2_RGMII_MDIO	ENET_MDIO	enet1.MDIO	I/O	RGMII_MDIO
189	ETH_2_RGMII_INT#	GPIO1_IO10	gpio1.IO[10]	I	Control interrupt input

5.4 Wi-Fi and Bluetooth

The Verdin iMX8M Mini is available with an optional on-module Wi-Fi and Bluetooth interfaces. The addition of "WB" in the product name indicates that a version features Wi-Fi and Bluetooth. These Verdin module versions make use of the AW-CM276NF Dual-Band Wi-Fi and Bluetooth module from Azurewave.

Features:

- Wi-Fi 802.11a/b/g/n/ac
- Dual-Band 5 GHz and 2.4GHz
- Up to 866.7 Mbps
- 20/40/80 MHz channel bandwidth
- Station/Client Mode, Access Point Mode, Wi-Fi- Direct Mode, and Simultaneous Station and Access point mode
- Bluetooth 5.0 (BR/EDR), BLE
- Murata HSC (MXHP32) connector for the dual external antenna in 2x2 configuration, compatible to IPX/IPEX connector MHF4 series
- Pre-certified for CE (Europe), FCC (United States), IC (Canada), TELEC (Japan) and WPC (India). See https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products

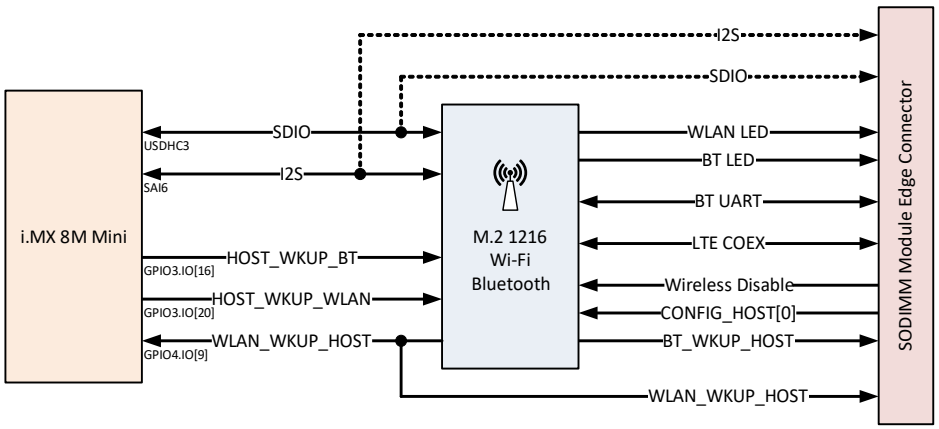

Figure 10: Wi-Fi and Bluetooth block diagram

The Wi-Fi module is connected over a 4-bit SDIO interface with the i.MX 8M Mini SoC. It uses the USDHC3 instance of the SoC. For Bluetooth Audio, there is an additional I²S interface available between the SoC and the Wi-Fi module which uses the SAI6 instance of the SoC. Using Bluetooth Audio requires a different firmware for the Azurewave module which is not provided in the default BSP. On Verdin modules without Wi-Fi, the SDIO and I²S are both available as additional interfaces on the *"Module-specific"* pins. This assembly option is shown in the block diagram with dashed lines.

Table 5-9 Signal Pins between AW-CM276NF and i.MX 8M Mini

AW-CM276NF Pin Name	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
SD_CMD	NAND_WP_B	usdhc3.CMD	I/O	4-bit SDIO interface for Wi-Fi and Bluetooth
SD_DAT[0]	NAND_DATA04	usdhc3.DATA0	I/O	
SD_DAT[1]	NAND_DATA05	usdhc3.DATA1	I/O	
SD_DAT[2]	NAND_DATA06	usdhc3.DATA2	I/O	
SD_DAT[3]	NAND_DATA07	usdhc3.DATA3	I/O	
SD_CLK	NAND_WE_B	usdhc3.CLK	I	
GPIO[6]/PCM_CLK	SAI1_RXD4	sai6.TX_BCLK	I	I²S interface for Bluetooth audio
GPIO[7]/PCM_SYNC	SAI1_RXD6	sai6.TX_SYNC	I	
GPIO[4]/PCM_DIN	SAI1_RXD5	sai6.TX_DATA[0]	I	
GPIO[5]/PCM_DOUT	SAI1_TXD5	sai6.RX_DATA[0]	O	
GPIO[15]/ TMS/ Host Wake WLAN	SAI5_RXC	gpio3.IO[20]	I	HOST_WKUP_WLAN : SoC to AW-CM276NF Wi-Fi Wakeup
GPIO[12]/ UART Host Wake BT	NAND_READY_B	gpio3.IO[16]	I	HOST_WKUP_BT: SoC to AW-CM276NF Bluetooth Wakeup
GPIO[14]/TCK/ WLAN Wake Host	SAI1_RXD7	gpio4.IO[9]	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output, signal is also available on SODIMM connector

The AW-CM276NF features four wake signals of which three are connected to the SoC. Two are input signals (one for the Wi-Fi and one for Bluetooth) which allow for waking up the radio. Only the output signal of the AW-CM276NF which is used by the Wi-Fi receiver to wake up the system (SoC) is connected to the SoC and is also available on the module edge connector. The wake output of the Bluetooth is only available on the SODIMM connector. The actual available sleep functions ad wake signals depend on the firmware that is loaded into the Azurewave module.

Table 5-10 *"Module-specific"* Signal Pins of the AW-CM276NF on SODIMM Connector

X1 Pin#	Verdin Std Function	AW-CM276NF Pin Name	I/O	Description
174	MSP_37	GPIO[14]/TCK/ WLAN Wake Host	O	WLAN_WKUP_HOST: AW-CM276NF Wi-Fi wake output, signal is also connected to the SoC
172	MSP_36	GPIO[13]/BT IRQ(O)	O	BT_WKUP_HOST: AW-CM276NF Bluetooth wake output
188	MSP_43	GPIO[2]/WLAN_LED	O	Wi-Fi activity LED
176	MSP_38	GPIO[3]/BT_LED	O	Bluetooth activity LED
190	MSP_44	GPIO[9]/UART_SIN	I	BT UART mode: RX data
192	MSP_45	GPIO[8]/UART_SOUT	O	BT UART mode: TX data
186	MSP_42	GPIO[11]/UART_RTSn	O	BT UART mode: Request to send
184	MSP_41	GPIO[10]/UART_CTSn	I	BT UART mode: Clear to send
142	MSP_24	GPIO[22]/PCIE_W_DISABLEn	I	PCIE Wireless Disable Input (active low), pull-up resistor on module, can be left floating
178	MSP_39	GPIO[16]/LTE_COEX_IN	I	Input signal for managing coexistence of LTE in close proximity
180	MSP_40	GPIO[17]/LTE_COEX_OUT	O	Output signal for managing coexistence of LTE in close proximity
144	MSP_25	CONFIG_HOST[0]	I	Strapping input, can be left floating. Connect to ground for UART Bluetooth feature (contact Toradex)

The usage of Wi-Fi and Bluetooth is regulated depending on the region and needs certification. More information can be found on this site: https://developer.toradex.com/knowledge-base/wi-fi-accessories-recommended-for-toradex-products.

5.5 USB

The i.MX 8M Mini features two identical USB 2.0 ports which are both OTG capable. However, in the Verdin standard, only the USB_1 port is an OTG port while USB_2 is only a host port. Therefore, it is recommended to use only USB_1 as an OTG port. The USB_1 port is also used for the serial mode (recovery mode). Since the i.MX 8M Mini SoC features only USB 2.0 High Speed, the SuperSpeed signals of the USB_2 port are left unconnected on the Verdin iMX8M Mini module.

Table 5-11 USB_1 Interface Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
165	USB_1_D_P	USB1_DP	USB1_DP	I/O	Positive Differential USB Signal, OTG capable
163	USB_1_D_N	USB1_DN	USB1_DN	I/O	Negative Differential USB Signal, OTG capable
159	USB_1_VBUS	USB1_VBUS	USB1_VBUS	I	Use this pin to detect if VBUS is present. This pin is a 5V input.
161	USB_1_ID	USB1_ID	USB1_ID	I	Use this pin to detect the ID pin if you use the port in OTG mode.
155	USB_1_EN	GPIO1_IO12	usb1.OTG_PWR	O	This pin enables the external USB voltage supply for the USB_1 interface.
157	USB_1_OC#	GPIO1_IO13	usb1.OTG_OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USB_1 interface.

Table 5-12 USB_2 Interface Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
183	USB_2_D_P	USB2_DP	USB2_DP	I/O	Positive Differential USB Signal
181	USB_2_D_N	USB2_DN	USB2_DN	I/O	Negative Differential USB Signal
177	USB_2_SSRX_P				USB 3.x SuperSpeed is not available. The pins are not connected on the module.
175	USB_2_SSRX_N				
171	USB_2_SSTX_P				
169	USB_2_SSTX_N				
185	USB_2_EN	GPIO1_IO14	usb2.OTG_PWR	O	This pin enables the external USB voltage supply for the USB_2 interface.
187	USB_2_OC#	GPIO1_IO15	usb2.OTG_OC	I	USB overcurrent, this pin can signal an overcurrent condition in the USB supply of the USB_2 interface.
218	GPIO_6	GPIO1_IO11	usb2.OTG_ID	I	OTG ID pin for USB_2 port. This is not a standard pin, **not compatible** with other Verdin modules.

5.6 Display

The i.MX 8M Mini SoC features a single display controller with MIPI DSI output with up to four lanes. The i.MX 8M Mini SoC does not have a native LVDS function. However, it is possible to add an MIPI DSI to LVDS (or other display interfaces) bridge on the carrier board. The MIPI DSI port is available as a *"Reserved"* interface of the Verdin standard. The HDMI port in the *"Reserved"* class of the Verdin is not available on the Verdin iMX8M Mini.

The interface uses the MIPI D-PHY for the physical layer, compatible with the version 1.2 specifications. The maximum data transfer per lane is 1.5Gbps. Bi-directional data transmission is available on lane 0. Resolutions up 1920x1080p60 and 1800x1200p60 are supported.

Table 5-13 DSI interface signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
37	DSI_1_CLK_P	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P	O	DSI Interface clock
35	DSI_1_CLK_N	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N		
49	DSI_1_D0_P	MIPI_DSI_D0_P	MIPI_DSI_D0_P	I/O	DSI Interface data lane 0
47	DSI_1_D0_N	MIPI_DSI_D0_N	MIPI_DSI_D0_N		
43	DSI_1_D1_P	MIPI_DSI_D1_P	MIPI_DSI_D1_P	O	DSI Interface data lane 1
41	DSI_1_D1_N	MIPI_DSI_D1_N	MIPI_DSI_D1_N		
31	DSI_1_D2_P	MIPI_DSI_D2_P	MIPI_DSI_D2_P	O	DSI Interface data lane 2
29	DSI_1_D2_N	MIPI_DSI_D2_N	MIPI_DSI_D2_N		
25	DSI_1_D3_P	MIPI_DSI_D3_P	MIPI_DSI_D3_P	O	DSI Interface data lane 3
23	DSI_1_D3_N	MIPI_DSI_D3_N	MIPI_DSI_D3_N		
55	I2C_2_DSI_SCL	I2C2_SCL	i2c2.SCL	O	I^2C interface, intended to be used as DDC or for controlling DSI bridges on carrier board
53	I2C_2_DSI_SDA	I2C2_SDA	i2c2.SDA	I/O	
19	PWM_3_DSI	GPIO1_IO01	pwm1.OUT	O	Display backlight brightness control
21	GPIO_10_DSI	NAND_CE2_B	gpio3.IO[3]	O	DSI_1_BKL_EN; Display backlight enable
17	GPIO_9_DSI	NAND_RE_B	gpio3.IO[15]	I	DSI_1_INT#; Interrupt input, intended to be used as hot plug detect or for interrupt messages from DSI bridges on carrier board

5.7 Camera Interface

The NXP i.MX 8M Mini supports one quad lane MIPI CSI-2 interface for connecting compatible cameras. The interface is compatible with single, dual, and quad lane CSI cameras. The interface uses MIPI D-PHY as the physical layer. The interface supports RGB, YUV, YCbCr, and RAW color space definitions. 24-bit down to 8-bit per pixel are supported. The MIPI CSI-2 signals are located in the *"Reserved"* class of the Verdin specifications.

Features

- Scalable data lane support, 1 to 4 Data Lanes
- Up to 1.5Gbps per lane, providing 1080p60 capability with all 4 lanes
- Supports 10Mbps data rate in low power modes
- Implements all three CSI-2 MIPI layers (pixel to byte backing, low-level protocol, and lane management)
- Unidirectional master operation supported

Table 5-14 MIPI CSI-2 interface signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	CSI Signal Name	I/O	Description
111	CSI_1_CLK_P	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P	I	CSI interface clock
113	CSI_1_CLK_N	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N		
123	CSI_1_D0_P	MIPI_CSI_D0_P	MIPI_CSI_D0_P	I/O	CSI interface data lane 0
125	CSI_1_D0_N	MIPI_CSI_D0_N	MIPI_CSI_D0_N		
117	CSI_1_D1_P	MIPI_CSI_D1_P	MIPI_CSI_D1_P	I	CSI interface data lane 1
119	CSI_1_D1_N	MIPI_CSI_D1_N	MIPI_CSI_D1_N		
105	CSI_1_D2_P	MIPI_CSI_D2_P	MIPI_CSI_D2_P	I	CSI interface data lane 2
107	CSI_1_D2_N	MIPI_CSI_D2_N	MIPI_CSI_D2_N		
99	CSI_1_D3_P	MIPI_CSI_D3_P	MIPI_CSI_D3_P	I	CSI interface data lane 3
101	CSI_1_D3_N	MIPI_CSI_D3_N	MIPI_CSI_D3_N		

In addition to the MIPI CSI-2 interface pins, the Verdin offers a dedicated I²C interface and a master clock output for the camera. Unfortunately, the iMX8M Mini MIPI CSI IP does not offer a dedicated clock. Thus, a master clock signal from the digital audio interface is provided on the module edge connector at pin 91. The clock source can be selected from either the SAI3 or SAI5 interface. Please carefully check whether the required signal is available from the SAI master clock and is not in conflict with any other digital audio interface. To reduce EMC and simplify software design, it is recommended to generate the master clock on the carrier board or at the camera.

Table 5-15 Additional Camera Interface Signals

X1 Pin#	Verdin Signal Name	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
95	I2C_4_CSI_SCL	I2C3_SCL	i2c3.SCL	I/O	Camera control I²C
93	I2C_4_CSI_SDA	I2C3_SDA	i2c3.SDA	O	
91	CSI_1_MCLK	SAI3_MCLK	sai3.MCLK	O	Camera master clock. Source: audio master clock of SAI5 or SAI3
			sai5.MCLK		

5.8 PCI Express

The NXP i.MX 8M Mini features a single lane PCI Express (PCIe) interface. The PCIe interface is compliant with the PCIe 4.0 base specifications and supports up to 16Gb/s data rate (Gen4). It is backward-compatible with previous standards that support 8Gb/s (Gen3), 5Gb/s (Gen2), and 2.5Gb/s (Gen1).

The 100MHz PCIe reference clock is generated by the SoC and is made available for the peripherals over the module edge connector pins. All the required source termination for the reference clock is on the Verdin module.

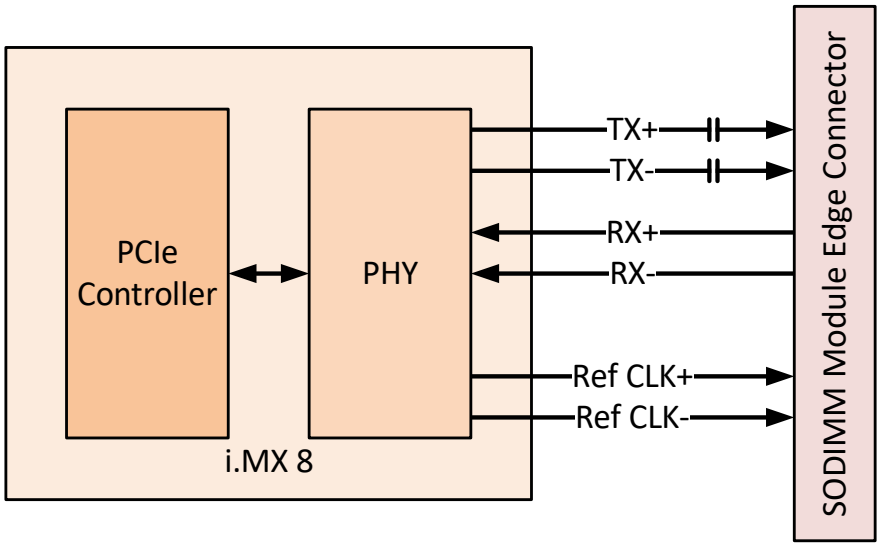

Figure 11: PCIe block diagram

PCIe is a high-speed interface that needs special layout requirements to be followed. Please carefully study the Verdin Carrier Board Design Guide and Layout Design Guide for more information.

Table 5-16 PCIe Interface Signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
228	PCIE_1_CLK_P	PCIE_CLK_P	PCIE_CLK_P	O	100MHz reference clock differential pair. Sourced by a reference clock oscillator
226	PCIE_1_CLK_N	PCIE_CLK_N	PCIE_CLK_N		
240	PCIE_1_L0_TX_P	PCIE_TXN_P	PCIE_TXN_P	O	Transmit data lane 0
238	PCIE_1_L0_TX_N	PCIE_TXN_N	PCIE_TXN_N		
234	PCIE_1_L0_RX_P	PCIE_RXN_P	PCIE_RXN_P	I	Receive data lane 0
232	PCIE_1_L0_RX_N	PCIE_RXN_N	PCIE_RXN_N		
244	PCIE_1_RESET#	SAI5_RXFS	gpio3.IO[19]	O	Dedicated reset output for PCIe

5.9 I²C

The NXP i.MX 8M Mini SoC features four I²C controllers; three of which can be used externally. They implement the I²C V2.1 specification. The port I2C1 is used for the on-module PMIC, RTC, EEPROM, Secure Element, and ADC and is therefore not available externally.

All three externally available I²C can be used for general purpose applications. However, the Verdin standard dedicates two of them for use with the MIPI CSI-2 camera and the MIPI DSI display output. The Verdin standard reserves a fourth I²C interface as *"Reserved"* which is dedicated to the HDMI port. Since the Verdin iMX8M Mini does not have an HDMI interface, the associated I²C is left unconnected on the module.

There are many low-speed devices that use I²C interfaces such as RTCs and sensors, but it is also commonly used to configure other devices such as cameras or displays. The I²C Bus can also be used to communicate with SMB (System Management Bus) devices.

Table 5-17 Verdin standard I²C Signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I2C Port	Description
14	I2C_1_SCL	I2C4_SCL	i2c4.SCL	I2C4	Generic I²C
12	I2C_1_SDA	I2C4_SDA	i2c4.SDA		
55	I2C_2_DSI_SCL	I2C2_SCL	i2c2.SCL	I2C2	I²C port for the DSI interface. Intended to be used as DDC or for controlling DSI bridges on carrier board.
53	I2C_2_DSI_SDA	I2C2_SDA	i2c2.SDA		
59	I2C_3_HDMI_SCL				Not available on Verdin iMX8M Mini
57	I2C_3_HDMI_SDA				
95	I2C_4_CSI_SCL	I2C3_SCL	i2c3.SCL	I2C4	I²C port for the camera interface
93	I2C_4_CSI_SDA	I2C3_SDA	i2c3.SDA		

5.9.1 Real-Time Clock (RTC)

The Verdin iMX8M Mini module features an RTC IC on the module. The RTC is equipped with an accurate 32.768 kHz quartz crystal and can be used for timekeeping. If the main power supply is provided to the module, the RTC is sourced from this rail. However, If the RTC needs to be retained even without the module's main voltage, a coin cell needs to be applied to the VCC_BACKUP (pin 249) supply pin.

5.10 UART

The i.MX 8MM SoC features a total of four UARTs. In the Verdin module specifications, there are four standard UARTs available. UART_1 and UART_2 are general-purpose interfaces. Only the RX and TX signals of these interfaces are in the *"Always Compatible"* section while the additional RTS/CTS signals for hardware flow control are located in the *"Reserved"* section.

UART_3 is in the *"Always Compatible"* section and is intended to be used for the main OS terminal (A53 cores) as a debug port. It could be used for general purposes, but we recommend making this interface available for debugging purposes. UART_4 is in the *"Reserved"* class. This interface is intended to be used for the real-time operating system (M4 core). The interface may be used as general-purpose UART.

The UARTs of the i.MX 8MM SoC can be configured either in the DTE (Data Terminal Equipment) or DCE (Data Communication Equipment) mode. Changing the mode will change the direction of all UART pins (data and all control signals). To ensure compatibility with the entire Verdin family, the

SoC needs to be configured in **DCE** mode, even though in the Verdin standard the data direction is defined in DTE mode.

Particular attention should be paid to the names of the i.MX 8MM data signals. In the correct DTE mode, TX and RTS signals are outputs while the RX and CTS signals are inputs. In DCE mode, all signals change their direction. Unfortunately, the data directions of the i.MX 8MM SoC are mixed up. In DCE mode, TX and CTS signals are outputs while RX and RTS are inputs. In DTE mode, RX and RTS are outputs and TX and CTS are inputs. Therefore, the SoC must be set to DCE mode with the RTS and CTS signals swapped on the module. This means the SoC signal UARTx_CTS_B is connected to the UART_x_RTS edge connector pin and vice versa.

Table 5-18 *"Always Compatible"* UART Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
129	UART_1_RXD	SAI3_TXFS	uart2.RX	I	Received Data of general purpose UART_1
131	UART_1_TXD	SAI3_TXC	uart2.TX	O	Transmitted Data of general purpose UART_1
137	UART_2_RXD	ECSPI1_SCLK	uart3.RX	I	Received Data of general purpose UART_2
139	UART_2_TXD	ECSPI1_MOSI	uart3.TX	O	Transmitted Data of general purpose UART_2
147	UART_3_RXD	SAI2_RXC	uart1.RX	I	Received Data of A53 debug UART_3
149	UART_3_TXD	SAI2_RXFS	uart1.TX	O	Transmitted Data of A53 debug UART_3

Table 5-19 *"Reserved"* UART Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
133	UART_1_RTS	SAI3_RXC	uart2.CTS_B	O	Request to Send of general purpose UART_1
135	UART_1_CTS	SAI3_RXD	uart2.RTS_B	I	Clear to Send of general purpose UART_1
141	UART_2_RTS	ECSPI1_MISO	uart3.CTS_B	O	Request to Send of general purpose UART_2
143	UART_2_CTS	ECSPI1_SS0	uart3.RTS_B	I	Clear to Send of general purpose UART_2
151	UART_4_RXD	UART4_RXD	uart4.RX	I	Received Data of M4 debug UART_4
153	UART_4_TXD	UART4_TXD	uart4.TX	O	Transmitted Data of M4 debug UART_4

In addition to the UART signals that are in the *"Always Compatible"* and *"Reserved"* class, there are UART signals available as alternate functions of other pins. These pins are not compatible with other Verdin modules. Therefore, they should be used very carefully.

Table 5-20 Alternate Function UART Signal Pins (not compatible)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
151	UART_4_RXD	UART4_RXD	uart2.CTS_B	O	Request to Send of general purpose UART_1
153	UART_4_TXD	UART4_TXD	uart2.RTS_B	I	Clear to Send of general purpose UART_1
210	GPIO_3	UART3_RXD	uart3.RX	O	Received Data of general purpose UART_2
212	GPIO_4	UART3_TXD	uart3.TX	I	Transmitted Data of general purpose UART_2
32	I2S_1_SYNC	SAI2_TXFS	uart1.CTS_B	O	Request to Send of A53 debug UART_3
210	GPIO_3	UART3_RXD			
36	I2S_1_D_IN	SAI2_RXD0	uart1.RTS_B	I	Clear to Send of A53 debug UART_3
212	GPIO_4	UART3_TXD			
196	SPI_1_CLK	ECSPI2_SCLK	uart4.RX	I	Received Data of M4 debug UART_4
200	SPI_1_MOSI	ECSPI2_MOSI	uart4.TX	O	Transmitted Data of M4 debug UART_4

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
198	SPI_1_MISO	ECSPI2_MISO	uart4.CTS_B	O	Request to Send of M4 debug UART_4
202	SPI_1_CS	ECSPI2_SS0	uart4.RTS_B	I	Clear to Send of M4 debug UART_4

5.11 SPI

The i.MX 8MM SoC features a total of three SPI interfaces. These interfaces are called Enhanced Configurable Serial Peripheral Interface (ECSPI) in the NXP documentation. One of the SPI interfaces is available on the Verdin module as an *"Always Compatible"* interface. A second SPI is available as an alternate function of other interface pins. The third SPI is used for the internal CAN controllers and therefore it is only available on the module edge connector pins for modules without a CAN interface.

The SPI ports operate at up to 52 Mbps and provide full duplex, synchronous, serial communication between the Verdin module and internal or external peripheral devices.

In the Verdin module standard, only the SPI master mode is specified. Therefore, the slave mode might not be compatible with other modules. The signal direction in the following tables corresponds to the SPI master mode.

Table 5-21 *"Always Compatible"* SPI Port Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
200	SPI_1_MOSI	ECSPI2_MOSI	ecspi2.MOSI	O	Master Output, Slave Input
198	SPI_1_MISO	ECSPI2_MISO	ecspi2.MISO	I	Master Input, Slave Output
202	SPI_1_CS	ECSPI2_SS0	ecspi2.SS0	I/O	Slave Select
196	SPI_1_CLK	ECSPI2_SCLK	ecspi2.SCLK	I/O	Serial Clock

Table 5-22 Alternate Function SPI Port Signal Pins (not compatible)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
139	UART_2_TXD	ECSPI1_MOSI	ecspi1.MOSI	O	Master Output, Slave Input
141	UART_2_RTS	ECSPI1_MISO	ecspi1.MISO	I	Master Input, Slave Output
143	UART_2_CTS	ECSPI1_SS0	ecspi1.SS0	I/O	Slave Select
137	UART_2_RXD	ECSPI1_SCLK	ecspi1.SCLK	I/O	Serial Clock

Table 5-23 Additional SPI Port Signal Pins (only available on modules without CAN interface)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
26	CAN_2_RX	UART1_TXD	ecspi3.MOSI	O	Master Output, Slave Input
20	CAN_1_TX	UART2_RXD	ecspi3.MISO	I	Master Input, Slave Output
24	CAN_2_TX	UART2_TXD	ecspi3.SS0	I/O	Slave Select
22	CAN_1_RX	UART1_RXD	ecspi3.SCLK	I/O	Serial Clock

5.12 Quad Serial Peripheral Interface (QuadSPI, QSPI)

In addition to the regular SPI controller (which is called ECSPI in the NXP documentation), the i.MX 8MM features a Flexible SPI Controller (FlexSPI) with up to two SPI channels. The controller supports single, dual, quad, and octal mode data transfer. For the octal mode, both four-bit SPI channels are combined. It can be used for interfacing NAND and NOR flashes with QuadSPI interfaces. Additionally, it can also be used for interfacing HyperBus and FPGA devices.

The Verdin standard offers one QuadSPI with two chip selects for up to two memory devices in the *"Reserved"* pin class. The second QuadSPI channel is only available on modules without Wi-Fi since the interface is located on alternate pins of the Wi-Fi SDIO interface.

Table 5-24 QSPI Modes

i.MX 8MM Function	Single Mode	Dual Mode	Quad Mode	Octal Mode
A_SCLK	SCLK (Flash A1 and A2)	SCLK (Flash A1 and A2)	SCLK (Flash A1 and A2)	SCLK (Flash A1 and A2)
A_SS0_B	SS_B (Flash A1)	SS_B (Flash A1)	SS_B (Flash A1)	SS_B (Flash A1)
A_SS1_B	SS_B (Flash A2)	SS_B (Flash A2)	SS_B (Flash A2)	SS_B (Flash A2)
A_DATA[0]	MOSI (Flash A1 and A2)	DATA0 (Flash A1 and A2)	DATA0 (Flash A1 and A2)	DATA0 (Flash A1 and A2)
A_DATA[1]	MISO (Flash A1 and A2)	DATA1 (Flash A1 and A2)	DATA1 (Flash A1 and A2)	DATA1 (Flash A1 and A2)
A_DATA[2]			DATA2 (Flash A1 and A2)	DATA2 (Flash A1 and A2)
A_DATA[3]			DATA3 (Flash A1 and A2)	DATA3 (Flash A1 and A2)
B_SCLK	SCLK (Flash B1 and B2)	SCLK (Flash B1 and B2)	SCLK (Flash B1 and B2)	
B_SS0_B	SS_B (Flash B1)	SS_B (Flash B1)	SS_B (Flash B1)	
B_SS1_B	SS_B (Flash B2)	SS_B (Flash B2)	SS_B (Flash B2)	
B_DATA[0]	MOSI (Flash B1 and B2)	DATA0 (Flash B1 and B2)	DATA0 (Flash B1 and B2)	DATA4 (Flash A1 and A2)
B_DATA[1]	MISO (Flash B1 and B2)	DATA1 (Flash B1 and B2)	DATA1 (Flash B1 and B2)	DATA5 (Flash A1 and A2)
B_DATA[2]			DATA2 (Flash B1 and B2)	DATA6 (Flash A1 and A2)
B_DATA[3]			DATA3 (Flash B1 and B2)	DATA7 (Flash A1 and A2)

Table 5-25 QSPI Signal Pins (in *"Reserved"* class)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
54	QSPI_1_CS#	NAND_CE0_B	qspi.A_SS0_B	O	Chip Select 0
64	QSPI_1_CS2#	NAND_CE1_B	qspi.A_SS1_B	O	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
52	QSPI_1_CLK	NAND_ALE	qspi.A_SCLK	O	Serial Clock
56	QSPI_1_IO0	NAND_DATA00	qspi.A_DATA[0]	I/O	Serial I/O for command, address, and data
58	QSPI_1_IO1	NAND_DATA01	qspi.A_DATA[1]	I/O	Serial I/O for command, address, and data
60	QSPI_1_IO2	NAND_DATA02	qspi.A_DATA[2]	I/O	Serial I/O for command, address, and data
62	QSPI_1_IO3	NAND_DATA03	qspi.A_DATA[3]	I/O	Serial I/O for command, address, and data
66	QSPI_1_DQS	NAND_DQS	qspi.A_DQS	I	Data Strobe signal, required on some high-speed DDR devices

Table 5-26 Second QSPI Channel Signal Pins (not available on modules with Wi-Fi, not compatible with other modules)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
21	GPIO_10_DSI	NAND_CE2_B	21	O	Chip Select 0
206	GPIO_1	NAND_CE3_B	206	O	Chip Select 1, used to select second instance of QuadSPI device (dual die flash require CS0 and CS1)
76	SD_1_PWR_EN	NAND_CLE	76	O	Serial Clock
162	MSP_32	NAND_DATA04	162	I/O	Serial I/O for command, address, and data
164	MSP_33	NAND_DATA05	164	I/O	Serial I/O for command, address, and data
166	MSP_34	NAND_DATA06	166	I/O	Serial I/O for command, address, and data
168	MSP_35	NAND_DATA07	168	I/O	Serial I/O for command, address, and data
17	GPIO_9_DSI	NAND_RE_B	17	I	Data Strobe signal, required on some high-speed DDR devices

5.13 PWM (Pulse Width Modulation)

The i.MX 8MM features a four-channel general-purpose Pulse Width Modulator (PWM). It has a 16-bit counter and is optimized to generate simple sound samples as well as generate tones. It has 16-bit resolution and there is a 4-level deep FIFO available in order to minimize the interrupt overhead. There is a 12-bit pre-scaler available for dividing the clock.

There are 3 PWM signals on the Verdin standard. PWM_1 is the only one in the *"Always Compatible"* class. Both PWM_1 and PWM_2 are general-purpose pulse with modulation outputs. The third interface is dedicated to the DSI output for the display backlight inverter control. The fourth PWM output of the i.MX 8MM SoC is available as an alternate function. Therefore, it is advised to prioritize the other PWM pins over the fourth one since it is not guaranteed that the pin is compatible with other modules.

Table 5-27 PWM Interface Signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
15	PWM_1	SPDIF_RX	pwm2.OUT	O	General purpose PWM *"Always Compatible"*
16	PWM_2	SPDIF_TX	pwm3.OUT	O	General purpose PWM *"Reserved"*
19	PWM_3_DSI	GPIO1_IO01	pwm1.OUT	O	Dedicated PWM for display backlight *"Reserved"*
187	USB_2_OC#	GPIO1_IO15	pwm4.OUT	O	Additional general purpose PWM *Alternate Function (not compatible)*

5.14 SD/MMC

The i.MX 8MM SoC provides three SDIO interfaces. One is used internally for the eMMC Flash. A second one is available on the module edge connector pins as *"Always Compatible"* Verdin SD Memory Card Interface. The third interface is used for the Wi-Fi and Bluetooth module. The interfaces are capable of interfacing with SD Memory Cards, SDIO, MMC, and eMMC devices. For Verdin modules without wireless features, the third SD interface is available on the *"Module-specific"* pins. Since this extra SD interface features only 1.8V (and regular SD cards need to start

the negotiation with 3.3V) the port can only be used for permanently attached devices like eMMC memory or an SDIO peripheral.

i.MX 8MM SDIO interface	Max Bus Width	Description
USDHC1	8-bit	Connected to internal eMMC boot device. Not available at the module edge connector
USDHC2	4-bit	*"Always Compatible"* Verdin SD interface
USDHC3	4-bit	Used for the on-module Wi-Fi and Bluetooth interface
	8-bit	Available on *"Module-specific"* pins and on alternate functions only on modules without Wi-Fi/Bluetooth. IO voltage level is 1.8V, therefore interface can only be used for eMMC and SDIO peripherals.

Features:

- Supports SD Memory Card Specification 2.0 and 3.0
- Supports SDIO Card Specification Version 2.0 and 3.0
- Supports MMC System Specification Version 4.2, 4.3, 4.4, 4.41, 5.0, and 5.1
- Supports addressing larger capacity SD 3.0 or SDXC cards up to 2 TB
- Supports SPI mode
- Supports SD UHS-I mode (up to 208MHz) with 1.8V IO voltage level.
- 3.3V and 1.8V IO voltage mode supported (only for USDHC2 port)

For being compliant with SD Memory Cards, the 3.3V IO voltage level needs to be supported. For higher bus speed in the UHS-I class, additional to the 3.3V, also 1.8V IO voltage level needs to be supported as well. Additionally, the interface needs to be able to switch between these two voltage levels. The SD interface in the *"Always Compatible"* class supports both IO voltage levels. No external pull-up resistors are required on the carrier board. There are pull-up resistors on the module.

On Verdin iMX8M Mini modules without the Wi-Fi and Bluetooth function, the third SDIO interface of the i.MX 8MM SoC is available. The main interface signals for the 4-bit interface are available on *"Module-specific"* interface pins while the rest of the signals are available on alternate functions of other interface pins. This SDIO interface only supports the 1.8V logic level. This makes the interface not compatible with SD Memory Card specifications. However, it is possible to use the interface for non-removable SDIO devices or eMMC flash memory.

Table 5-28 *SD Card Speed Modes (applicable only for USDHC2)*

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MB/s	3.3V	
High Speed	50 MHz	25 MB/s	3.3V	
SDR12	25 MHz	12.5 MB/s	1.8V	
SDR25	50 MHz	25 MB/s	1.8V	
DDR50	50 MHz	50 MB/s	1.8V	UHS-I
SDR50	100 MHz	50 MB/s	1.8V	
SDR104	208 MHz	104 MB/s	1.8V	

The IO voltage of the SDIO power block can be changed independently from the other IO blocks, but all signals of the SDIO block change their voltages together. The IO voltage of the Verdin *"Always Compatible"* interface (i.MX 8MM USDHC2) is provided by the LDO5 output of the power management IC (PMIC). The voltage level is controlled by the dedicated VSELECT output of the USDHC2 interface which is located on the GPIO1_IO04 ball of the SoC.

Table 5-29 *"Always Compatible"* SD Card Interface Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Voltage	Description
74	SD_1_CMD	SD2_CMD	usdhc2.CMD	I/O	3.3/1.8V	Command, 47kΩ pull-up resistor on module
80	SD_1_D0	SD2_DATA0	usdhc2.DATA0	I/O	3.3/1.8V	Serial Data 0, 47kΩ pull-up resistor on module
82	SD_1_D1	SD2_DATA1	usdhc2.DATA1	I/O	3.3/1.8V	Serial Data 1, 47kΩ pull-up resistor on module
70	SD_1_D2	SD2_DATA2	usdhc2.DATA2	I/O	3.3/1.8V	Serial Data 2, 47kΩ pull-up resistor on module
72	SD_1_D3	SD2_DATA3	usdhc2.DATA3	I/O	3.3/1.8V	Serial Data 3, 47kΩ pull-up resistor on module
78	SD_1_CLK	SD2_CLK	usdhc2.CLK	O	3.3/1.8V	Serial Clock
84	SD_1_CD#	SD2_CD_B	usdhc2.CD_B	I	3.3/1.8V	Card Detect, 10kΩ pull-up resistor on module
76	SD_1_PWR_EN	NAND_CLE	gpio3.IO[5]	O	1.8V	Enable pin for SD card power rail. Regular GPIO pin which does not change IO voltage level with the rest of the SD card signal pins

Table 5-30 Secondary SD Card Interface Signal Pins (only available on modules without Wi-Fi)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Voltage	Description
160	MSP_31	NAND_WP_B	usdhc3.CMD	I/O	1.8V	Command
162	MSP_32	NAND_DATA04	usdhc3.DATA0	I/O	1.8V	Serial Data 0
164	MSP_33	NAND_DATA05	usdhc3.DATA1	I/O	1.8V	Serial Data 1
166	MSP_34	NAND_DATA06	usdhc3.DATA2	I/O	1.8V	Serial Data 2
168	MSP_35	NAND_DATA07	usdhc3.DATA3	I/O	1.8V	Serial Data 3
17	GPIO_9_DSI	NAND_RE_B	usdhc3.DATA4	I/O	1.8V	Serial Data 4
21	GPIO_10_DSI	NAND_CE2_B	usdhc3.DATA5	I/O	1.8V	Serial Data 5
206	GPIO_1	NAND_CE3_B	usdhc3.DATA6	I/O	1.8V	Serial Data 6
76	SD_1_PWR_EN	NAND_CLE	usdhc3.DATA7	I/O	1.8V	Serial Data 7
156	MSP_30	NAND_WE_B	usdhc3.CLK	O	1.8V	Serial Clock
185	USB_2_EN	GPIO1_IO14	usdhc3.CD_B	I	1.8V	Card Detect
210	GPIO_3	UART3_RXD	usdhc3.RESET_B	O	1.8V	Dedicated reset output
64	QSPI_1_CS2#	NAND_CE1_B	usdhc3.STROBE	I	1.8V	Input clock for eMMC HS400 mode
187	USB_2_OC#	GPIO1_IO15	usdhc3.WP	I	1.8V	Card write protect

5.15 Digital Audio Interfaces

The i.MX 8MM SoC features five Synchronous Audio Interfaces (SAI). The SAI interfaces can be used as I²S (also known as Inter-IC Sound, Integrated Interchip Sound or IIS) or as Intel® Audio Codec '97 (also known as AC'97 or AC97). The Verdin standard defines two I²S interfaces in the *"Reserved"* pin class. Since AC'97 is not part of the Verdin standard, it is recommended to use I²S for better compatibility with other Verdin modules. In addition to the two standard I²S interfaces, another I²S is connected to the Wi-Fi module for Bluetooth audio features. The following table provides an overview of the SAI interfaces. Please note the numbering of the SAI ports in the SoC. The ports are numbered from 1 to 3 and from 5 to 6. SAI port 4 does not exist.

Table 5-31 SAI Instance Configuration

Instance	Tx/Rx Data Lines (stereo)	Max. Sampling Rate	Use Case
SAI1	8/8	384KHz/32-bit	Available on module edge connector as alternate function.
SAI2	2/2	768KHz/32-bit	Available as Verdin standard I2S_1 interface
SAI3	2/2	768KHz/32-bit	Available on module edge connector as alternate function.
SAI5	4/4	384KHz/32-bit	Available as Verdin standard I2S_2 interface
SAI6	1/1	384KHz/32-bit	Connected to the Wi-Fi/Bluetooth module. Available on *"Module-specific"* pins for modules without radio.
SPDIF-1	1/1		Available on module edge connector as an alternate function.
PDM	0/4		PDM Microphone Interface. Available on module edge connector as an alternate function.

The SAI interfaces support word sizes of between 8-bits and 32-bit. Some instances support up to 8 RX and 8 TX lines. However, not all combinations are possible due to limitations in the pin multiplexing. The Toradex Pinout Designer tool can help check the pin multiplexing, especially for the alternate functions which are not standard in the Verdin specifications. Each transmit and receive data line features an asynchronous 128x32-bit FIFO that provides an automatic graceful restart after FIFO error without software intervention.

Table 5-32 Standard Digital Audio Port Signals (compatible with other modules)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
36	I2S_1_D_IN	SAI2_RXD0	sai2.RX_DATA[0]	I	Data Input to i.MX 8MM
34	I2S_1_D_OUT	SAI2_TXD0	sai2.TX_DATA[0]	O	Data Output from i.MX 8MM
32	I2S_1_SYNC	SAI2_TXFS	sai2.TX_SYNC	I/O	Field Select (Transmit Frame Sync)
30	I2S_1_BCLK	SAI2_TXC	sai2.TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
38	I2S_1_MCLK	SAI2_MCLK	sai2.MCLK	O	Master clock output.
48	I2S_2_D_IN	SAI5_RXD0	sai5.RX_DATA[0]	I	Data Input to i.MX 8MM
46	I2S_2_D_OUT	SAI5_RXD3	sai5.TX_DATA[0]	O	Data Output from i.MX 8MM
44	I2S_2_SYNC	SAI5_RXD1	sai5.TX_SYNC	I/O	Field Select (Transmit Frame Sync)
42	I2S_2_BCLK	SAI5_RXD2	sai5.TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)

For controlling the I²S codec, an additional I²C interface may be required, and the generic I²C interface I2C_1is recommended for this purpose. There are alternate multiplexings available for the SAI ports that are used as standard Verdin I²S interfaces. These signals are available as alternate functions of other interfaces. Therefore, they are not compatible with other Verdin modules and should be used with care.

Table 5-33 Additional Multiplexings for I2S_1 (SAI2) Standard Digital Audio Port

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
149	UART_3_TXD	SAI2_RXFS	sai2.RX_DATA[1]	I	Data Input to i.MX 8MM
32	I2S_1_SYNC	SAI2_TXFS	sai2.TX_DATA[1]	O	Data Output from i.MX 8MM
149	UART_3_TXD	SAI2_RXFS	sai2.RX_SYNC	I/O	Field Select (Receive Frame Sync)
147	UART_3_RXD	SAI2_RXC	sai2.RX_BCLK	I/O	Serial Clock (Receive Bit Clock)

Table 5-34 Additional Multiplexing for I2S_2 (SAI5) Standard Digital Audio Port

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
92	MSP_3	SAI1_RXD0	sai5.RX_DATA[0]	I	Alternate Data Input to i.MX 8MM
135	UART_1_CTS	SAI3_RXD			
44	I2S_2_SYNC	SAI5_RXD1	sai5.RX_DATA[1]	I	Data Input to i.MX 8MM
94	MSP_4	SAI1_RXD1			
129	UART_1_RXD	SAI3_TXFS			
42	I2S_2_BCLK	SAI5_RXD2	sai5.RX_DATA[2]	I	Data Input to i.MX 8MM
96	MSP_5	SAI1_RXD2			
131	UART_1_TXD	SAI3_TXC			
46	I2S_2_D_OUT	SAI5_RXD3	sai5.RX_DATA[3]	I	Data Input to i.MX 8MM
100	MSP_6	SAI1_RXD3			
102	MSP_7	SAI1_RXFS	sai5.RX_SYNC	I/O	Field Select (Receive Frame Sync)
244	PCIE_1_RESET#	SAI5_RXFS			
252	CTRL_WAKE1_MICO#	SAI3_RXFS			
90	MSP_2	SAI1_RXC	sai5.RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
133	UART_1_RTS	SAI3_RXC			
36	I2S_1_D_IN	SAI2_RXD0	sai5.TX_DATA[0]	O	Alternate Data Output from i.MX 8MM
106	MSP_9	SAI1_TXD0			
32	I2S_1_SYNC	SAI2_TXFS	sai5.TX_DATA[1]	O	Data Output from i.MX 8MM
108	MSP_10	SAI1_TXD1			
149	UART_3_TXD	SAI2_RXFS			
30	I2S_1_BCLK	SAI2_TXC	sai5.TX_DATA[2]	O	Data Output from i.MX 8MM
112	MSP_11	SAI1_TXD2			
34	I2S_1_D_OUT	SAI2_TXD0	sai5.TX_DATA[3]	O	Data Output from i.MX 8MM
114	MSP_12	SAI1_TXD3			
120	MSP_15	SAI1_TXFS	sai5.TX_SYNC	I/O	Alternate Field Select (Transmit Frame Sync)
149	UART_3_TXD	SAI2_RXFS			
104	MSP_8	SAI1_TXC	sai5.TX_BCLK	I/O	Alternate Serial Clock (Transmit Bit Clock)
147	UART_3_RXD	SAI2_RXC			
38	I2S_1_MCLK	SAI2_MCLK	sai5.MCLK	O	Master clock output.
88	MSP_1	SAI1_MCLK			
91	CSI_1_MCLK	SAI3_MCLK			

In addition to the two SAI interfaces that are available as standard I²C interfaces, there are other SAI instances available as alternate functions of other interfaces. These signals are not compatible with other Verdin modules. Carefully check the pin multiplexing since not all combinations are possible.

Table 5-35 SAI1 Signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
92	MSP_3	SAI1_RXD0	sai1.RX_DATA[0]	I	Data Input to i.MX 8MM
94	MSP_4	SAI1_RXD1	sai1.RX_DATA[1]	I	Data Input to i.MX 8MM
96	MSP_5	SAI1_RXD2	sai1.RX_DATA[2]	I	Data Input to i.MX 8MM
100	MSP_6	SAI1_RXD3	sai1.RX_DATA[3]	I	Data Input to i.MX 8MM
148	MSP_26	SAI1_RXD4	sai1.RX_DATA[4]	I	Data Input to i.MX 8MM
152	MSP_28	SAI1_RXD5	sai1.RX_DATA[5]	I	Data Input to i.MX 8MM
154	MSP_29	SAI1_RXD6	sai1.RX_DATA[6]	I	Data Input to i.MX 8MM
174	MSP_37	SAI1_RXD7	sai1.RX_DATA[7]	I	Data Input to i.MX 8MM
102	MSP_7	SAI1_RXFS	sai1.RX_SYNC	I/O	Field Select (Receive Frame Sync)
152	MSP_28	SAI1_RXD5			
90	MSP_2	SAI1_RXC	sai1.RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
106	MSP_9	SAI1_TXD0	sai1.TX_DATA[0]	O	Data Output from i.MX 8MM
244	PCIE_1_RESET#	SAI5_RXFS			
92	MSP_3	SAI1_RXD0	sai1.TX_DATA[1]	O	Data Output from i.MX 8MM
108	MSP_10	SAI1_TXD1			
48	I2S_2_D_IN	SAI5_RXD0	sai1.TX_DATA[2]	O	Data Output from i.MX 8MM
112	MSP_11	SAI1_TXD2			
44	I2S_2_SYNC	SAI5_RXD1	sai1.TX_DATA[3]	O	Data Output from i.MX 8MM
114	MSP_12	SAI1_TXD3			
42	I2S_2_BCLK	SAI5_RXD2	sai1.TX_DATA[4]	O	Data Output from i.MX 8MM
116	MSP_13	SAI1_TXD4			
174	MSP_37	SAI1_RXD7			
46	I2S_2_D_OUT	SAI5_RXD3	sai1.TX_DATA[5]	O	Data Output from i.MX 8MM
150	MSP_27	SAI1_TXD5			
118	MSP_14	SAI1_TXD6	sai1.TX_DATA[6]	O	Data Output from i.MX 8MM
42	I2S_2_BCLK	SAI5_RXD2	sai1.TX_SYNC	I/O	Field Select (Transmit Frame Sync)
44	I2S_2_SYNC	SAI5_RXD1			
46	I2S_2_D_OUT	SAI5_RXD3			
120	MSP_15	SAI1_TXFS			
174	MSP_37	SAI1_RXD7			
88	MSP_1	SAI1_MCLK	sai1.TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
104	MSP_8	SAI1_TXC			
88	MSP_1	SAI1_MCLK	sai1.MCLK	O	Master clock output.

Table 5-36 SAI3 Signals

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
135	UART_1_CTS	SAI3_RXD	sai3.RX_DATA[0]	I	Data Input to i.MX 8MM
252	CTRL_WAKE1_MICO#	SAI3_RXFS	sai3.RX_DATA[1]	I	Data Input to i.MX 8MM
252	CTRL_WAKE1_MICO#	SAI3_RXFS	sai3.RX_SYNC	I/O	Field Select (Receive Frame Sync)
133	UART_1_RTS	SAI3_RXC	sai3.RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
129	UART_1_RXD	SAI3_TXFS	sai3.TX_DATA[1]	O	Data Output from i.MX 8MM
129	UART_1_RXD	SAI3_TXFS	sai3.TX_SYNC	I/O	Field Select (Transmit Frame Sync)
131	UART_1_TXD	SAI3_TXC	sai3.TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
91	CSI_1_MCLK	SAI3_MCLK	sai3.MCLK	O	Master clock output.

Table 5-37 SAI6 Signals (not available on modules with Wi-Fi/Bluetooth)

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
150	MSP_27	SAI1_TXD5	sai6.RX_DATA[0]	I	Data Input to i.MX 8MM
152	MSP_28	SAI1_RXD5			
118	MSP_14	SAI1_TXD6	sai6.RX_SYNC	I/O	Field Select (Receive Frame Sync)
154	MSP_29	SAI1_RXD6			
116	MSP_13	SAI1_TXD4	sai6.RX_BCLK	I/O	Serial Clock (Receive Bit Clock)
148	MSP_26	SAI1_RXD4			
150	MSP_27	SAI1_TXD5	sai6.TX_DATA[0]	O	Data Output from i.MX 8MM
152	MSP_28	SAI1_RXD5			
118	MSP_14	SAI1_TXD6	sai6.TX_SYNC	I/O	Field Select (Transmit Frame Sync)
154	MSP_29	SAI1_RXD6			
116	MSP_13	SAI1_TXD4	sai6.TX_BCLK	I/O	Serial Clock (Transmit Bit Clock)
148	MSP_26	SAI1_RXD4			
174	MSP_37	SAI1_RXD7	sai6.MCLK	O	Master clock output.

5.15.1 Synchronous Audio Interface used as I²S

The SAI can be used as I²S interfaces which is the default use case for the Verdin standard. The interface supports either master or slave mode. In the Verdin standard, the master configuration is most compatible with other modules. Therefore, it is the preferred configuration. The following signals are used for a simple I²S interface:

Table 5-38 Synchronous Audio Interface used as Maser I2S

i.MX 8MM Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 8MM
SAIx.RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 8MM
SAIx.TX_SYNC	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx.TX_BCLK	SCK	I/O	Serial Continuous Clock

Table 5-39 Synchronous Audio Interface used as Slave I²S

i.MX 8MM Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.RX_DATA[0]	SDOUT	I	Serial Data Input to i.MX 8MM
SAIx.TX_DATA[0]	SDIN	O	Serial Data Output from i.MX 8MM
SAIx.RX_SYNC	WS	I/O	Word Select, also known as Field Select or LRCLK
SAIx.RX_BCLK	SCK	I/O	Serial Continuous Clock

5.15.2 Synchronous Audio Interface used as AC'97

The SAI interface can be configured as an AC'97 compatible interface. The AC'97 Audio interface does not need an additional I²C for the control communication. The codec is controlled directly through the AC'97 Audio interface. The AC'97 Audio codec does require a master reference clock. This can be either one of the SAI master clock outputs or a separate crystal/oscillator can be used. Please take care of the pin naming of some codecs. Some devices name their data input pin as SDATA_OUT and the data output pin as SDATA_IN. The names refer to the signals they should be connected to on the host, and not to the signal direction.

Table 5-40 Synchronous Audio Interface used as AC'97

i.MX 8MM Port Name	I²S Signal Name (Names at Codec)	I/O (at SoC)	Description
SAIx.RX_DATA[0]	SDATA_IN	I	AC'97 Audio Serial Input to i.MX 8MM
SAIx.TX_DATA[0]	SDATA_OUT	O	AC'97 Audio Serial Output from i.MX 8MM
SAIx.TX_SYNC	SYNC	O	AC'97 Audio Sync
SAIx.TX_BCLK	BIT_CLK	I	AC'97 Audio Bit Clock
GPIOx	RESET#	O	AC'97 Master H/W Reset (use any GPIO)

5.15.3 PDM Microphone Interface

The i.MX 8M Mini SoC features up to four PDM microphone input signals. PDM stands for Pulse-Density Modulation and is a popular digital interface for delivering audio from microphones to the SoC. The PDM bit stream is time-multiplexed and contains audio information in two channels (left and right). This means a total of eight microphones can be attached to the PDM interface of the i.MX 8M Mini.

Since the PDM is not a standard interface of Verdin, these signals are available only as alternate functions. Therefore, the PDM microphone interface is not compatible with other Verdin Modules.

Table 5-41 PDM Microphone Interface Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
48	I2S_2_D_IN	SAI5_RXD0	pdm.BIT_STREAM[0]	I	Stereo PDM microphone stream
92	MSP_3	SAI1_RXD0			
44	I2S_2_SYNC	SAI5_RXD1	pdm.BIT_STREAM[1]	I	Stereo PDM microphone stream
94	MSP_4	SAI1_RXD1			
42	I2S_2_BCLK	SAI5_RXD2	pdm.BIT_STREAM[2]	I	Stereo PDM microphone stream
96	MSP_5	SAI1_RXD2			
46	I2S_2_D_OUT	SAI5_RXD3	pdm.BIT_STREAM[3]	I	Stereo PDM microphone stream
100	MSP_6	SAI1_RXD3			
88	MSP_1	SAI1_MCLK	pdm.CLK	O	Clock output for microphones

5.15.4 S/PDIF (Sony-Philips Digital Interface)

The S/PDIF interface supports both input and output. The input controller can digitally recover a clock from the received stream. The controller conforms to the AES/EBU IEC 60958 standard.

The S/PDIF interface is not part of the Verdin standard. Therefore, the signals are available as alternate functions of other interface pins. This means the S/PDIF is not compatible with other Verdin modules.

Table 5-42 S/PDIF Data Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
16	PWM_2	SPDIF_TX	spdif1.OUT	O	Serial data output
15	PWM_1	SPDIF_RX	spdif1.IN	I	Serial data input
208	GPIO_2	SPDIF_EXT_CLK	spdif1.EXT_CLK	I	External clock input

5.16 Analog Inputs

The i.MX 8M Mini SoC itself does not feature an ADC input. Since analog inputs are in the *"Reserved"* category of Verdin interfaces, there is a dedicated I²C ADC on the Verdin iMX8M Mini module. The 12-bit ADC TLA2024 from Texas Instruments offers up to four single-ended analog inputs. The delta-sigma ADC features an internal reference voltage.

The TLA2024 can be configured into the differential mode as well. In this mode, the ADC_1 and ADC_2 are combined to a differential input while the ADC_3 and ADC_4 are combined. This differential mode is not part of the Verdin standard and therefore potentially not compatible with other modules.

The ADC features a programmable input gain which can be selected for input ranges of ±256mV, 512mV, ±1.024V, ±2.048V, and ±4.096V. Since the ADC is powered with 3.3V, the actual input range is limited by the absolute maximum input voltage range of -0.3V to 3.6V. However, to be compatible with other Verdin modules, it is recommended to limit the input voltage from 0V to 1.8V.

The TLA2024 is connected to the I2C1 I²C port of the SoC. The device has the address 0x49. The same I²C port is also shared with the on-module PMIC, RTC, EEPROM, and Secure Element.

Features

- 12-bit ADC
- Delta-Sigma algorithm
- Programmable gain amplifier from ±256mV to ±4.096V
- 4-channel single-ended or 2-channel fully differential
- Internal FIFO with channel-scan mode
- Programmable data rate from 128SPS to 3.3kSPS

Table 5-43 Analog Inputs Pins

X1 Pin#	Verdin Std Function	TLA2024 Pin#	TLA2024 Pin Name	I/O	Remarks
2	ADC_1	7	AIN3	I	Analog Input 1
4	ADC_2	6	AIN2	I	Analog Input 2
6	ADC_3	5	AIN1	I	Analog Input 3
8	ADC_4	4	AIN0	I	Analog Input 4

5.17 Controller Area Network (CAN)

The i.MX 8M Mini SoC does not feature an integrated CAN controller. However, there are up to two MCP2518 external CAN FDs from Microchip on the module. Some standard SKUs of the Verdin iMX8M Mini feature only one MCP2518, and therefore only a single CAN interface. There are also standard SKUs without CAN (see also section 1.2.3). Modules with both CAN controllers assembled are available on request (see also section 1.6).

The two MCP2518 CAN controllers share the same SPI interface for connecting to the SoC. The chip select signal for the second CAN controller is a regular GPIO signal since the SPI interfaces of the i.MX 8M Mini only feature single chip selects. The interfaces have individual interrupt connections for a faster response time. The SPI interface is also shared with the optional TPM 2.0 (Trusted Platform Module).

Features:

- CAN FD support
- Mixed CAN 2.0B and CAN FD Mode
- Compliant with ISO11898-1:2015
- Bit rate up to 8Mb/s
- Arbitration bit rate up to 1Mb/s
- 31 FIFOs, configurable as transmit or receive FIFO
- Transmit Event FISO with 32-bit timestamp
- Programmable automatic retransmission

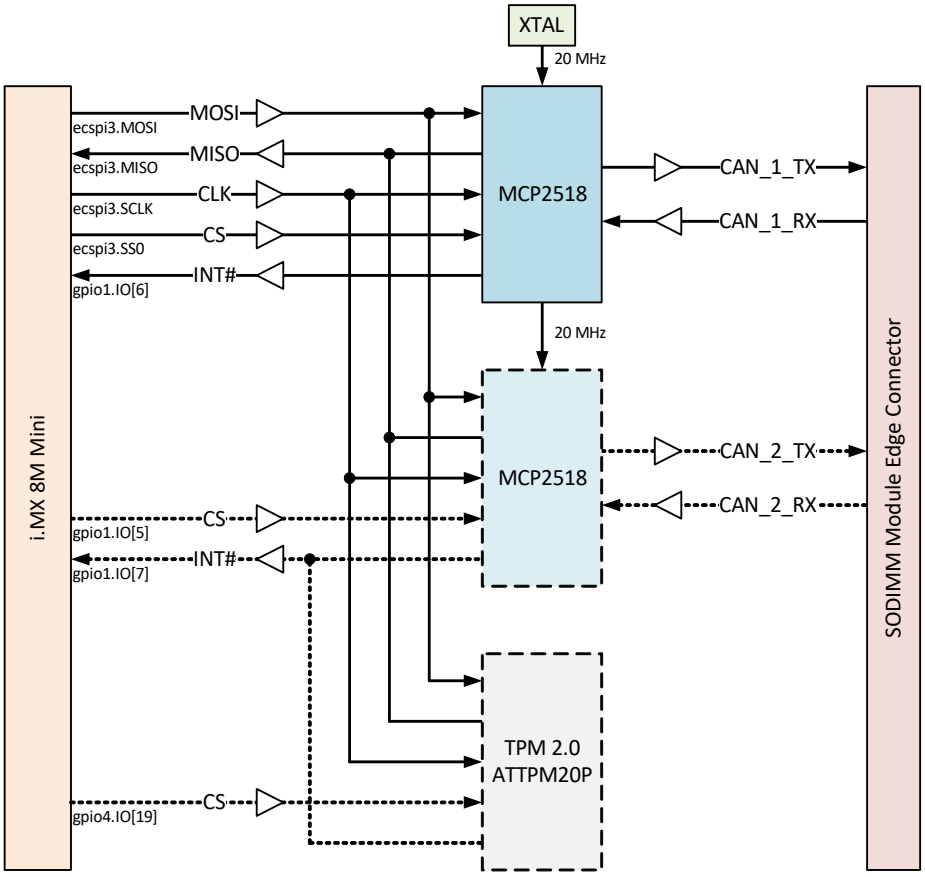

Figure 12: CAN block diagram

Table 5-44 CAN Signal Pins

X1 Pin#	Verdin Signal Name	MCP2518 Pin#	MCP2518 Pin Name	I/O	Description
20	CAN_1_TX	1	TXCAN	O	CAN port 1 transmit pin, not available on all modules
22	CAN_1_RX	2	RXCAN	I	CAN port 1 receive pin, not available on all modules
24	CAN_2_TX	1	TXCAN	O	CAN port 2 transmit pin, only available on request
26	CAN_2_RX	2	RXCAN	I	CAN port 2 receive pin, only available on request

5.18 JTAG

The JTAG interface is normally not required for programming the Verdin, however, it can be useful for debugging of the Cortex-M4 Core or very advanced debugging of the Cortex-A Cores. It is possible to reprogram the module using the Recovery Mode over USB. To flash the module in recovery mode (and for debugging) it is strongly recommended that the USB_1 interface is accessible even if not needed in the production system. Additionally, UART_3 for the console of the main CPUs (A53) and UART_4 for debugging the M4 core should be accessible as well.

Table 5-45 JTAG Signal Pins

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
1	JTAG_1_TDI	JTAG_TDI	cjtag_wrapper.TDI	I	Test Data In

X1 Pin#	Verdin Std Function	i.MX 8MM Ball Name	i.MX 8MM Function	I/O	Description
5	JTAG_1_TDO	JTAG_TDO	cjtag_wrapper.TDO	O	Test Data Out
9	JTAG_1_TCK	JTAG_TCK	cjtag_wrapper.TCK	I	Test Clock
13	JTAG_1_TMS	JTAG_TMS	cjtag_wrapper.TMS	I	Test Mode Select
3	JTAG_1_TRST#	JTAG_TRST_B	cjtag_wrapper.TRST_B	I	Test Reset
7	JTAG_1_VREF			O	1.8V reference output for JTAG adapter

6. Recovery Mode

The recovery mode (USB serial loader) can be used to download new software to the Verdin iMX8M Mini even when the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in recovery mode, the USB_1 interface is used to connect it to a host computer. You will find additional information at our Developer Center (http://developer.toradex.com).

In order to enter recovery mode, the dedicated recovery pin (SODIMM pin 246) needs to be pulled down with ≤1kΩ during the initial power-on (cold boot) of the module. The CTRL_RECOVERY_MICO# function on the SODIMM pin 246 is standardized in the Verdin module specifications. It is highly recommended to add at least a test point on the carrier board to the pin 246 to be able to enter recovery mode. There is no need for a pull-up resistor on the carrier board.

Important: make sure that there is no bootable SD card plugged into the slot. Otherwise, the module will try to boot from the external SD card instead of going into the USB serial loader.

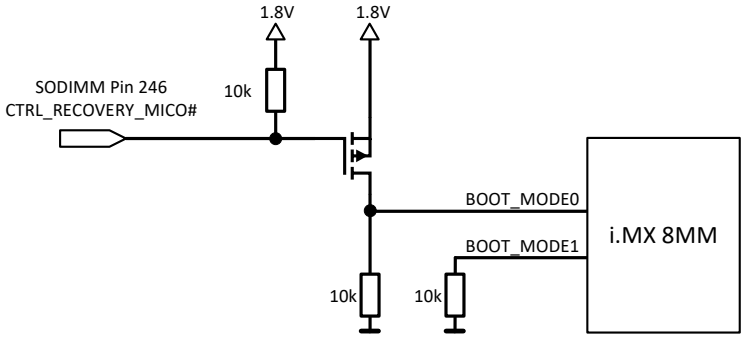

Figure 13: Recovery Mode Circuit

7. Known Issues

Up-to-date information about all known hardware issues can be found in the errata document which can be downloaded from our website at:

https://developer.toradex.com/products/verdin-imx8m-mini#8-erratakown-issues

8. Technical Specifications

8.1 Absolute Maximum Ratings

Table 8-1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VCC	Main power supply	-0.3	6	V
VCC_BACKUP	RTC power supply	-0.3	6.5	V
IO_1.8V	SoC IO pins with 1.8V logic level	-0.3	2.1	V
IO_3.3V	SoC IO pins with 3.3V logic level (SDIO)	-0.3	3.6	V
ADC	ADC analog input	-0.3	3.6	V
USB_1_VBUS	Input voltage at USB_1_VBUS	-0.3	5.5	V

8.2 Recommended Operation Conditions

Table 8-2 Recommended Operation Conditions

Symbol	Description	Min	Typical	Max	Unit
VCC	Main power supply	3.135	3.3 or 5	5.5	V
VCC_BACKUP	RTC power supply	1.1	3.0	5.5	V

8.3 Electrical Characteristics

Table 8-3 Typical Power Consumption

Symbol	Description (VCC = 5.0V)	Typical	Unit
IDD_IDL	CPU Idle	TBD	A
IDD_HIGHCPU	Maximal CPU Load, 3D-graphic test	TBD	A
IDD_HD	Full HD Video on MIPI-DSI (h.264 decoding, CPU full load)	TBD	A
IDD_SUSPEND	Module in Suspend State	TBD	mA
IDD_BACKUP	Current consumption of internal RTC	TBD	µA

These are typical values. The actual consumption varies between different modules and is temperature-dependent as well. The current consumption can be higher than IDD_HIGHCPU, depending on the load of the GPU and the temperature.

8.4 Power Ramp-Up Time Requirements

The carrier board needs to follow the power supply ramp-up requirements of the Verdin module standard. This specification can be found in the Verdin Carrier Board Design Guide.

8.5 Mechanical Characteristics

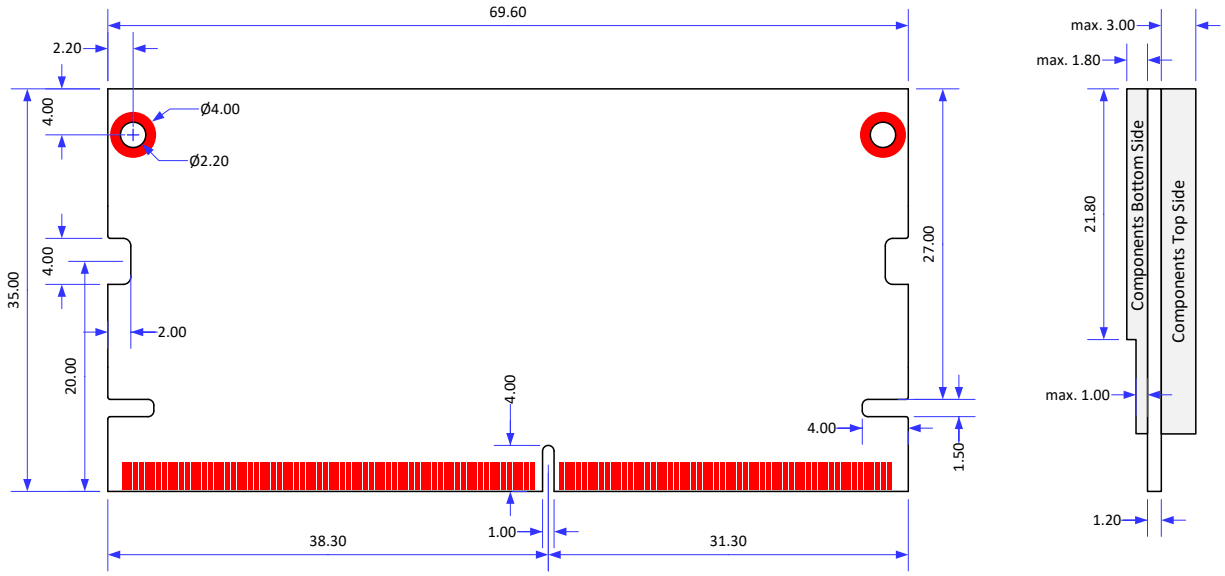

Figure 14 Mechanical dimensions of the Verdin module (top view)
Tolerance for all measures: +/- 0.1mm, unless otherwise specified

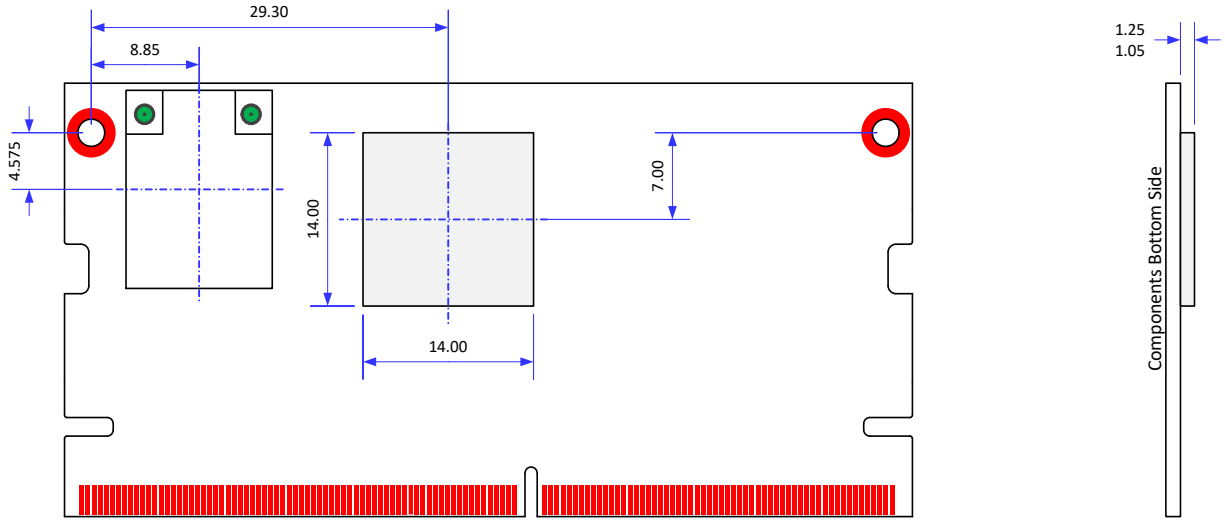

Figure 15 Mechanical position of i.MX 8MM SoC (top view)
Tolerance for all measures: +/- 0.1mm, unless otherwise specified

8.5.1 Sockets for the Verdin Modules

The Verdin module uses the SODIMM DDR4 memory module edge connector. This connector has 260 pins and is available from different manufacturers in various board-to-board stacking heights from 4mm to 9.2mm. Toradex recommends using the TE Connectivity 2309409-2 which has a stacking height of 5.2mm which provides a board-to-board distance of 2.62mm.

A list of other SODIMM DDR4 connector manufacturers is given below:

Amphenol: https://www.amphenol-icc.com/product-series/ddr4-so-dimm.html
TE Connectivity: https://www.te.com/usa-en/products/connectors/card-socket-connectors/memory-sockets.html

8.6 Thermal Specification

The Verdin iMX8M Mini incorporates DVFS (Dynamic Voltage and Frequency Scaling) and Thermal Throttling which enables the system to continuously adjust the operating frequency and voltage in response to the changes in workload and temperature. The i.MX 8M Mini SoC features DVFS on the CPU cluster, as well as on the GPU. This allows the Verdin iMX8M Mini to deliver higher performance at lower average power consumption compared to other solutions.

The Verdin iMX8M Mini modules come with embedded temperature sensors. The sensors measure the die (junction) temperature and are used for determining whether the cores need to be throttled in order to prevent overheating. If the temperature of the i.MX 8MM reaches the maximum permitted temperature limit, the system will automatically shut down.

Here are some general considerations for you to follow:

- If you only use the peak performance for a short time period, heat dissipation is less of a problem because the advanced power management reduces power consumption when full performance is not required.
- A lower die temperature will also lower the power consumption due to the smaller leakage currents while idle. A die temperature increase from 25°C to 125°C will increase the leakage by a factor of 10.

In general, the more effective the thermal solution is, the more performance you can get out of the Verdin iMX8M Mini Module.

Table 8-4 1.1 Thermal Specification Verdin iMX8M Mini Quad 2GB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MM only. ($R_{\theta JA}$)[2]		22.9		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MM chip case. ($R_{\theta JCtop}$)[2]		4		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The Wi-Fi module is currently only validated from -30°C to 85°C. Validation down to -40°C is pending. The rest of the components are rated for the complete -40°C to 85°C temperature range.

Table 8-5 1.1 Thermal Specification Verdin iMX8M Mini Quad 2GB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MM only. ($R_{\theta JA}$)[2]		22.9		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MM chip case. ($R_{\theta JCtop}$)[2]		4		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.

Table 8-6 1.1 Thermal Specification Verdin iMX8M Mini DualLite 1GB WB IT

Description	Min	Typ	Max	Unit
Operating temperature range	-40[3]		85[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	-40		105	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MM only. ($R_{\theta JA}$)[2]		22.9		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MM chip case. ($R_{\theta JCtop}$)[2]		4		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.
[3] The Wi-Fi module is currently only validated from -30°C to 85°C. Validation down to -40°C is pending. The rest of the components are rated for the complete -40°C to 85°C temperature range.

Table 8-7 1.1 Thermal Specification Verdin iMX8M Mini DualLite 1GB

Description	Min	Typ	Max	Unit
Operating temperature range	0		70[1]	°C
Storage Temperature (eMMC flash memory is the limiting device)	-40		85	°C
Junction temperature SoC	0		95	°C
Thermal Resistance Junction-to-Ambient, i.MX 8MM only. ($R_{\theta JA}$)[2]		22.9		°C/W
Thermal Resistance Junction-to-Top of i.MX 8MM chip case. ($R_{\theta JCtop}$)[2]		4		°C/W

[1] Depending on cooling solution.
[2] A High K JEDEC four-layer Board as defined by JEDEC Standard JESD51-3, board mounted horizontal, natural convection.

8.7 Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Mineral, REACH, etc. can be found on our website at: http://www.toradex.com/support/product-compliance