# SY26406FCC

## High Efficiency, 0.6A, 100V Input Synchronous Step Down Regulator

## General Description

The SY26406 develops a high efficiency synchronous step-down DC/DC converter capable of delivering 0.6A current. The SY26406 operates over a wide input voltage range from 7V to 100V and integrates a main switch and a synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The SY26406 always operates under Continuous Conduction Mode. The SY26406 adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

## Applications

- Isolated Telecom Bias Supply
- Secondary High Voltage Post Regulator
- Automotive Systems

## Features

- Wide Input Voltage Range: 7-100V
- Internal 500mΩ Main Switch and 285mΩ Synchronous Switch
- 0.6A Output Current Capability
- COT Ripple-Based Control to Achieve Fast Transient Responses
- Programmable Switching Frequency Range: 200kHz~600kHz.
- 2ms Internal Soft-start Limits the Inrush Current
- Accurate Feedback Set Point: 1.225V±2%
- Cycle-by-cycle Peak/Valley Current Limit
- Cycle-by-cycle Reverse Current Limit
- Auto Recovery for Over Temperature (OTP)
- RoHS Compliant and Halogen Free
- Compact Package: SO8E

## Typical Applications

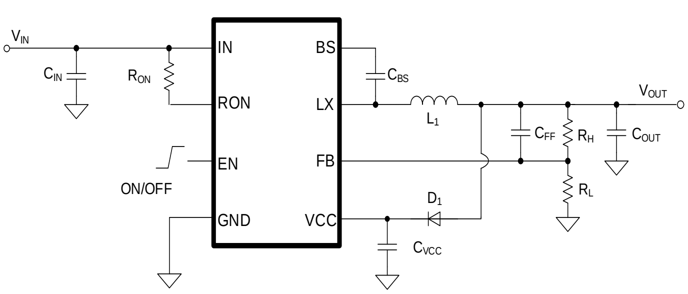



**Figure1. Typical Application Circuit**

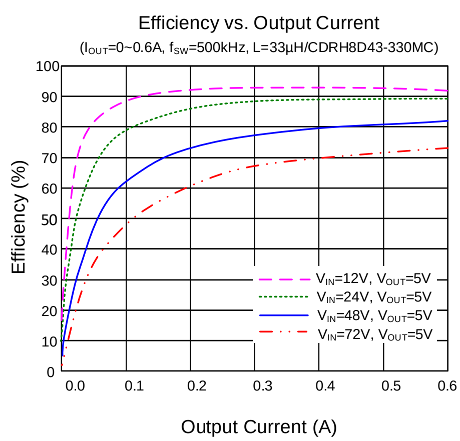


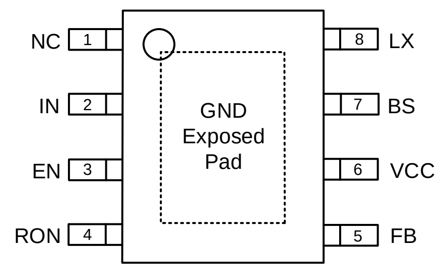

**Figure2. Efficiency vs. Output Current**

## Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|---|---|---|
| SY26406FCC | SO8E<br>RoHS Compliant and Halogen Free | **DRD*xyz*** |

***x* = year code, *y* = week code, *z* = lot number code**

## Pinout (top view)




## Pin Description

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| NC | 1 | Not connected. |
| IN | 2 | Input pin. Decouple this pin to GND with a low ESR ceramic capacitor. |
| EN | 3 | Enable control pin. This pin can also be used for programming $V_{IN}$ turn on voltage with the resistor divider. The device has an accurate 1.225V rising threshold. |
| RON | 4 | Connect a resistor from this pin to the IN to set the top switch ON time. The switching frequency can be calculated using the following equation: $f_{sw}(kHz) = \frac{11 \times V_{OUT}(V) + 500}{R_{ON}(M\Omega)}$ |
| FB | 5 | Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=1.225\times(1+R_H/R_L)$ |
| VCC | 6 | Supply input of internal LDO. |
| BS | 7 | Boot-Strap Pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin. |
| LX | 8 | Inductor pin. Connect this pin to the switching node of inductor. |
| GND | Exposed Pad | Ground pin. |

## Block Diagram

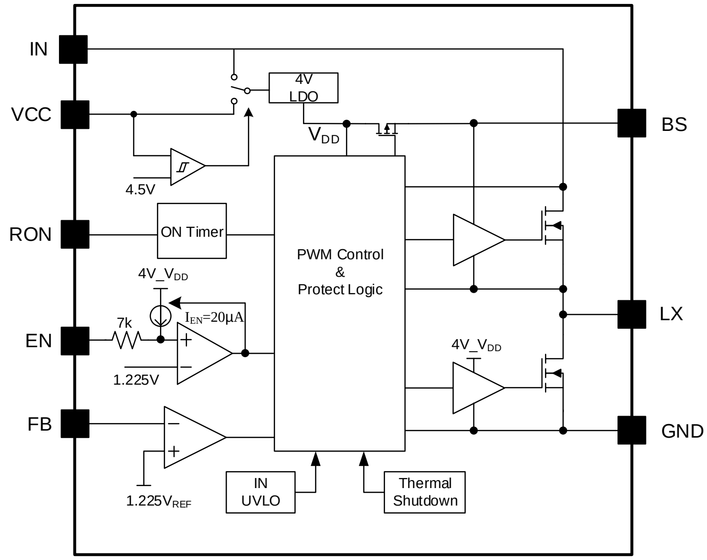



**Figure3. Block Diagram**

| Absolute Maximum Ratings (1) | Min | Max | Unit |
|---|---|---|---|
| IN | -0.3 | 100 | V |
| EN,RON | -0.3 | IN+ 0.3 | |
| LX | -0.3 | IN+ 0.3 | |
| BS-LX,FB | -0.3 | 6 | |
| VCC | -0.3 | 30 | |
| LX, 50ns duration | IN+3 | GND-5 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering,10sec.) | | 260 | |
| Storage Temperature | -65 | 150 | |

| Thermal Information (2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-ambient Thermal Resistance | 30 | °C/W |
| $\theta_{JC}$ Junction-to-case Thermal Resistance | 10 | |
| $P_D$ Power Dissipation $T_A$=25°C | 3.3 | W |

| Recommended Operating Conditions (3) | Min | Max | Unit |
|---|---|---|---|
| IN | 7 | 100 | V |
| Ambient Temperature | -40 | 85 | °C |
| Junction Temperature | -40 | 125 | |

# Electrical Characteristics

($V_{IN}$ = 48V, $V_{OUT}$ = 5V, L = 33μH, $C_{OUT}$ = 10μF, $I_{OUT}$ = 0.6A unless otherwise specified. Typical value corresponds to $T_J$ = 25°C. Minimum and maximum limits apply over -40°C to 125°C junction temperature range.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 7 | | 100 | V |
| Input UVLO Rising Threshold | $V_{IN,UVLO}$ | | 5.8 | 6.3 | 6.8 | V |
| Input UVLO Hysteresis | $V_{HYS}$ | | | 0.25 | | V |
| Shutdown Current | $I_{SHDN}$ | EN=0 | | 8 | 30 | μA |
| Feedback Reference Voltage | $V_{REF}$ | | 1.2 | 1.225 | 1.25 | V |
| FB Input Current | $I_{FB}$ | $V_{FB}$=3.3V | -100 | | 100 | nA |
| Top FET RON | $R_{DS(ON)1}$ | | | 500 | | mΩ |
| Bottom FET RON | $R_{DS(ON)2}$ | | | 285 | | mΩ |
| Top FET peak Current Limit | $I_{LIM,TOP}$ | | 0.9 | 1.2 | 1.5 | A |
| Bottom FET Valley Current Limit | $I_{LIM,BOTTOM}$ | | 0.6 | 0.8 | 1 | A |
| Negative Current Limit | $I_{LIM,NEG}$ | | -480 | -650 | -820 | mA |
| VCC Input Rising UVLO Threshold | $V_{VCC,UVLO}$ | | | 4.5 | | V |
| VCC Input UVLO Hysteresis | $V_{VCC,HYS}$ | | | 0.3 | | V |
| EN Rising Threshold | $V_{EN}$ | | 1.185 | 1.225 | 1.265 | V |
| EN Hysteresis Input Current | $I_{EN,\ HYS}$ | | -10 | -20 | -29 | μA |
| Switching Frequency | $f_{OSC}$ | $V_{IN}$=48V, $R_{ON}$=1.1MΩ | 350 | 500 | 650 | kHz |
| Min ON Time | $t_{ON}$ | | | 90 | | ns |
| Min OFF Time | $t_{OFF}$ | | | 200 | | ns |
| Thermal Shutdown Temperature | $T_{SD}$ | | | 150 | | °C |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 15 | | °C |

**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E packages is the case position for $\theta_{JC}$ measurement.

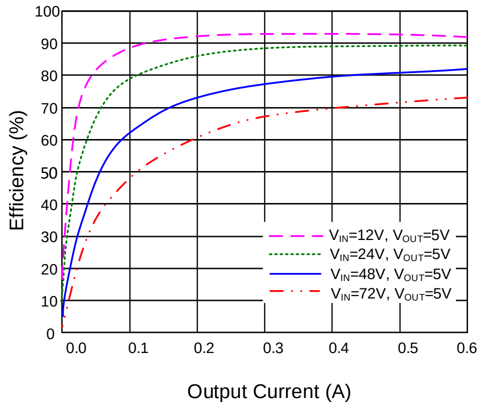
**Note 3:** The device is not guaranteed to function outside its operating conditions.

# Typical Performance Characteristics

($T_A$ = 25℃, $V_{IN}$ = 48V, $V_{OUT}$ = 5V, L = 33μH, $C_{OUT}$ = 10μF, $f_{SW}$ = 500kHz, unless otherwise noted)

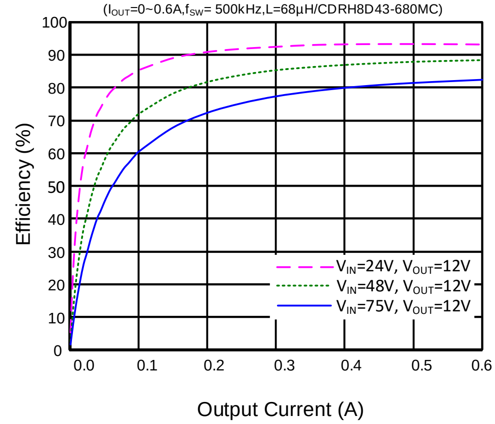
Efficiency vs. Output Current

($I_{OUT}$=0~0.6A, $f_{SW}$=500kHz, L=33μH/CDRH8D43-330MC)

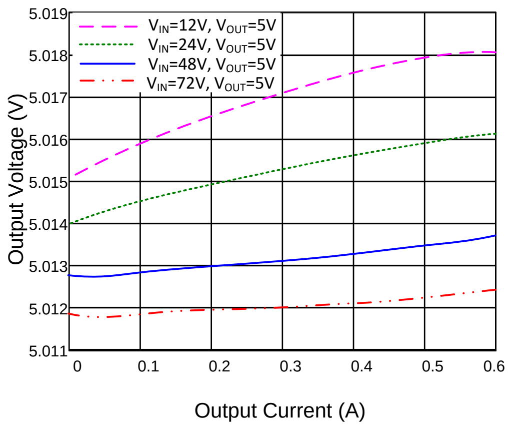



Efficiency vs Output Current

($I_{OUT}$=0~0.6A,$f_{SW}$= 500kHz,L=68μH/CDRH8D43-680MC)

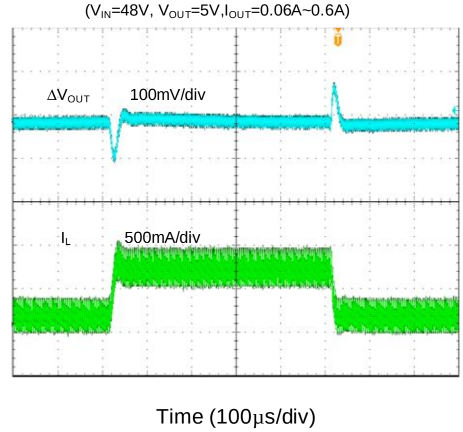



Output Voltage vs Output Current



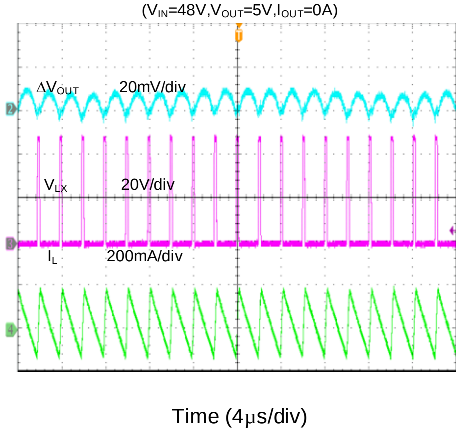

Load Transient

($V_{IN}$=48V, $V_{OUT}$=5V,$I_{OUT}$=0.06A~0.6A)



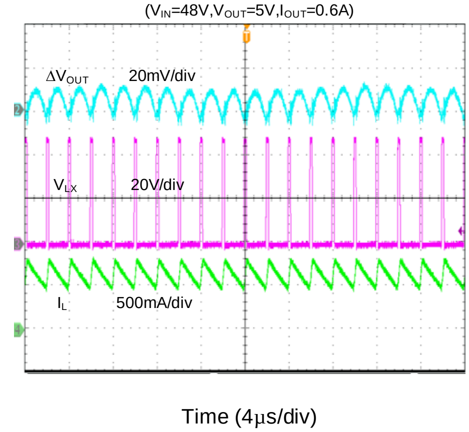

Output Ripple

($V_{IN}$=48V,$V_{OUT}$=5V,$I_{OUT}$=0A)

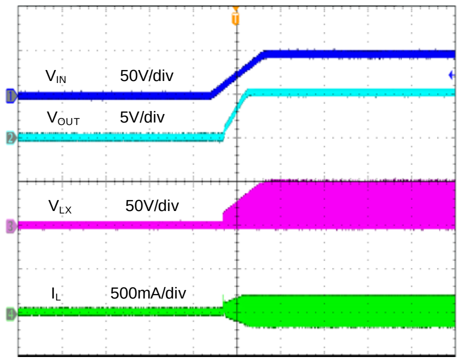



Output Ripple

($V_{IN}$=48V,$V_{OUT}$=5V,$I_{OUT}$=0.6A)

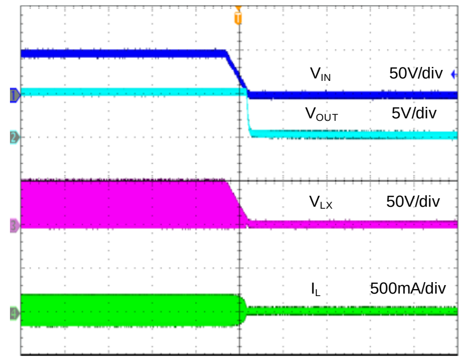


Startup from $V_{IN}$
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0A)



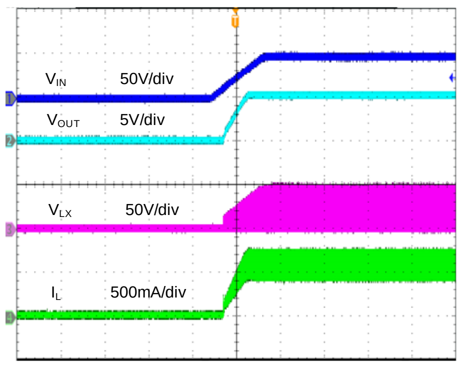

Time (4ms/div)

Shutdown from $V_{IN}$
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0A)



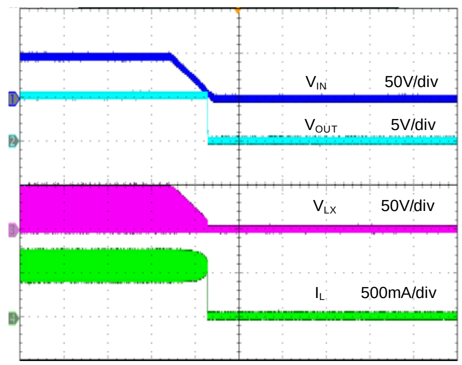

Time (200ms/div)

Startup from $V_{IN}$
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0.6A)



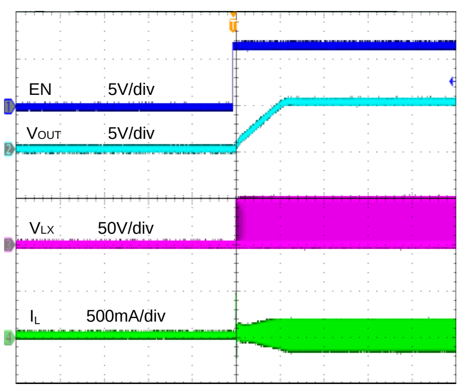

Time (4ms/div)

Shutdown from $V_{IN}$
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0.6A)



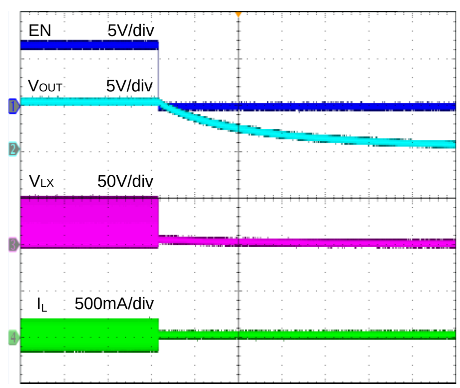

Time (100ms/div)

Startup from EN
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0A)




Time (2ms/div)

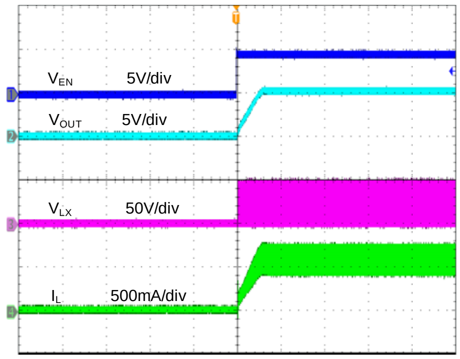
Shutdown from EN
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0A)




Time (400ms/div)

Startup from EN

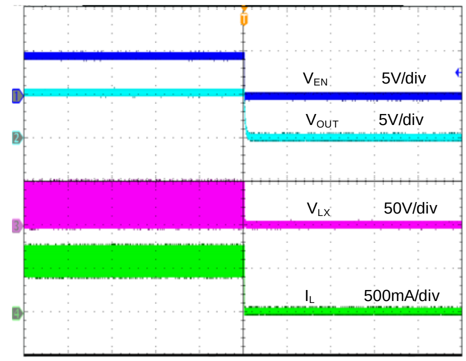
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0.6A)




Time (4ms/div)

Shutdown from EN

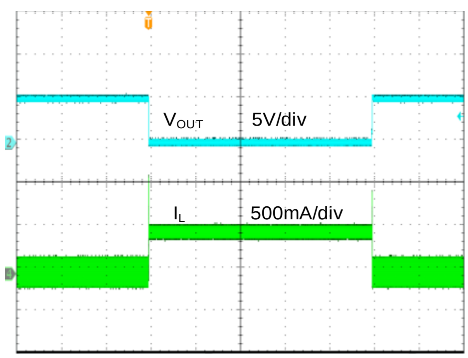
($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0.6A)




Time (4ms/div)

Short Circuit Protection

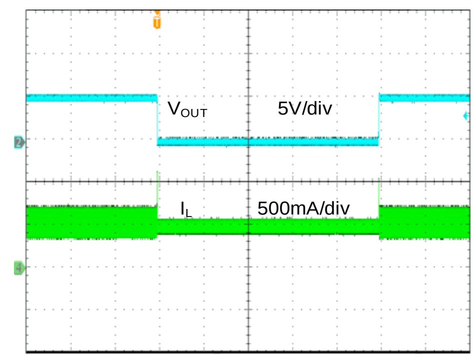
($V_{IN}$=48V, $V_{OUT}$=5V,$I_{OUT}$=0A~Short)




Time (10ms/div)

Short Circuit Protection

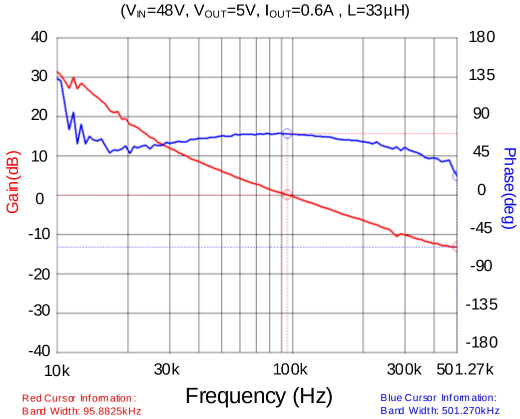
($V_{IN}$=48V, $V_{OUT}$=5V,$I_{OUT}$=0.6A~Short)




Time (10ms/div)

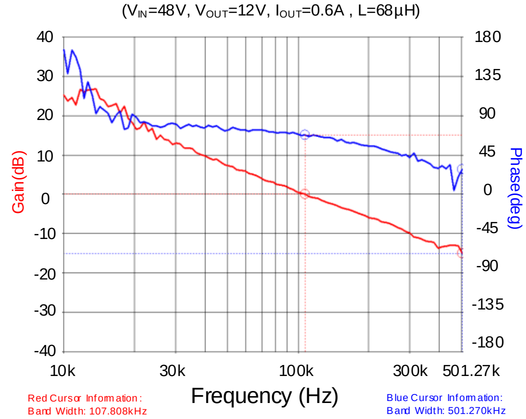
Bode Plot

($V_{IN}$=48V, $V_{OUT}$=5V, $I_{OUT}$=0.6A , L=33μH)




Bode Plot

($V_{IN}$=48V, $V_{OUT}$=12V, $I_{OUT}$=0.6A , L=68μH)



## Detailed Description

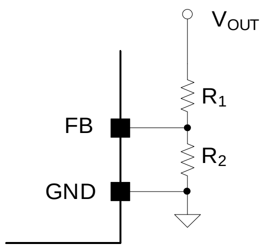
The SY26406 is highly integrated, so only the input capacitor $C_{IN}$, the output capacitor $C_{OUT}$, the output inductor L, and the feedback resistors $R_H$ and $R_L$ need to be selected for the targeted application specifications.

### Output Voltage Program

Choose $R_1$ and $R_2$ to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both $R_1$ and $R_2$.

$$V_{OUT} = (1+\frac{R_1}{R_2}) \times V_{FB}$$

1.225V is a typical value for $V_{FB}$.




### Output Inductor L

There are several considerations in choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The inductance is calculated as:

$$L_1 = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN\_MAX})}{f_{SW} \times I_{OUT\_MAX} \times 40\%}$$

Where $f_{SW}$ is the switching frequency and $I_{OUT\_MAX}$ is the maximum load current.

The SY26406 regulator is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculated value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN\_MAX})}{2f_{SW} \times L_1}$$

The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

### Input Capacitor $C_{IN}$

The ripple current through the input capacitor is calculated as：

$$I_{CIN\_RMS} = I_{OUT\_MAX} \times \sqrt{D(1-D)}$$

The capacitance of the input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times f_{SW} \times \eta \times V_{IN}^2}$$

$\Delta V_{IN}$ is desired input voltage ripple. η is the efficiency.

To minimize the potential noise problem, a typical X5R or a better grade ceramic capacitor is placed really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by $C_{IN}$ and the IN/GND pins. In this case, a 1μF low ESR ceramic capacitor is recommended.

### Output Capacitor $C_{OUT}$

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. It is recommended to use an X5R or a better grade ceramic capacitor with greater than 10μF capacitance.

### On-time

The on-time for the SY26406 is determined by the $R_{ON}$ resistor, and is inversely proportional to the input voltage, resulting in a nearly constant frequency as $V_{IN}$ is varied over its range. The required on-time adjust resistance for various frequencies and output voltages are given in Table 1.

Frequency vs. $R_{ON}$ Resistor:

$$f_{SW}(kHz) = \frac{11 \times V_{OUT}(V) + 500}{R_{ON}(M\Omega)}$$

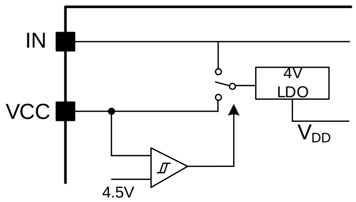
Table 1. On-Time Adjust Resistance For Various Frequencies and Output Voltages

| $F_{SW}$ (kHz) | $R_{ON}$(MΩ) | | | |
|---|---|---|---|---|
| | $V_{OUT}$ = 1.8V | $V_{OUT}$ = 5V | $V_{OUT}$ = 12 V | $V_{OUT}$ = 24 V |
| 200 | 2.6 | 2.8 | 3.15 | 3.8 |
| 400 | 1.3 | 1.4 | 1.6 | 1.9 |
| 600 | 0.85 | 0.9 | 1.05 | 1.3 |

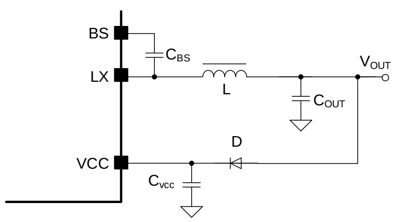
Notice: Final switch frequency is not only affected by the tolerance of component but also by minimum off and on-time limit.

## Internal LDO Regulator

The SY26406 has two power supply ways for 4V LDO. Upon power up, the 4V LDO regulator will be power supplied by $V_{IN}$. When the voltage on the VDD reaches the under-voltage lockout threshold voltage, the Buck regulator will be enabled. After soft-start is done, if the VCC pin voltage is larger than 4.5V, the power supply of 4V LDO will be switched to VCC. A 0.1μF ceramic capacitor is recommended for $C_{VCC}$ in most applications.




In applications, the input pin (IN) can be connected directly to the line voltage up to 100 Volts, where power dissipation in the 4V LDO regulator is a concern, an auxiliary voltage can be connected to the VCC pin via a diode. Setting the auxiliary voltage to 4.8 -28V will shut off the LDO power supply from IN and reduce internal LDO power dissipation.




## Soft-start

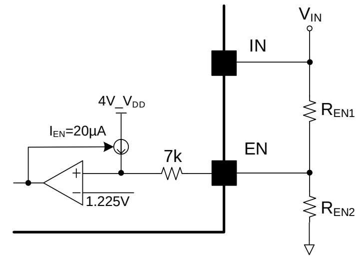
The SY26406 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during the IC start-up. The typical soft-start time is 2ms.

## Adjusting Under Voltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device will start to operate. If the EN pin voltage is pulled below the threshold, the regulator will stop switching and enter shutdown state. An external set-point voltage divider from $V_{IN}$ to GND can be used for setting the minimum operating voltage of the regulator. Minimum $V_{UVLO}$ value needs larger than 6.8V.

$$V_{IN,UVLO}(V)=(1+\frac{R_{EN1}}{R_{EN2}})\times V_{EN}$$

1.225V is a typical value for $V_{EN}$.

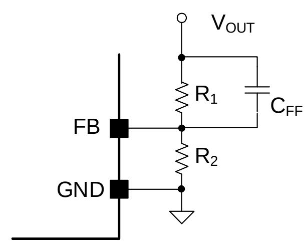



UVLO hysteresis is accomplished with an internal 20μA current source that is switched on or off into the impedance of the set-point divider. When the EN threshold is exceeded, the current source will be activated to quickly raise the voltage at the EN pin. The UVLO hysteresis is calculated as

$$V_{HYS}(V)=I_{EN}\times R_{EN1}+I_{EN}\times 7k\times(1+\frac{R_{EN1}}{R_{EN2}})$$

## Load Transient Considerations

The SY26406 regulator adopts COT ripple-based control to achieve good stability and fast transient responses. Adding a $C_{ff}$ ceramic capacitor in parallel with $R_1$ is recommended.




## External Boot-strap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

## Over Current Protection

The SY26406 provides cycle-by-cycle over current limit on both high side MOSFET and low-side MOSFET. Under over current condition, if the output voltage drops below 33% of set-point, the device will fold back valley current limit to 0.5×typical value.

**Over-temperature Protection (OTP)**

The device includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold

## Application Schematic ($V_{OUT}$ = 5V)

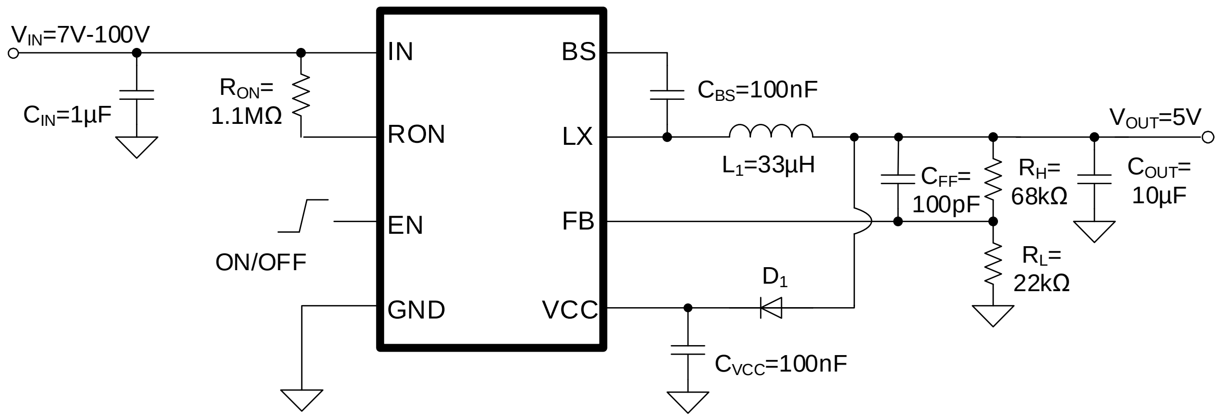



**Figure 4. Buck Schematic**

## BOM List

| Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_{IN}$ | 1μF/100V/X7R,1206 | C3216X7R2A105K | TDK |
| $C_{OUT}$ | 10μF/25V/X5R, 1206 | C3216X5R1E106M | TDK |
| $C_{VCC}$ | 0.1μF/50V/X7R, 0603 | C1608X7R1H104K | TDK |
| $C_{BS}$ | 0.1μF/50V/X7R, 0603 | C1608X7R1H104K | TDK |
| $C_{FF}$ | 100pF/50V/X5R, 0603 | C1608C0G1H101J | TDK |
| L | 33μH, inductor | CDRH8D43-330NC | Sumida |
| $R_{ON}$ | 1.1MΩ, 1%, 0603 | | |
| $R_H$ | 68kΩ, 1%, 0603 | | |
| $R_L$ | 22kΩ, 1%, 0603 | | |
| $D_1$ | BAT54 | | |

## Recommend Table for Typical Applications

| $V_{OUT}$(V) | $R_H$(kΩ ) | $R_L$(kΩ ) | $C_{FF}$(pF) | $L_1$/Part Number |
|---|---|---|---|---|
| 5 | 68 | 22 | 100 | 33μH/CDRH8D43-330NC |
| 12 | 105 | 12 | 220 | 68μH/CDRH8D43-680NC |

## Application Schematic ($V_{OUT}$ = 5V)

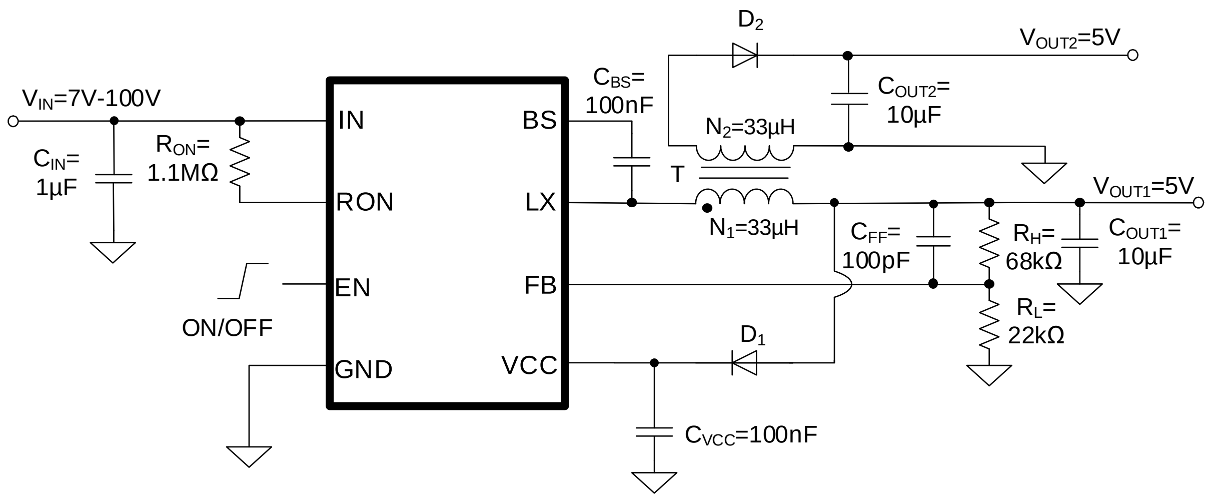



**Figure 5. Fly-Buck Schematic**

## BOM List

| Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_{IN}$ | 1µF/100V/X7R,1206 | C3216X7R2A105K | TDK |
| $C_{OUT1}$ | 10µF/25V/X5R, 1206 | C3216X5R1E106M | TDK |
| $C_{OUT2}$ | 10µF/25V/X5R, 1206 | C3216X5R1E106M | TDK |
| $C_{VCC}$ | 0.1µF/50V/X7R, 0603 | C1608X7R1H104K | TDK |
| $C_{BS}$ | 0.1µF/50V/X7R, 0603 | C1608X7R1H104K | TDK |
| $C_{FF}$ | 100pF/50V/X5R, 0603 | C1608C0G1H101J | TDK |
| T | $N_1$:33µH, $N_2$:33µH | | |
| $R_{ON}$ | 1.1MΩ, 1%, 0603 | | |
| $R_H$ | 68kΩ, 1%, 0603 | | |
| $R_L$ | 22kΩ, 1%, 0603 | | |
| $D_1$ | BAT54 | | |
| $D_2$ | SS310 | | |

## Recommend Table for Typical Applications

| $V_{OUT}$(V) | $R_H$(kΩ ) | $R_L$(kΩ ) | $C_{FF}$(pF) | T(µH) |
|---|---|---|---|---|
| 5 | 68 | 22 | 100 | 33 |
| 12 | 105 | 12 | 220 | 68 |

## Application Schematic ($V_{OUT}$ = -5V)

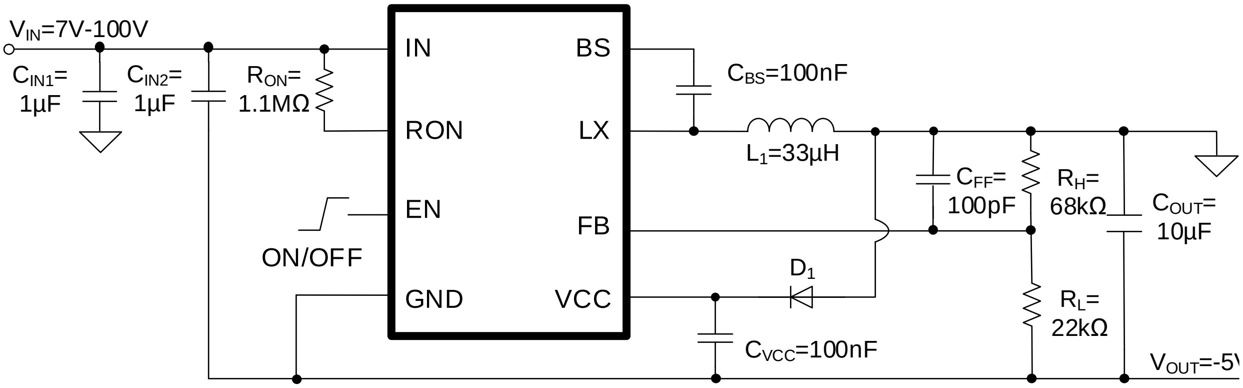



**Figure 6. Buck-Boost Schematic**

## BOM List

| Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| $C_{IN1}$ | 1µF/100V/X7R,1206 | C3216X7R2A105K | TDK |
| $C_{IN2}$ | 1µF/100V/X7R,1206 | C3216X7R2A105K | TDK |
| $C_{OUT}$ | 10µF/25V/X5R, 1206 | C3216X5R1E106M | TDK |
| $C_{VCC}$ | 0.1µF/50V/X7R, 0603 | C1608X7R1H104K | TDK |
| $C_{BS}$ | 0.1µF/50V/X7R, 0603 | C1608X7R1H104K | TDK |
| $C_{FF}$ | 100pF/50V/X5R, 0603 | C1608C0G1H101J | TDK |
| L | 33µH, inductor | CDRH8D43-330NC | Sumida |
| $R_{ON}$ | 1.1MΩ, 1%, 0603 | | |
| $R_H$ | 68kΩ, 1%, 0603 | | |
| $R_L$ | 22kΩ, 1%, 0603 | | |
| $D_1$ | BAT54 | | |

## Recommend Table for Typical Applications

| $V_{OUT}$(V) | $R_H$(kΩ ) | $R_L$(kΩ ) | $C_{FF}$(pF) | $L_1$/Part Number |
|---|---|---|---|---|
| 5 | 68 | 22 | 100 | 33µH/CDRH8D43-330NC |
| 12 | 105 | 12 | 220 | 68µH/CDRH8D43-680NC |

## Layout Design

For optimal design, follow these PCB layout considerations:

- It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.
- $C_{IN}$ must be close to the pins IN and GND. The loop area formed by $C_{IN}$ and GND must be minimized.
- $C_{VCC}$ should be placed close to the VCC pin and the GND pin.
- The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
- The feedback components $R_H$ and $R_L$ and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.
- If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

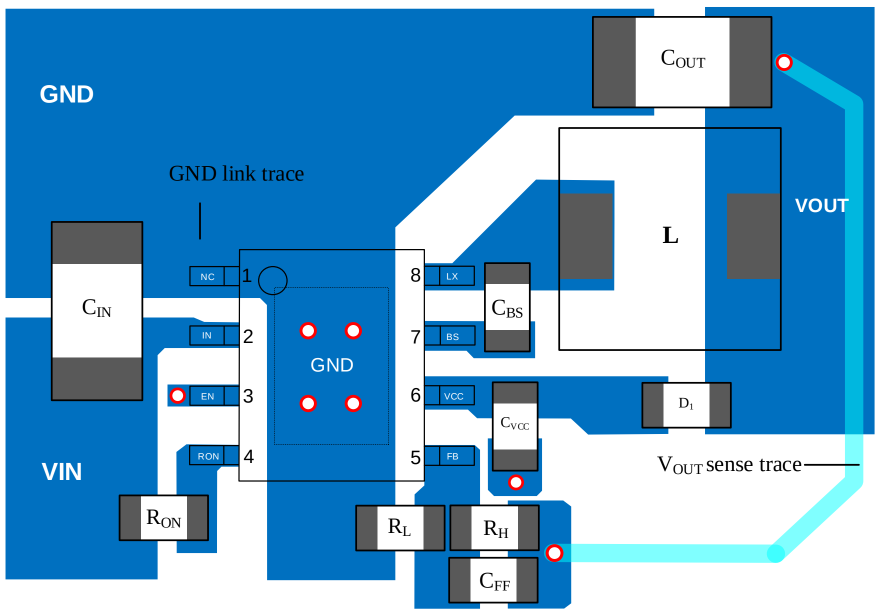
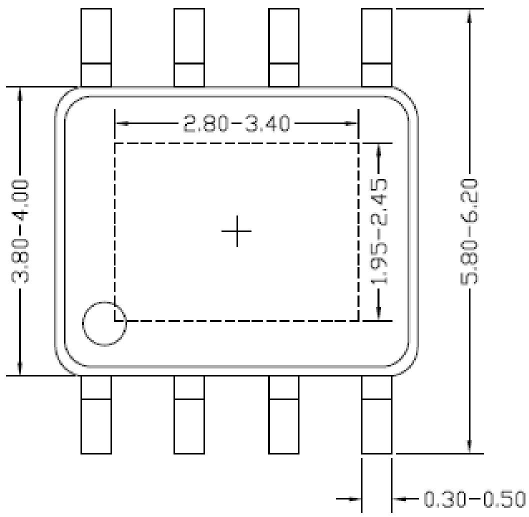
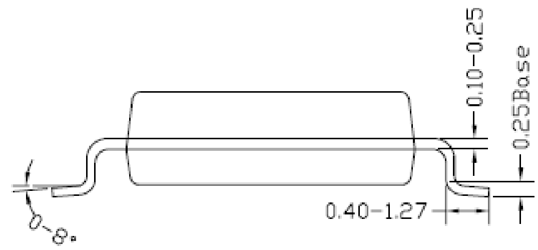



**Figure7. PCB Layout Suggestion**

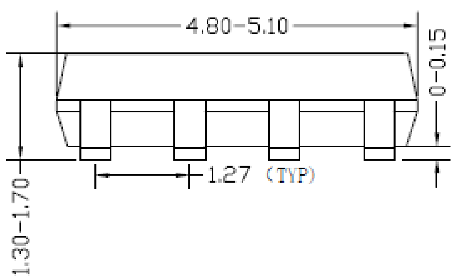
# SO8E Package Outline & PCB Layout



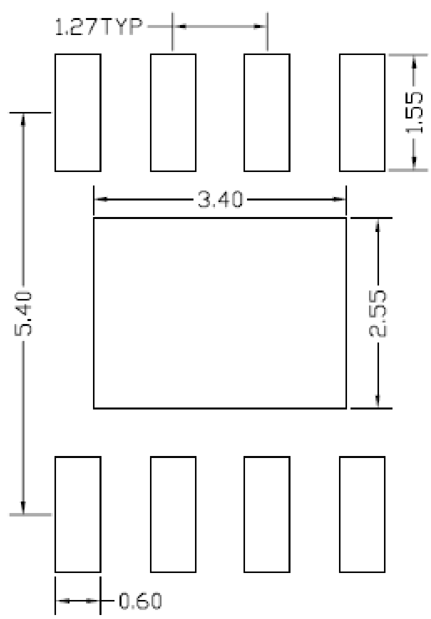

**Top view**




**Side view**




**Front view**



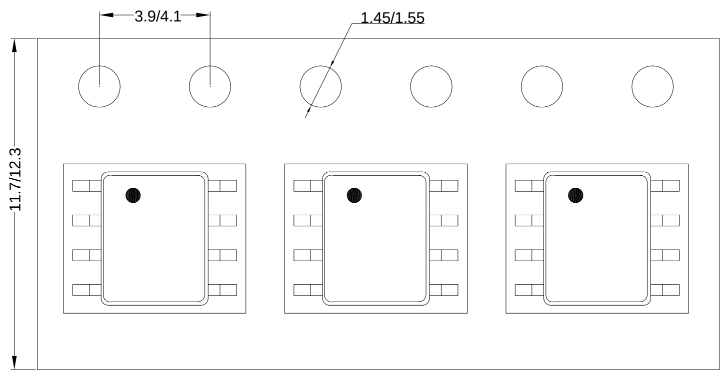

**Recommended PCB layout (Reference Only)**

**Notes:** **All dimension in millimeter and exclude mold flash & metal burr.**

# Taping & Reel Specification

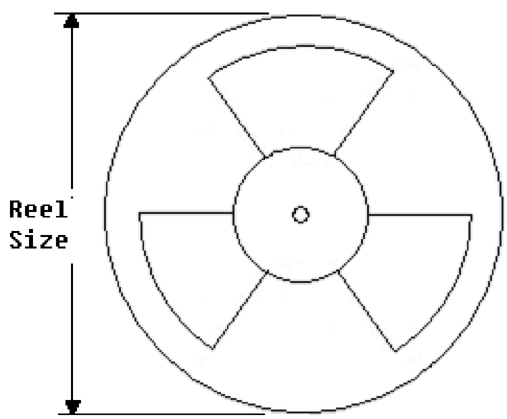
## 1. Taping orientation

**SO8E**




**Feeding direction**

## 2. Carrier Tape & Reel specification for packages




| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| SO8E | 12 | 8 | 13" | 400 | 400 | 2500 |

## 3. Others: NA

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