SHARP

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To;

SPECIFICATIONS

Product Type 128M (x16) Flash Memory + 32M (x16) SmartCombo RAM

LRS18AC

Model No. (LRS18AC)

*This specifications contains 68 pages including the cover and appendix.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: M. Nawaki

M.NAWAKI

Dept. General Manager

REVIEWED BY: R. Mitsuyama

PREPARED BY: S. Kouchi

Product Development Dept. II
System-Flash Division
Integrated Circuits Group
SHARP CORPORATION

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- Office electronics
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- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Description

The LRS18AC is a combination memory organized as 8,388,608 x16 bit flash memory and 2,097,152 x16 bit SmartCombo RAM in one package.

Features

-Power supply	• • • •	1.7V to 1.95V (Flash) 1.7V to 1.95V (SmartCombo RAM)
-Input/Output Power Supply	• • • •	1.7V to 1.95V
-Operating temperature	• • • •	-25°C to +85°C

-Not designed or rated as radiation hardened

-88 pin (LCSP088-P-0811)plastic package

-Flash memory has P-type bulk silicon, and SmartCombo RAM has P-type bulk silicon

-For specifications of Flash memory, SmartCombo RAM, refer to specification of each chip

Standby current of Flash memory and SmartCombo RAM

-Power supply current (The current for F-$V_{CC,}$ SC-V_{CC} pin and V_{PP} pin)	• • • •	175 µA	(Max.)

Flash Memory (128M (x16) bit Flash Memory)

-Access Time (Address Access / Page Access)	• • • •	85 ns/25 ns(Max.)	
-Synchronous Burst Mode (Clock Frequency)	• • • •	54 MHz	(Max.)
-Power supply current (The current for F-V_{CC} pin and V_{PP} pin)			
Read	• • • •	22 mA	(Max. t_{CYCLE} = 200ns, CMOS Input)
Word write	• • • •	70 mA	(Max.)
Block erase	• • • •	50 mA	(Max.)
Reset	• • • •	65 µA	(Max. $\overline{RST}$ = GND ± 0.2V)
Standby	• • • •	65 µA	(Max. F-$\overline{CE}$ = $\overline{RST}$ = V_{CCQ})

-Extended Cycling Capability

100,000 Block Erase Cycles	(V_{PP} = 0.9V to V_{CCQ})
1,000 Block Erase Cycles and total 80 hours	(V_{PP} = 8.5V to 9.5V)

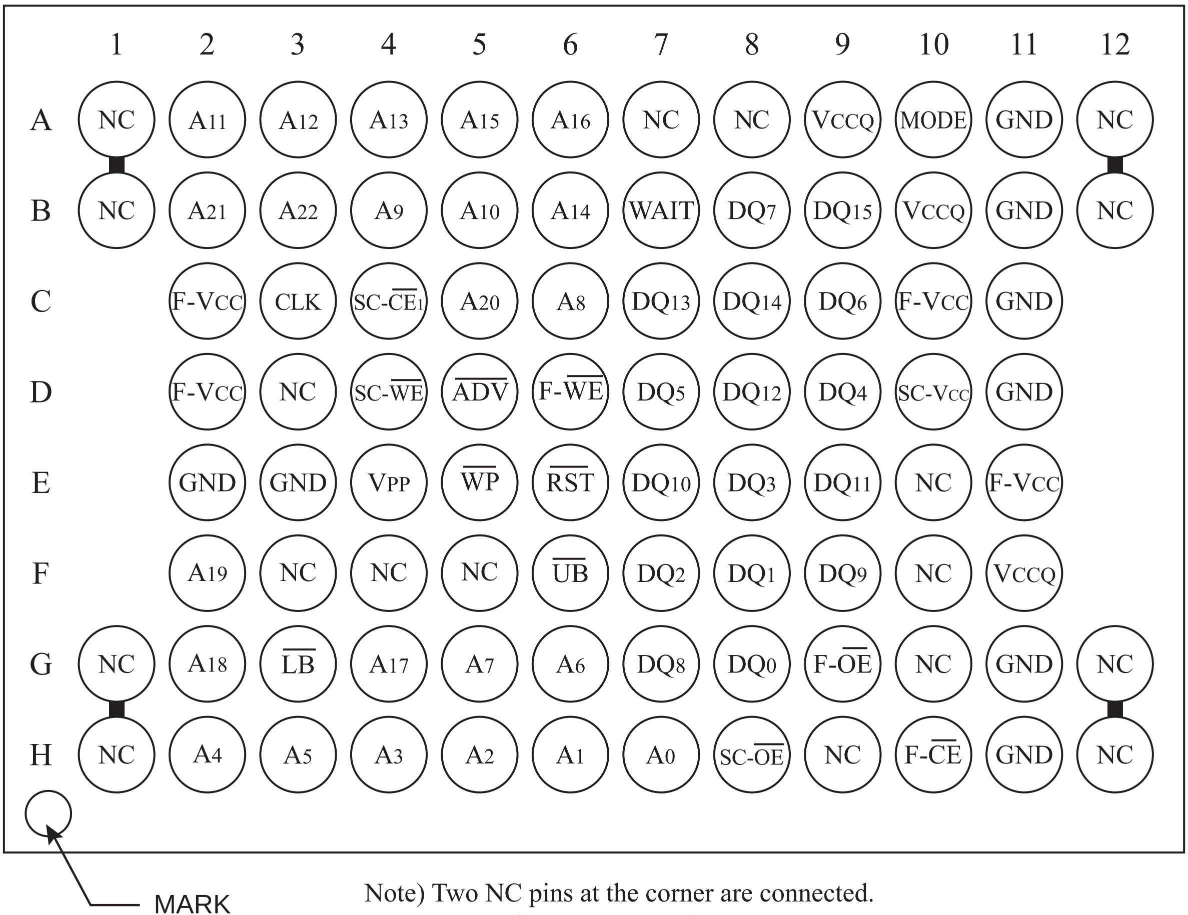
-OTP Block
4 Word +132 Word Array

SmartCombo RAM (32M (x16) bit SmartCombo RAM)

-Access Time (Address Access / Page Access)	• • • •	70 ns/20 ns(Max.)	
-Cycle time	• • • •	70 ns	(Min.)
-Power Supply current			
Operating current (Asynchronous Random READ/WRITE)	• • • •	30 mA	(Max. t_{RC}, t_{WC} = Min.)
Standby current	• • • •	110 µA	

2. Pin Configuration

(TOP View)

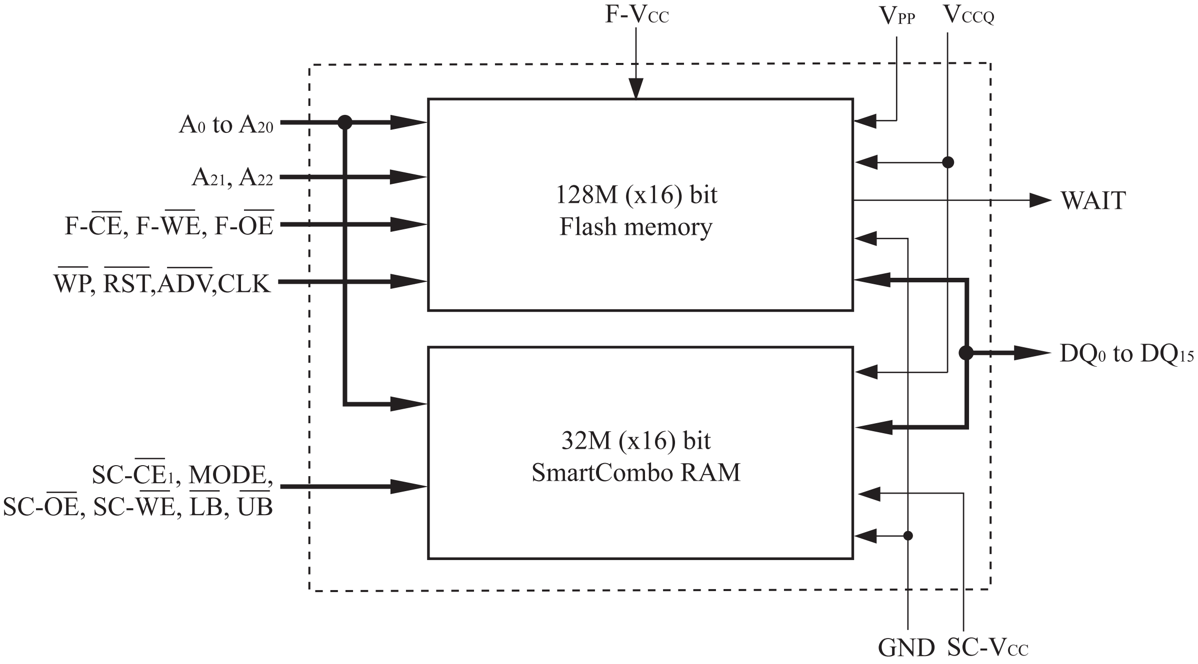


	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	A_{11}	A_{12}	A_{13}	A_{15}	A_{16}	NC	NC	V_{CCQ}	MODE	GND	NC
B	NC	A_{21}	A_{22}	A_{9}	A_{10}	A_{14}	WAIT	DQ_{7}	DQ_{15}	V_{CCQ}	GND	NC
C		F-V_{CC}	CLK	SC-$\overline{CE}_{1}$	A_{20}	A_{8}	DQ_{13}	DQ_{14}	DQ_{6}	F-V_{CC}	GND	
D		F-V_{CC}	NC	SC-$\overline{WE}$	$\overline{ADV}$	F-$\overline{WE}$	DQ_{5}	DQ_{12}	DQ_{4}	SC-V_{CC}	GND	
E		GND	GND	V_{PP}	$\overline{WP}$	$\overline{RST}$	DQ_{10}	DQ_{3}	DQ_{11}	NC	F-V_{CC}	
F		A_{19}	NC	NC	NC	$\overline{UB}$	DQ_{2}	DQ_{1}	DQ_{9}	NC	V_{CCQ}	
G	NC	A_{18}	$\overline{LB}$	A_{17}	A_{7}	A_{6}	DQ_{8}	DQ_{0}	F-$\overline{OE}$	NC	GND	NC
H	NC	A_{4}	A_{5}	A_{3}	A_{2}	A_{1}	A_{0}	SC-$\overline{OE}$	NC	F-$\overline{CE}$	GND	NC

Note) Two NC pins at the corner are connected.
Do not float any GND pins.
All of F-V_{CC} should be connected.
All of V_{CCQ} should be connected.

Pin	Description	Type
A_0 to A_{20}	Address Inputs (Common)	Input
A_{21}, A_{22}	Address Inputs (Flash)	Input
F-$\overline{\text{CE}}$	Chip Enable Input (Flash)	Input
SC-$\overline{\text{CE}}_1$	Chip Enable Input (SmartCombo RAM)	Input
MODE	Sleep State Input (SmartCombo RAM)	Input
F-$\overline{\text{WE}}$	Write Enable Input (Flash)	Input
SC-$\overline{\text{WE}}$	Write Enable Input (SmartCombo RAM)	Input
F-$\overline{\text{OE}}$	Output Enable Input (Flash)	Input
SC-$\overline{\text{OE}}$	Output Enable Input (SmartCombo RAM)	Input
CLK	Clock Input (Flash) CLK synchronizes the device to the system bus frequency during synchronous burst mode. CLOCK INPUT is applicable only in synchronous burst mode.	Input
$\overline{\text{ADV}}$	Address Valid (Flash) Addresses are input to the memory when $\overline{\text{ADV}}$ is low (V_{IL}).	Input
WAIT	Wait Output (Flash) The WAIT signal indicates valid data during synchronous burst modes. WAIT is applicable only in synchronous burst mode. Shared WAIT pin of nomal access SmartCombo RAM and Flash.	Output
$\overline{\text{LB}}$	Byte Enable Input: DQ_0 to DQ_7 (SmartCombo RAM)	Input
$\overline{\text{UB}}$	Byte Enable Input: DQ_8 to DQ_{15} (SmartCombo RAM)	Input
$\overline{\text{RST}}$	Reset Input (Flash) Block erase and Write : V_{IH} Read : V_{IH} Reset : V_{IL}	Input
$\overline{\text{WP}}$	Write Protect Input (Flash) When $\overline{\text{WP}}$ is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When $\overline{\text{WP}}$ is V_{IH}, lock-down is disabled.	Input
DQ_{0-15}	Data Inputs and Outputs (Common)	Input / Output
V_{PP}	Monitoring Power Supply Voltage (Flash) Block Erase and Write : $V_{PP} = V_{PPH1/2}$	Input / Power
F-V_{CC}	Power Supply (Flash)	Power
SC-V_{CC}	Power Supply (SmartCombo RAM)	Power
V_{CCQ}	Input/Output Power Supply (Common)	Power
GND	GND (Common)	Power
NC	Non Connection	-

3. Block Diagram



Note: Only one between F-$\overline{CE}$ and SC-$\overline{CE}_1$ can be "low".
Two or more should not be "low".

4. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
F-V_{CC}	Supply Voltage	1,2	-0.2 to +2.3	V
SC-V_{CC}	Supply Voltage	1	-0.2 to +2.3	V
V_{CCQ}	I/O Supply Voltage	1,2	-0.2 to +2.3	V
V_{IN}	Input Voltage	1,2,3	-0.2 to V_{CCQ}+0.3 (Max. 2.3)	V
T_A	Operating Temperature		-25 to +85	°C
T_{STG}	Storage Temperature		-55 to +125	°C
V_{PP}	V_{PP} Voltage	1,3,4	-0.2 to +10	V

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. Except V_{PP} .
3. -1.0V undershoot is allowed when the pulse width is less than 2 nsec.
4. Applying 8.5V to 9.5V to V_{PP} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{PP} may be connected to 8.5V to 9.5V for total of 80 hours maximum. +11.0V overshoot is allowed when the pulse width is less than 20 nsec.

5. Recommended DC Operating Conditions

(T_A = -25°C to +85°C)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
F-V_{CC}	Supply Voltage		1.7		1.95	V
SC-V_{CC}	Supply Voltage		1.7		1.95	V
V_{CCQ}	I/O Supply Voltage		1.7		1.95	V
V_{PP}	V_{PP} Voltage (Write Operation)		0.9		V_{CCQ}	V
	V_{PP} Voltage (Read Operation)		0		V_{CCQ}	V
V_{IH}	Input Voltage (Flash)		V_{CCQ}-0.3		V_{CCQ}	V
	Input Voltage (SmartCombo RAM)		V_{CCQ}-0.3		V_{CCQ}	V
V_{IL}	Input Voltage (Flash)		-0.2		0.4	V
	Input Voltage (SmartCombo RAM)		-0.2		0.4	V

6. Flash Memory

6.1 Truth Table

6.1.1 Bus Operation (1, 2)

Flash	Notes	$\overline{RST}$	F-$\overline{CE}$	F-$\overline{OE}$	F-$\overline{WE}$	$\overline{ADV}$	WAIT	Address	DQ_{0-15}
Read Array	5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	(7)	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	X	High-Z
Standby		V_{IH}	V_{IH}	X	X	X	High-Z	X	High-Z
Reset		V_{IL}	X	X	X	X	High-Z	X	High-Z
Read Identifier Codes/OTP	5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{OH} or V_{OL}	See Section 6.2	
Read Query	5, 6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{OH} or V_{OL}	X	D_{OUT}
Read Status Register	5	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{OH} or V_{OL}	X	D_{OUT}
Write	3,4,5	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High-Z	X	D_{IN}

Notes:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses.
3. Command writes involving block erase, (page buffer) program or OTP program are reliably executed when $V_{PP}=V_{PPH1/2}$ and F-V_{CC}=1.7V-1.95V.
   Command writes involving buffered advanced factory program is reliably executed when $V_{PP}=V_{PPH2}$ and F-V_{CC}=1.7V-1.95V.
4. Refer to Section 6.2 Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. Never hold F-$\overline{OE}$ and F-$\overline{WE}$ low at the same timing.
6. Query code = Common Flash Interface (CFI) code.
7. WAIT indicates data valid in synchronous burst modes. WAIT is used only for synchronous burst mode.

6.1.2 Simultaneous Operation Modes Allowed with 8 Planes (1, 2)

IF ONE PLANE IS:	THEN THE MODES ALLOWED IN THE OTHER PLANE IS:									
	Read Array	Read ID/ OTP/ Query	Read Status	Program	Page Buffer Program	OTP Program	Block Erase	Buffered Advanced Factory Program (BAFP)	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X (3)	X (3)	X (3)	X (3)		X	X
Read ID/OTP/Query	X	X	X	X (3)	X (3)		X (3)		X	X
Read Status	X	X	X	X	X	X	X	X	X	X
Program	X (3)	X (3)	X							X
Page Buffer Program	X (3)	X (3)	X							X
OTP Program	X (3)		X							
Block Erase	X (3)	X (3)	X							
Buffered Advanced Factory Program (BAFP)			X							
Program Suspend	X	X	X							X
Block Erase Suspend	X	X	X	X	X				X	

Notes:

1. “X” denotes the operation available.
2. Dual Work Restrictions:
   Status register reflects WSM (Write State Machine) state.
   Only one plane can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.
   It is not possible to do burst reads that cross plane boundaries.
3. While block erasing, programming, page buffer programming, or OTP programming, read array and read OTP/query are restricted as shown in the next table.

6.1.3 The Restriction of Reading Operation While Erasing or Programming (1)

Erasing or Programming Operation:	Read Operation:		
	Read Array in the Parameter Plane	Read Array in Main Plane	Read OTP/Query
In the Parameter Plane, Block Erasing, Programming, or Page Buffer Programming		X	
In a Main Plane, Block Erasing, Programming, or Page Buffer Programming	X	X (2)	X
OTP Programming		X	

Notes:

1. "X" denotes the operation available.
2. Read operation is available for other main planes except a main plane while block erasing, programming, or page buffer programming. Read operation is not available for a main plane while block erasing, programming, or page buffer programming.

6.2 Command Definitions for Flash Memory

6.2.1 Command Definitions (11)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper (1)	Address (2)	Data	Oper (1)	Address (2)	Data (3)
Read Array	1		Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	4	Write	PA	90H	Read	IA, OA	ID, OD
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	X	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Program	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5, 7	Write	WA	E8H	Write	WA	N-1
Buffered Advanced Factory Program	≥ 2	5,9,12	Write	WA0	80H	Write	WA0	D0H
Block Erase and (Page Buffer) Program Suspend	1	8, 9	Write	X	B0H			
Block Erase and (Page Buffer) Program Resume	1	8, 9	Write	X	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
OTP Program	2	9	Write	OA	C0H	Write	OA	OD
Set Read Configuration Register	2		Write	RCRC	60H	Write	RCRC	03H

Notes:

1. Bus operations are defined in 6.1.1 Bus Operation.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X = Any valid address within the device.
   PA = Address within the selected plane.
   IA = Identifier codes address (See 6.2.2 Identifier Codes and OTP Address for Read Operation).
   QA = Query codes address.
   BA = Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA = Address of memory location for the Program command or the first address for the Page Buffer Program command.
   WA0 = First address for the buffered advanced factory program command.
   OA = Address of OTP block to be read or programmed (See 6.2.3 OTP Block Address Map).
   RCRC = Read configuration register code presented on the addresses A_0-A_{15}.
3. ID = Data read from identifier codes (See 6.2.2 Identifier Codes and OTP Address for Read Operation).
   QD = Data read from query database.
   SRD = Data read from status register (See 6.3 Register Definition for a description of the status register bits).
   WD = Data to be programmed at location WA. Data is latched on the rising edge of F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$ (whichever goes high first) during command write cycles.
   OD = Data within OTP block. Data is latched on the rising edge of F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$ (whichever goes high first) during command write cycles.
   N-1 = N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, read configuration register code and the data within OTP block (See 6.2.2 Identifier Codes and OTP Address for Read Operation).
   The Read Query command is available for reading CFI (Common Flash Interface) information.

5. Block erase, buffered advanced factory program or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when $\overline{\text{RST}}$ is $V_{IH.}$
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, input the program sequential address and write data of “N” times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H).
8. If the program operation in one plane is suspended and the erase operation in other plane is also suspended, the suspended program operation is resumed first.
9. Buffered advanced factory program and OTP program operations can not be suspended. The OTP Program command and Buffered advanced factory program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when $\overline{\text{WP}}$ is V_{IL}.
    When $\overline{\text{WP}}$ is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.
12. At buffered advanced factory program, 80H initiates buffered advanced factory program mode at the first cycle of two-cycle command. After D0H is set at the second cycle of two-cycle command, the CUI (Command User Interface) latches address and data, and prepares the device for buffered advanced factory program mode. When buffered advanced factory program mode begins, all other commands can not be accepted and interpreted as data to be written.

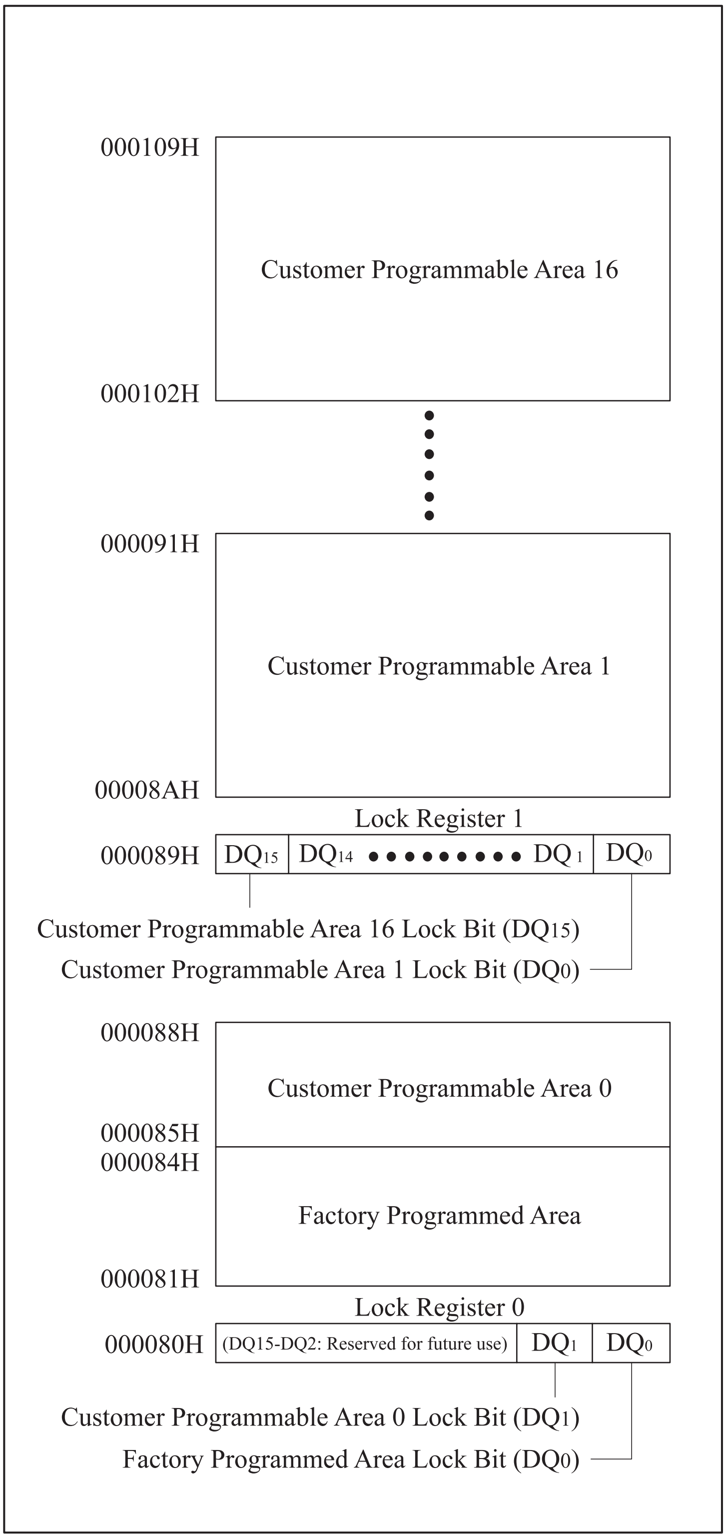
6.2.2 Identifier Codes and OTP Address for Read Operation

	Code	Address [A_{15}-A_0]	Data [DQ_{15}-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	1
Device Code	128M (x16) Bottom Parameter Device Code	0001H	001BH	1
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	$DQ_0 = 0$	2, 3
	Block is Locked		$DQ_0 = 1$	2, 3
	Block is not Locked-Down		$DQ_1 = 0$	2, 3
	Block is Locked-Down		$DQ_1 = 1$	2, 3
Device Configuration Code	Plane Configuration Register	0005H	RCRC	1, 4
OTP	Lock Register 0	0080H	OTP-LK0	1, 5
	Factory Programmed Area and Customer Programmable Area 0	0081-0088H	OTP0	1, 6
	Lock Register 1	0089H	OTP-LK1	1, 7
	Customer Programmable Area 1-16	008A-0109H	OTP1	1, 8

Notes:

1. A_{22}-A_{16} must be the address within the plane to which the Read Identifier Codes/OTP command (90H) has been written.
2. Block Address = The beginning location of a block address within the plane to which the Read Identifier Codes/OTP command (90H) has been written.
3. DQ_{15}-DQ_2 is reserved for future implementation.
4. RCRC = Read Configuration Register Code.
5. OTP-LK0 = OTP Block Lock configuration for Factory Programmed Area and Customer Programmable Area 0.
6. OTP0 = OTP Block data for Factory Programmed Area and Customer Programmable Area 0.
7. OTP-LK1 = OTP Block Lock configuration for Customer Programmable Area 1-16.
8. OTP1 = OTP Block data for Customer Programmable Area 1-16.

6.2.3 OTP Block Address Map



6.2.4 Functions of Block Lock (1) and Block Lock-Down

Current State					Erase/Program Allowed (3)
State	$\overline{WP}$	DQ_1(2)	DQ_0(2)	State Name	
[000]	0	0	0	Unlocked	Yes
[001](4)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](4)	1	0	1	Locked	No
[110](5)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

1. OTP (One Time Program) block has the lock function which is different from those described above.
2. $DQ_0 = 1$: a block is locked; $DQ_0 = 0$: a block is unlocked.
   $DQ_1 = 1$: a block is locked-down; $DQ_1 = 0$: a block is not locked-down.
3. Erase and program are general terms, respectively, to express: block erase, buffered advanced factory program and (page buffer) program operations.
4. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] ($\overline{WP} = 0$) or [101] ($\overline{WP} = 1$), regardless of the states before power-off or reset operation.
5. When $\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

6.2.5 Block Locking State Transitions upon Command Write (4)

Current State				Result after Lock Command Written (Next State)		
State	$\overline{WP}$	DQ_1	DQ_0	Set Lock (1)	Clear Lock (1)	Set Lock-down (1)
[000]	0	0	0	[001]	No Change	[011] (2)
[001]	0	0	1	No Change (3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] (2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] (2)
[111]	1	1	1	No Change	[110]	No Change

Notes:

1. “Set Lock” means Set Block Lock Bit command, “Clear Lock” means Clear Block Lock Bit command and “Set Lock-down” means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0 = 0$), the corresponding block is locked-down and automatically locked at the same time.
3. “No Change” means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that $\overline{WP}$ is not changed and fixed V_{IL} or V_{IH}.

6.2.6 Block Locking State Transitions upon $\overline{WP}$ Transition (4)

Previous State	Current State				Result after $\overline{WP}$ Transition (Next State)	
	State	$\overline{WP}$	DQ_1	DQ_0	$\overline{WP}$ = 0→1 (1)	$\overline{WP}$ = 1→0 (1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] (2)	[011]	0	1	1	[110]	-
Other than [110] (2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

Notes:

1. "$\overline{WP}$ = 0→1" means that $\overline{WP}$ is driven to V_{IH} and "$\overline{WP}$ = 1→0" means that $\overline{WP}$ is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When $\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

6.3 Register Definition

Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BES	PBPBAF-POPS	VPPS	PBPSS	DPS	PPES
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7= WRITE STATE MACHINE STATUS (WSMS)
1 = Ready, Page Buffer available
0 = Busy, Page Buffer not available

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASESTATUS (BES)
1 = Error in Block Erase
0 = Successful Block Erase

SR.4 = (PAGE BUFFER) PROGRAM, BUFFERED ENHANCED FACTORY PROGRAM(BAFP) AND OTP PROGRAM STATUS (PBPBAFPOPS)
1 = Error in (Page Buffer) Program, BAFP or OTP Program
0 = Successful (Page Buffer) Program, BAFP or OTP Program

SR.3 = V_{PP} STATUS (VPPS)
1 = V_{PP} LOW Detect, Operation Abort
0 = V_{PP} OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
1 = (Page Buffer) Program Suspended
0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
1 = Erase or Program Attempted on a Locked Block, Operation Abort
0 = Unlocked

SR.0 = PLANE PROGRAM AND ERASE STATUS (PPES)
1 = Another Plane is busy.
BAFP: Program or Verify busy.
0 = Depending on status of SR.7.
The addressed plane is busy or no plane is busy.
BAFP: Program or Verify done, BAFP ready.

Notes:
Status Register indicates the status of the WSM (Write State Machine).

Check SR.7 to determine block erase, buffered advanced factory program, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7= “0”.

If both SR.5 and SR.4 are “1”s after a block erase, buffered advanced factory program, page buffer program, set/clear block lock bit, set block lock-down bit attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, buffered advanced factory program, (page buffer) program or OTP program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1/2}$ or V_{PPLK}.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after block erase, buffered advanced factory program, (page buffer) program or OTP program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 are reserved for future use and should be masked out when polling the status register.

If SR.7 = “0” and SR.0 = “0”, the addressed plane is busy and other plane is not busy. In BAFP Mode, it indicates that the device is finished programming or verifying data or is ready for data.

If SR.7 = “0” and SR.0 = “1”, another plane is busy (the addressed plane is not busy). In BAFP Mode, it indicates that the device is programming or verifying data.

If SR.7 = “1” and SR.0 = “0”, no plane is busy. In BAFP Mode, it indicates that the device has exited BAFP mode.

SR.7 = “1” and SR.0 = “1” will not occur.

Read Configuration Register Definition

RM	R	FC2	FC1	FC0	WT	DOC	WC
15	14	13	12	11	10	9	8
BS	CC	R	R	BW	BL2	BL1	BL0
7	6	5	4	3	2	1	0

RCR.15 = READ MODE (RM)
0 = Synchronous Burst Reads Enabled
1 = Asynchronous Reads Enabled (Default)

RCR.14 = RESERVED FOR FUTURE ENHANCEMENTS

RCR.13-11 = FREQUENCY CONFIGURATION (FC2-0)
000 = Code 0 reserved for future use
001 = Code 1 reserved for future use
010 = Code 2
011 = Code 3
100 = Code 4
101 = Code 5
110 = Code 6
111 = Code 7
(Other bit setting are reserved)

RCR.10 = WAIT SIGNAL POLARITY (WT)
0 = When WAIT signal is low, output data is invalid.
1 = When WAIT signal is high, output data is invalid.

RCR.9 = DATA OUTPUT CONFIGURATION (DOC)
0 = Hold Data for One Clock
1 = Hold Data for Two Clocks

RCR.8 = WAIT CONFIGURATION (WC)
0 = WAIT Asserted During Delay
1 = WAIT Asserted One Data Cycle Before Delay

RCR.7 = BURST SEQUENCE (BS)
0 = Reserved for Future Enhancements
1 = Linear Burst Order

RCR.6 = CLOCK CONFIGURATION (CC)
0 = Burst Starts and Data Output on Falling Clock Edge
1 = Burst Starts and Data Output on Rising Clock Edge

RCR.5-4 = RESERVED FOR FUTURE
ENHANCEMENTS (R)

RCR.3 = BURST WRAP (BW)
0 = Wrap Burst Reads within Burst Length set
by RCR.2-0
1 = No Wrap Burst Reads within Burst Length set
by RCR.2-0

RCR.2-0 = BURST LENGTH (BL2-0)
001 = 4-Word Burst
010 = 8-Word Burst
011 = 16-Word Burst
111 = Continuous (Linear) Burst
(Other bit setting are reserved)

Notes:

Read configuration register affects the read operations from main and parameter blocks. Read operations for status register, query code, identifier codes, OTP block and device configuration codes support single read cycles.

RCR.5 and RCR.4 bits are reserved for future use and should be masked out when checking the read configuration register.

Refer to Frequency Configuration in Page19 for information about the frequency configuration RCR.13-11.

Undocumented combinations of bits RCR.13-11 are reserved for future implementations and should not be used.

Refer to Page19 for information about Data Output configuration RCR.9.

Refer to Page20 for information about Burst Wrap configuration RCR.3.

In the asynchronous page mode, the burst length always equals 8 words.

All the bits in the read configuration register are set to “1” after power-up or device reset.

When the bit RCR.15 is set to “1”, other bits are invalid.

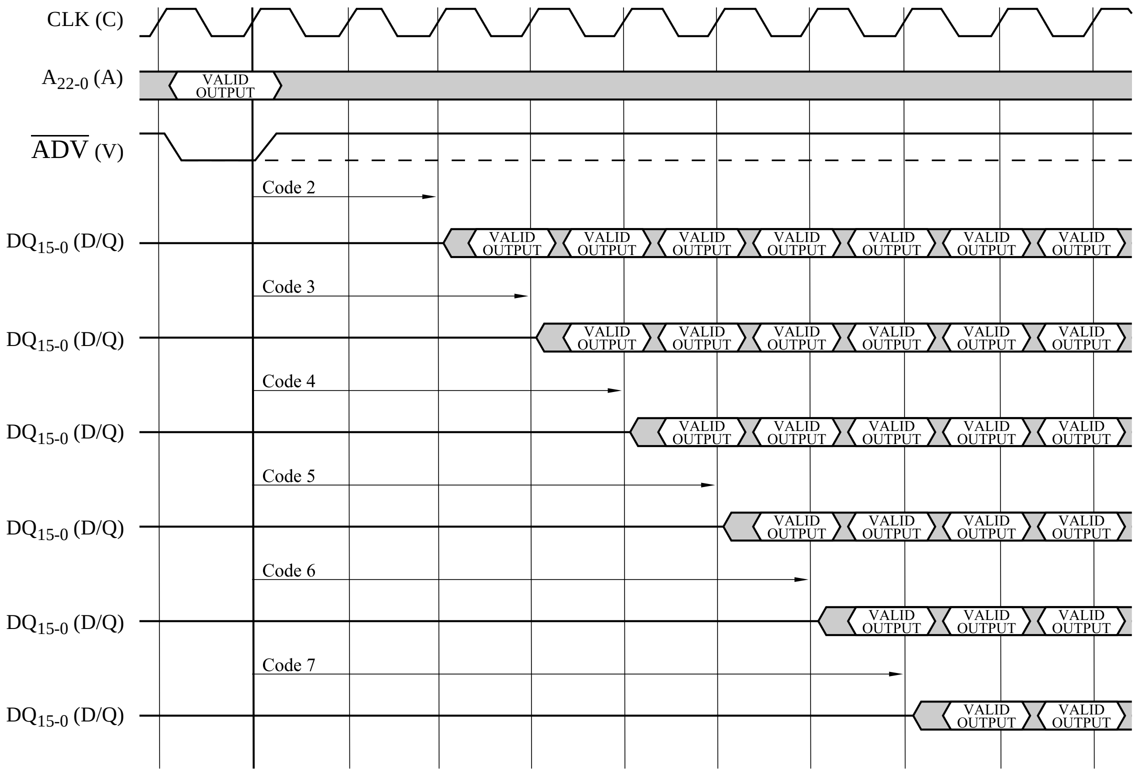
Reserved bits RCR.14, 5, 4 should be cleared (“0”).

RCR.7 is set to “1”, it should not be used with setting “0”.

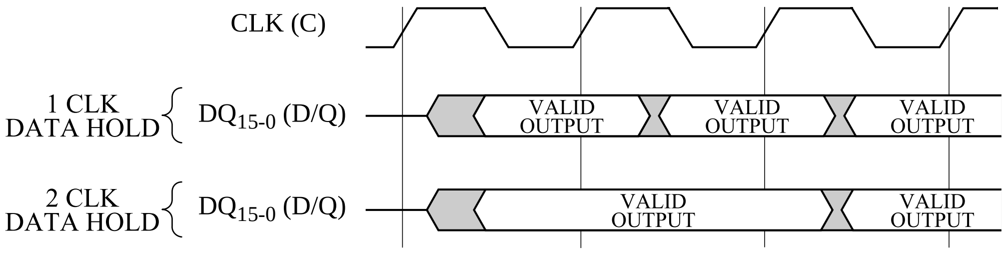
Frequency Configuration Settings

Read Configuration Register			Frequency Configuration Code	Input Clock Frequency (F-V_{CC}=1.7V-1.95V)
RCR.13	RCR.12	RCR.11		85 ns
0	1	0	2	≤ 22 MHz
0	1	1	3	≤ 38 MHz
1	0	0	4	≤ 52 MHz
1	0	1	5	≤ 54 MHz
1	1	0	6	≤ 54 MHz
1	1	1	7	≤ 54 MHz

Frequency Configuration



Data Output Configuration



6.3.1 Read Sequence and Burst Length

Starting Address [Decimal]	Burst Wrap(1) (RCR.3=)	Burst Addressing Sequence [Decimal]			
		4-Word Burst Length (RCR.2-0=001)	8-Word Burst Length (RCR.2-0=010)	16-Word Burst Length (RCR.2-0=011)	Continuous Burst (RCR.2-0=111)
		Linear	Linear	Linear	Linear
0	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15	0-1-2-3-4-5-6…
1	0	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5…15-0	1-2-3-4-5-6-7…
2	0	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6…15-0-1	2-3-4-5-6-7-8…
3	0	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7…15-0-1-2	3-4-5-6-7-8-9…
4	0	4-5-6-7	4-5-6-7-0-1-2-3	4-5-6-7-8…15-0-1-2-3	4-5-6-7-8-9-10…
5	0	5-6-7-4	5-6-7-0-1-2-3-4	5-6-7-8-9…15-0-1-2-3-4	5-6-7-8-9-10-11…
6	0	6-7-4-5	6-7-0-1-2-3-4-5	6-7-8-9-10…15-0-1-2-3-4-5	6-7-8-9-10-11-12…
7	0	7-4-5-6	7-0-1-2-3-4-5-6	7-8-9-10…15-0-1-2-3-4-5-6	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮
14	0	14-15-12-13	14-15-8-9-10-11-12-13	14-15-0-1-2…12-13	14-15-16-17-18-19-20…
15	0	15-12-13-14	15-8-9-10-11-12-13-14	15-0-1-2-3…13-14	15-16-17-18-19-20-21…
⋮	⋮	⋮	⋮	⋮	⋮
0	1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4…14-15	0-1-2-3-4-5-6…
1	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5…15-16	1-2-3-4-5-6-7…
2	1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6…15-16-17	2-3-4-5-6-7-8…
3	1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7…15-16-17-18	3-4-5-6-7-8-9…
4	1	4-5-6-7	4-5-6-7-8-9-10-11	4-5-6-7-8…15-6-17-18-19	4-5-6-7-8-9-10…
5	1	5-6-7-8	5-6-7-8-9-10-11-12	5-6-7-8-9…15-16-17-18-19-20	5-6-7-8-9-10-11…
6	1	6-7-8-9	6-7-8-9-10-11-12-13	6-7-8-9-10…15-16-17-18-19-20-21	6-7-8-9-10-11-12…
7	1	7-8-9-10	7-8-9-10-11-12-13-14	7-8-9-10…15-16-17-18-19-20-21-22	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮
14	1	14-15-16-17	14-15-16-17-18-19-20-21	14-15-16-17-18…28-29	14-15-16-17-18-19-20…
15	1	15-16-17-18	15-16-17-18-19-20-21-22	15-16-17-18-19…29-30	15-16-17-18-19-20-21…

Note:

1. The burst wrap bit (RCR.3) determines whether 4, 8 or 16-word burst-accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses.

6.4 Memory Map for Flash Memory

Bottom Parameter

		[A_{22-0}]
PLANE3	64-Kword Block 66	3F0000H - 3FFFFFH
	64-Kword Block 65	3E0000H - 3EFFFFH
	64-Kword Block 64	3D0000H - 3DFFFFH
	64-Kword Block 63	3C0000H - 3CFFFFH
	64-Kword Block 62	3B0000H - 3BFFFFH
	64-Kword Block 61	3A0000H - 3AFFFFH
	64-Kword Block 60	390000H - 39FFFFH
	64-Kword Block 59	380000H - 38FFFFH
	64-Kword Block 58	370000H - 37FFFFH
	64-Kword Block 57	360000H - 36FFFFH
	64-Kword Block 56	350000H - 35FFFFH
	64-Kword Block 55	340000H - 34FFFFH
	64-Kword Block 54	330000H - 33FFFFH
	64-Kword Block 53	320000H - 32FFFFH
	64-Kword Block 52	310000H - 31FFFFH
	64-Kword Block 51	300000H - 30FFFFH

PLANE3 : 16 Mbit

		[A_{22-0}]
PLANE1	64-Kword Block 34	1F0000H - 1FFFFFH
	64-Kword Block 33	1E0000H - 1EFFFFH
	64-Kword Block 32	1D0000H - 1DFFFFH
	64-Kword Block 31	1C0000H - 1CFFFFH
	64-Kword Block 30	1B0000H - 1BFFFFH
	64-Kword Block 29	1A0000H - 1AFFFFH
	64-Kword Block 28	190000H - 19FFFFH
	64-Kword Block 27	180000H - 18FFFFH
	64-Kword Block 26	170000H - 17FFFFH
	64-Kword Block 25	160000H - 16FFFFH
	64-Kword Block 24	150000H - 15FFFFH
	64-Kword Block 23	140000H - 14FFFFH
	64-Kword Block 22	130000H - 13FFFFH
	64-Kword Block 21	120000H - 12FFFFH
	64-Kword Block 20	110000H - 11FFFFH
	64-Kword Block 19	100000H - 10FFFFH

PLANE1 : 16 Mbit

		[A_{22-0}]
PLANE2	64-Kword Block 50	2F0000H - 2FFFFFH
	64-Kword Block 49	2E0000H - 2EFFFFH
	64-Kword Block 48	2D0000H - 2DFFFFH
	64-Kword Block 47	2C0000H - 2CFFFFH
	64-Kword Block 46	2B0000H - 2BFFFFH
	64-Kword Block 45	2A0000H - 2AFFFFH
	64-Kword Block 44	290000H - 29FFFFH
	64-Kword Block 43	280000H - 28FFFFH
	64-Kword Block 42	270000H - 27FFFFH
	64-Kword Block 41	260000H - 26FFFFH
	64-Kword Block 40	250000H - 25FFFFH
	64-Kword Block 39	240000H - 24FFFFH
	64-Kword Block 38	230000H - 23FFFFH
	64-Kword Block 37	220000H - 22FFFFH
	64-Kword Block 36	210000H - 21FFFFH
	64-Kword Block 35	200000H - 20FFFFH

PLANE2 : 16 Mbit

		[A_{22-0}]
PLANE0	64-Kword Block 18	0F0000H - 0FFFFFH
	64-Kword Block 17	0E0000H - 0EFFFFH
	64-Kword Block 16	0D0000H - 0DFFFFH
	64-Kword Block 15	0C0000H - 0CFFFFH
	64-Kword Block 14	0B0000H - 0BFFFFH
	64-Kword Block 13	0A0000H - 0AFFFFH
	64-Kword Block 12	090000H - 09FFFFH
	64-Kword Block 11	080000H - 08FFFFH
	64-Kword Block 10	070000H - 07FFFFH
	64-Kword Block 9	060000H - 06FFFFH
	64-Kword Block 8	050000H - 05FFFFH
	64-Kword Block 7	040000H - 04FFFFH
	64-Kword Block 6	030000H - 03FFFFH
	64-Kword Block 5	020000H - 02FFFFH
	64-Kword Block 4	010000H - 01FFFFH
	16-Kword Block 3	00C000H - 00FFFFH
	16-Kword Block 2	008000H - 00BFFFH
	16-Kword Block 1	004000H - 007FFFH
	16-Kword Block 0	000000H - 003FFFH

PLANE0 : 16 Mbit

Bottom Parameter (Cont)

		[A_{22-0}]
PLANE7	64-Kword Block 130	7F0000H - 7FFFFFH
	64-Kword Block 129	7E0000H - 7EFFFFH
	64-Kword Block 128	7D0000H - 7DFFFFH
	64-Kword Block 127	7C0000H - 7CFFFFH
	64-Kword Block 126	7B0000H - 7BFFFFH
	64-Kword Block 125	7A0000H - 7AFFFFH
	64-Kword Block 124	790000H - 79FFFFH
	64-Kword Block 123	780000H - 78FFFFH
	64-Kword Block 122	770000H - 77FFFFH
	64-Kword Block 121	760000H - 76FFFFH
	64-Kword Block 120	750000H - 75FFFFH
	64-Kword Block 119	740000H - 74FFFFH
	64-Kword Block 118	730000H - 73FFFFH
	64-Kword Block 117	720000H - 72FFFFH
	64-Kword Block 116	710000H - 71FFFFH
	64-Kword Block 115	700000H - 70FFFFH

PLANE7 : 16 Mbit

		[A_{22-0}]
PLANE5	64-Kword Block 98	5F0000H - 5FFFFFH
	64-Kword Block 97	5E0000H - 5EFFFFH
	64-Kword Block 96	5D0000H - 5DFFFFH
	64-Kword Block 95	5C0000H - 5CFFFFH
	64-Kword Block 94	5B0000H - 5BFFFFH
	64-Kword Block 93	5A0000H - 5AFFFFH
	64-Kword Block 92	590000H - 59FFFFH
	64-Kword Block 91	580000H - 58FFFFH
	64-Kword Block 90	570000H - 57FFFFH
	64-Kword Block 89	560000H - 56FFFFH
	64-Kword Block 88	550000H - 55FFFFH
	64-Kword Block 87	540000H - 54FFFFH
	64-Kword Block 86	530000H - 53FFFFH
	64-Kword Block 85	520000H - 52FFFFH
	64-Kword Block 84	510000H - 51FFFFH
	64-Kword Block 83	500000H - 50FFFFH

PLANE5 : 16 Mbit

		[A_{22-0}]
PLANE6	64-Kword Block 114	6F0000H - 6FFFFFH
	64-Kword Block 113	6E0000H - 6EFFFFH
	64-Kword Block 112	6D0000H - 6DFFFFH
	64-Kword Block 111	6C0000H - 6CFFFFH
	64-Kword Block 110	6B0000H - 6BFFFFH
	64-Kword Block 109	6A0000H - 6AFFFFH
	64-Kword Block 108	690000H - 69FFFFH
	64-Kword Block 107	680000H - 68FFFFH
	64-Kword Block 106	670000H - 67FFFFH
	64-Kword Block 105	660000H - 66FFFFH
	64-Kword Block 104	650000H - 65FFFFH
	64-Kword Block 103	640000H - 64FFFFH
	64-Kword Block 102	630000H - 63FFFFH
	64-Kword Block 101	620000H - 62FFFFH
	64-Kword Block 100	610000H - 61FFFFH
	64-Kword Block 99	600000H - 60FFFFH

PLANE6 : 16 Mbit

		[A_{22-0}]
PLANE4	64-Kword Block 82	4F0000H - 4FFFFFH
	64-Kword Block 81	4E0000H - 4EFFFFH
	64-Kword Block 80	4D0000H - 4DFFFFH
	64-Kword Block 79	4C0000H - 4CFFFFH
	64-Kword Block 78	4B0000H - 4BFFFFH
	64-Kword Block 77	4A0000H - 4AFFFFH
	64-Kword Block 76	490000H - 49FFFFH
	64-Kword Block 75	480000H - 48FFFFH
	64-Kword Block 74	470000H - 47FFFFH
	64-Kword Block 73	460000H - 46FFFFH
	64-Kword Block 72	450000H - 45FFFFH
	64-Kword Block 71	440000H - 44FFFFH
	64-Kword Block 70	430000H - 43FFFFH
	64-Kword Block 69	420000H - 42FFFFH
	64-Kword Block 68	410000H - 41FFFFH
	64-Kword Block 67	400000H - 40FFFFH

PLANE4 : 16 Mbit

6.5 DC Electrical Characteristics for Flash Memory

DC Electrical Characteristics

(T_A = -25°C to +85°C, F-V_{CC} = 1.7V to 1.95V, V_{CCQ} = 1.7V to 1.95V)

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		6		6	8	pF	V_{IN} = 0V, f = 1MHz, T_A=25°C
C_{IO}	I/O Capacitance		6		6	10	pF	$V_{I/O}$ = 0V, f = 1MHz, T_A=25°C
I_{LI}	Input Leakage Current		1			±1.0	µA	F-V_{CC} = F-V_{CC} Max., V_{CCQ} = V_{CCQ} Max., $V_{I/O}$ = V_{CCQ} or GND
I_{LO}	Output Leakage Current		1			±1.0	µA	
I_{CCS}	F-V_{CC} Standby Current		1, 9		20	60	µA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = $\overline{RST}$ = V_{CCQ} , $\overline{WP}$, $\overline{ADV}$ = V_{CCQ} or GND
I_{CCAS}	F-V_{CC} Automatic Power Savings Current		1, 5, 9		20	60	µA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = GND ±0.2V, $\overline{WP}$, $\overline{ADV}$ = V_{CCQ} or GND
I_{CCD}	F-V_{CC} Reset Current		1, 9		20	60	µA	$\overline{RST}$ = GND ±0.2V
I_{CCR}	Average F-V_{CC} Read Current Normal Mode		1, 8, 9		18	22	mA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = V_{IL}, F-$\overline{OE}$ = V_{IH}, f = 5MHz
	Average F-V_{CC} Read Current Page Mode	8 Word Read	1, 8, 9		2.5	3	mA	
	Average F-V_{CC} Read Current Synchronous CLK = 54 MHz	Burst Length = 4	1,3,8,9		15	18	mA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = V_{IL}, F-$\overline{OE}$ = V_{IH}, f = 54 MHz
		Burst Length = 8	1,3,8,9		18	22	mA	
		Burst Length = 16	1,3,8,9		21	25	mA	
		Burst Length = Continuous	1,3,8,9		22	27	mA	
I_{CCW}	F-V_{CC} (Page Buffer) Program, Buffered Advanced Factory Program Current		1,6,8,9		20	70	mA	V_{PP} = V_{PPH1}
			1,6,8,9		14	50	mA	V_{PP} = V_{PPH2}
I_{CCE}	F-V_{CC} Block Erase Current		1,6,8,9		35	50	mA	V_{PP} = V_{PPH1}
			1,6,8,9		25	32	mA	V_{PP} = V_{PPH2}
I_{CCWS} I_{CCES}	F-V_{CC} (Page Buffer) Program or Block Erase Suspend Current		1,2,8,9		10	200	µA	F-$\overline{CE}$ = V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current		1,7,8,9		2	5	µA	V_{PP} ≤ F-V_{CC}
I_{PPW}	V_{PP} (Page Buffer) Program, Buffered Advanced Factory Program Current		1,6,7,8,9		2	5	µA	V_{PP} = V_{PPH1}
			1,6,7,8,9		0.8	1	mA	V_{PP} = V_{PPH2}
I_{PPE}	V_{PP} Block Erase Current		1,6,7,8,9		2	5	µA	V_{PP} = V_{PPH1}
			1,6,7,8,9		5	15	mA	V_{PP} = V_{PPH2}
I_{PPWS}	V_{PP} (Page Buffer) Program Suspend Current		1,7,8,9		2	5	µA	V_{PP} = V_{PPH1}
			1,7,8,9		10	200	µA	V_{PP} = V_{PPH2}
I_{PPES}	V_{PP} Block Erase Suspend Current		1,7,8,9		2	5	µA	V_{PP} = V_{PPH1}
			1,7,8,9		10	200	µA	V_{PP} = V_{PPH2}

DC Electrical Characteristics (Continued)

(T_A = -25°C to +85°C, F-V_{CC} = 1.7V to 1.95V, V_{CCQ} = 1.7V to 1.95V)

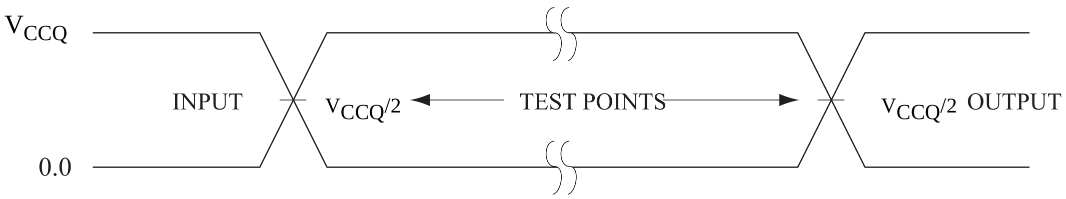
Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	6	-0.2		0.4	V	
V_{IH}	Input High Voltage	6	V_{CCQ} -0.3		V_{CCQ}	V	
V_{OL}	Output Low Voltage	6			0.1	V	F-V_{CC}=F-V_{CC}Min., V_{CCQ} = V_{CCQ}Min., I_{OL} = 100µA
V_{OH}	Output High Voltage	6	V_{CCQ} -0.1			V	F-V_{CC}=F-V_{CC}Min., V_{CCQ} = V_{CCQ}Min., I_{OH} = -100µA
V_{PPLK}	V_{PP} Lockout Voltage during Normal Operations	4,6,7			0.4	V	
V_{PPH1}	V_{PP} during Block Erase, (Page Buffer) Program or OTP Program Operations	7	0.9		V_{CCQ}	V	
V_{PPH2}	F-V_{CC} during Block Erase, Buffered Advanced Factory Program, (Page Buffer) Program or OTP Program Operations	7	8.5	9.0	9.5	V	
V_{LKO}	F-V_{CC} Lockout Voltage		1.0			V	

Notes:

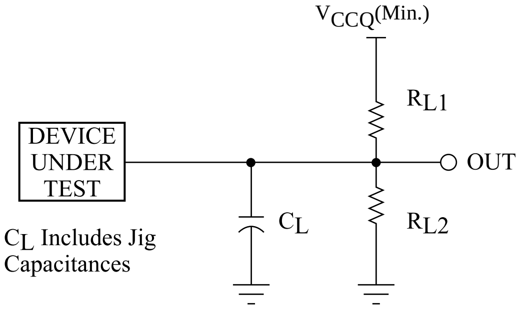
1. All currents are in RMS unless otherwise noted. Typical values are the reference values at F-V_{CC} = 1.8V, V_{CCQ} = 1.8V, T_A = +25°C unless F-V_{CC} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
3. The burst wrap bit (RCR.3) determines whether 4, 8 or 16-word burst-accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses.
4. Block erase, buffered advanced factory program, (page buffer) program and OTP Program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (Max.) and V_{PPH1} (Min.), between V_{PPH1} (Max.) and V_{PPH2} (Min.), and above V_{PPH2} (Max.).
5. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
6. Sampled, not 100% tested.
7. V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, buffered advanced factory program, (page buffer) program and OTP Program cannot be executed and should not be attempted.
   Applying 9.0V±0.5V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the F-V_{CC} power bus.
   Applying 9.0V±0.5V to V_{PP} during erase/program can only be done for a maximum of 1,000 cycles on each block. V_{PP} may be connected to 9.0V±0.5V for a total of 80 hours maximum.
8. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
9. For all pins other than those shown in test conditions, input level is V_{CCQ} or GND±0.2V.

6.6 AC Electrical Characteristics for Flash Memory

6.6.1 AC Test Conditions



AC test inputs are driven at V_{CCQ} (Min.) for a Logic “1” and 0.0V for a Logic “0”.
Input timing begins, and output timing ends at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5ns.
Worst case speed conditions are when F-V_{CC} = F-V_{CC} (Min.).



F-V_{CC} = 1.7V to 1.95V
CL = 50 pF
R_{L1} = 15.0kΩ
R_{L2} = 15.0 kΩ

6.6.2 Read-Only Operations

(T_A = -25°C to +85°C, F-V_{CC} = 1.7V to 1.95V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{CLK}	CLK Period		18.5		ns
t_{CH} (t_{CL})	CLK High (Low) Time		3		ns
t_{CHCL} (t_{CLCH})	CLK Fall (Rise) Time			2	ns
t_{AVCH}	Address Setup to CLK		7		ns
t_{VLCH}	$\overline{\text{ADV}}$ Setup to CLK	4	7		ns
t_{ELCH}	F-$\overline{\text{CE}}$ Setup to CLK	4	7		ns
t_{CHQV}	CLK to Output Delay			14	ns
t_{CHQX}	Output Hold from CLK		3		ns
t_{CHAX}	Address Hold from CLK		10		ns
t_{CHTV}	CLK to WAIT Valid			14	ns
t_{ELTV}	F-$\overline{\text{CE}}$ Low to WAIT Valid			15	ns
t_{EHTZ}	F-$\overline{\text{CE}}$ High to WAIT High-Z			15	ns
t_{GLTV}	F-$\overline{\text{OE}}$ Low to WAIT Valid			15	ns
t_{GHTZ}	F-$\overline{\text{OE}}$ High to WAIT High-Z			15	ns
t_{EHIGH}	F-$\overline{\text{CE}}$ High between Subsequent Synchronous Reads	2	18.5		ns
t_{AVVH}	Address Setup to $\overline{\text{ADV}}$		7		ns
t_{ELVH}	F-$\overline{\text{CE}}$ Setup to $\overline{\text{ADV}}$		10		ns
t_{AVAV}	Read Cycle Time		85		ns
t_{AVQV}	Address to Output Delay			85	ns
t_{ELQV}	F-$\overline{\text{CE}}$ to Output Delay	3		85	ns
t_{VLQV}	$\overline{\text{ADV}}$ to Output Delay			85	ns
t_{VLVH}	$\overline{\text{ADV}}$ Pulse Width Low		10		ns
t_{VHVL}	$\overline{\text{ADV}}$ Pulse Width High		10		ns
t_{VHAX}	Address Hold from $\overline{\text{ADV}}$		10		ns
t_{APA}	Page Address Access Time			25	ns
t_{GLQV}	F-$\overline{\text{OE}}$ to Output Delay	3		15	ns
t_{PHQV}	$\overline{\text{RST}}$ High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	F-$\overline{\text{CE}}$ or F-$\overline{\text{OE}}$ to Output in High-Z, Whichever Occurs First	1		15	ns
t_{ELQX}	F-$\overline{\text{CE}}$ to Output in Low-Z	1	0		ns
t_{GLQX}	F-$\overline{\text{OE}}$ to Output in Low-Z	1	0		ns
t_{OH}	Output Hold from First Occurring Address, F-$\overline{\text{CE}}$ or F-$\overline{\text{OE}}$ change	1	0		ns

Notes:

1. Sampled, not 100% tested.
2. Applies only to subsequent synchronous reads.
3. F-$\overline{\text{OE}}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of F-$\overline{\text{CE}}$ without impact to t_{ELQV}.
4. Setup time (t_{VLCH}, t_{ELCH}) is defined from the first clock edge after driving $\overline{\text{ADV}}$ or F-$\overline{\text{CE}}$ low (whichever goes low last).

6.6.3 Write Operations (1, 2)

(T_A = -25°C to +85°C, F-V_{CC} = 1.7V to 1.95V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		85		ns
t_{PHWL} (t_{PHEL})	$\overline{\text{RST}}$ High Recovery to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	F-$\overline{\text{CE}}$ (F-$\overline{\text{WE}}$) Setup to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going Low		0		ns
t_{WLWH} (t_{ELEH})	F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Pulse Width	4	40		ns
t_{VLVH}	$\overline{\text{ADV}}$ Pulse Width		10		ns
t_{DVWH} (t_{DVEH})	Data Setup to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going High	8	40		ns
t_{VLWH} (t_{VLEH})	$\overline{\text{ADV}}$ Setup to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going High		40		ns
t_{AVVH}	Address Setup to $\overline{\text{ADV}}$ High		6		ns
t_{WHEH} (t_{EHWH})	F-$\overline{\text{CE}}$ (F-$\overline{\text{WE}}$) Hold from F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) High		0		ns
t_{VHAX}	Address Hold from $\overline{\text{ADV}}$ High		10		ns
t_{WHWL} (t_{EHEL})	F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Pulse Width High	5	15		ns
t_{SHWH} (t_{SHEH})	$\overline{\text{WP}}$ High Setup to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going High	3	0		ns
t_{VVWH} (t_{VVEH})	V_{PP} Setup to F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		0		ns
t_{QVSL}	$\overline{\text{WP}}$ High Hold from Valid SRD	3, 6	0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD	3, 6	0		ns
t_{WHR0} (t_{EHR0})	F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) high to SR.7 Going “0”	3		t_{AVQV}+35	ns
t_{WHQVR} (t_{EHQVR})	F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) high to Output Delay	3, 7		t_{AVQV}+35	ns

Notes:

1. The timing characteristics for reading the status register during block erase, buffered advanced factory program, (page buffer) program and OTP Program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$ (whichever goes low last) to the rising edge of F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$ (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$ (whichever goes high first) to the falling edge of F-$\overline{\text{CE}}$ or F-$\overline{\text{WE}}$ (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. V_{PP} should be held at $V_{PP}=V_{PPH1/2}$ until determination of block erase, (page buffer) program or OTP program success (SR.1/3/4/5=0) and held at $V_{PP}=V_{PPH2}$ until determination of buffered advanced factory program success (SR.0/1/3/4=0).
7. The delay time from F-$\overline{\text{WE}}$ (F-$\overline{\text{CE}}$) high to valid data output.
8. Refer to 6.2.1 Command Definitions for valid address and data for block erase, buffered advanced factory program, (page buffer) program, OTP program or lock bit configuration.

6.6.4 Block Erase, (Page Buffer) Program, Buffered Advanced Factory Program and OTP Program Performance (3)

(T_A = -25°C to +85°C, F-V_{CC} = 1.7V to 1.95V)

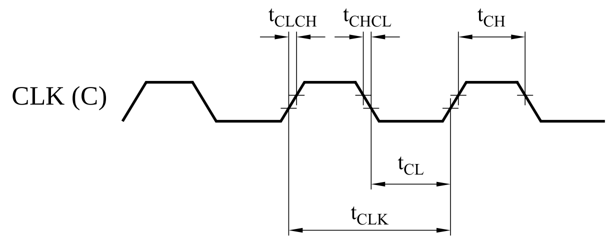
Symbol	Parameter	Notes	PBP (Page Buffer) is Used,BAFP (Buffered Advanced Factory Program) is Used or not	$V_{PP}=V_{PPH1}$ (In System)			$V_{PP}=V_{PPH2}$ (In Manufacturing)			Unit
				Min.	Typ.(1)	Max.(2)	Min.	Typ.(1)	Max.(2)	
t_{WPB}	16K-Word Parameter Block Program Time	2	-		2.55	7.65		2.55	7.65	s
		2	PBP		0.33	0.99		0.29	0.87	s
		2, 6, 7	BAFP	N/A	N/A	N/A		1.14	3.42	s
t_{WMB}	64K-Word Main Block Program Time	2	-		9.84	29.52		9.84	29.52	s
		2	PBP		1.31	3.93		1.18	3.54	s
		2, 6	BAFP	N/A	N/A	N/A		1.14	3.42	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	-		150	450		150	450	µs
		2	PBP		20	60		20	60	µs
		2, 6	BAFP	N/A	N/A	N/A		19.4	58.2	µs
t_{WHOV1}/ t_{EHOV1}	OTP Program Time	2	-		170	510		155	465	µs
t_{WHQV2}/ t_{EHQV2}	16K-Word Parameter Block Erase Time	2	-		0.4	2.5		0.4	2.5	s
t_{WHQV3}/ t_{EHQV3}	64K-Word Main Block Erase Time	2	-		1	4		0.9	4	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		20	40		20	40	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		20	40		20	40	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			500			µs
t_{BRES}	Latency Time for BAFP Set-UP	2, 6	BAFP	N/A	N/A	N/A		10	15	µs

Notes:

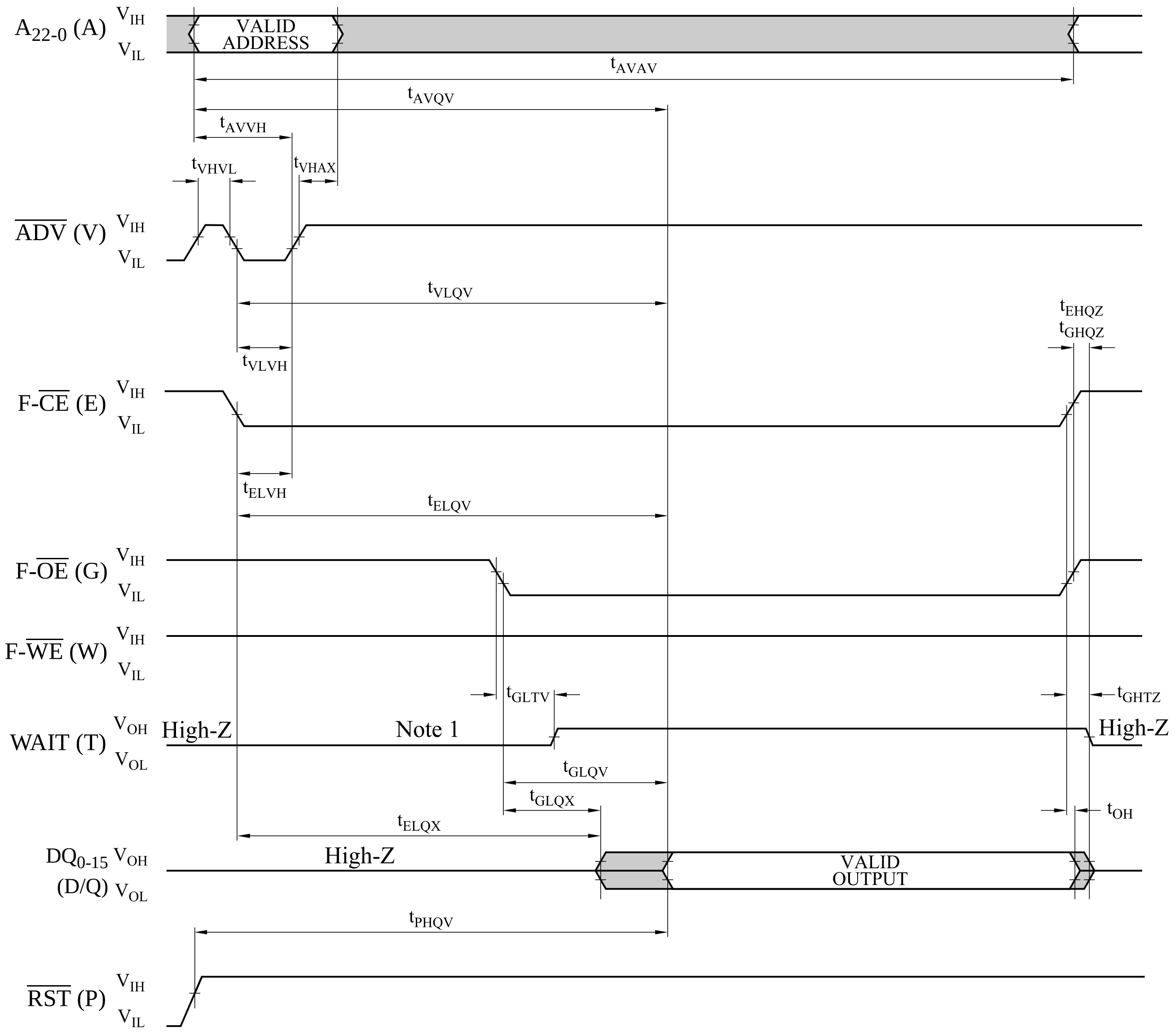
1. Typical values measured at F-V_{CC} = 1.8V, V_{PP} = 1.8V or 9.0V, and T_A = +25°C Assumes corresponding block lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (F-$\overline{WE}$ or F-$\overline{CE}$ going high) until SR.7 going “1”.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.
6. BAFP mode is allowed only when T_A=+20°C to +30°C.
7. BAFP mode, eight 16K-word parameter blocks are programmed at a time. Specification shown above is the program time per each 16K-word parameter block.

6.6.5 Flash Memory AC Characteristics Timing Chart

AC Waveform for CLK Input



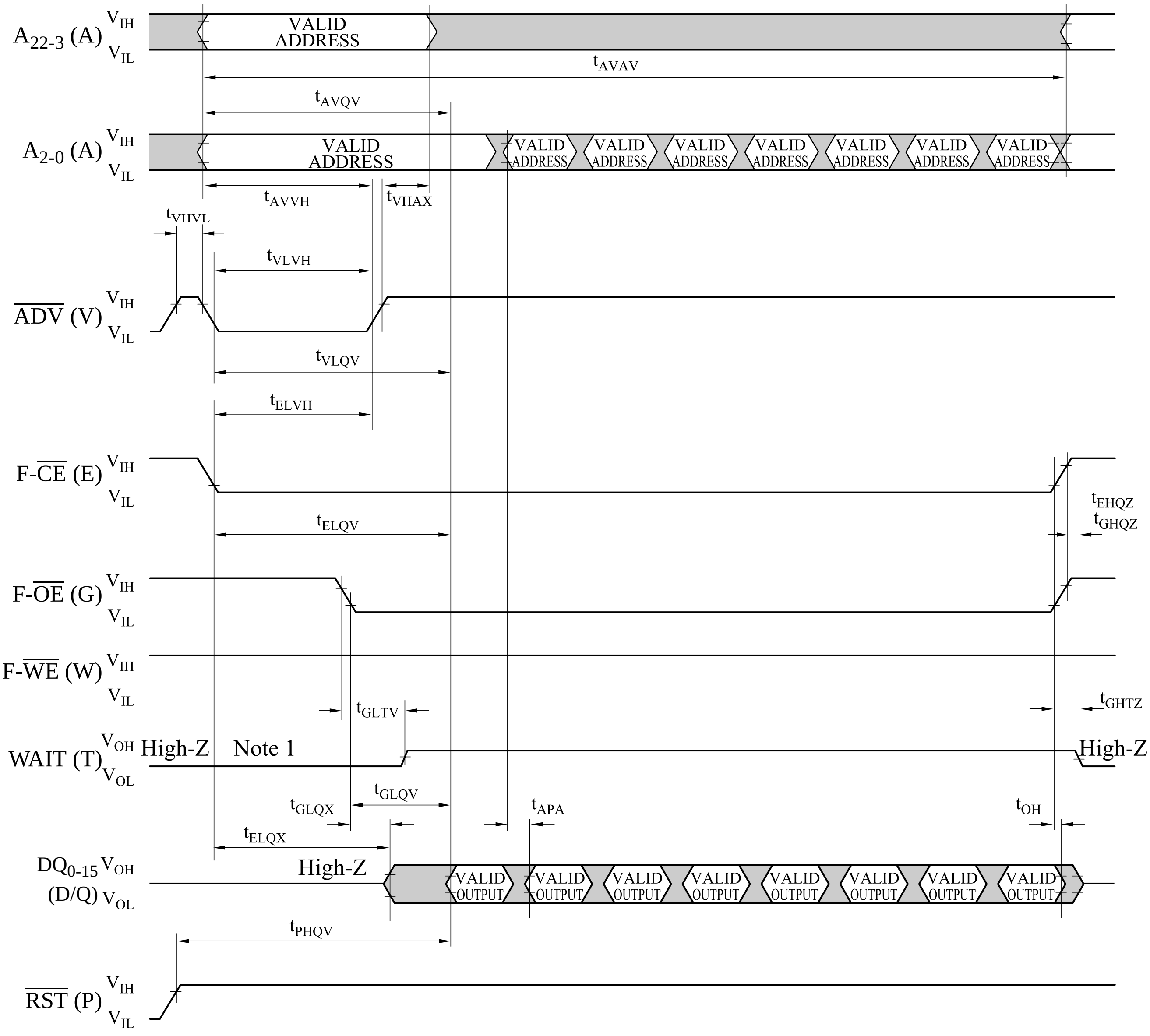
AC Waveform for single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code



Note:

1. This waveform illustrates the case when RCR.10 = “0”.

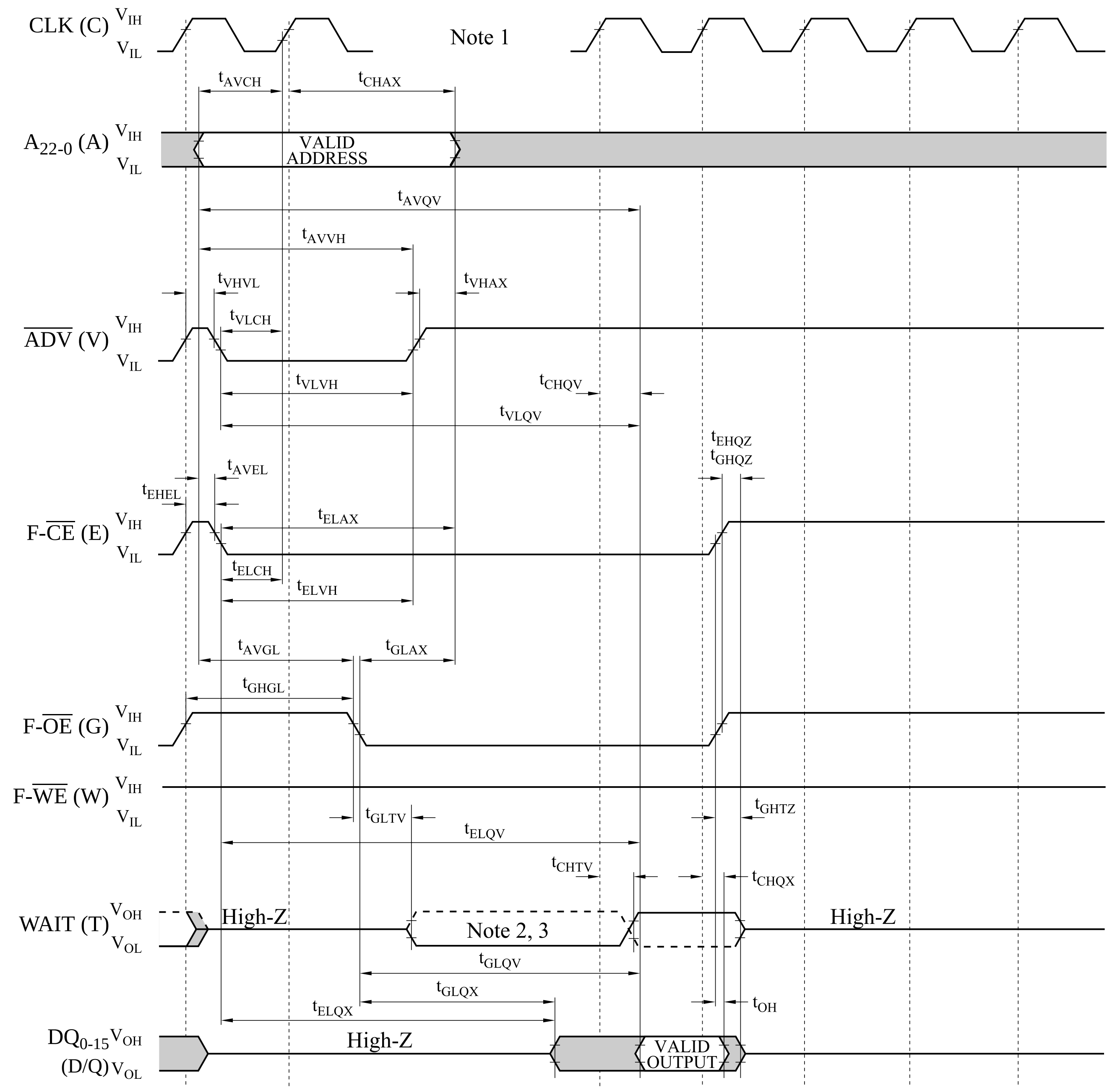
AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



Note:

1. This waveform illustrates the case when RCR.10 = “0”.

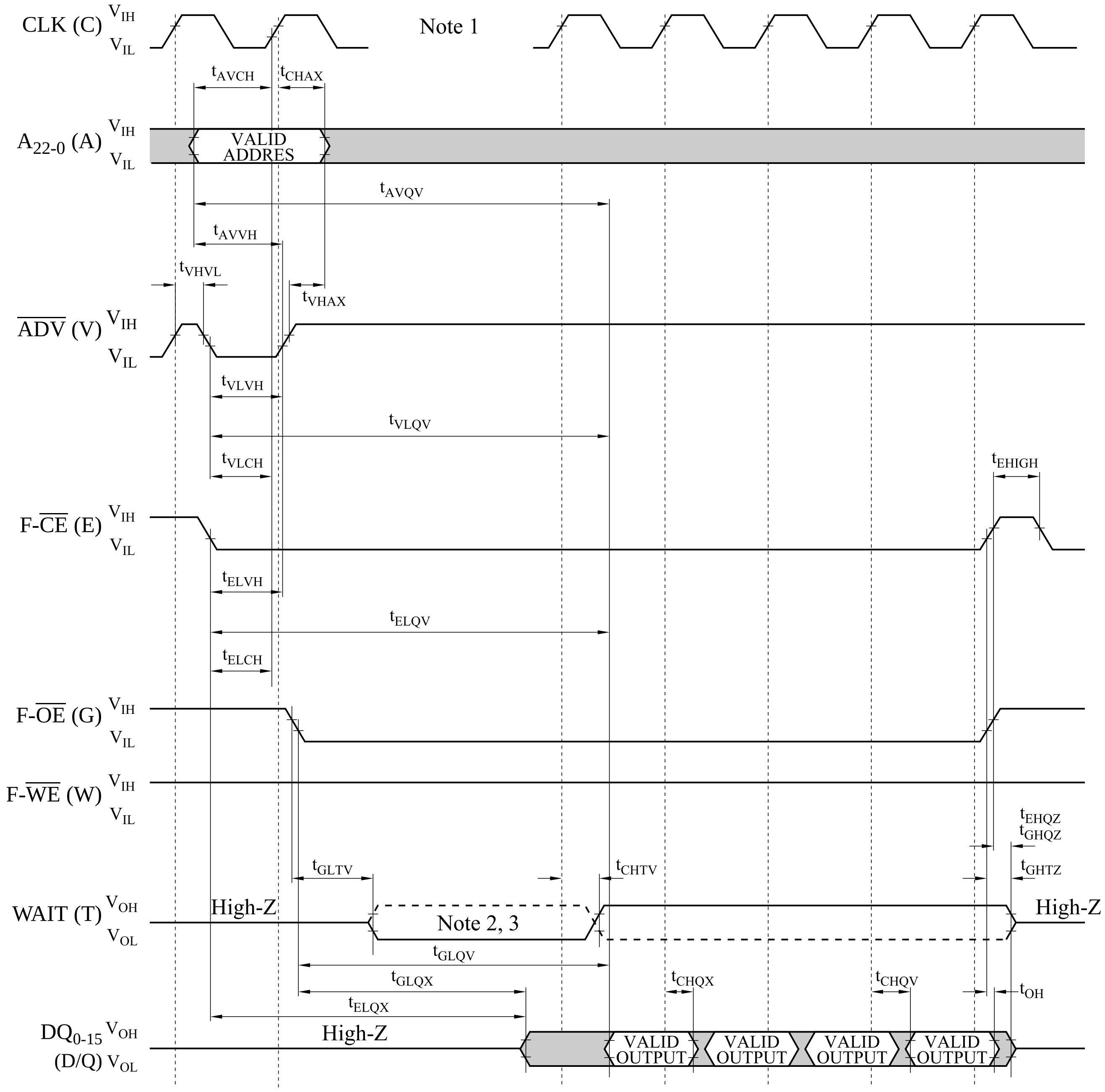
AC Waveform for Single Synchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code



Notes:

1. Depending upon the frequency configuration code in the read configuration register, insert clock cycles:
   - Frequency Configuration Code 2, insert two clock cycles•Frequency Configuration Code 5, insert five clock cycles
   - Frequency Configuration Code 3, insert three clock cycles•Frequency Configuration Code 6, insert six clock cycles
   - Frequency Configuration Code 4, insert four clock cycles•Frequency Configuration Code 7, insert seven clock cycles
2. WAIT configuration allows assertion one CLK cycle before or during an output delay.
3. This waveform illustrates the case when RCR.10 = “0”.

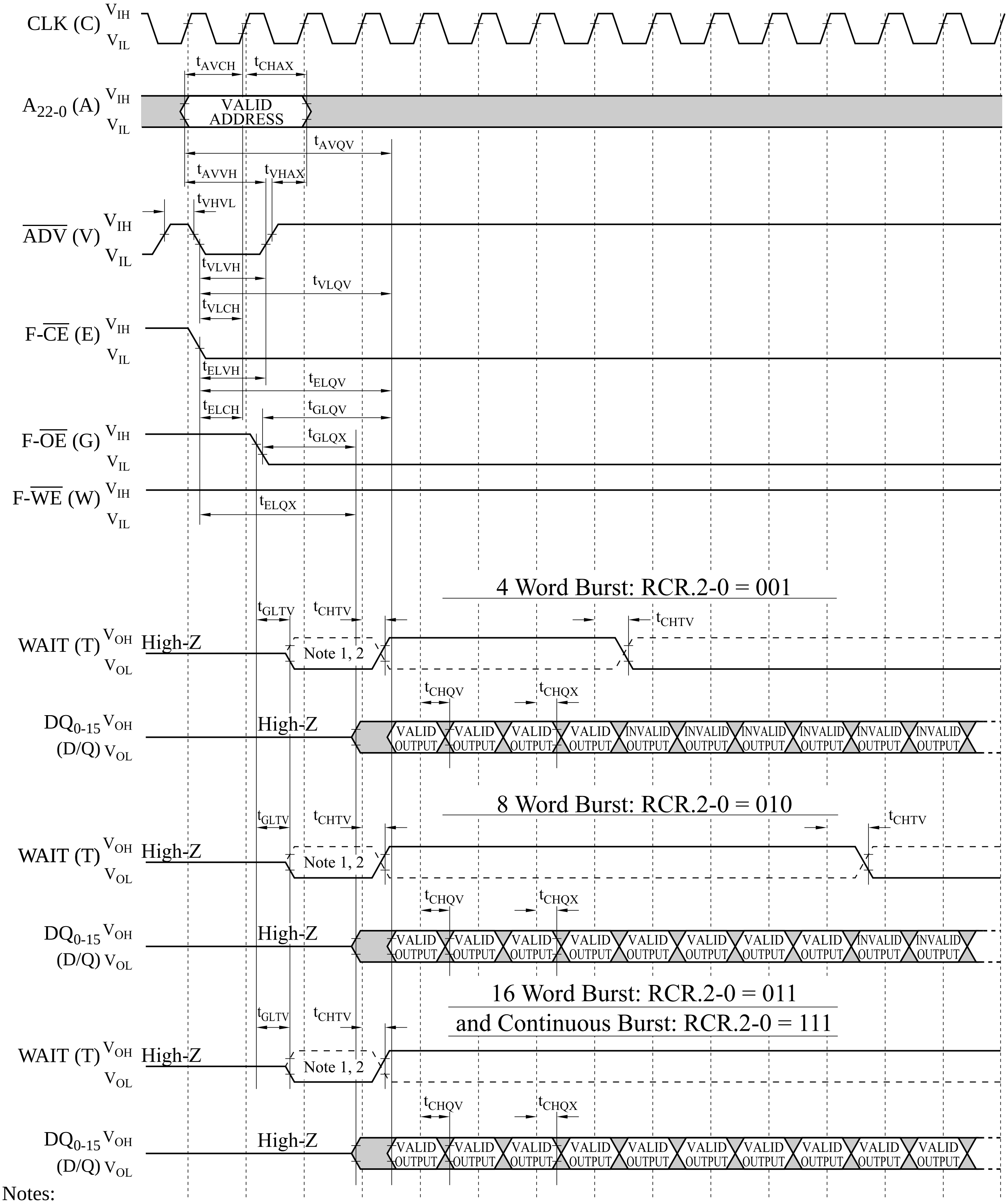
AC Waveform for Synchronous Burst Mode Read Operations from Main Blocks or Parameter Blocks
(4 Word Burst: RCR.2-0=001)



Notes:

1. Depending upon the frequency configuration code in the read configuration register, insert clock cycles:
   - Frequency Configuration Code 2, insert two clock cycles•Frequency Configuration Code 5, insert five clock cycles
   - Frequency Configuration Code 3, insert three clock cycles•Frequency Configuration Code 6, insert six clock cycles
   - Frequency Configuration Code 4, insert four clock cycles•Frequency Configuration Code 7, insert seven clock cycles
2. WAIT configuration allows assertion one CLK cycle before or during an output delay.
3. This waveform illustrates the case when RCR.10 = “0”.

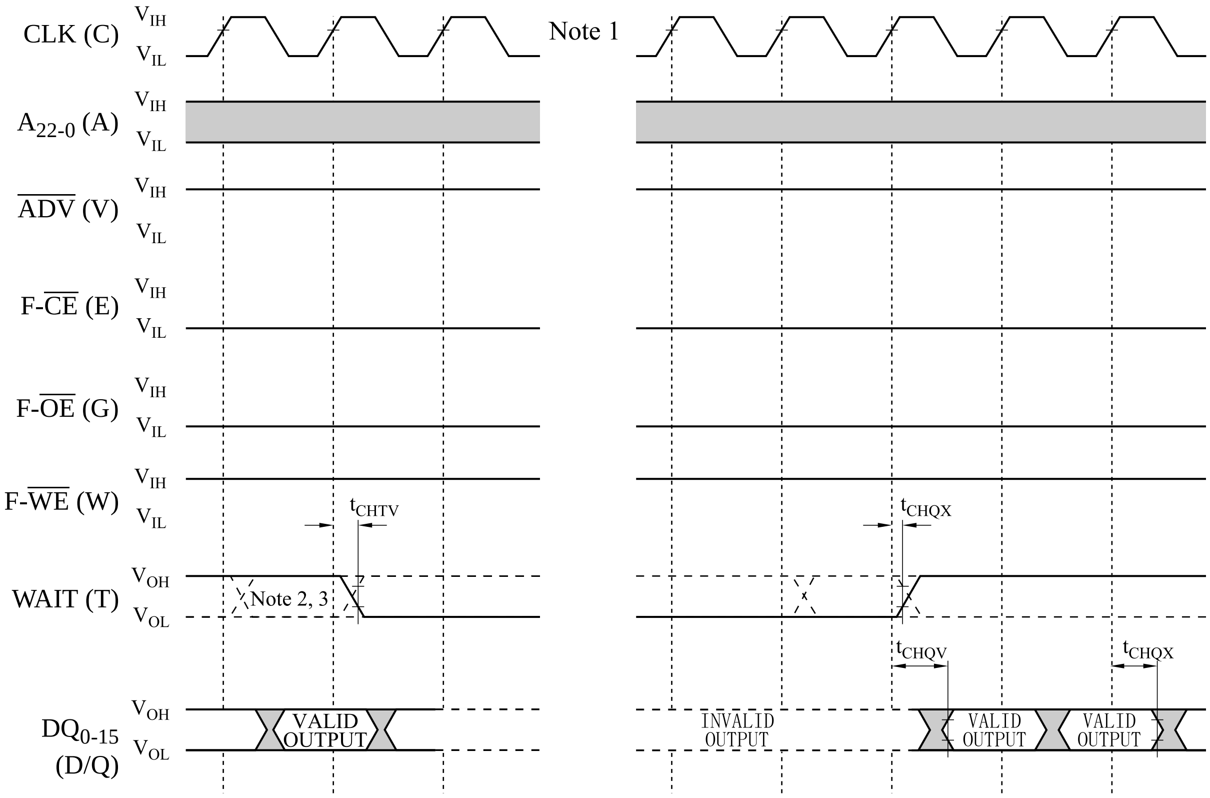
AC Waveform for Synchronous Burst Mode Read Operations from Main Blocks or Parameter Blocks
(Frequency Configuration: RCR.13-11=010)



Notes:

1. WAIT configuration allows assertion one CLK cycle before or during an output delay.
2. This waveform illustrates the case when RCR.10 = “0”.

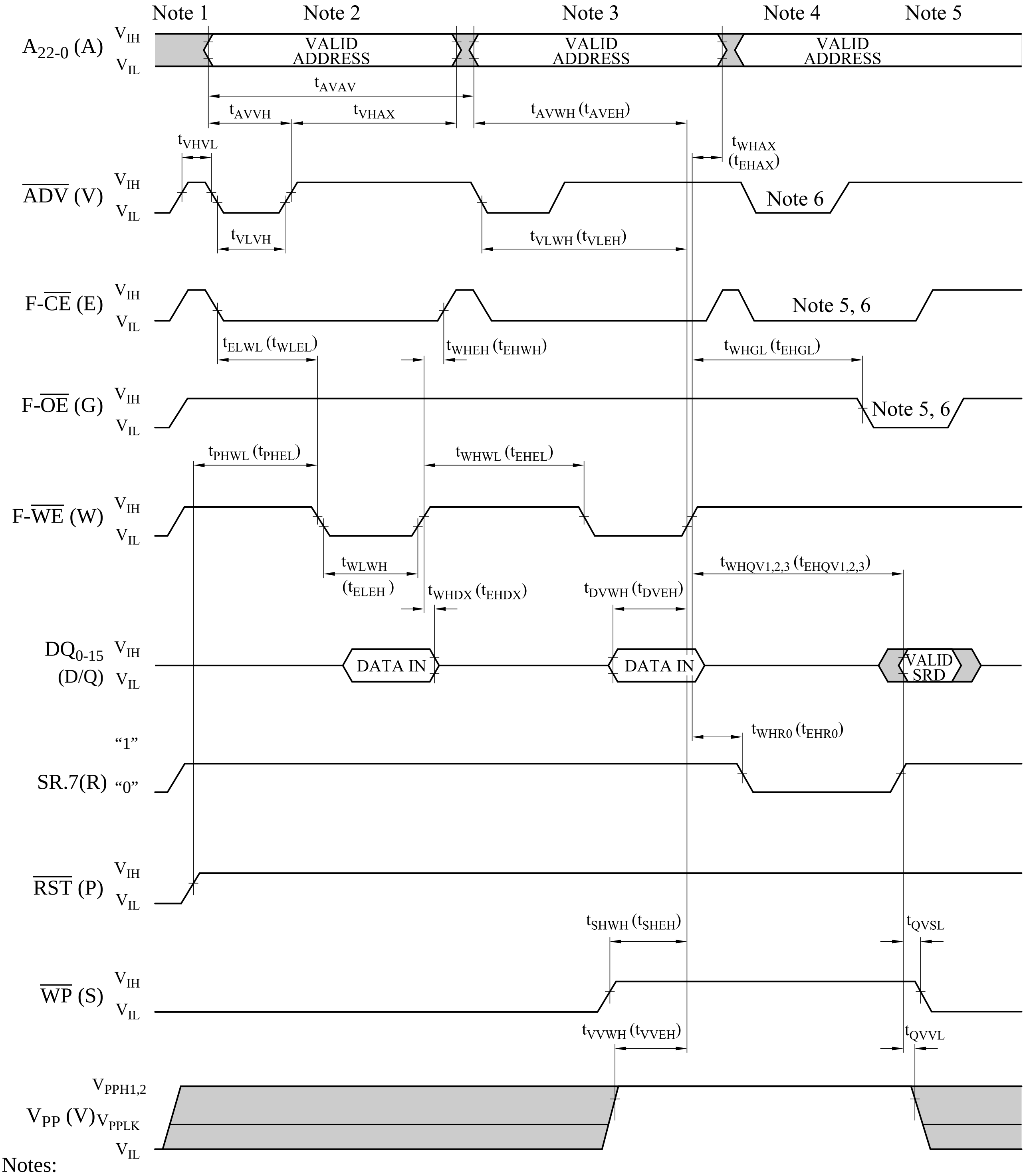
AC Waveform for an Output Delay when Continuous Burst Read with Data Output Configurations Set to One Clock



Notes:

1. This delay occurs only in continuous burst mode or 4, 8, 16-Word burst with no-wrap mode.
2. WAIT configuration allows assertion one CLK cycle before or during an output delay.
3. This waveform illustrates the case when RCR.10 = “0”.

AC Waveform for Write Operations



Notes:

1. $F\text{-}V_{CC}$ power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, F-$\overline{OE}$, F-$\overline{CE}$ and $\overline{ADV}$ must be driven active F-$\overline{WE}$ de-asserted.

6.6.6 Reset Operations

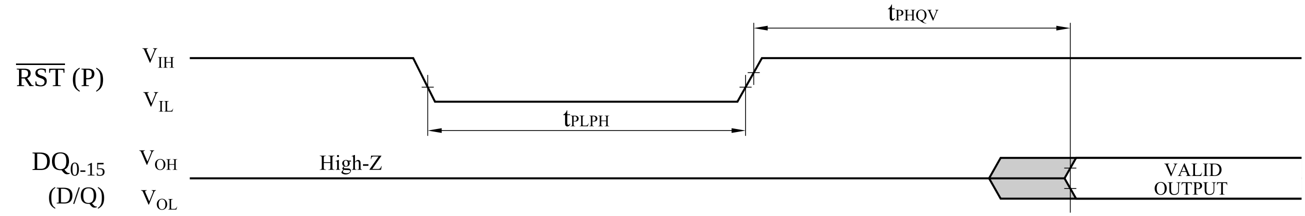
(T_A = -25°C to +85°C, F-V_{CC} = 1.7V to 1.95V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	$\overline{\text{RST}}$ Low to Reset during Read ($\overline{\text{RST}}$ should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	$\overline{\text{RST}}$ Low to Reset during Erase or Program	1, 3, 4		40	µs
t_{2VPH}	F-V_{CC} = 1.7V to $\overline{\text{RST}}$ High	1, 3, 5	100		ns
t_{VHQV}	F-V_{CC} = 1.7V to Output Delay	3		1	ms
t_{VHWL}	F-V_{CC} = 1.7V to F-$\overline{\text{WE}}$ Low	3		1	ms

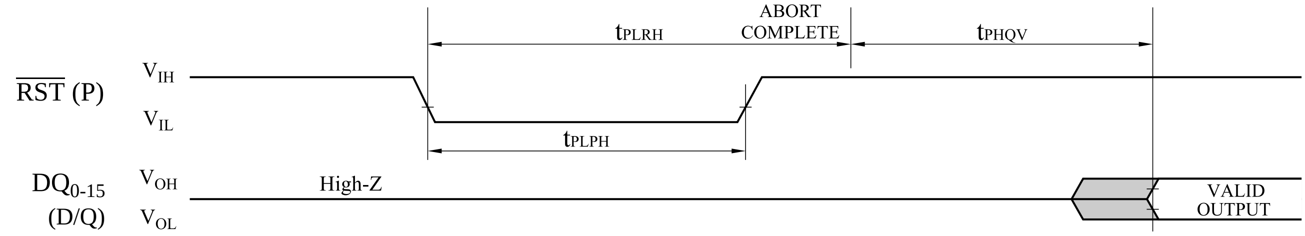
Notes:

1. A reset time, t_{PHQV}, is required from the later of erase (or program) abortion completed or $\overline{\text{RST}}$ going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If $\overline{\text{RST}}$ asserted while a block erase, buffered advanced factory program, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding $\overline{\text{RST}}$ low minimum 100ns is required after F-V_{CC} has been in predefined range and also has been in stable there.

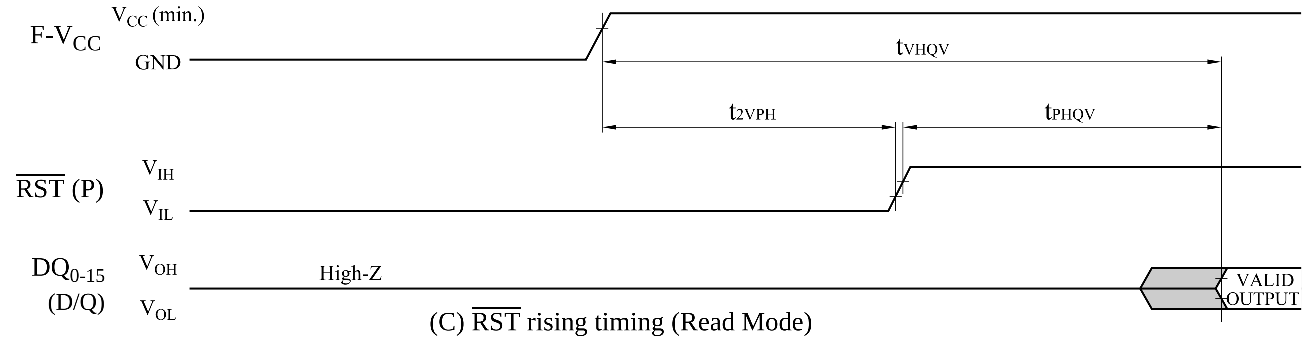
AC Waveform for Reset Operations



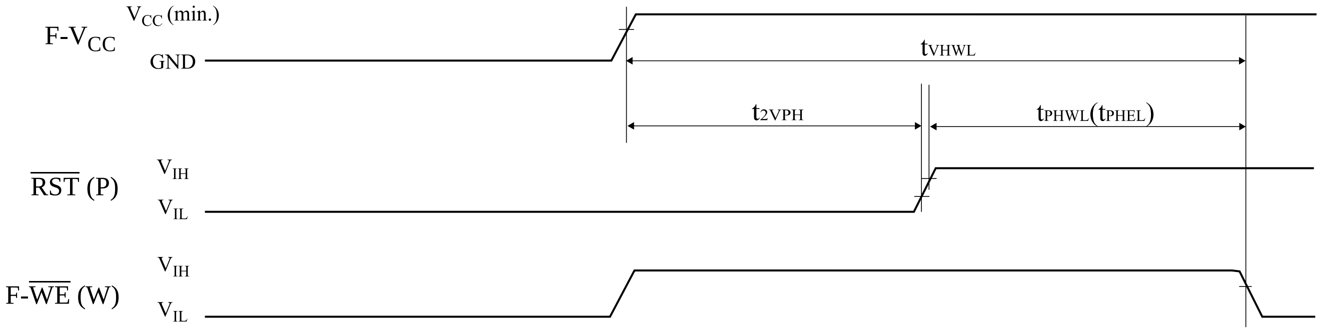
(A) Reset during Read Array Mode



(B) Reset during Erase or Program Mode



(C) $\overline{RST}$ rising timing (Read Mode)



(D) $\overline{RST}$ rising timing (Erase or Program Mode)

7. SmartCombo RAM

7.1 Truth Table

7.1.1 Bus Operation (1)

Mode	Notes	SC-$\overline{\text{CE}}_1$	SC-$\overline{\text{WE}}$	SC-$\overline{\text{OE}}$	$\overline{\text{LB}}$/ $\overline{\text{UB}}$	MODE	$\text{DQ}_{0\text{-}15}$	Power
Standby	3, 6	H	X	X	X	H	High-Z	Standby
Read	2, 5	L	H	L	L	H	Data-Out	Active
Write	2, 4, 5	L	L	X	L	H	Data-In	
No Operation	5, 6	L	X	X	X	H	X	Idle
DPD	7	H	X	X	X	L	High-Z	Deep Power-Down
Load Configuration Register		L	L	X	X	L	High-Z	Active

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance.
2. When $\overline{\text{LB}}$ and $\overline{\text{UB}}$ are in select mode (Low), DQ[15:0] are affected. When $\overline{\text{LB}}$ only is in select mode, only DQ[7:0] are affected. When $\overline{\text{UB}}$ only is in the select mode, DQ[15:8] are affected.
3. When the device is in standby mode, control inputs (SC-$\overline{\text{WE}}$, SC-$\overline{\text{OE}}$), address inputs, and data inputs/outputs are internally isolated from any external influence.
4. When SC-$\overline{\text{WE}}$ is invoked, the SC-$\overline{\text{OE}}$ input is internally disabled and has no effect on the I/Os.
5. The device will consume active power in this mode whenever addresses are changed.
6. V_{IN} = V_{CCQ} or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.
7. DPD is enabled when configuration register bit CR[4] is “0”.

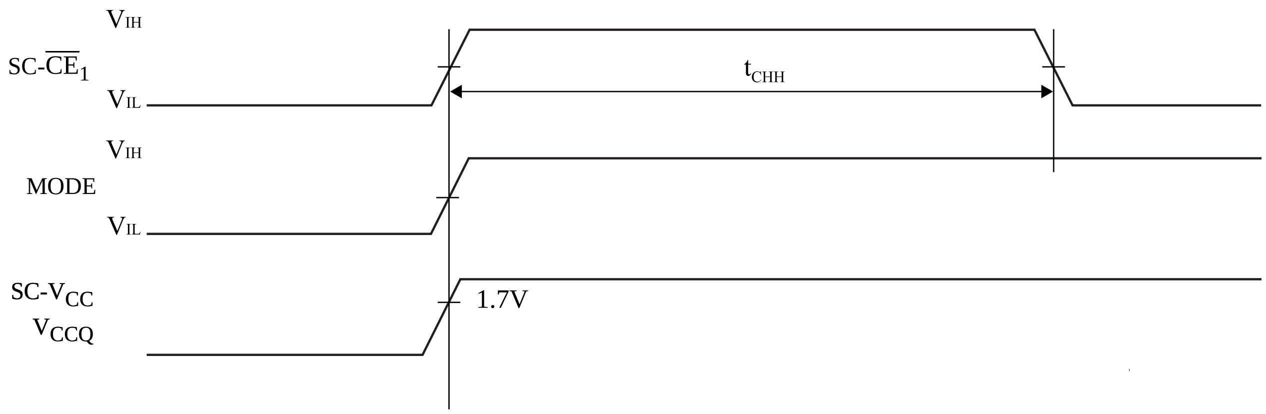
7.2 Standard Operation

7.2.1 Power-Up Initialization

SC-V_{CC} and V_{CCQ} must be applied simultaneously, and when they reach a stable level above 1.7V, the device will require 300µs to complete its self-initialization process (see Figure Power-Up Initialization Timing below). During the initialization period, SC-$\overline{\text{CE}}_1$ should remain HIGH. When initialization is complete, the device is ready for normal operation.

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{CHH}	SC-$\overline{\text{CE}}_1$ High Hold Time following MODE High after Power Up		300		µs

Power-Up Initialization Timing



Notes:

1. The t_{CHH} specifies after SC-V_{CC}, V_{CCQ} reaches specified 1.7V.

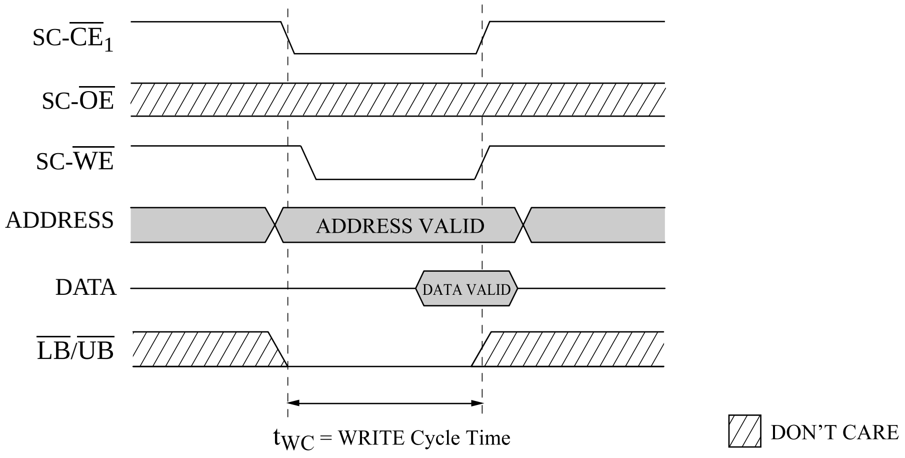
7.2.2 Bus Operating Modes

This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

7.2.3 Asynchronous Write Mode

SmartCombo RAM power up in the asynchronous operating mode. These modes uses the industry-standard SRAM control interface (SC-$\overline{\text{CE}}_1$, SC-$\overline{\text{OE}}$, SC-$\overline{\text{WE}}$, $\overline{\text{LB}}$ / $\overline{\text{UB}}$). Read operations are initiated by bringing SC-$\overline{\text{CE}}_1$, SC-$\overline{\text{OE}}$, and $\overline{\text{LB}}$/$\overline{\text{UB}}$ LOW while keeping SC-$\overline{\text{WE}}$ HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE Operation (Page 40) occur when SC-$\overline{\text{CE}}_1$, SC-$\overline{\text{WE}}$, and $\overline{\text{LB}}$/$\overline{\text{UB}}$ are driven LOW. During WRITE operations, the level of SC-$\overline{\text{OE}}$ is a “Don't Care”; SC-$\overline{\text{WE}}$ will override SC-$\overline{\text{OE}}$.
The data to be written will be latched on the rising edge of SC-$\overline{\text{CE}}_1$, SC-$\overline{\text{WE}}$, or $\overline{\text{LB}}$/$\overline{\text{UB}}$ (whichever occurs first). If SC-$\overline{\text{CE}}_1$ and SC-$\overline{\text{WE}}$ are both LOW for extended periods, the address must change at least every t_{CEM}.

WRITE Operation



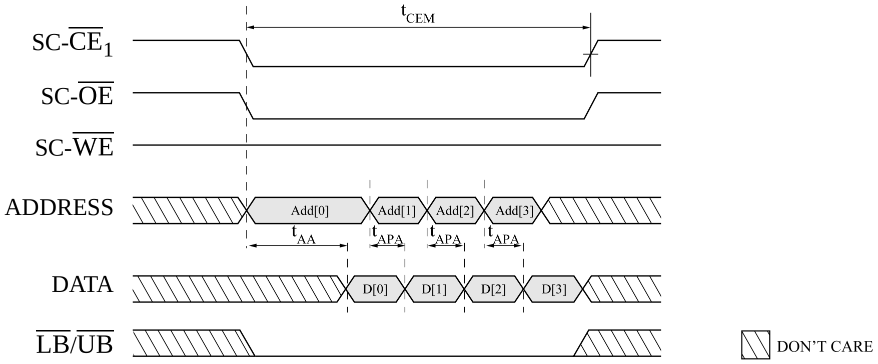
7.2.4 Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In this product, an initial asynchronous read access is performed, then adjacent addresses can be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address SmartCombo RAM page. Any change in addresses A[4] or higher will initiate a new t_{AA} access. Figure Page READ Operation shows the timing diagram for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

The SC-$\overline{\text{CE}}_1$ LOW time is limited by refresh considerations. SC-$\overline{\text{CE}}_1$ must not stay LOW longer than t_{CEM}.

Page READ Operation



7.2.5 $\overline{\text{LB}}$/$\overline{\text{UB}}$ Operation

The lower byte ($\overline{\text{LB}}$) enable and upper byte ($\overline{\text{UB}}$) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the memory array and the internal value will remain unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of SC-$\overline{\text{CE}}_1$, SC-$\overline{\text{WE}}$, $\overline{\text{LB}}$, or $\overline{\text{UB}}$, whichever occurs first.

When both the $\overline{\text{LB}}$ and $\overline{\text{UB}}$ are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, the device remains in an active mode as long as SC-$\overline{\text{CE}}_1$ remains LOW.

7.3 Low Power Operation

7.3.1 Standby Mode Operation

Standby operation occurs when SC-$\overline{CE}_1$ and MODE are HIGH.

The device will enter a reduced power state during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

7.3.2 Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the SmartCombo RAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the SmartCombo RAM device will require 300μs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

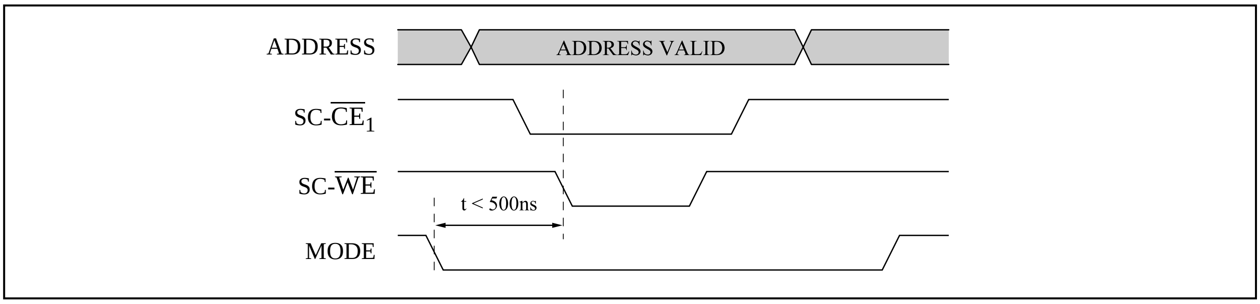
The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing the MODE pin to the LOW state for longer than 10μs. Returning MODE to HIGH will cause the device to exit DPD and begin a 300μs initialization process. During this 300μs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

7.4 Configuration Register Operation

The configuration register (CR) defines how the SmartCombo RAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the CR. This register can be updated anytime while the device is operating in a standby state. Table Configuration Register Bit Mapping on page44 describes the control bits used in the CR.

The CR can be loaded using a WRITE operation immediately after MODE makes a HIGH-to-LOW transition (Figure Load Configuration Register Operation below). The values placed on addresses A[20:0] are latched into the CR on the rising edge of SC-$\overline{CE}_1$ or SC-$\overline{WE}$, whichever occurs first. $\overline{LB}$/$\overline{UB}$ are "Don't Care." Access using MODE is WRITE only.

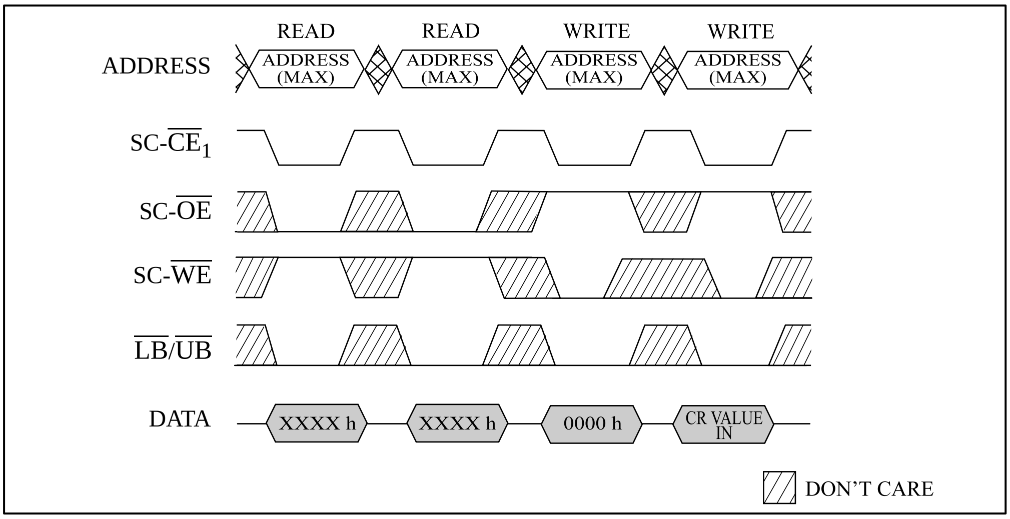
Load Configuration Register Operation



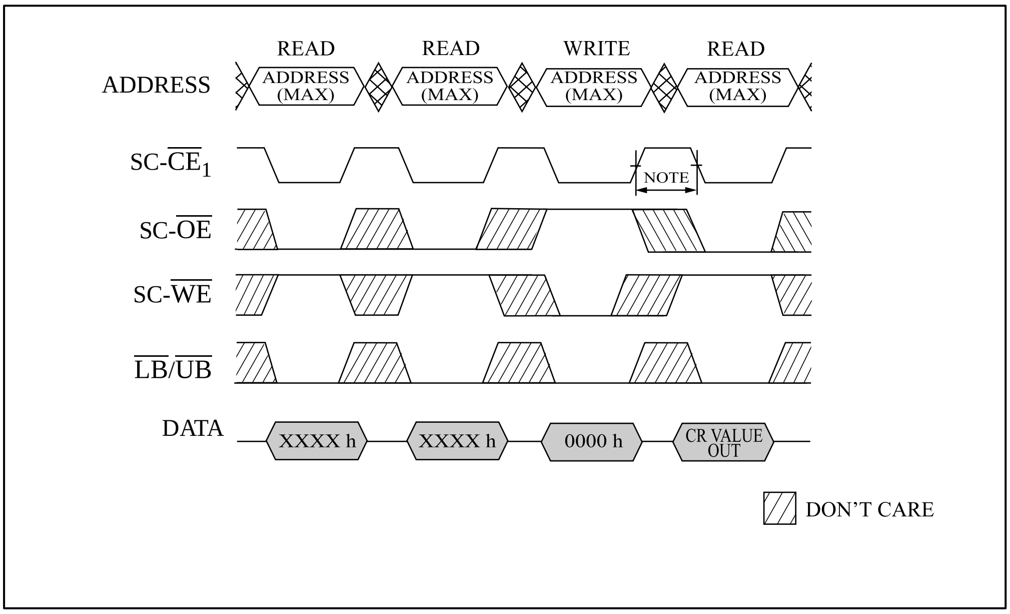
7.4.1 Software Access to the Configuration Register

The contents of the CR can either be read or modified using a software sequence. The nature of this access mechanism may eliminate the need for the MODE pin. If the software mechanism is used, the MODE pin can simply be tied to V_{CCQ}. The port line typically used for MODE control purposes will no longer be required. How-ever, MODE should not be tied to V_{CCQ} if the system will use DPD; DPD cannot be enabled or disabled using the software access sequence. The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure below). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure on page43). The address used during all READ and WRITE operations is the highest address of the SmartCombo RAM device being accessed (1FFFFFh); the contents of this address are not changed by using this sequence.The data bus is used to transfer data into or out of theCR.Writing to the CR using the software sequence modifies the function of the MODE pin. Once the software sequence loads the CR, the level of the MODE pin no longer enables PAR operation. PAR operation will be updated whenever the software sequence loads a new value into the CR. This MODE functionality will continue until the next time the device is powered-up. The operation of the MODE pin is not affected if the software sequence is only used to read the contents of the CR.The use of the software sequence does not affect the ability to perform the standard (MODE controlled) method of loading the CR.

Software Access Load Configuration Register



Software Access Read Configuration Register



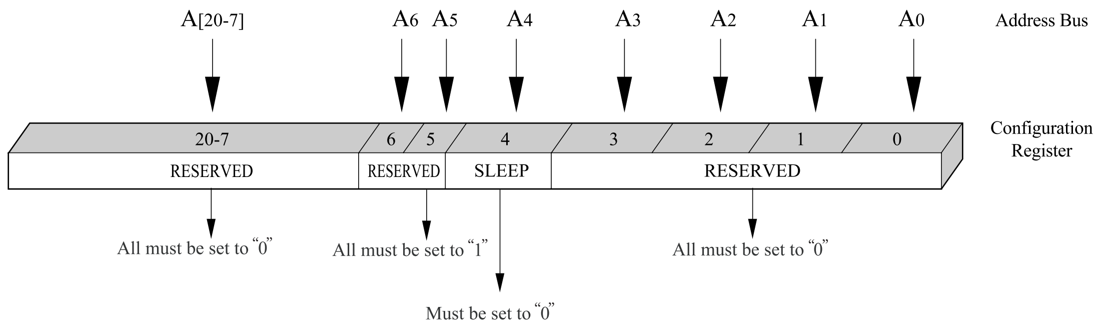
Notes:
SC-$\overline{CE}_1$ must be HIGH for 150 ns before performing the cycle that reads the configuration register.

7.4.2 Sleep Mode(CR[4])

Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when MODE is driven LOW. If CR[4]= 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables MODE initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; this should only be done using MODE to access the CR. DPD operation disables all refresh-related activity. This mode will be used when the system does not require the storage provided by the SmartCombo RAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the SmartCombo RAM device will require 300µs to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

Configuration Register Bit Mapping



7.5 DC Electrical Characteristics for SmartCombo RAM

7.5.1 DC Electrical Characteristics

(T_A = -25°C to +85°C, SC-V_{CC} = 1.7V to 1.95V, V_{CCQ} = 1.7V to 1.95V)

Symbol	Parameter	Notes	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance	5		6.5	pF	T_A = +25°C, f = 1MHz, V_{IN} = 0V
C_{IO}	Data Input/Output Capacitance (DQ)			6.5	pF	
V_{IH}	Input High Voltage	1	V_{CCQ}-0.3	V_{CCQ}	V	
V_{IL}	Input Low Voltage	2	-0.2	0.4	V	
V_{OH}	Output High Voltage		0.80V_{CCQ}		V	I_{OH} = -0.2mA
V_{OL}	Output Low Voltage			0.20V_{CCQ}	V	I_{OL} = 0.2mA
I_{LI}	Input Leakage Current			1	µA	V_{IN} = 0 to V_{CCQ}
I_{LO}	Output Leakage Current			1	µA	SC-$\overline{OE}$ = V_{IH} or Chip Disabled
I_{CC1}	Asynchronous Random READ/WRITE	3		30	mA	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0
I_{CC2}	Asynchronous Page READ	3		15	mA	V_{IN} = V_{CCQ} or 0V Chip Enabled
I_{SB}	Standby Current	4		110	µA	V_{IN} = V_{CCQ} or 0V, SC-$\overline{CE}_1$ = V_{CCQ}

Notes:

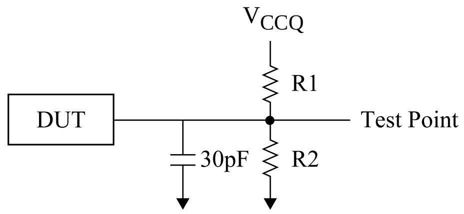
1. Input signals may overshoot to V_{CCQ} + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to GND - 1.0V for periods less than 2ns during transitions
3. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
4. In order to achieve low standby current, all inputs must be driven to V_{CCQ} or GND. I_{SB} might be slightly higher for up to 500ms after power-up.
5. These parameters are verified in device characterization and are not 100% tested.

7.5.2 Deep Power-Down Specifications and Conditions

Symbol	Parameter	Typ.	Units	Test Conditions
I_{ZZ}	Deep Power-Down	10	µA	V_{IN} = V_{CCQ} or 0V, +25°C MODE = 0V CR[4] = 0

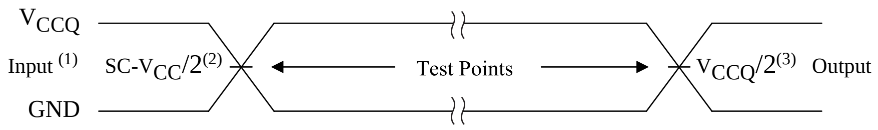
7.6 AC Electrical Characteristics for SmartCombo RAM

Output Load Circuit



V_{CCQ}	R1/R2
1.8 V	2.7kΩ

AC Input/Output Reference Waveform



Notes:

1. AC test inputs are driven at V_{CCQ} for a logic 1 and GND for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at SC-V_{CC}/2. Due to the possibility of a difference between SC-V_{CC} and V_{CCQ}, the input test point may not be shown to scale.
3. Output timing ends at V_{CCQ}/2.

7.6.1 Read Cycle

(T_A = -25°C to +85°C, SC-V_{CC} = 1.7V to 1.95V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AA}	Address Access Time			70	ns
t_{APA}	Page Access Time			20	ns
t_{BA}	$\overline{LB}$/$\overline{UB}$ Access Time			70	ns
t_{BHZ}	$\overline{LB}$/$\overline{UB}$ Disable to High-Z Output	2		8	ns
t_{BLZ}	$\overline{LB}$/$\overline{UB}$ Enable to Low-Z Output	1	10		ns
t_{CEM}	Maximum SC-$\overline{CE}_1$ Pulse Width	3		8	µs
t_{CO}	Chip Select Access Time			70	ns
t_{HZ}	Chip Disable to High-Z Output	2		8	ns
t_{LZ}	Chip Enable to Low-Z Output	1	10		ns
t_{OE}	Output Enable to Valid Output			20	ns
t_{OH}	Output Hold from Address Change		5		ns
t_{OHZ}	Output Disable to High-Z Output	2		8	ns
t_{OLZ}	Output Enable to Low-Z Output	1	5		ns
t_{PC}	Page Cycle Time		20		ns
t_{RC}	Read Cycle Time		70		ns

Notes:

1. High-Z to Low-Z timings are tested with the circuit shown in Figure Output Load Circuit on page 46. The Low-Z timings measure a 100mV transition away from the High-Z (V_{CCQ}/2) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure Output Load Circuit on page 46. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ}/2.
3. Page mode enabled only.

7.6.2 Write Cycle

(T_A = -25°C to +85°C, SC-V_{CC} = 1.7V to 1.95V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AS}	Address Setup Time		0		ns
t_{AW}	Address Valid to End of Write		70		ns
t_{BW}	Byte Select to End of Write		70		ns
t_{CEH}	SC-$\overline{CE}_1$ HIGH Time During Write		5		ns
t_{CW}	Chip Enable to End of Write		70		ns
t_{DH}	Data Hold from Write Time		0		ns
t_{DW}	Data Write Setup Time		23		ns
t_{LZ}	Chip Enable to Low-Z Output	1	10		ns
t_{OW}	End Write to Low-Z Output		5		ns
t_{WC}	Write Cycle Time		70		ns
t_{WHZ}	Write to High-Z Output	2		8	ns
t_{WP}	Write Pulse Width	3	46		ns
t_{WPH}	Write Pulse Width HIGH		10		ns
t_{WR}	Write Recovery Time		0		ns

Notes:

1. High-Z to Low-Z timings are tested with the circuit shown in Figure Output Load Circuit on page 46. The Low-Z timings measure a 100mV transition away from the High-Z (V_{CCQ}/2) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure Output Load Circuit on page 46. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ}/2.
3. If SC-$\overline{CE}_1$ and SC-$\overline{WE}$ are both LOW for an extended period, the address must change at least evert 8µs (t_{CEM}).

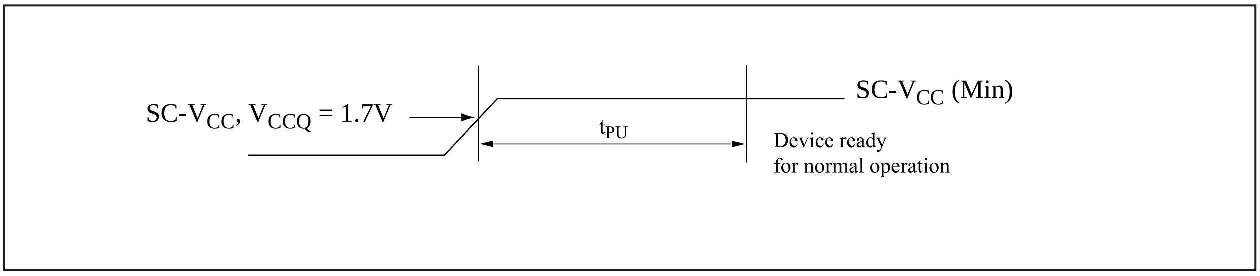
7.6.3 Load Configuration Register

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AS}	Address Setup Time		0		ns
t_{AW}	Address Valid to End of Write		70		ns
t_{CDZZ}	Chip Deselect to MODE LOW		5		ns
t_{CW}	Chip Enable to End of Write		70		ns
t_{WC}	Write Cycle Time		70		ns
t_{WP}	Write Pulse Width		40		ns
t_{WR}	Write Recovery Time		0		ns
t_{ZZWE}	MODE LOW to SC-$\overline{\text{WE}}$ LOW		10	500	ns

7.6.4 Deep Power-Down

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{CDZZ}	Chip Deselect to MODE LOW		5		ns
t_R	Deep Power-Down Recovery		300		µs
t_{ZZMIN}	Minimum MODE Pulse Width		10		µs

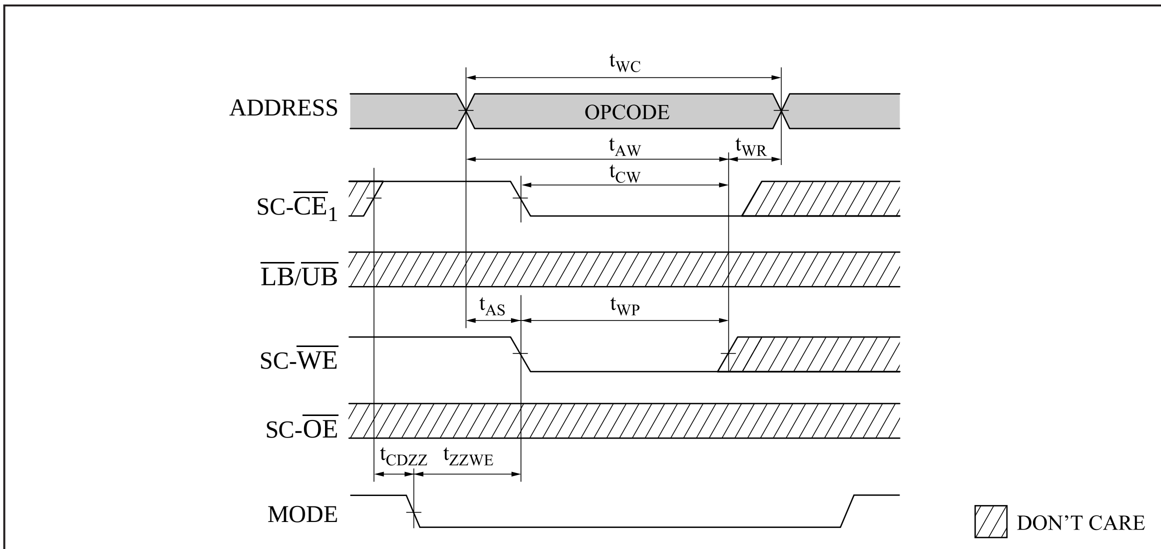
Initialization Period



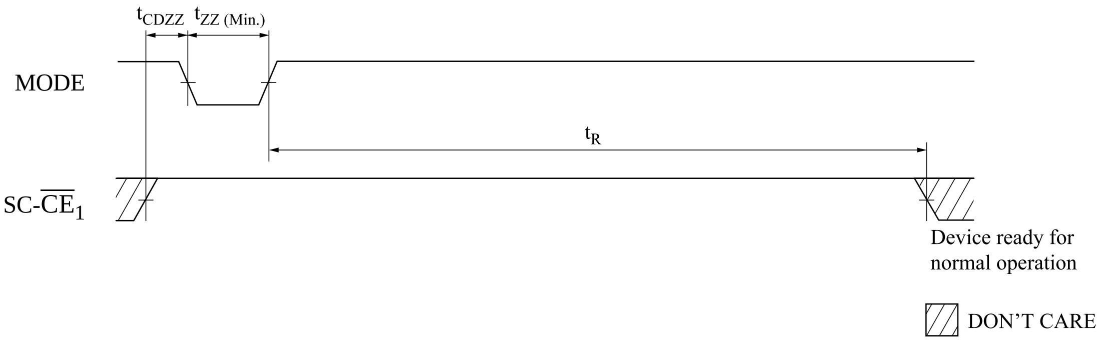
7.6.5 Power-Up Initialization

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PU}	Initialization Period (required before normal operations)		300		µs

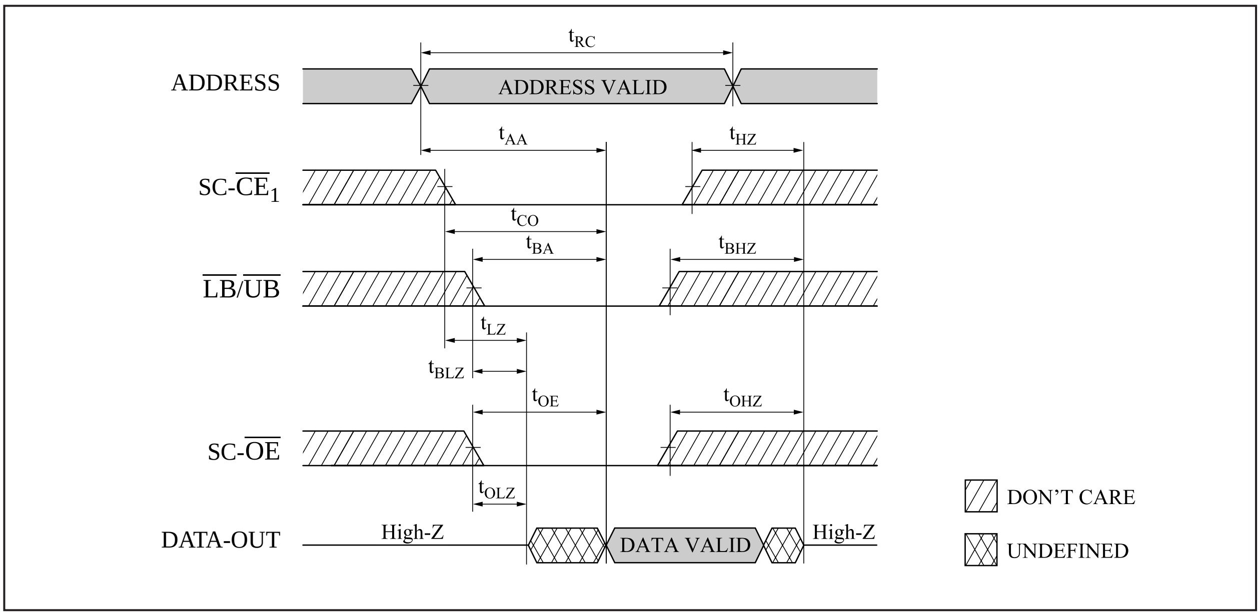
Load Configuration Register



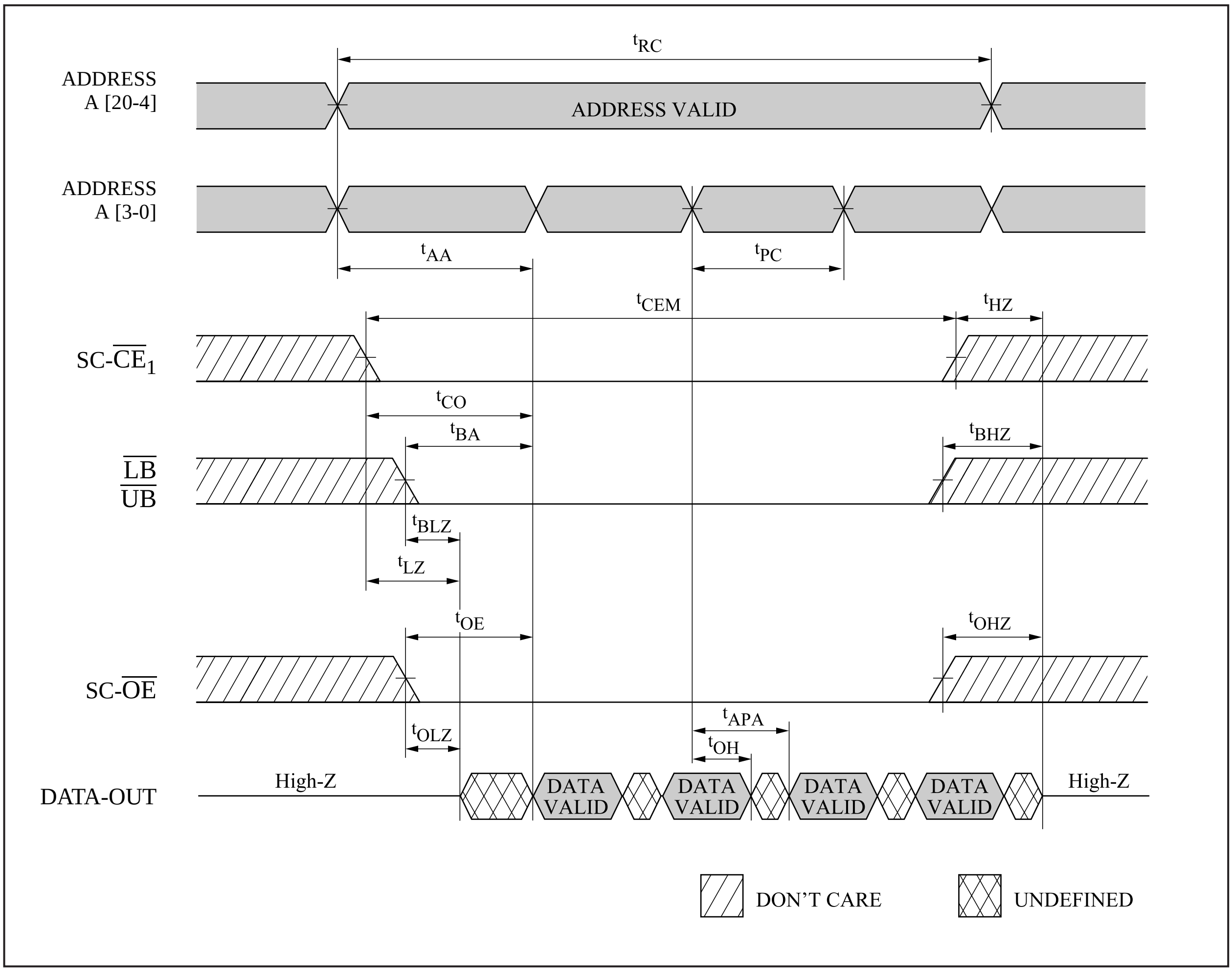
Deep Power-Down/Entry/Exit



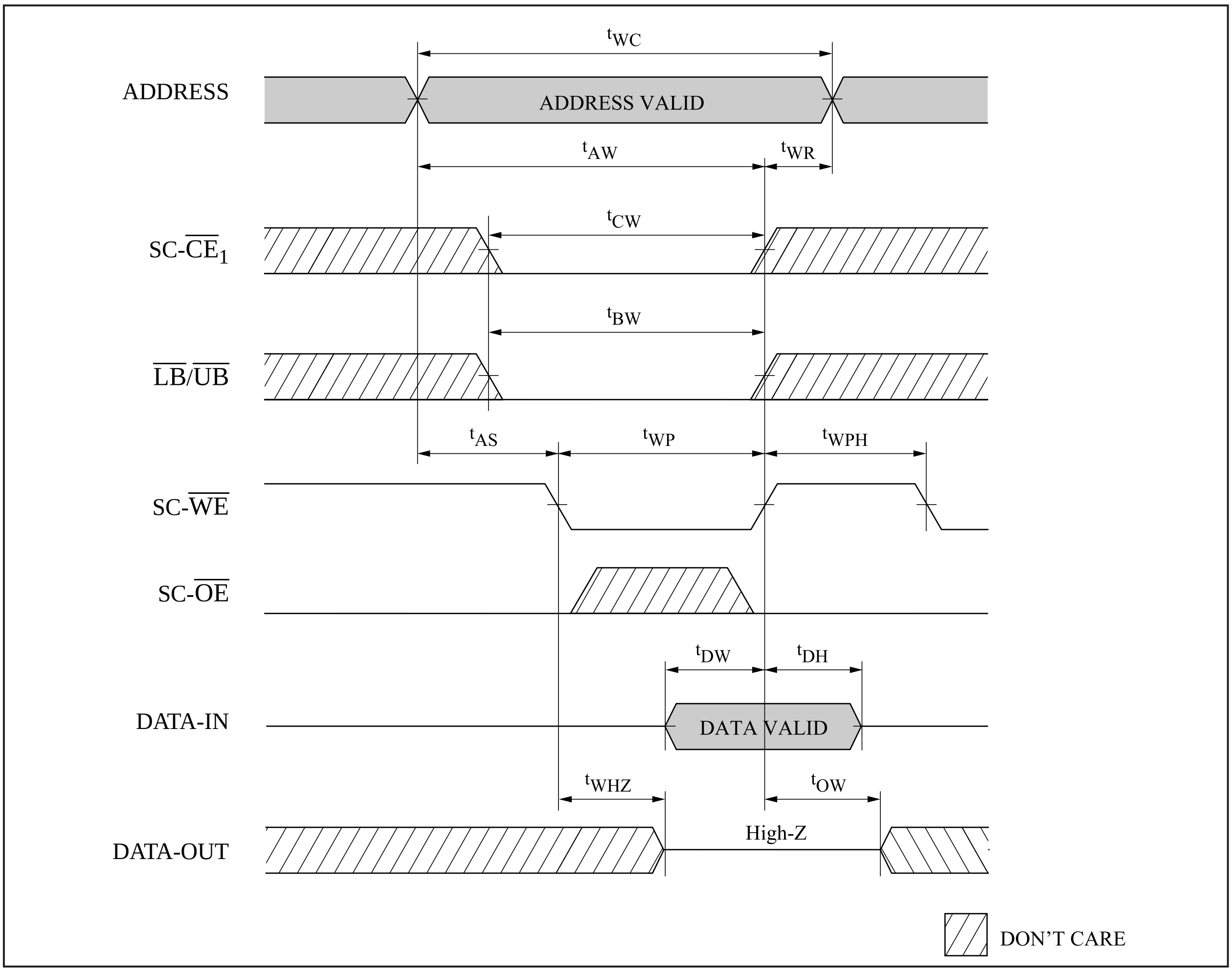
Single READ Operation (SC-$\overline{WE}$ = V_{IH})



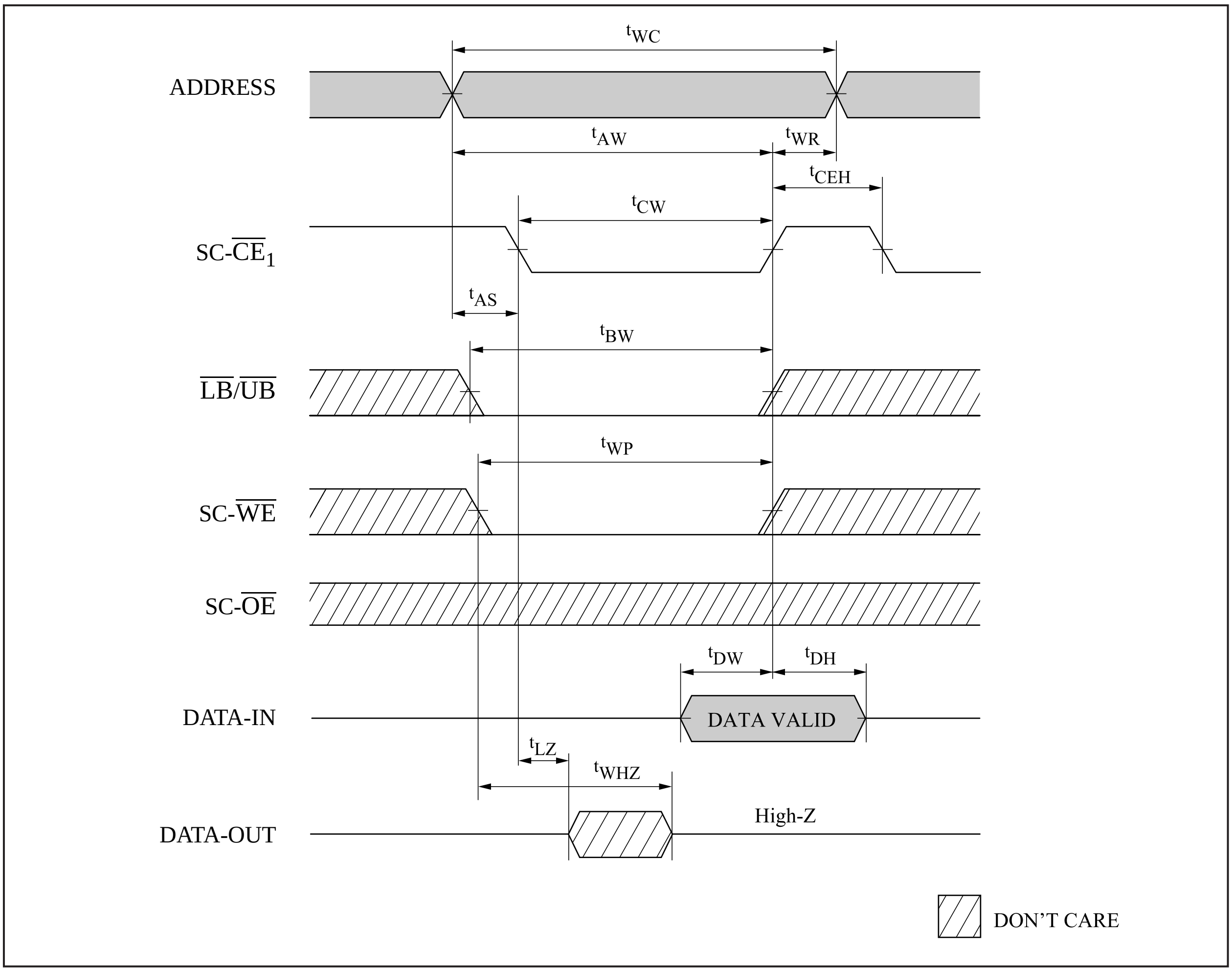
Page Mode READ Operation (SC-$\overline{WE}$ = V_{IH})



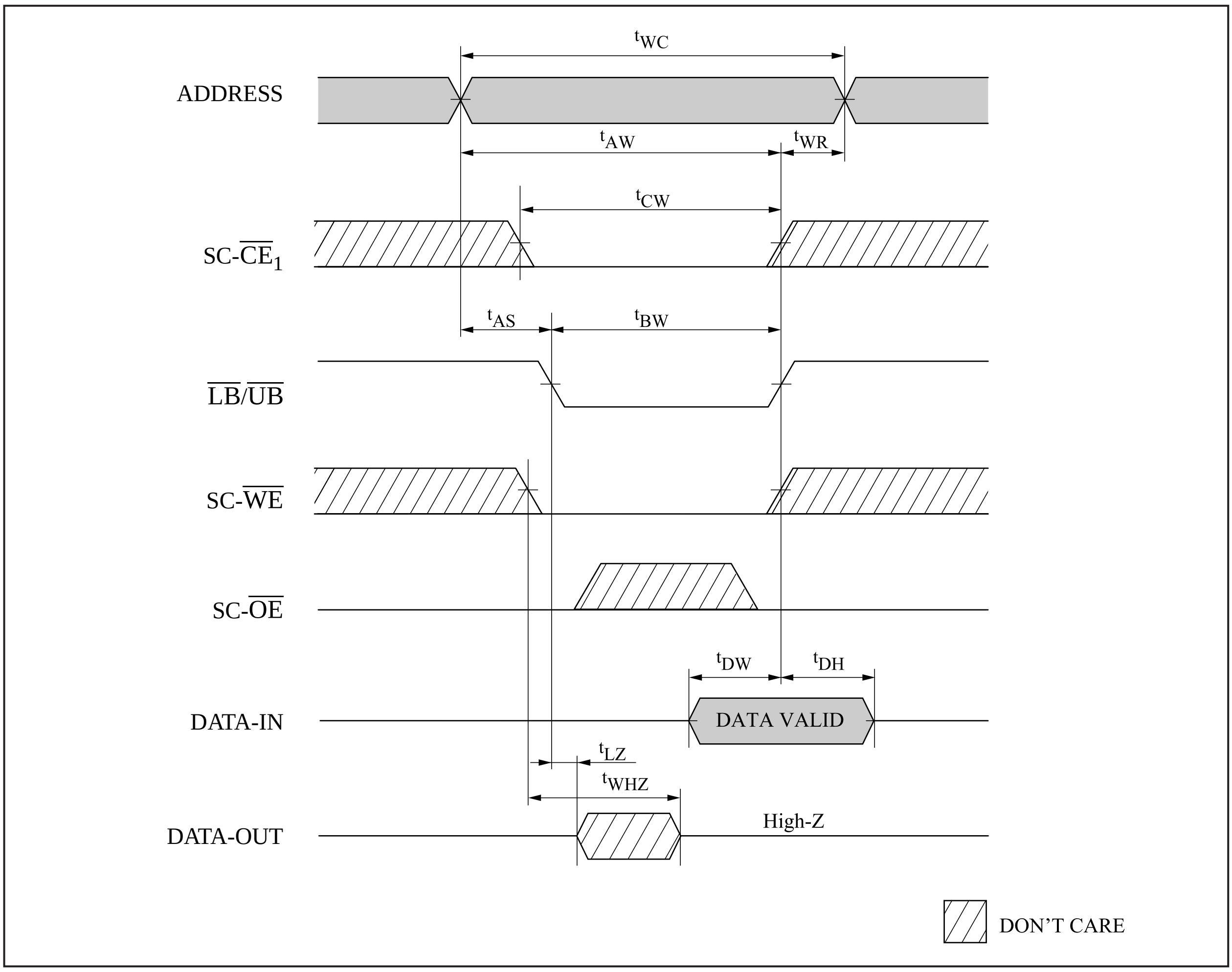
WRITE Cycle (SC-$\overline{\text{WE}}$ Control)



WRITE Cycle (SC-$\overline{CE}_1$ Control)



WRITE Cycle ($\overline{\text{LB}}$/$\overline{\text{UB}}$ Control)



8. Notes

This product is a stacked CSP package that a 128M (x16) bit Flash Memory and a 32M (x16) bit SmartCombo RAM are assembled into.

-Supply Power

Maximum difference (F-V_{CC}, SC-V_{CC}, V_{CCQ}) of the voltage is less than 0.3V.

-Power Supply and Chip Enable of Flash Memory and SmartCombo RAM

Flash Memory and SmartCombo RAM should not be active simultaneously.
If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.
Both F-V_{CC} and SC-V_{CC} are needed to be applied by the recommended supply voltage at the same time.

-Power Up Sequence

When turning on Flash memory power supply, keep $\overline{RST}$ low. After F-V_{CC} reaches over 1.7V, keep $\overline{RST}$ low for more than 100 nsec.

-Device Decoupling

The power supply is needed to be designed carefully because one of the SmartCombo RAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SmartCombo RAM and Flash Memory. Note peak current caused by transition of control signals.

9. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F-$\overline{\text{WE}}$ signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

■ The below describes data protection method.

1. Protection of data in each block
    - Any locked block by setting its block lock bit is protected against the data alternation. When $\overline{\text{WP}}$ is low, any locked-down block by setting its block lock-down bit is protected from lock status changes.
      By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
    - For detailed block locking scheme, see Section 6.2 Command Definitions for Flash Memory.

2. Protection of data with V_{PP} control
    - When the level of V_{PP} is lower than V_{PPLK} (V_{PP} lockout voltage), write functions to all blocks including OTP block are disabled. All blocks are locked and the data in the blocks are completely protected.

3. Protection of data with $\overline{\text{RST}}$
    - Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing $\overline{\text{RST}}$ to low, which inhibits write operation to all blocks including OTP block.
    - For detailed description on $\overline{\text{RST}}$ control, see Section 6.6.6 Reset Operations.

■ Protection against noises on F-$\overline{\text{WE}}$ signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on F-$\overline{\text{WE}}$ signal.

10. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory and SmartCombo RAM power switching characteristics, each device should have a 0.1µF ceramic capacitor connected between F-V_{CC} and GND, between SC-V_{CC} and GND, between V_{CCQ} and GND and between V_{PP} and GND.
Low inductance capacitors should be placed as close as possible to package leads.

2. V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the F-V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprograming “0” for the bit which has already been programed “0”. Overwrite operation may generate unerasable bit.

In case of reprograming “0” to the data which has been programed “1”.
•Program “0” for the bit in which you want to change data from “1” to “0”.
•Program “1” for the bit which has already been programed “0”.

For example, changing data from “1011110110111101” to “1010110110111100”
requires “1110111111111110” programing.

4. Power Supply

Block erase, (page buffer) program and OTP program with an invalid V_{PP} (See Chapter 6.5 DC Electrical Characteristics for Flash Memory) produce spurious results and should not be attempted.
Device operations at invalid F-V_{CC} voltage (See Chapter 6.5 DC Electrical Characteristics for Flash Memory) produce spurious results and should not be attempted.

11 Package and packing specification

[Applicability]

This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80%(Relative humidity) max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow[*1], IR/Convection reflow.[*1])

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow[*1], IR/Convection reflow.[*1])

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after completion of the 1st reflow.

[*1]:Air or nitrogen environment.

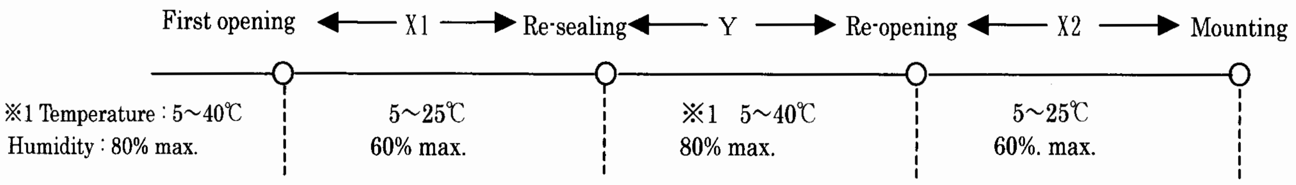
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1＋X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened. (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period :
  120＋10／-0℃ for 2～3 hours.
- The above baking conditions apply since the trays are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

3. Surface mount conditions.

The following soldering condition are recommended to ensure device quality.

(Use paste recommends Sn-Ag-Cu paste. However, Sn-Pb paste is not recommended.)

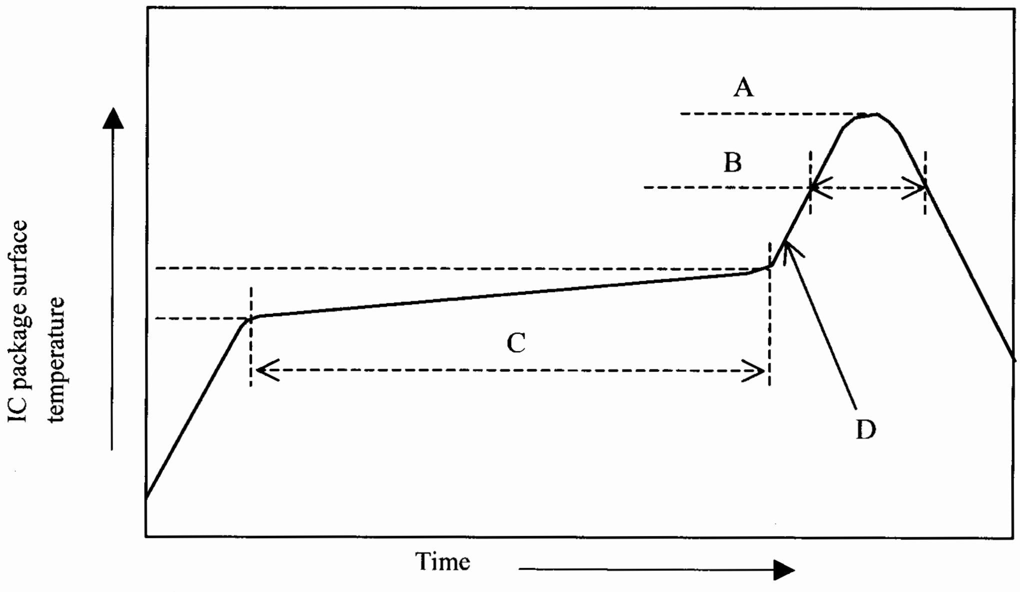
3-1.Soldering.

(1) Convection reflow or IR/Convection. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :

A)	Peak temperature.	250℃ max.
B)	Heating temperature.	40 to 60 seconds as 220℃
C)	Preheat temperature.	It is 150 to 200℃, and is 120±30 seconds
D)	Temperature increase rate.	It is 1 to 3℃/seconds

- Measuring point : IC package surface.
- Temperature profile :



3-2.Recommended heating condition for repair.

Pre heating : 100℃ or more within 90 sec. from room temperature to 90±30 sec.

Reflow heating : within ten sec. at a temperature of 250℃ to 260℃

(Please confirm not only melting solder of the repair area but also the back of the PCB.)

4. Condition for removal of residual flux.
   (1) Ultrasonic washing power : 25 watts / liter max.
   (2) Washing time : Total 1 minute max.
   (3) Solvent temperature : 15～40℃

5. Package outline specification.
   Refer to the attached drawing.
   (Plastic body dimensions do not include burr of resin.)
   The contents of LEAD-FREE TYPE application of the specifications. (*2)

6. Markings.

6-1.Marking details. (The information on the package should be given as follows.)

(1) Product name : LRS18AC
(2) Company name : S
(3) Date code : (Example) YYWW XXX

YY	→	Denotes the production year. (Last two digits of the year.)
WW	→	Denotes the production week. (01・02・～・52・53)
XXX	→	Denotes the production ref. code (1～3 digits).

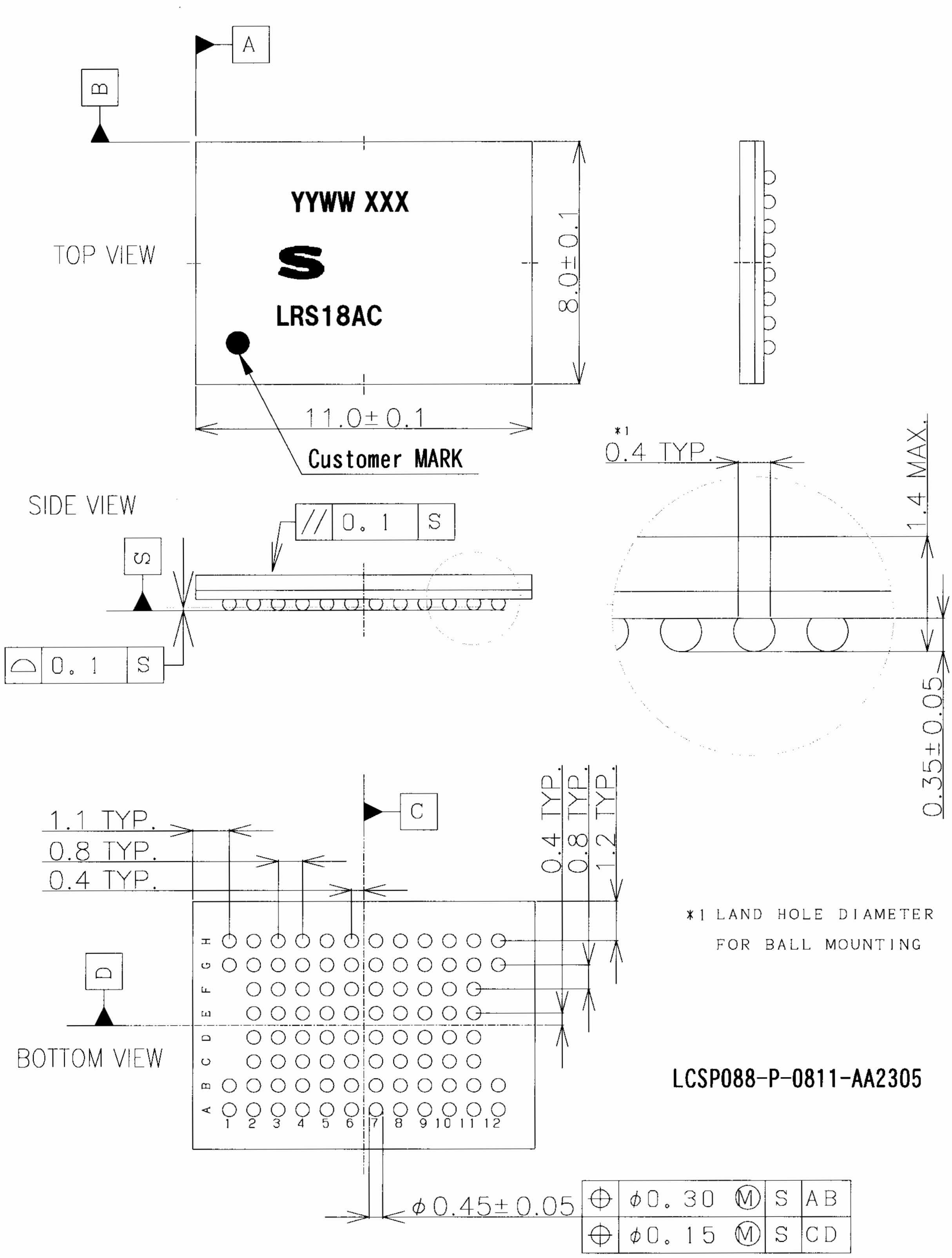
(4) “” indicates the country of origin.

6-2.Marking layout.
The layout is shown in the attached drawing.
(However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Ag-Cu)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note) It is those with an underline printing in a date code because of a LEAD-FREE type.



NAME	LFBGA088-P-0811			BALL TYPE
DRAWING NO.	AA2305	UNIT	mm	Sn-Ag-Cu
NAME	Plastic body dimensions do not include burr of resin.			

7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (2310 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (231 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (9240 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

Refer to the attached drawing.

7-3.Outline dimension of carton.

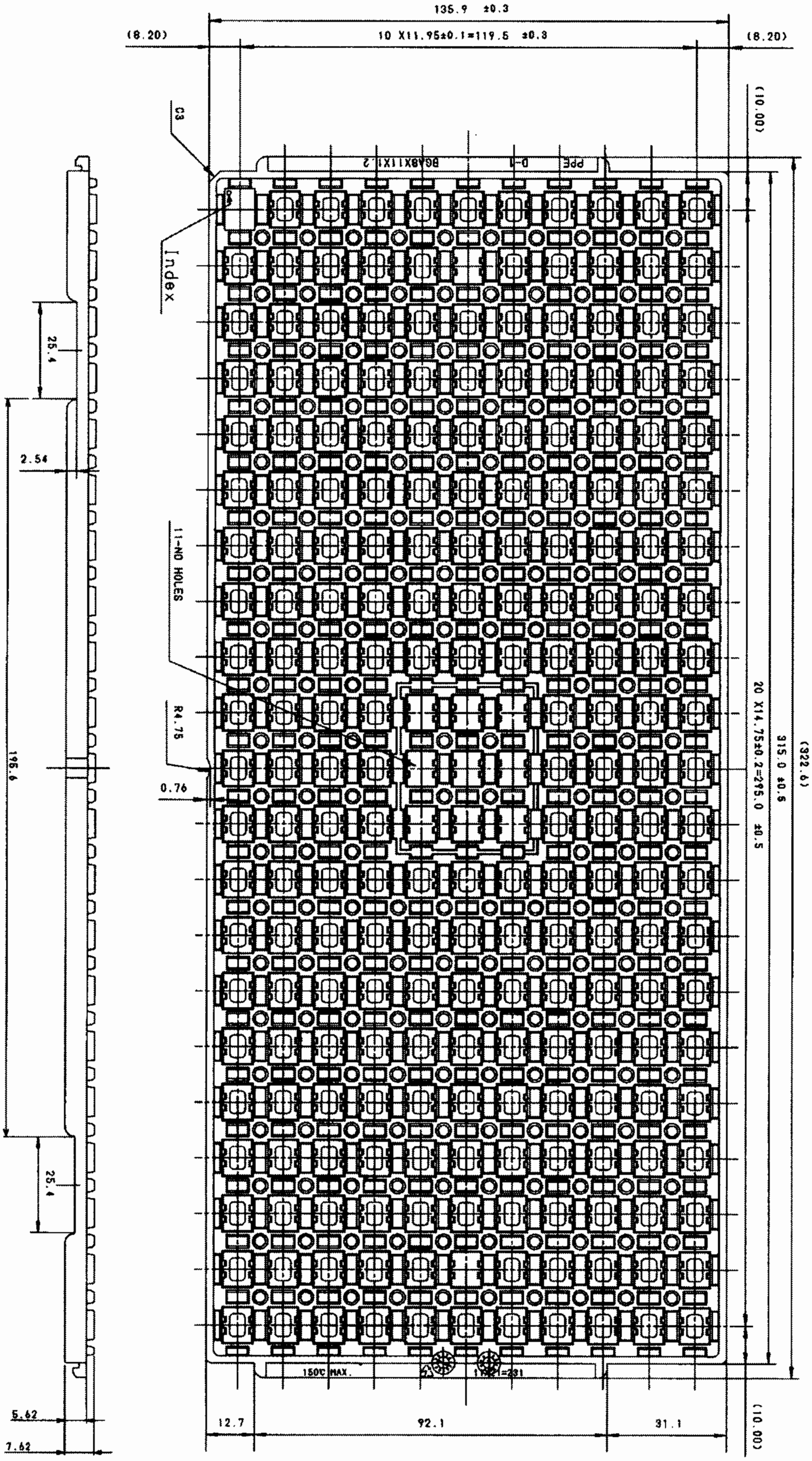
Refer to the attached drawing.

8. Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.

(3) The devices should be mounted within one year of the date of delivery.

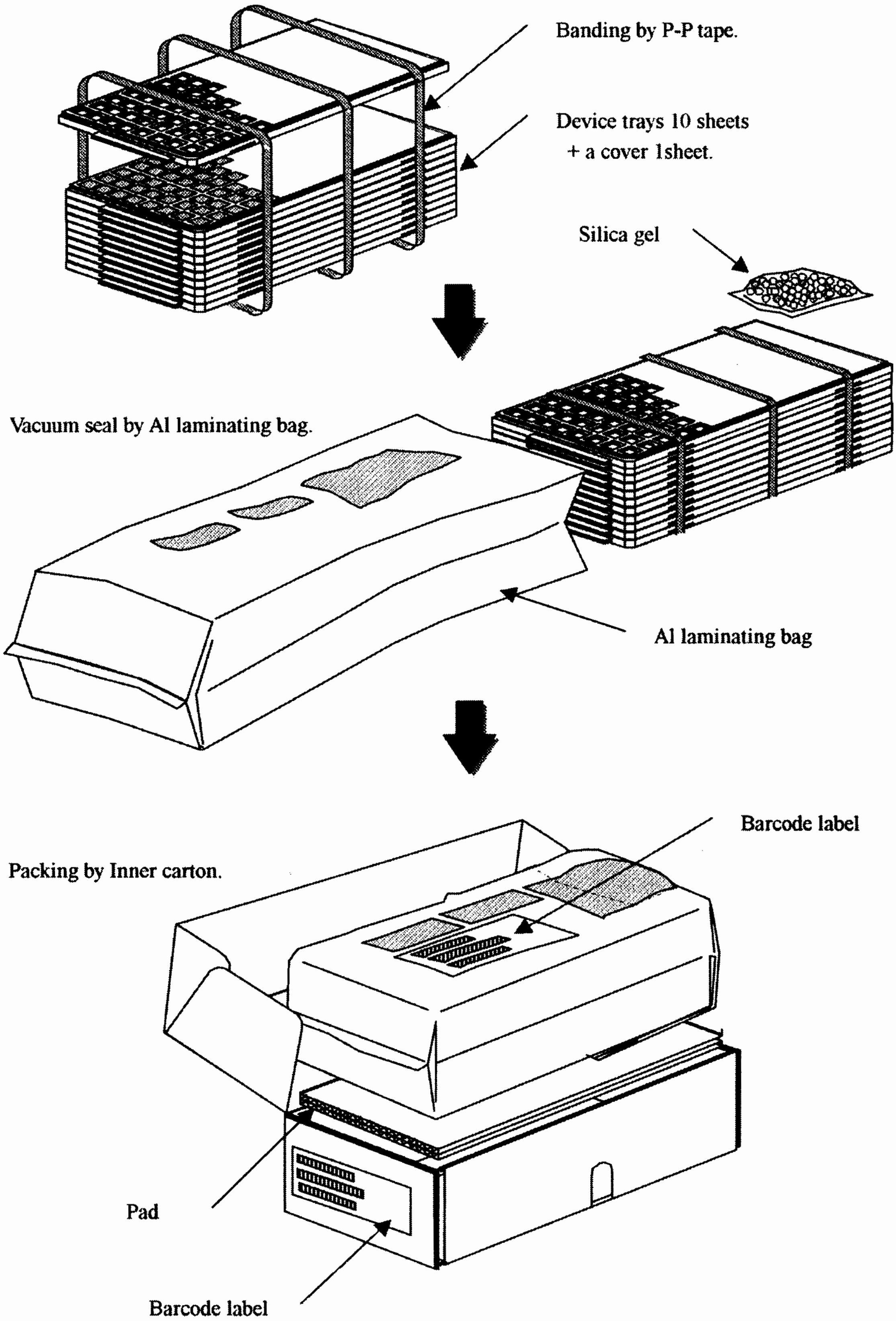


名称 NAME	BGA8X11X1.2		備考 NOTE
DRAWING NO.	CV867i	単位 UNIT	mm

(1) Banding device tray together.

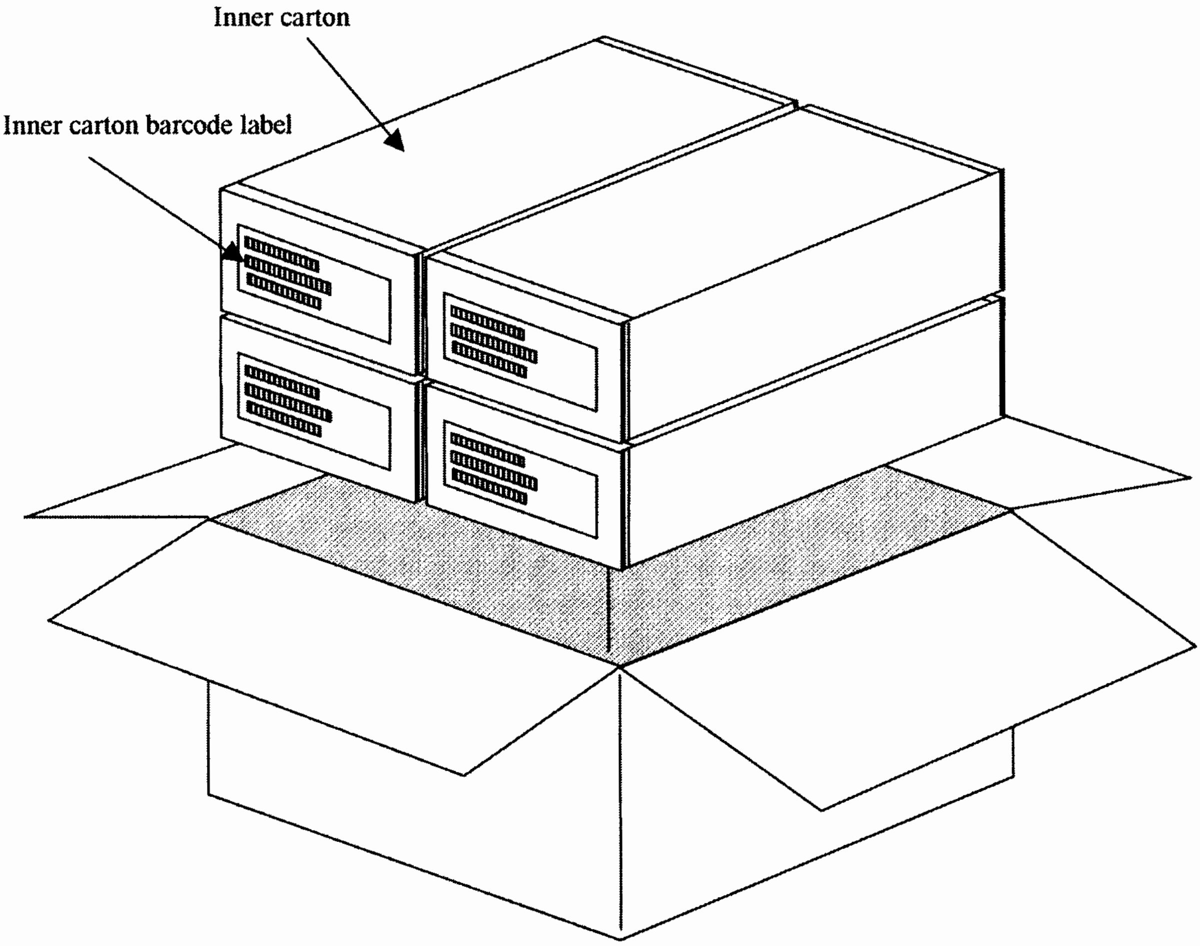
(2) Vacuum seal by Al laminating bag.

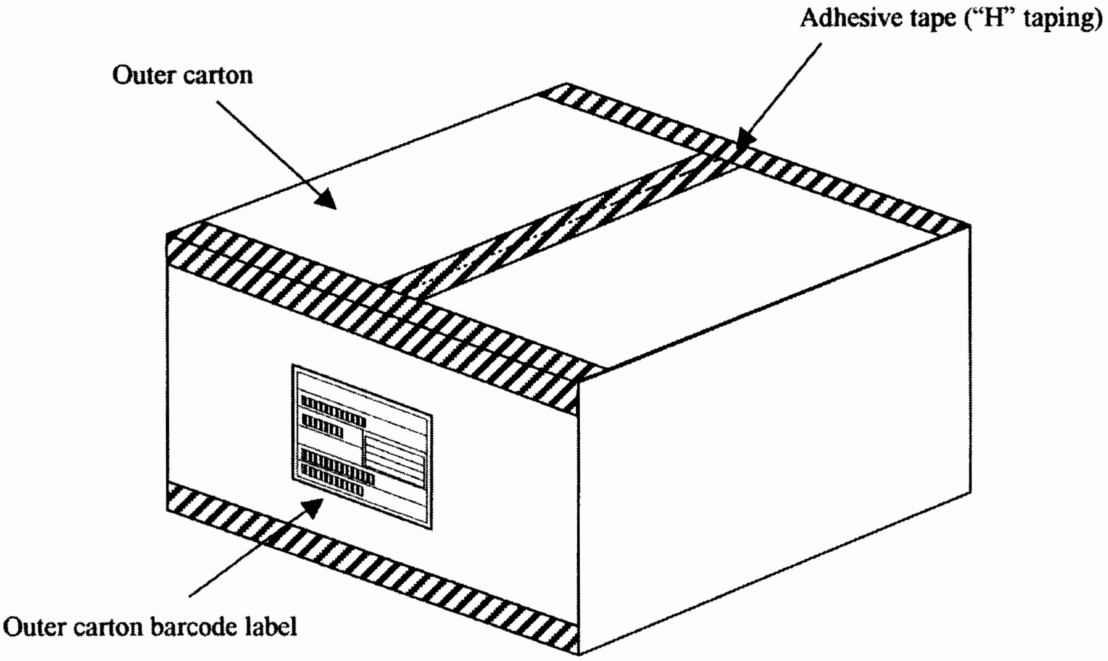
(3) Packing by Inner carton.



NAME	Packing specifications		
DRAWING NO.	BJ433c	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.





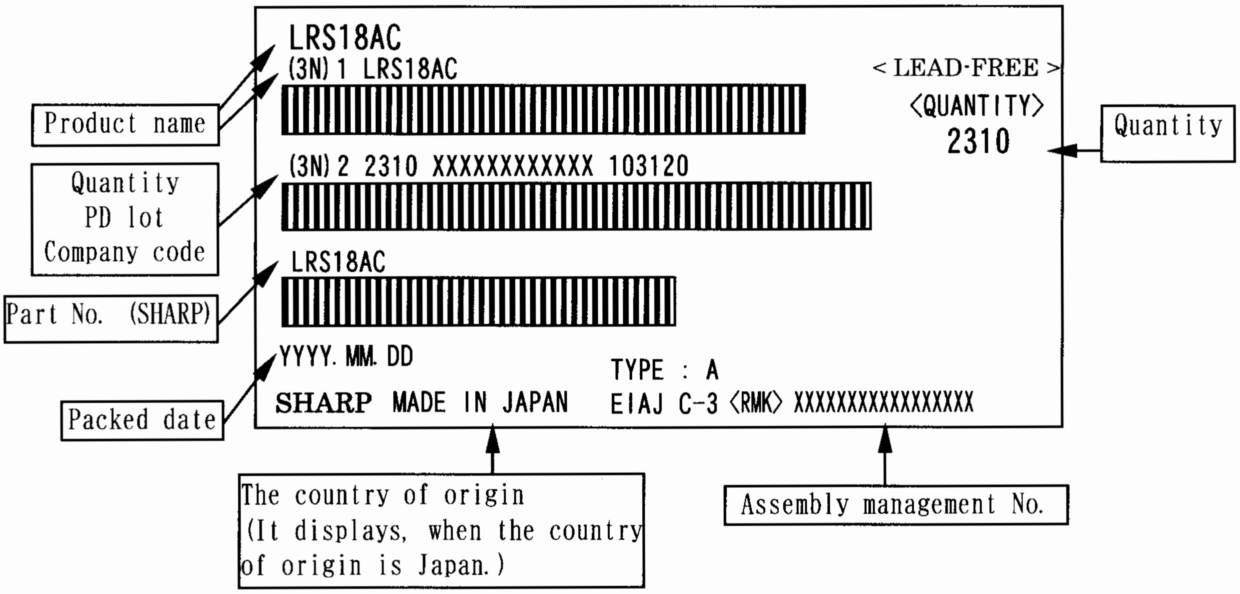
L × W× H
Inner carton - Outer dimensions : 360×150×95
Outer carton - Outer dimensions : 390×335×230

NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

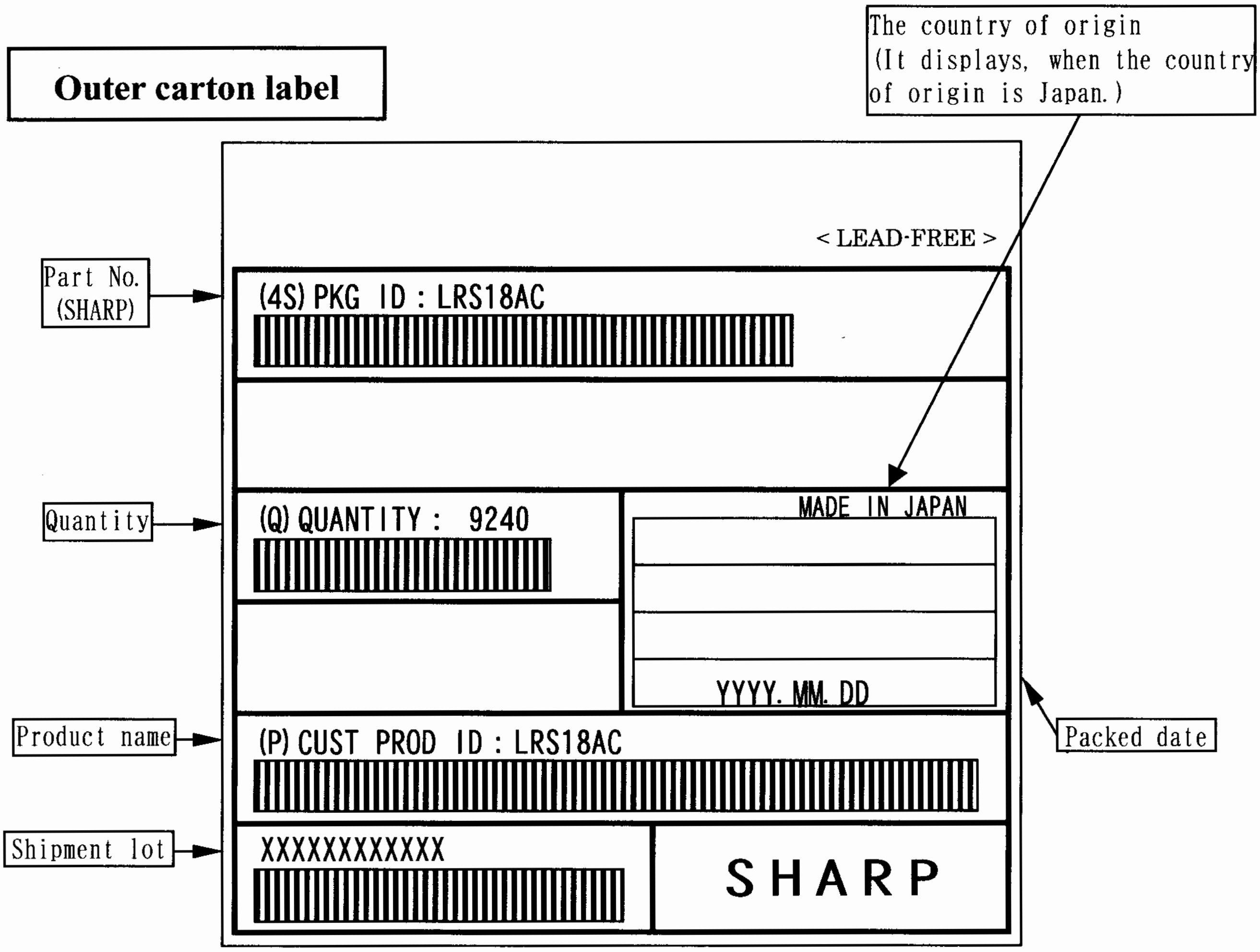
NOTE There is a possibility different from this specification when the number of shipments is fractions.

(Note) The <LEAD-FREE> display shows a lead-free article.

Inner carton label



Outer carton label



(Former) EIAJ B Standard conforming

LRS18AC Combination MEMORY ERRATA

1. Software Access of Configuration Register Operation (for SmartCombo RAM)

PROBLEM

“Software Access Operation” can not be used.

WORKAROUND

Do not use “Software Access Operation”.

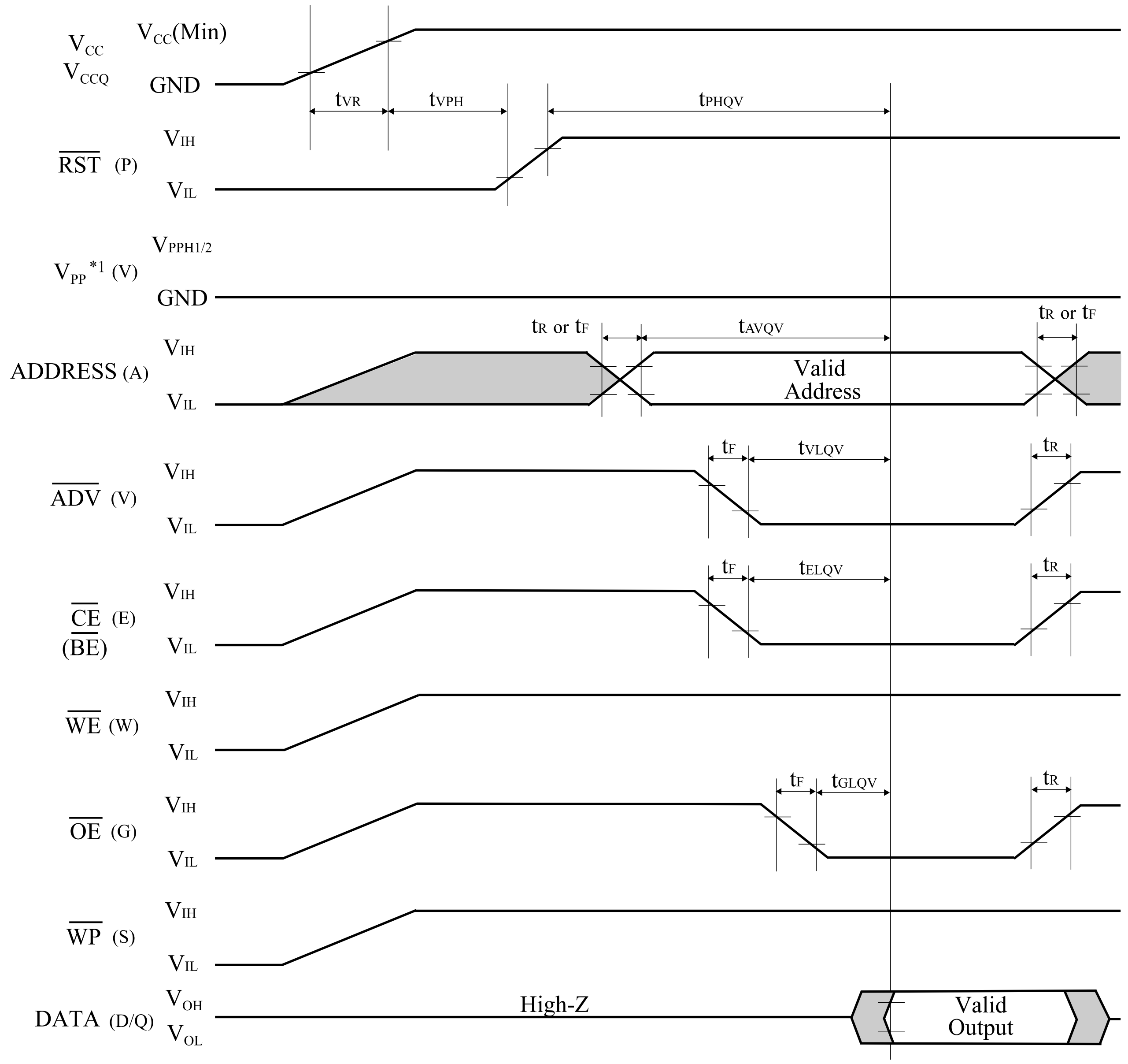
STATUS

This is intended to be fixed in future devices.

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{PP} to 0V during read operations and $V_{PPH1/2}$ during write or erase operations.
See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the "AC Electrical Characteristics for Flash Memory" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

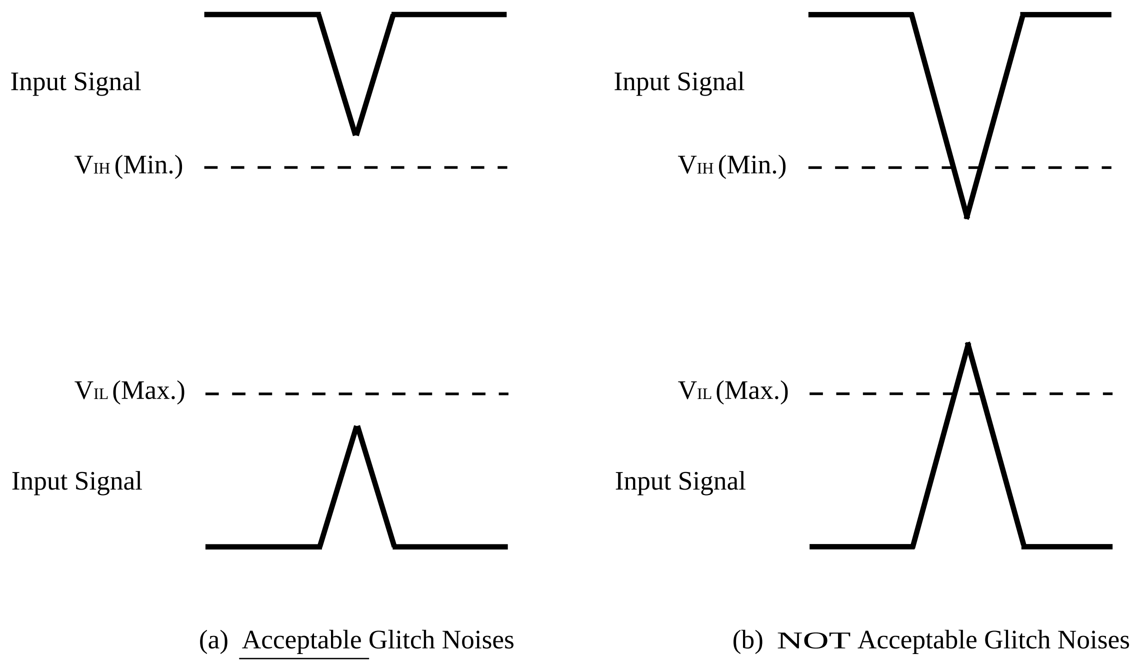
Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	F-V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).



(a) Acceptable Glitch Noises (b) NOT Acceptable Glitch Noises

Figure A-2. Waveform for Glitch Noises

See the "DC Electrical Characteristics" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.