

PROTECTION PRODUCTS

Description

RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over voltage caused by ESD (electrostatic discharge) and CDE (Cable Discharge Events).

RClamp03384P has a maximum capacitance of only 0.20 pF between I/O pins and GND. ESD characteristics are highlighted by high ESD withstand voltage ($\pm 10\text{kV}$ Contact per IEC 61000-4-2), each device will protect four lines operating at 3.3 volts.

RClamp03384P is in a DFN 2.5 x 1.0 x 0.55mm 10-Lead package. The flow-through package design simplifies PCB layout.

Features

- Transient Protection to
 - ♦ IEC 61000-4-2 (ESD) $\pm 15\text{ kV}$ (Air), $\pm 10\text{ kV}$ (Contact)
 - ♦ IEC 61000-4-5 (Lightning) 5A (8/20 μs)
- Protects four High-Speed Data Lines
- Package design optimized for high speed lines
- Working voltage: 3.3V
- Low clamping voltage
- Low capacitance: 0.20pF maximum (I/O to GND)
- Solid-State Silicon-Avalanche Technology

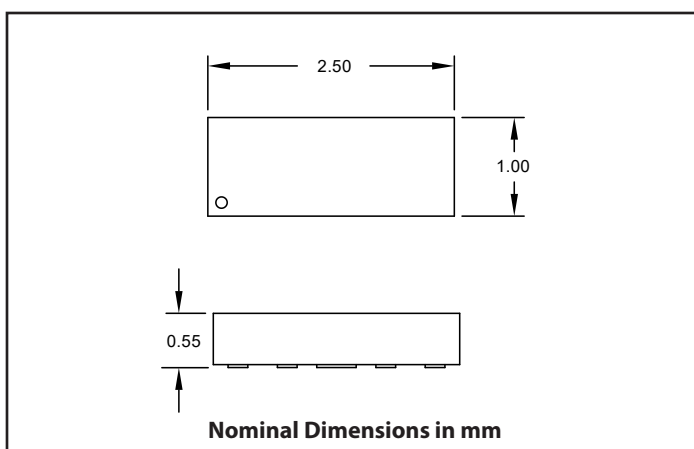
Mechanical Characteristics

- Package: DFN 2.5 x 1.0 x 0.55mm 10-Lead
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

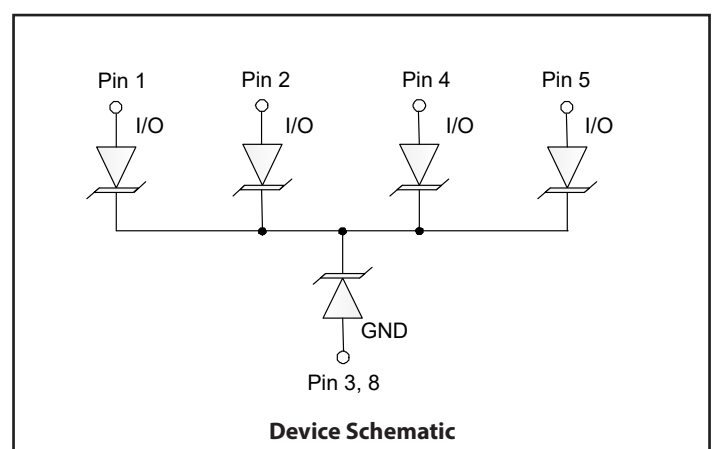
Applications

- HDMI 2.0 and 2.1
- Embedded Display Port (eDP)
- Display Port
- LVDS
- V-by-One

Nominal Dimension



Functional Schematic



Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20μs)	P _{PK}	27.5	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	5	A
ESD per IEC 61000-4-2 (Contact) ⁽¹⁾ ESD per IEC 61000-4-2 (Air) ⁽¹⁾	V _{ESD}	±10 ±15	kV
Operating Temperature	T _{OP}	-55 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	
Reverse Stand-Off Voltage	V _{RWM}	Any I/O pin to GND			3.3	V	
Reverse Breakdown Voltage	V _{BR}	I _t = 10mA	-40°C to +85 °C	5.5	8.3	10	V
Holding Current	I _H			80		mA	
Reverse Leakage Current	I _R	V _{RWM} = 3.3V		<1	50	nA	
Clamping Voltage	V _C	I _{pp} = 5A, tp= 1.2/50us (voltage), 8/20μs (current) combination waveform		5.2	5.5	V	
ESD Clamping Voltage ⁽²⁾	V _C	tp = 0.2/100ns (TLP), Any I/O pin to GND	I _{pp} = 4A		3.8	V	
			I _{pp} = 16A		6.7		
Dynamic Resistance ^{(2),(3)}	R _{DYN}	tp = 0.2/100ns (TLP)		0.25		Ohms	
Junction Capacitance	C _J	V _R = 0V, f = 1MHz, any I/O pin to GND		0.17	0.20	pF	

Notes:

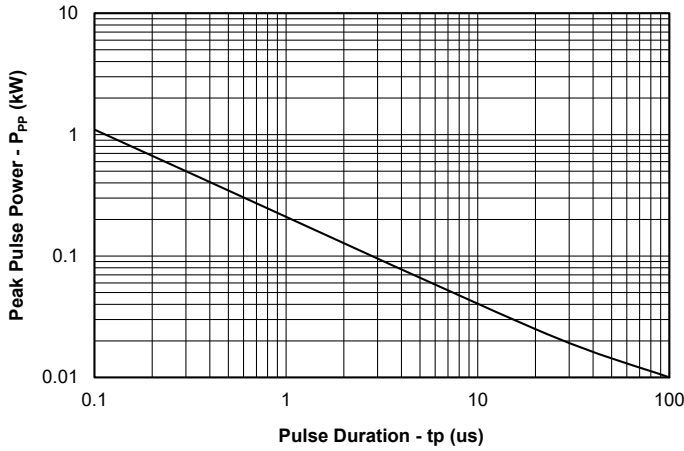
(1) ESD gun return path connected to Ground Reference Plane (GRP)

(2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, ITLP and VTLP averaging window: t1 = 70ns to t2 = 90ns.

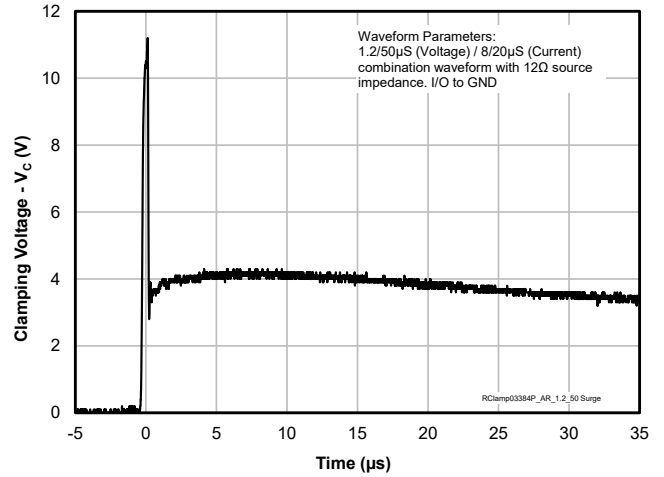
(3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

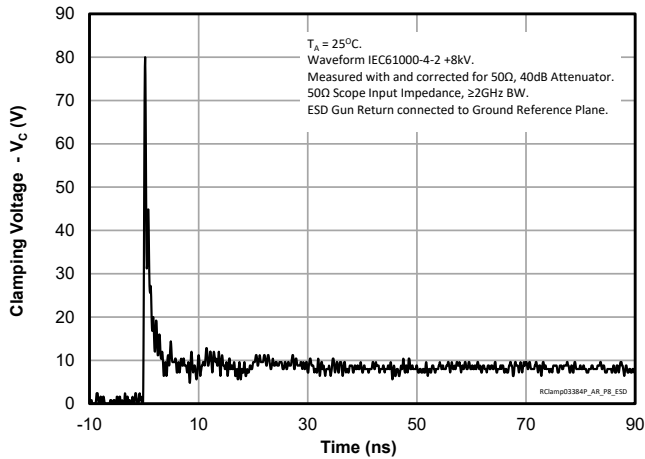
Non-Repetitive Peak Pulse Power vs. Pulse Time



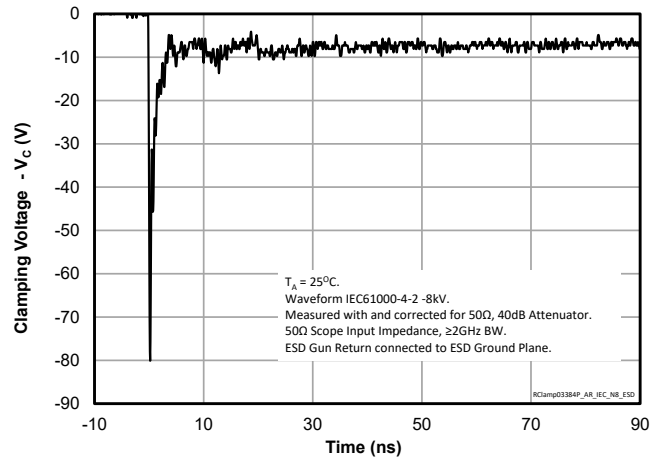
Clamping Characteristic (5A, Combination Waveform)



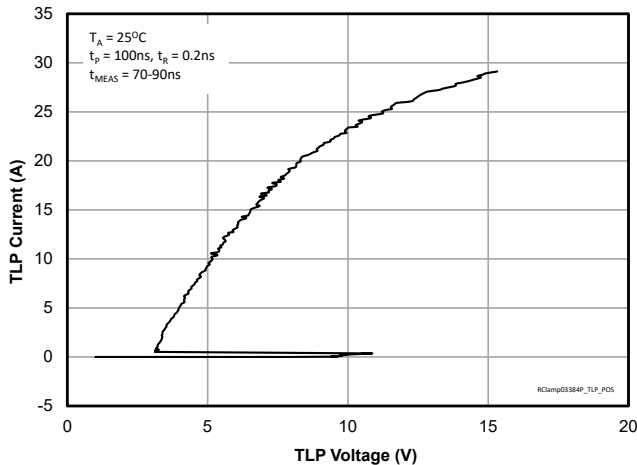
ESD Clamping (+8kV Contact per IEC 61000-4-2)



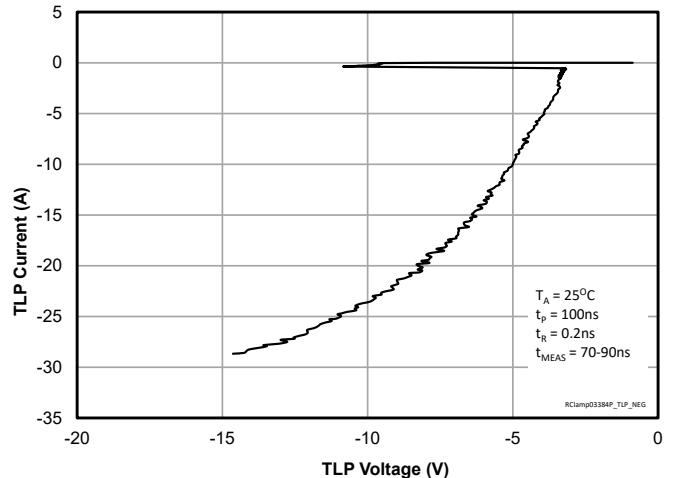
ESD Clamping (-8kV Contact per IEC 61000-4-2)



TLP Characteristic (Positive Pulse)

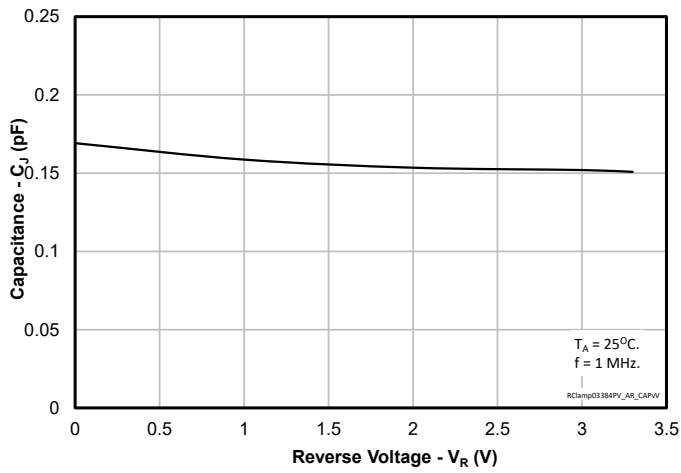


TLP Characteristic (Negative Pulse)

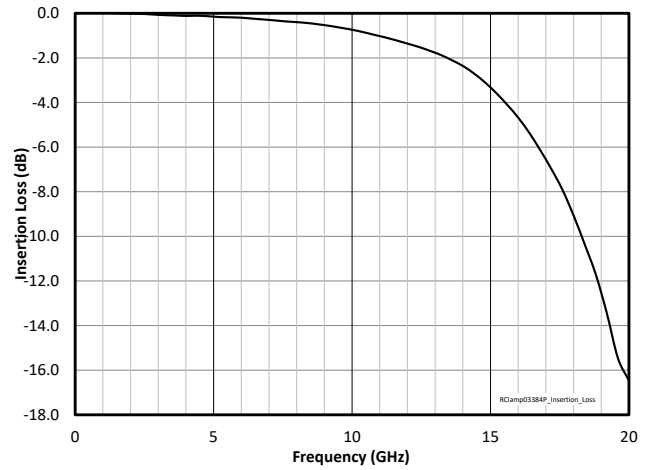


Typical Characteristics

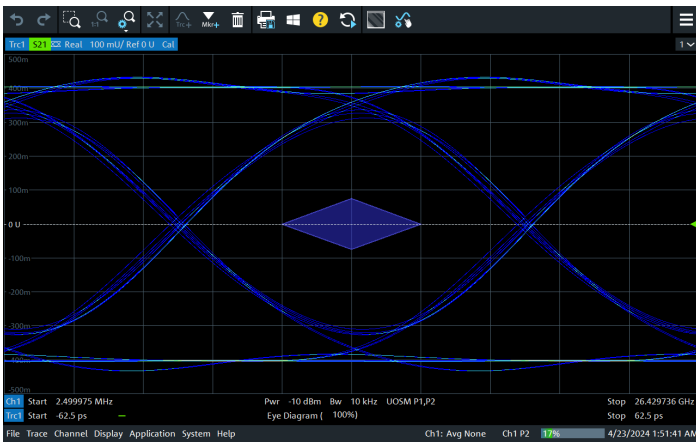
Capacitance vs. Reverse Voltage



Insertion Loss (S21)



HDMI 2.0 and 2.1 Eye-Diagram



Applications Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 2. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. The area ratio of a rectangular aperture is given as:

$$\text{Area Ratio} = (L * W) / (2 * (L + W) * T)$$

Where:

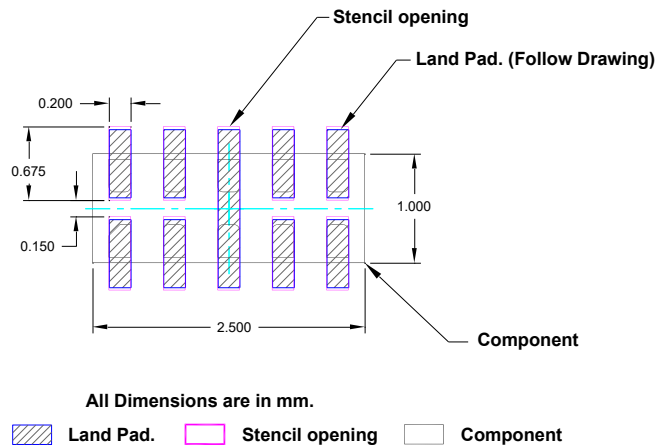
L = Aperture Length

W = Aperture Width

T = Stencil Thickness

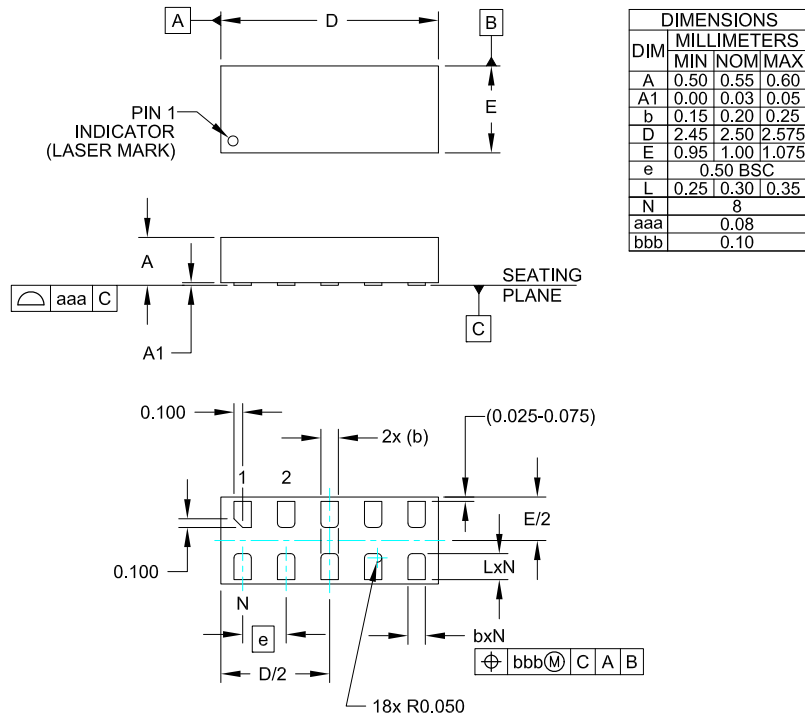
Semtech recommends a stencil thickness of 0.100mm - 0.125mm for this device. The stencil should be laser cut with electro-polished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. Due to the small aperture size, a solder paste with Type 4 or smaller particles is recommended. Assuming a 125um thick stencil, the aperture dimensions shown will yield an area ratio of 0.72 for the small pads and 1.25 for the large.

Recommended Stencil Design

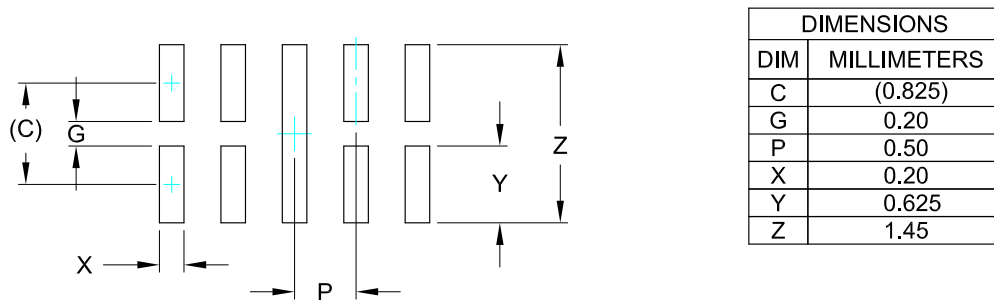


Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular
Solder Stencil Thickness	0.100mm (0.004") - 0.125mm (0.005")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder pad Design	Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

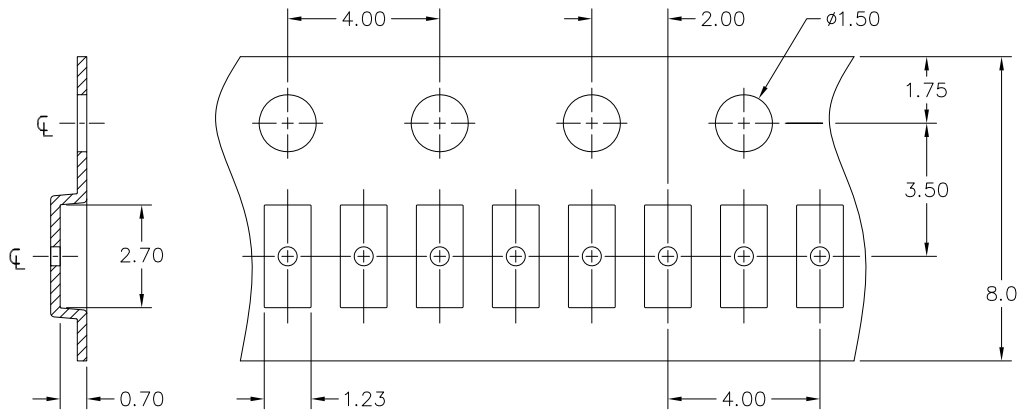
Outline Drawing - DFN 2.5 x 1.0 x 0.55mm 10-Lead



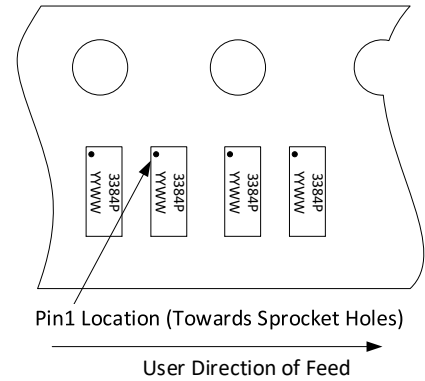
Land Pattern - DFN 2.5 x 1.0 x 0.55mm 10-Lead



Tape and Reel Specification (2mm)



Note: All dimensions are nominal dimensions in mm.



Ordering Information

Part Number	Qty per Reel	Pocket Pitch	Reel Size
RClamp03384P.C	3,000	4mm	7"
RClamp03384P.A	5,000	4mm	7"
RClamp03384P.N	10,000	2mm	7"
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