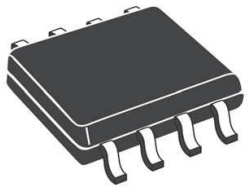
AP239

4A Dual Low Side MOSFET Driver

Feature summary

- Dual independent Low Side MOSFET Driver with 4A sink and source capability
- Independent enable for each driver
- Driver output parallelability to support higher driving capability
- Matched propagation delays
- CMOS/TTL Compatible Input levels
- Wide input Supply Voltage Range: 5V to 18V
- Embedded Driver Anti-Shoot-Through protection
- Low bias switching current
- Short propagation delays
- Wide operative temperature range: -40°C to 105°C
- Industry Standard SOP8 Package



SOP8

Description

AP239 is a flexible, high-frequency dual Low-Side driver specifically designed to work with high capacitive MOSFETs and IGBTs.

Both AP239 outputs can sink and source 4A independently. Higher driving current can be obtained by putting in parallel the two PWM output.

AP239 provides two enable pins which can be used to enable the operation of one or both of the output lines.

AP239 works with CMOS/TTL compatible PWM signal.

The device is available in SOP8 package.

Applications

- Switch Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers
- Class D Switching Amplifiers

Order Codes

Part Number	Temp Range, °C	Package	Packing
AP239	-40 - 105	SOP8	Tube
AP239TR	-40 - 105	SOP8	Tape & Reel

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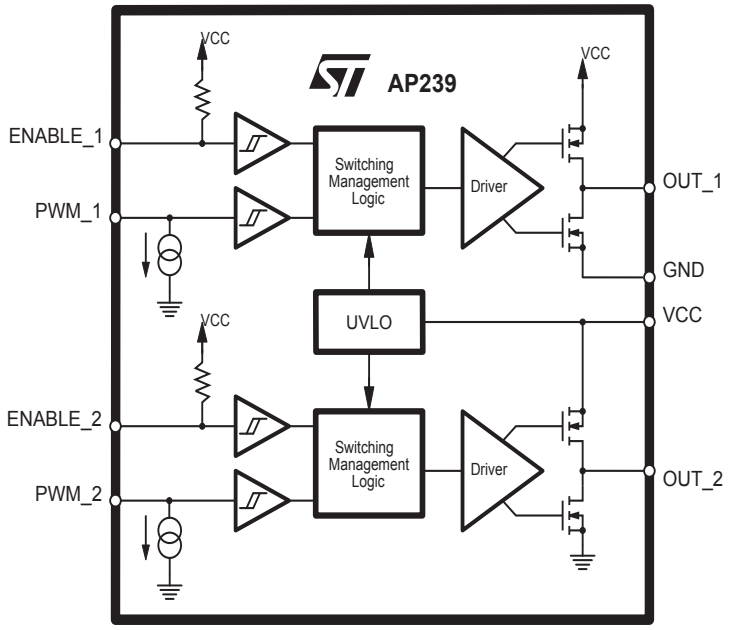
1 Typical application circuit and block diagram

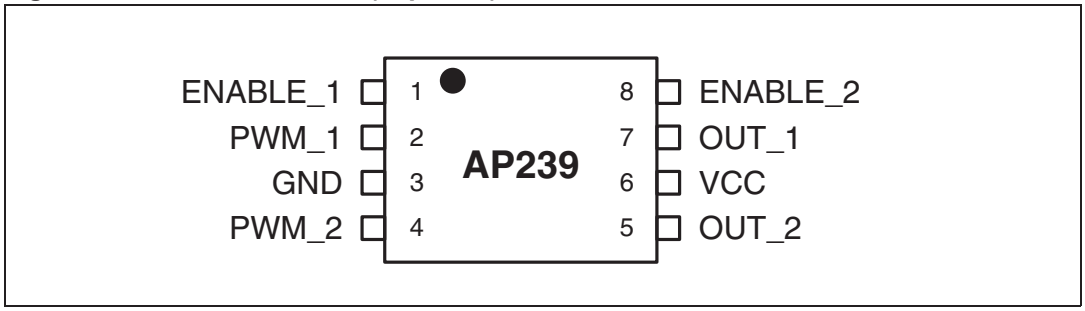
1.1 Block diagram

Figure 1. Block diagram



2 Pins description and connection diagrams

Figure 2. Pins connection (Top view)



2.1 Pin description

Table 1. Pins Descriptions

Pin #	Name	Function
1	ENABLE_1	Enable input for Driver 1.Pull low to disable Driver1 (OUT1 will be low, PWM1 will be ignored). Even though internally pulled up to VCC with a typ. 100kOhm resistor, it is reccomended to pull high up to VCC to enable the section. The pin features TTL/CMOS compatible thresholds.
2	PWM_1	PWM input signal for driver 1 featuring TTL/CMOS compatible threshold and hysteresis. It is internally pulled down to GND with a 10 µA current generator.
3	GND	All internal references, logic and drivers are referenced to this pin. Connect to the PCB ground plane.
4	PWM_2	PWM input signal for driver 2 featuring TTL/CMOS compatible threshold and hysteresis. It is internally pulled down to GND with a 10 µA current generator.
5	OUT_2	Driver2 output. The output stage is capable of providing up to 4A drive current to the gate of a power MOSFET. IGBT are supported as well. A small series resistor can be useful to reduce dissipated power.
6	VCC	AP239 supply voltage. Bypass with low-ESR MLCC capacitor to GND.
7	OUT_1	Driver1 output. The output stage is capable of providing up to 4A drive current to the gate of a power MOSFET. IGBT are supported as well. A small series resistor can be useful to reduce dissipated power.
8	ENABLE_2	Enable input for Driver2. .Pull low to disable Driver2 (OUT2 will be low, PWM2 will be ignored). Even though internally pulled up to VCC with a typ. 100kOhm resistor it is reccomended to pull high up to VCC to enable the section. The pin features TTL/CMOS compatible thresholds.

2.2 Thermal data

Table 2. Thermal Data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance Junction to Ambient (Device soldered on 2s2p PC Board - 67mm x 67mm)	85	℃/W
T_{MAX}	Maximum Junction Temperature	150	℃
T_{STG}	Storage Temperature Range	-40 to 150	℃
T_J	Junction Temperature Range	-40 to 150	℃
T_A	Operating Ambient Temperature Range	-40 to 105	℃
P_{TOT}	Maximum Power Dissipation at 25℃ (Device soldered on 2s2p PC Board)	1.4	W

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
All pins	to GND	-0.3 to 19	V
I_{OUTx}	DC output current	500	mA
V_{HBM}	ESD capability, Human Body Model	2	kV

3.2 Electrical characteristics

Table 4. Electrical Characteristics

(V_{CC} = 5V to 18V, T_j = -40℃ to 105℃ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY CURRENT AND POWER-ON						
I_{CC}	VCC Supply current	OUT_1, OUT_2 = OPEN VCC= 10V; Tj=25℃		3.5		mA
$UVLO_{VCC}$	VCC Turn-ON	VCC Rising		4.4	4.6	V
	VCC Turn-OFF	VCC Falling	3.6	3.8		V
INPUT THRESHOLD						
PWM_x, ENABLE_x	Input High - V_{IH}	Rising threshold		2.2	2.5	V
	Input Low - V_{IL}	Falling threshold	0.8	1.1		V
DRIVERS (OUT_1, OUT_2)						
R_{DSON_H}	Source resistance	VCC = 10V; IOUT100mA; Tj=25℃		1	1.3	Ω
		VCC = 10V; IOUT100mA; full temp. range			1.5	Ω
I_{SOURCE}	Source Current (1)	VCC = 10V; C_{OUT} to GND = 10nF		4		A
I_{SINK}	Sink Current (1)	VCC = 10V; C_{OUT} to GND = 10nF		5		A
R_{DSON_L}	Sink Resistance	VCC = 10V; IOUT100mA ; Tj=25℃		0.7	1	Ω
		VCC = 10V; IOUT100mA ; full temp. range			1.3	Ω
SWITCHING TIME (PWM_1,PWM_2)						
t_R	Rise time	VCC = 10V; C_{OUT} to GND = 2.5nF		10	20	ns
		VCC = 10V; C_{OUT} to GND = 14nF		45	75	ns

Table 4. Electrical Characteristics (continued)
(V_{CC} = 5V to 18V, T_j = -40℃ to 105℃ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_F	Fall time	VCC = 10V; C_{OUT} to GND = 2.5nF		10	20	ns
		VCC = 10V; C_{OUT} to GND = 14nF		35	75	ns
PROPAGATION DELAY						
t_{D_LH}	Delay - Low to High	C_{OUT} to GND = 2.5nF	15	25	35	ns
t_{D_HL}	Delay - High to Low	C_{OUT} to GND = 2.5nF	20	30	40	ns
	Matching between propagation delays		-5		5	ns

Note: 1 Parameter guaranteed by designed, not fully tested in production

4 Device Description and Operation

AP239 is a dual low side driver suitable for charging and discharging large capacitive loads like MOSFETs or IGBTs used in power supplies and DC/DC modules. AP239 can sink and source 4A on both low side driver branch but higher driving current can be obtained by paralleling its outputs.

Even though this device has been designed to cope with loads requiring high peak current and fast switching time, the ultimate driving capability depends on the power dissipation in the device which must be kept below the power dissipation capability of the package. This aspect will be discussed in *Section 5.2*.

For enhanced control of operation AP239 make provision of dual indipendent active high enable pins (ENABLE_1 and ENABLE_2). Connecting those pin to GND pin, will disable the corresponding low side driver.

AP239 uses the VCC pin for supply and GND pin for return.

The dual low-side driver has been design to work with supply voltage in the range of 5 to 18V.

Before VCC overcome the UVLO threshold ($UVLO_{VCC}$), AP239 keeps firmly-OFF both Low-Side MOSFETs then, after the UVLO has crossed, the PWM input keeps the control of the driver operations provided that the corresponding enable pin is active. Both PWM_1 and PWM_2 are internally pulled down so if left floating the corresponding ouptut pins are discharged.

Input pins (PWM_1, PWM_2, ENABLE_1 and ENABLE_2) are CMOS/TTL compatible with capability to work also with voltages up to VCC.

4.1 Input Stage

4.1.1 PWM inputs

The input of the AP239 dual low side driver are compatible to CMOS/TTL levels with capability to be pulled up to VCC.

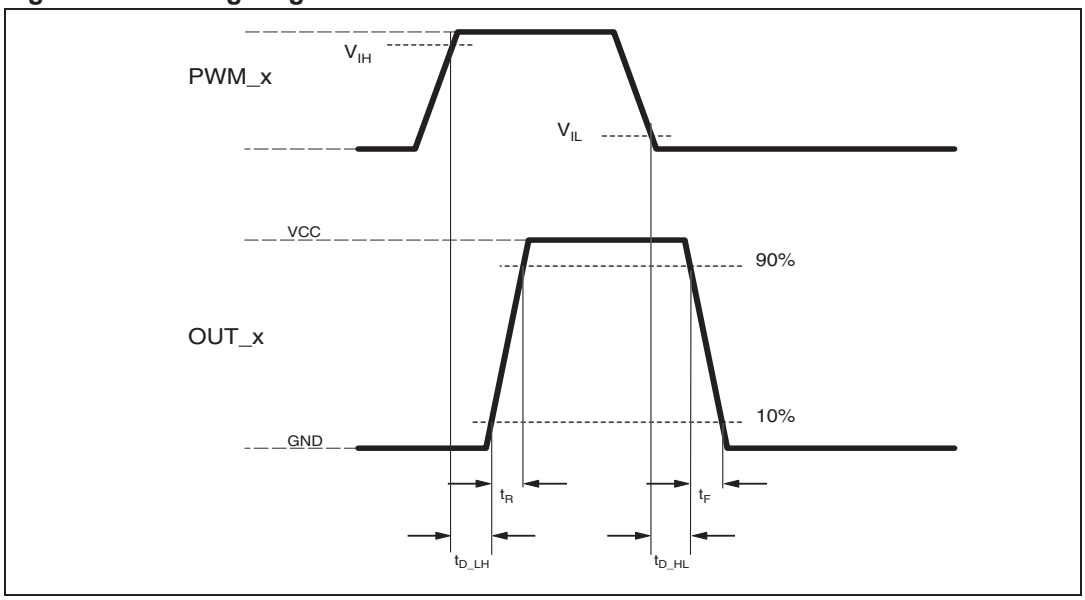
The relation between the input pins (PWM_1, PWM_2) and the corresponding PWM output is depicted in *Figure 3*. In the worst case, input levels above 2.5V are recognized as high voltage and value below 0.8V are recognized as low logic value.

Propagation delays for high-low (t_{D_HL}) and low-high (t_{D_LH}) and rise (t_R) and fall (t_R) times have been designed to ensure operation in fast switching environment.

Matching between delays in the two branches of the AP239 ensure symmetry in the operations and allows parallel output functionality.

Each PWM input feature 10µA pulldown to default OFF the status of the external MOSFET / IGBT.

Figure 3. Timing diagram



4.1.2 Enable Pins

AP239 features two independent enable signals, namely ENABLE_1 and ENABLE_2, to control the operation of each low side driver. Both enable pins are internally pulled up to VCC with a typ. 100kOhm resistance and are active high.

In application where ENABLE_1 and ENABLE_2 are not in use, It is strongly reccomended to connect these pins to VCC directly or with a pull-up resistor.

ENABLE_1 and ENABLE_2 are compatible to CMOS/TTL levels and can be directly pulled up to VCC.

By default, because of the internal pull-up, both drivers are enabled. It is possible to disable one or both low side drivers connecting the corresponding enable signal to GND.

4.2 Output Stage

The output stage of the AP239 make use of ST proprietary lateral DMOS as depicted in *Figure 1.* Both N-DMOS and P-DMOS have been sized to exhibit high driving peak current as well as low ON-resistance: typical peak current is 4A while output resistances are 1Ω and 0.7Ω for P-DMOS and N-DMOS resistance respectively.

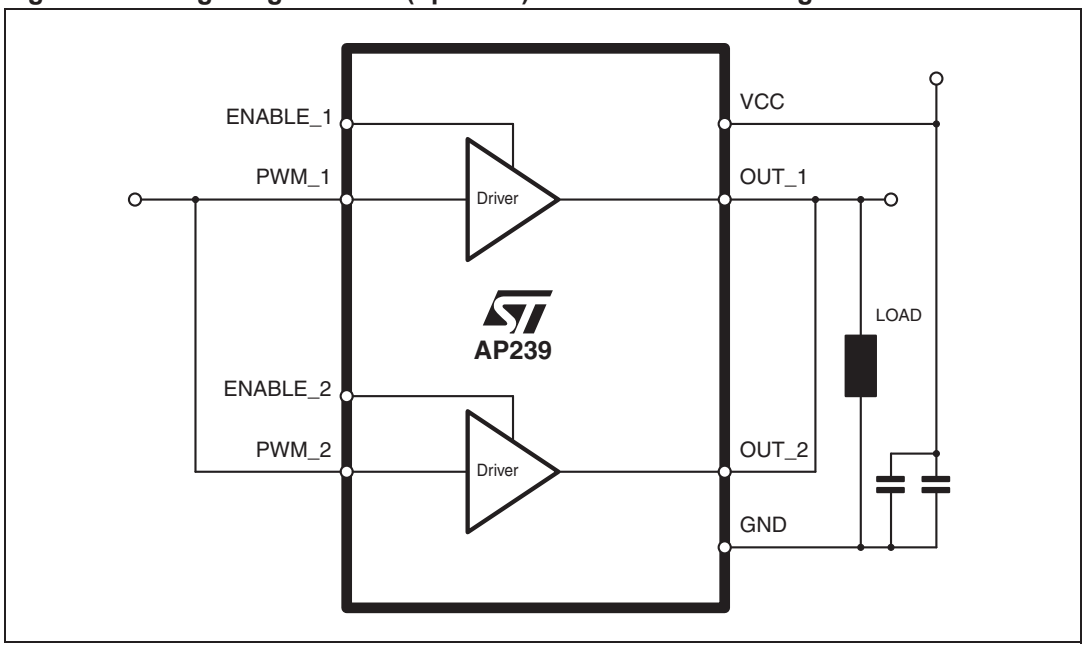
The device features adaptive anti cross-conduction protection. AP239 continuously monitors the status of the internal N-DMOS and P-DMOS: in case of a PWM transition, before switching on the desired DMOS, the device waits until the other DMOS is completely turned-off. No static current will then flow from VCC to GND.

4.3 Parallel Output Operation

For applications demanding high driving current capability (in excess of the 4A provided by the single section), AP239 allows paralleling the operation of the two drivers in order to reach higher current, up to 8A.

This configuration is depicted in *Figure 4* where both PWM_1 and PWM_2 and OUT_1 and OUT_2 are tied together. The matching of internal propagation delays guarantee that the two drivers are switched on and off simultaneously.

Figure 4. Single high current (up to 8A) low-side driver configuration.



4.4 Gate Driver Voltage Flexibility

AP239 allows the user to freely-select the gate drive voltage in order to optimize the efficiency of the application.

The Low-Side MOSFET driving voltage depends on the voltage applied to VCC and can range between 5V to 18V.

5 Design Guidelines

5.1 Output series resistance

An output resistance is generally introduced to allow high frequency operation without exceeding the maximum power dissipation of the driver package.

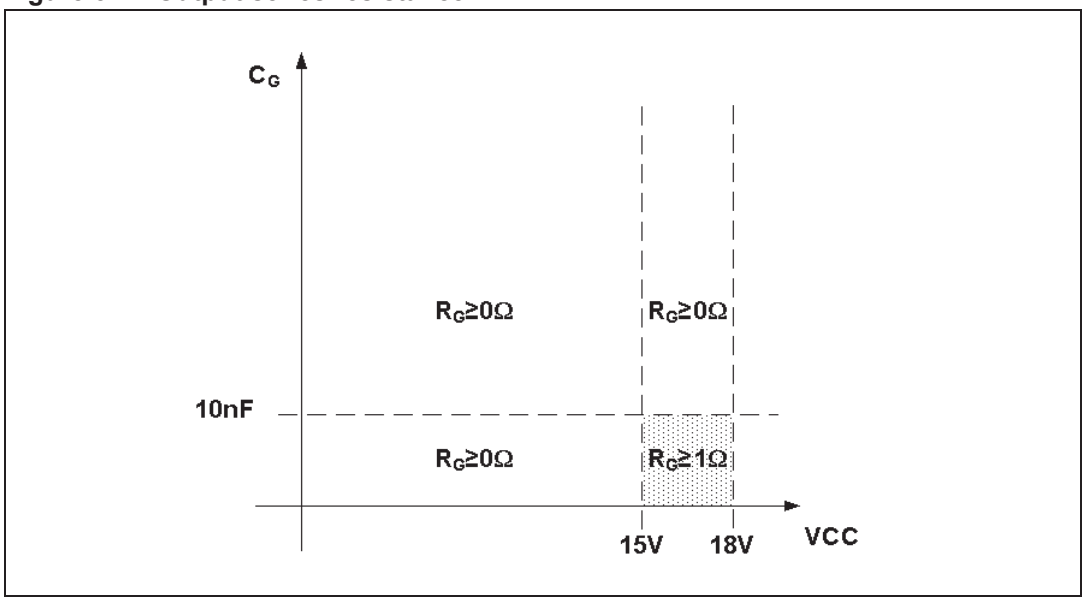
The value of the output resistance can be obtained as described in *Section 5.2*

For application with supply voltages (VCC) greater than 15V, with low capacitive loads (C_G<10nF), caution must be taken when designing with AP239.

In these circumstances, due to its high peak current capability, severe undervoltage on the output pins may occur, which, if not limited in some way, can violate the safe operating area of the output stage of the device.To avoid this phenomena it is mandatory to add a gate resistor R_G of at least 1 Ohm.

Figure 5. is a synthetic view of the boundaries for safe operations of AP239.

Figure 5. Output series resistance



5.2 Power Dissipation

AP239 embeds two high current low side drivers that can be used to drive high capacitive MOSFETs. This section estimates the power dissipated inside the device in normal applications.

Two main terms contribute in the device power dissipation: bias power and drivers' power.

- Bias Power (P_{DC}) depends on the static consumption of the device through the supply pins and it is simply obtained as follow:

  $$P_{DC} = V_{CC} \cdot I_{CC}$$

- Drivers' power is the power needed by the driver to continuously switch ON and OFF the external MOSFETs; it is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs is dissipated by three main factors: external gate resistance (when present), intrinsic MOSFET resistance and intrinsic driver resistance. This last term has to be determined to calculate the device power dissipation.

  The total power dissipated by each section to switch an external mosfets with gate charge Q_G is:

  $$P_{SW} = F_{SW} \cdot (Q_G \cdot V_{CC})$$

When designing an application based on AP239 it is recommended to take into consideration the effect of external gate resistors on the power dissipated by the driver. External gate resistors helps the device to dissipate the switching power since the same power P_{SW} will be shared between the internal driver impedance and the external resistor resulting in a general cooling of the device.

Referring to *Figure 6*, classical mosfet driver can be represented by a push-pull output stage with two different mosfets: P-DMOS to drive the external gate high and N-DMOS to drive the external gate low (with their own R_{dsON}: R_{hi}, R_{lo}). The external power mosfet can be represented in this case as a capacitance (C_G) that stores the gate-charge (Q_G) required by the external power MOSFET to reach the driving voltage (V_{CC}). This capacitance is charged and discharged at the driver switching frequency F_{SW}.

The total power Psw is dissipated among the resistive components distributed along the driving path. According to the external Gate resistance and the power-MOSFET intrinsic gate resistance, the driver dissipates only a portion of Psw as follow (per section):

$$P_{SW} = \frac{1}{2} \cdot C_G \cdot (V_{CC})^2 \cdot Fsw \cdot \left(\frac{R_{hi}}{R_{hi} + R_{Gate} + R_i} + \frac{R_{lo}}{R_{lo} + R_{Gate} + R_i} \right)$$

The total power dissipated from the driver can then be determined as follow:

$$P = P_{DC} + 2 \cdot P_{SW}$$

Figure 6. Equivalent circuit for MOSFET drive.

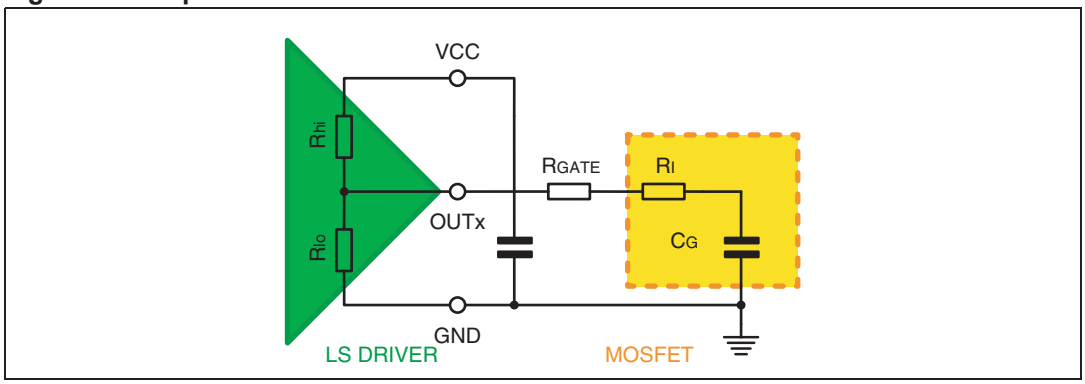
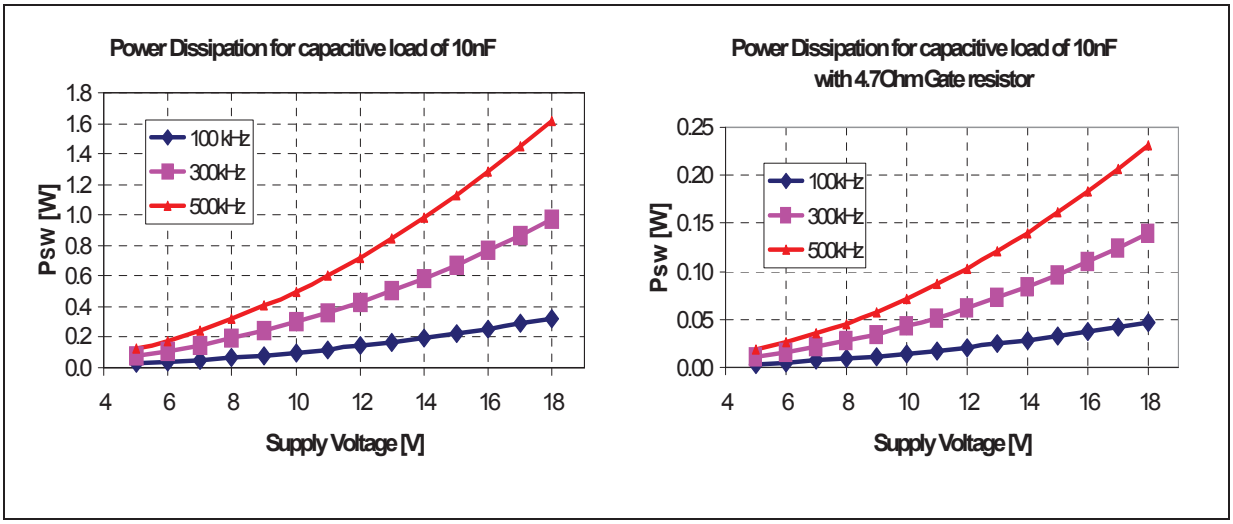


Figure 7. Power dissipation (P_{SW}) estimation.



5.3 Layout Guidelines

The first priority when placing components for these applications has to be reserved to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (also EMI and losses) power connections must be a part of a power plane and anyway realized by wide and thick copper traces: loop must be anyway minimized.

Traces between the driver and the MOSFETS should be short and wide to minimize the inductance of the trace so minimizing ringing in the driving signals. Moreover, VIAs count needs to be minimized to reduce the related parasitic effect.

Small signal components and connections to critical nodes of the application as well as bypass capacitors for the device supply are also important. Locate the bypass capacitor (VCC capacitors) close to the device with the shortest possible loop and use wide copper traces to minimize parasitic inductance.

To improve heat dissipation, place copper area under the IC. This copper area may be connected with other layers (if available) through VIAs to improve the thermal conductivity. The combination of copper pad, copper plane and VIAs under the driver allows the device to reach its best thermal performances.

Figure 8. Driver turn-on and turn-off paths

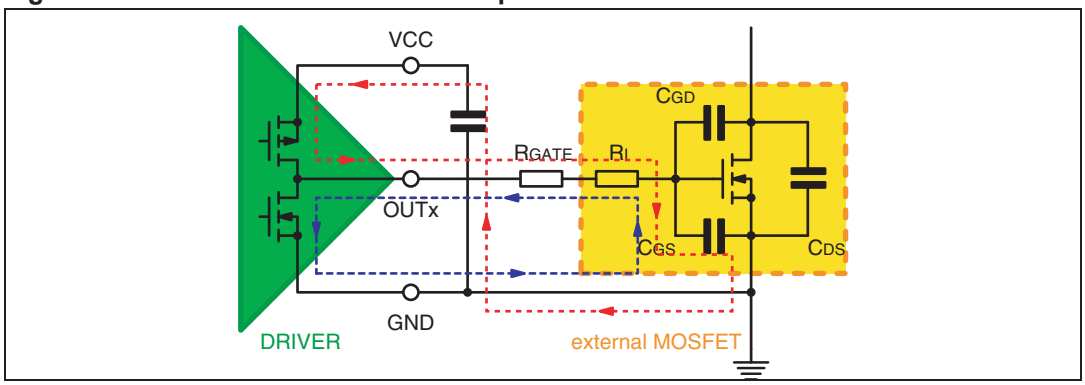
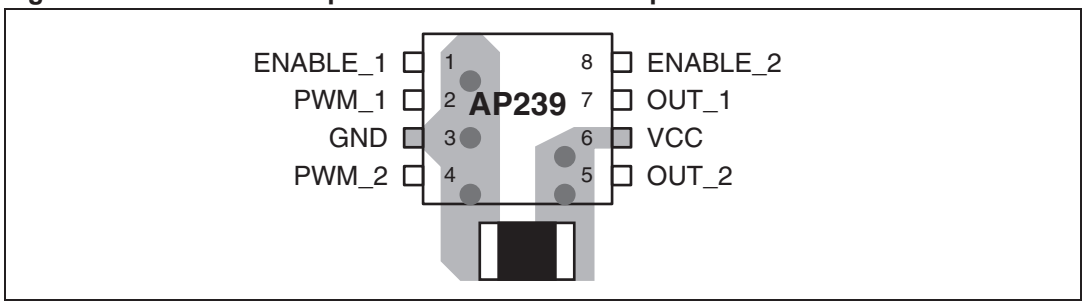


Figure 9. External Components Placement Example.



6 Package Mechanical Data

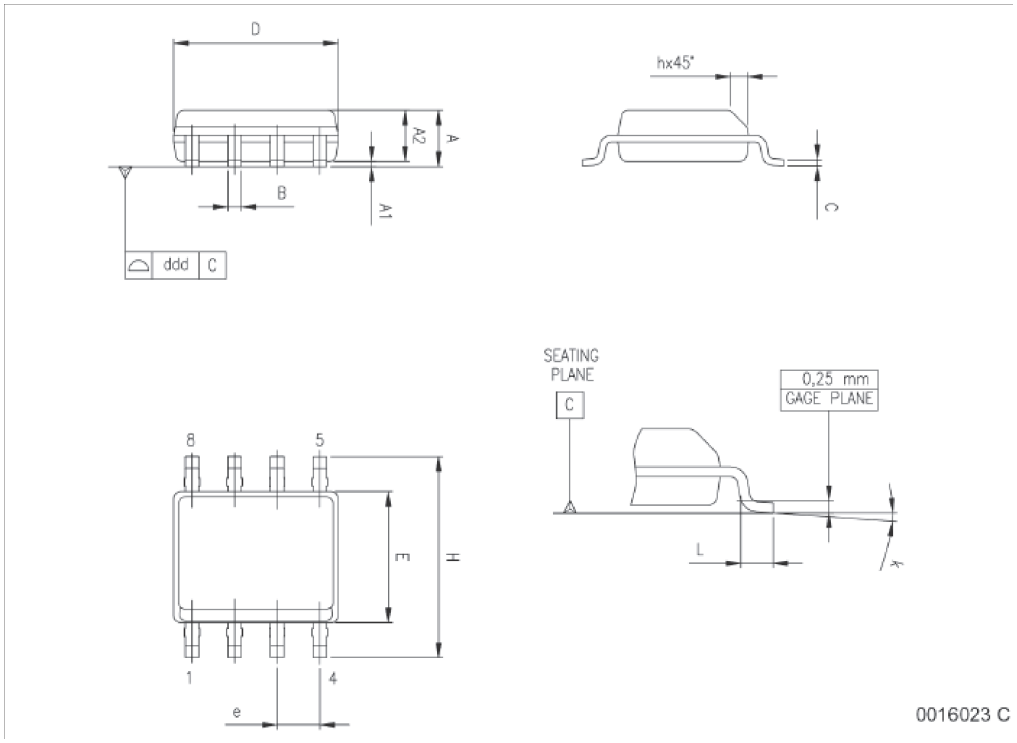
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 5. SO-8 Mechanical Data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. D and F does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

Figure 10. Package Dimensions



7 Revision history

Table 6. Document Revision History

Date	Revision	Changes
Aug. 2007	0.1	Initial release.
Oct.2007	0.2a	Minor text modification
March 2008	0.3	Changes to electrical characteristics, device description Content reworked in order to improve readability
October 2008	1.0	Changes to *Table 1.*, *Table 2.* and sectiot$_{D_LH}$. Content reworked in order to improve readability
June 2009	1.1	Inserted internal Pullup resistors on ENABLE pins in *Figure 1*. Updated values of t_{D_LH} and t_{D_HL} in *Table 4*. Updated *Table 1.* and section *4.1.2*

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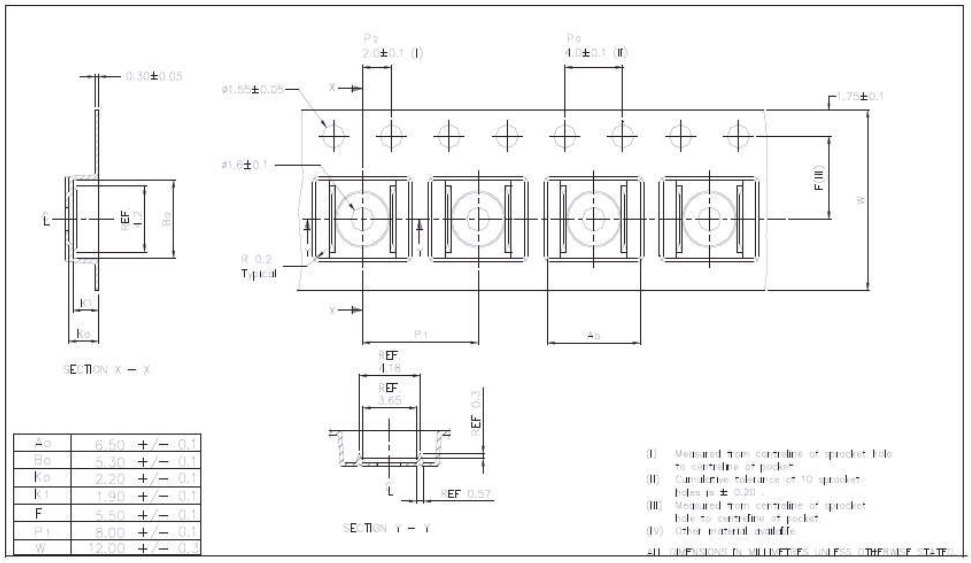
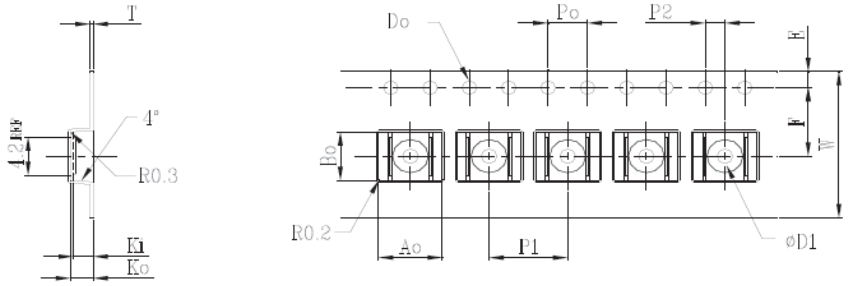
TIPICAL PACKING SPECS
FOR DEVICES ON SO8 NARROW PACKAGE

Fig 1: C-PAK SOIC 8L Narrow Body Carrier Tape Drawing



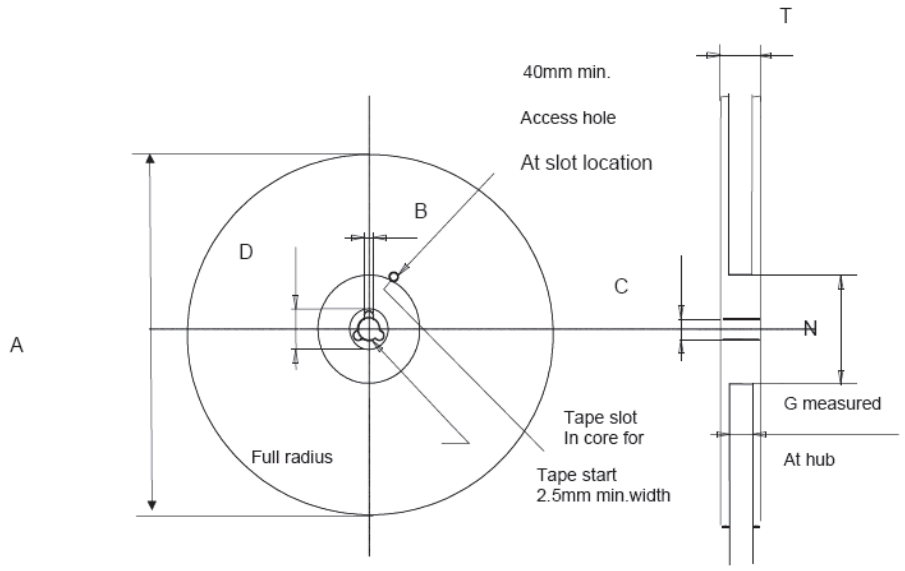
Ao	6.50 +/– 0.1
Bo	5.30 +/– 0.1
Ko	2.20 +/– 0.1
K1	1.90 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

Fig 2: PCT SOIC 8L Narrow Body Carrier Tape Drawing



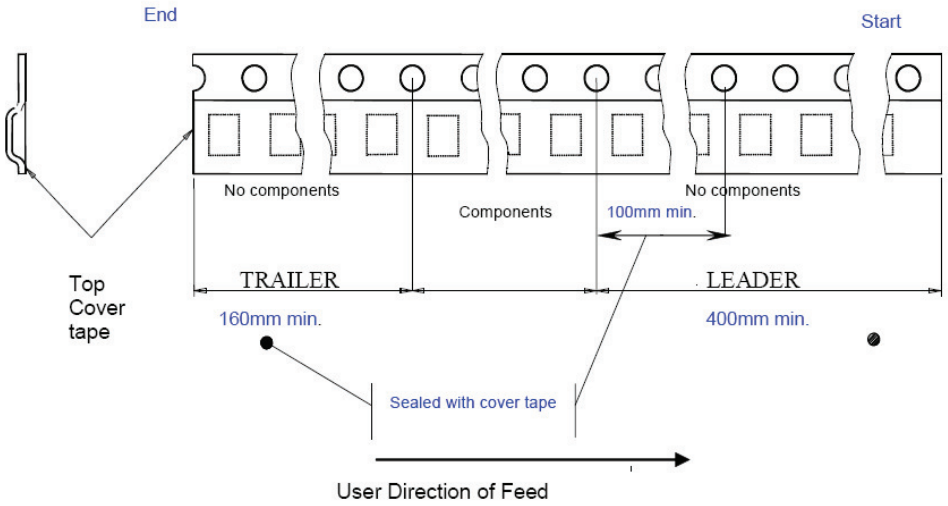
Part Number	Ao ±0.1	Bo ±0.1	Ko ±0.1	Ki ±0.1	T +0.05	E ±0.1	F ±0.05	Po ±0.1	P1 ±0.1	P2 ±0.05	Do +0.1	D1 +0.1	W ±0.3
PC1-S08FP-2203-360C-SD	6.5	5.3	2.2	1.9	0.30	1.75	5.5	4.0	8.0	2.0	ø1.5	ø1.5	12.0

REEL DIMENSIONS



LEADER AND TRAILER

FIGURE 3



TAPE SIZES	A max.	B min.	C	D min.	N min.	G	T max.
12 mm	330	1.5	13 -/+ 0.2	20.2	60	12.4 +2/-0	18.4

TAPE SIZES	D	E	Po	T max.	Ao Bo Ko
8/12/16	1.5 + 0.1 / 0	1.75 + /- 0.1	4 +/- 0.1	0.4	See notes

TAPE SIZES	B1 max.	D1 min.	F	K max.	P2	R min.	W
12 mm	8.2	1.5	5.5 +/- 0.05	4.5	2 +/- 0.05	30	12 +/- 0.3