

## P-channel 20 V, 0.075 $\Omega$ typ., 4 A STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet – target specification

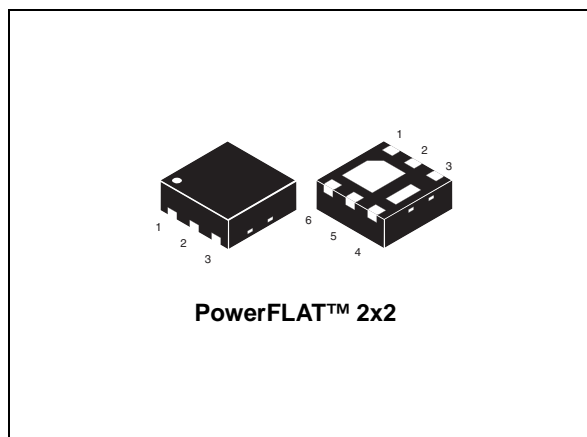
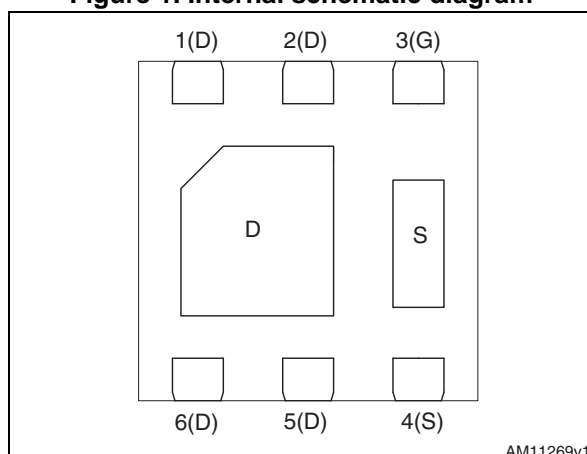


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL4P2UH7	20 V	0.1 $\Omega$ @ 4.5 V	4 A

- Ultra logic level
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power losses

### Applications

- Switching applications

### Description

This device exhibits low on-state resistance and capacitance for improved conduction and switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL4P2UH7	4L2U	PowerFLAT™ 2x2	Tape and reel

**Note:** For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 8$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.5	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	2.4	W
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-pcb}$
2. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max, single operation	52	$^\circ\text{C/W}$

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

**Note:** For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	20			V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0$			10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	0.4		1	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$		0.075	0.1	$\Omega$
		$V_{GS} = 2.5\text{ V}$ , $I_D = 2\text{ A}$		0.1	0.135	$\Omega$
		$V_{GS} = 1.8\text{ V}$ , $I_D = 2\text{ A}$		0.15	0.2	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 15\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	530	-	pF
$C_{oss}$	Output capacitance		-	90	-	pF
$C_{rss}$	Reverse transfer capacitance		-	50	-	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 3</a> )	-	5.5	-	nC
$Q_{gs}$	Gate-source charge		-	1	-	nC
$Q_{gd}$	Gate-drain charge		-	1.5	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 1\text{ }\Omega$ , $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 4</a> )	-	5	-	ns
$t_r$	Rise time		-	13	-	ns
$t_{d(off)}$	Turn-off delay time		-	13	-	ns
$t_f$	Fall time		-	20	-	ns

**Note:** For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1\text{ A}$ , $V_{GS} = 0$	-	-	1	V
$t_{rr}$	Reverse recovery time	$V_{DD} = 16\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $I_{SD} = 1\text{ A}$ $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 4</a> )	-	15		ns
$Q_{rr}$	Reverse recovery charge		-	5		nC
$I_{RRM}$	Reverse recovery current		-	0.7		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Note:** For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

### 3 Test circuits

Figure 2. Switching times test circuit for resistive load

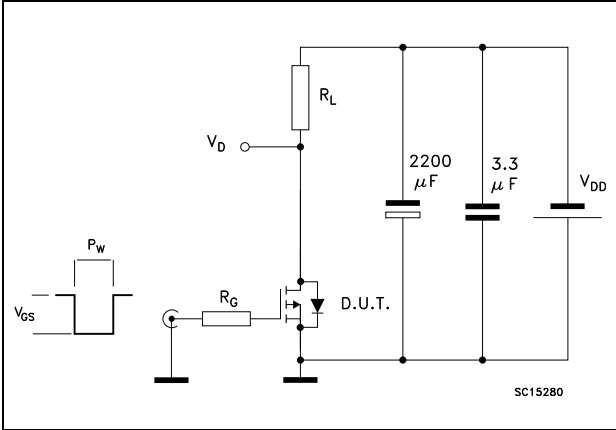


Figure 3. Gate charge test circuit

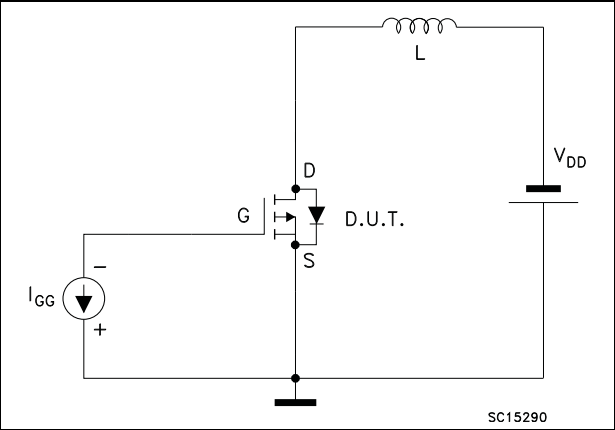
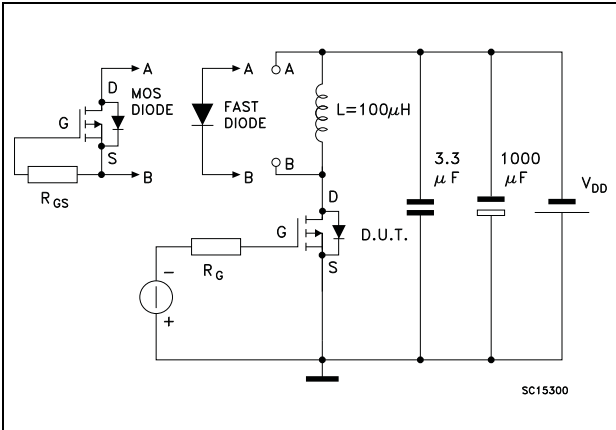


Figure 4. Test circuit for inductive load switching and diode recovery times



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 8. PowerFLAT™ 2 x 2 mechanical data**

Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 5. Drawing dimension PowerFLAT™ 2 x 2

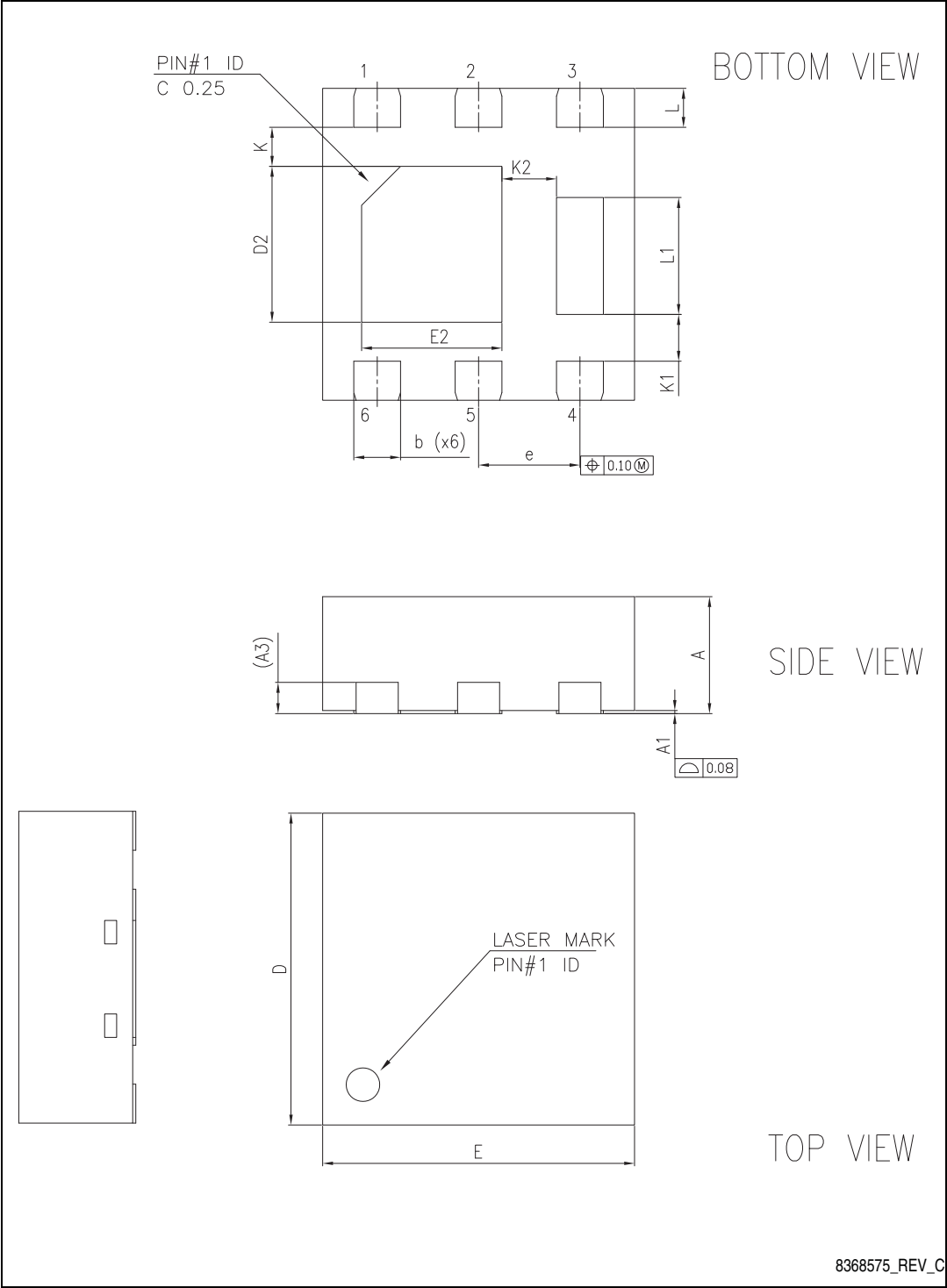
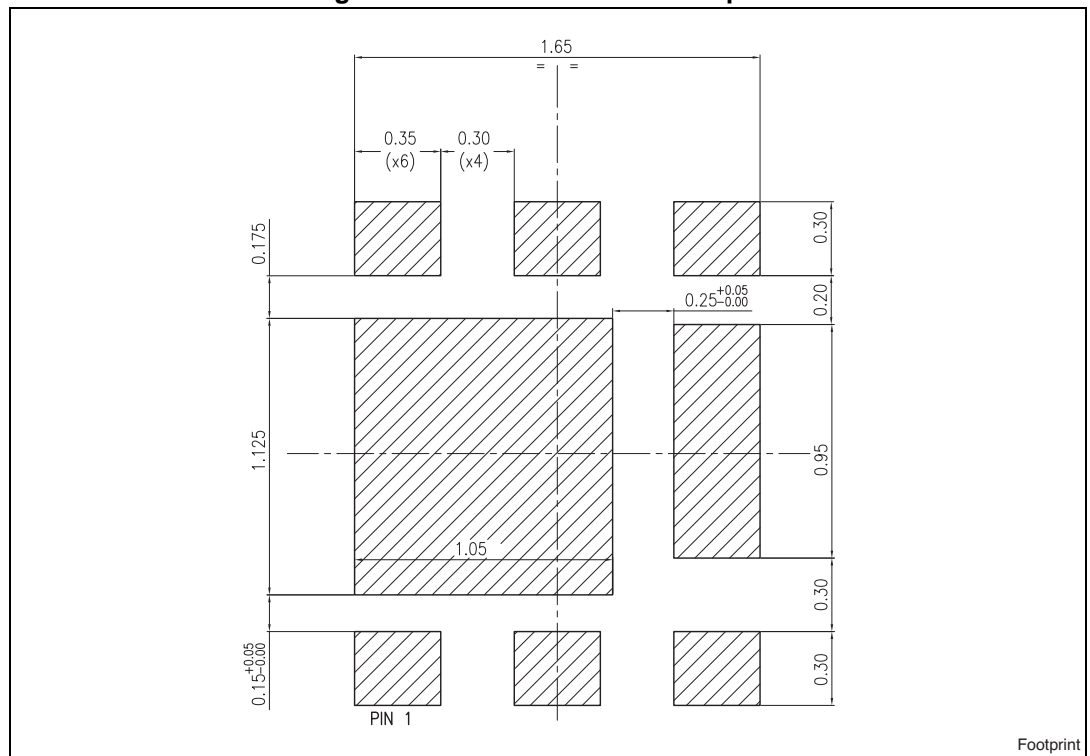




Figure 6. PowerFLAT™ 2 x 2 footprint



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
22-Jul-2013	1	First release.

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