STA8088EX

High flexible GPS/Galileo/Glonass/QZSS receiver with powerful processing (ARM9)

Data brief

Features

- STMicroelectronics® 3rd generation positioning receiver with 32 tracking channels and 2 fast acquisition channels compatible with GPS, Galileo, Glonass and QZSS systems
- Embedded RF front-end with built-in LNA
- -162dBm indoor sensitivity (tracking mode)
- Fast TTFF < 1 s in hot start and 35 s in cold start
- Support of ST-AGPSTM Multimode Assisted GPS (extended ephemeris solution)
- High performance ARM946 MCU (up to 208 MHz)
- 256 Kbyte embedded TCM/SRAM
- FSMC external memory interface (NAND, NOR and SRAM)
- External SQI Flash interface
- One 16-bit Extended Function Timer (EFT) with input capture/ output compare and PWM.
- Four 32-bit free running timers/ counters
- Real Time Clock (RTC) circuit
- 3 UARTs (one full for modem support)
- 1 I^2C master/slave interface
- 1 Synchronous Serial Port (SSP, Motorola-SPI supported)
- USB2.0 dual role full speed (12 MHz) with integrated physical layer transceiver
- 2 Secure-Digital Multimedia Memory Card Interfaces (SDMMC)
- 2 Controller Area Network (CAN)
- 1 Multichannel Serial Port (MSP)
- GPIO port for a total of up to 64 GPIOs
- 8-channels ADC (10 bit)
- Selectable 1.8 V or 3.3 V I/Os for specific I/O ports
- 3 embedded 1.8 V voltage regultators

TFBGA169

- Operating condition:
  - V_{DD12}: 1.2 V ±10 %
  - $V_{DD18/RF18}$: 1.8 V ±5 %
  - V_{LPVR}: 1.62 V to 3.6 V
  - V_{ddIO}: 1.8 V -5 %/ +10 %; 3.3 V ±10 %
- Package:
  - TFBGA169 9 x 9 x 1.2 mm 0.65 pitch
- Ambient temperature range: -40/ +85 °C

Description

STA8088EX is a single die standalone positioning receiver IC working on multiple constellations (GPS/GALILEO/GLONASS/QZSS).

By combining the ARM946 microcontroller core with the large number of peripherals/ interfaces, STA8088EX provides a highly-flexible and cost effective solution for hand-held and telematic applications.

The device is the ideal solution for sensor-based and sensor-less ST Dead Reckoning technologies which enhance positioning accuracy even in areas without GPS signals, like tunnels and indoor parking.

Table 1. Device summary

Package	Order code	
	GNSS	GPS only
TFBA169 9 x 9 mm	STA8088EXG	STA8088EX
	STA8088EXGA	STA8088EXA

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1 Overview

STA8088EX is an integrated System-On-Chip device designed for a highly-flexible and cost effective solution for vehicle, hand-held navigation and telematic applications.

It combines a high performance ARM946 microprocessor with embedded enhanced peripherals and I/O capabilities, RF front-end and base band processor to support GPS, Galileo, Glonass and QZSS satellite systems.

It also provides clock generation via PLL, backup logic with real time clock and it supports USB2.0 standard at full speed.

STA8088EX is software compatible with the ARM processor family. The device is power supplied with 1.8 V and uses three on-chip voltage regulators to internally supply the RF front-end, core logic the backup logic. In order to reduce the power consumption the chip can be directly powered with 1.2 V bypassing the embedded voltage regulators.

I/O lines are compatible with 1.8 V and 3.3 V.

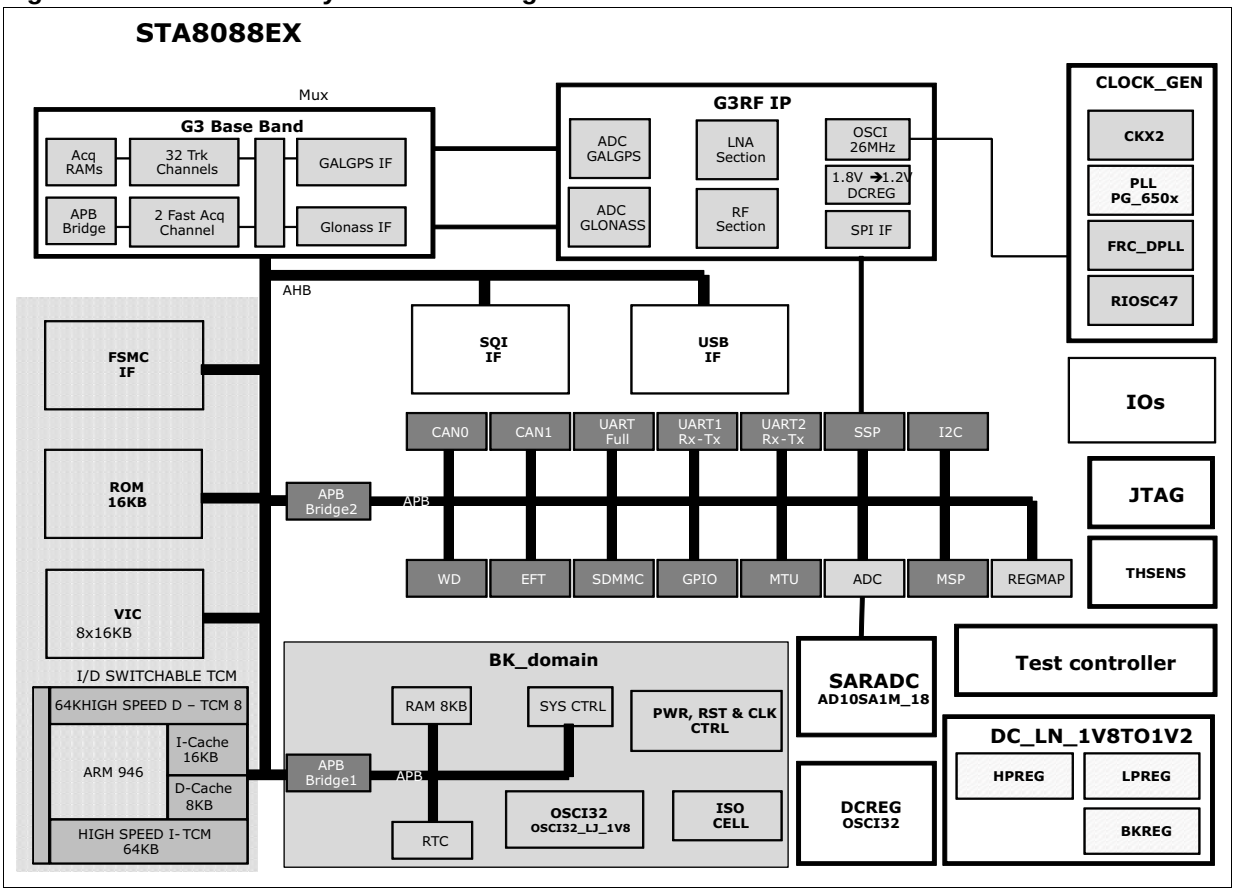
The chip, using STMicroelectronics CMOSRF technology, is housed in a TFBGA169 (9 x 9 x 1.2 mm) package.

STA8088EXA version fulfilling high quality and service level automotive market requirements, is the ideal solution for OEM telematic applications.

2 Pin description

2.1 Block diagram

Figure 1. STA8088EX system block diagram



2.2 TFBGA169 ball out

Table 2. TFBGA169 ball out

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GNDIO	USB_DM (UART1_RX)	USB_DP (UART1_TX)	CAN0TX	FSMC ADD22 (P1.30)	FSMC ADD18 (P1.26)	FSMC ADD9 (P1.17)	FSMC ADD16 (P1.24)	FSMC DATA15	FSMC DATA8	FSMC DATA5	FSMC DATA4	GNDIO
B	VDDIO_r2	CAN1TX (P0.8)	CAN1RX (P0.9)	CAN0RX	FSMC ADD23 (P1.31)	FSMC ADD19 (P1.27)	FSMC ADD6 (P1.14)	FSMC ADD10 (P1.18)	FSMC DATA14	FSMC DATA2	VDDIO_r3	FSMC BLn1	FSMC BLn0
C	MSPOUT SCLK (P0.31)	MSPOUT LRCLK (P0.30)	MSPOUT_SD/ Iopwrsel_r2 (P0.29)	VDDIO_r5	FSMC WTn	FSMC ADD20 (P1.28)	FSMC ADD1 (P1.9)	FSMC ADD14 (P1.22)	FSMC DATA12	FSMC DATA10	FSMC CS2	FSMC_CS3/ Iopwrsel_r3	FSMC DATA0
D	MMC_CLK	MMC_CMD (P0.28)	VDD18 MVR	VDD12_MVR	FSMC WEN	FSMC ADD21 (P1.29)	FSMC ADD2 (P1.10)	FSMC ADD11 (P1.19)	FSMC CLK	FSMC ADV	FSMC DATA9	FSMC CS1	FSMC CS0
E	MMC_D0 (P0.20)	MMC_D1 (P0.21)	MMC_D2 (P0.22)	MMC_D3 (P0.23)	FSMC OutEN	FSMC ADD4 (P1.12)	FSMC ADD7 (P1.15)	FSMC ADD17 (P1.25)	FSMC ADD13 (P1.21)	FSMC DATA1	FSMC DATA3	GPIO2 (P0.2)	GPIO5 (P0.5)
F	MMC_D4 (P0.24)	MMC_D5 (P0.25)	MMC_D6 (P0.26)	MMC_D7 (P0.27)	FSMC ADD5 (P1.13)	FSMC ADD3 (P1.11)	FSMC ADD0 (P1.8)	FSMC ADD8 (P1.16)	FSMC ADD12 (P1.20)	FSMC DATA7	SPI_CLK (P1.1)	GPIO1 (P0.1)	GPIO4 (P0.4)
G	TMS	TRSTn	TDI	TCK	GND	GND	GND	VDD18 MVR	FSMC DATA11	FSMC DATA6	SPI_DO (P1.3)	VDDIO_r1	GPIO7 (P0.7)
H	VRF12 RFADC	TP_IF_P	GND_RF	TDO	VDD12 LPVR	GNDIO	GND	GND	FSMC ADD15 (P1.23)	FSMC DATA13	SPI_DI (P1.2)	GPIO3 (P0.3)	GPIO6 (P0.6)
J	VRF12 LNA	TP_IF_N	GND_RF	GND_RF	STBY_OUT	STDBYn	VDD12_MVR	VDD LPVR	VDD12_MVR	PPS_OUT	SPI_CSN/ IOpwrsel_r1 (P1.0)	UART0 RTS (P0.14)	GPIO0 (P0.0)
K	LNA IN	GND LNA	GND_RF	GND_RF	GND_RF	GND_RF	WAKEUP	RSTn	ADC_IN8	VDDIO_r4	UART2_TX/ BOOT_0 (P1.5)	UART2_RX (P1.4)	UART0_TX/ BOOT_1 (P1.7)
L	GND LNA	GND LNA	GND_RF	GND_RF	VRF12 RFVCO	VRF12 RFDIG	ADC_IN1	ADC_IN4	ADC_IN2	SQI_SIO2 (P0.12)	SQI_SCK	UART0 DTR (P0.18)	UART0_RX (P1.6)
M	LNA OUT	VRF18 RFVR	GND_RF	GND_RF	VRF12 MIX	XTAL OUT	ADC_IN3	ADC_IN6	RTC_XTI	SQI_SIO1 (P0.11)	SQI_Cen/ Iopwrsel_r4 (P0.19)	UART0 CTS (P0.15)	UART0 DSR (P0.16)
N	GND_RF	VRF12OUT RFVR	VRF12 RFA	RFA IN	VRF12_IF	XTAL IN	ADC_IN7	ADC_IN5	RTC_XTO	SQI_SIO3 (P0.13)	SQI_SIO0 (P0.10)	UART0 DCD (P0.17)	GNDIO

2.3 Power supply pins

Table 3. Power supply pins

Symbol	I/O	Functions	TFBGA169
VDD18_MVR	Pwr	Digital supply voltage for main voltage regulator (1.8 V)	D3, G8
VDD12_MVR	Pwr	Digital supply voltage for core circuitry (1.2 V). When using the MVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	J7, D4, J9
VDD_LPVR	Pwr	Digital supply voltage for low power voltage regulator (1.62 V - 3.6 V)	J8
VDD12_LPVR	Pwr	Digital supply voltage for backup logic (1.2 V). When using the LPVR, this pin shall not be driven by an external voltage supply, but a capacitance shall be connected between these pins and GND to guarantee on-chip voltage stability.	H5
VDD_IOR1	Pwr	Digital supply voltage for I/O ring 1 (1.8 V or 3.3 V)	G12
VDD_IOR2	Pwr	Digital supply voltage for I/O ring 2 (1.8 V or 3.3 V)	B1
VDD_IOR3	Pwr	Digital supply voltage for I/O ring 3 (1.8 V or 3.3 V)	B11
VDD_IOR4	Pwr	Digital supply voltage for I/O ring 4 (1.8 V or 3.3 V)	K10
VDD_IOR5	Pwr	Digital supply voltage for I/O ring 5 (3.3 V)	C4
VRF18_RFVR	Pwr	Analog supply voltage for RF voltage regulator (1.8 V)	M2
GND	GND	Digital supply ground for core (5 pins)	G5, G6, G7, H7, H8
GND_IO	GND	Digital supply ground for I/O circuitry (4 pins)	A1, A13, H6, N13
VRF12OUT_RFVR	Pwr	RF voltage regulator 1.2 V output	N2
VRF12_LNA	Pwr	Analog supply voltage for LNA (1.2 V)	J1
VRF12_RFA	Pwr	Analog supply voltage for RFA (1.2 V)	N3
VRF12_Mix	Pwr	Analog supply voltage for Mixer (1.2 V)	M5
VRF12_IF	Pwr	Analog supply voltage for IF (1.2 V)	N5
VRF12_RFDig	Pwr	Analog supply voltage for RF Digital (1.2 V)	L6
VRF12_RFVCO	Pwr	Analog supply voltage for VCO (1.2 V)	L5
VRF12_RFADC	Pwr	Analog supply voltage for RF ADC (1.2 V)	H1
GND_LNA	GND	Analog supply ground for LNA (3 pins)	K2, L1, L2
GND_RF	GND	Analog supply ground to RF (12 pins)	H3, J3, J4, K3, K4, K5, K6, L3, L4, M3, M4, N1

2.4 Main function pins

Table 4. Main function pins

Symbol	I/O voltage	I/O	Functions	TFBGA169
RSTn	1.2 V	I	Reset Input with Schmitt-Trigger characteristics and noise filter.	K8
STDBYn	1.2 V	I	When low, the chip is forced in Standby mode. All pins in high impedance except the ones powered by backup supply	J6
WAKEUP	1.2 V	I	WAKEUP from STANDBY mode	K7
STDBY_Out	1.2 V	O	When low, indicates the chip is in Standby mode.	J5
PPS_Out	VDD_IOR1	O	Pulsed per second output	J10
RTC_XTI	1.5 V (max)	I	Input of the 32 KHz oscillator amplifier circuit and input of the internal real time clock circuit.	M9
RTC_XTO	1.5 V (max)	O	Output of the oscillator amplifier circuit.	N9
CAN0TX	VDD_IOR5	O	CAN 0 - transmit data output	A4
CAN0RX	VDD_IOR5	I	CAN 0 - receive data input	B4
USB_DM/UART1_RX	VDD_IOR5	USB/O	USB D- signal / UART 1 Rx data	A2
USB_DP/UART1_TX	VDD_IOR5	USB/I	USB D+ signal / UART 1 Tx data	A3
ADC_IN[1:8]	1.4 V – 0 V typ range	I	ADC analog input [1:8]	L7, L9, M7, L8, N8, M8, N7, K9
MMC_CLK	VDD_IOR2	O	MMC_CLK: multimedia clock line	D1

2.5 Test / emulated dedicated pins

Table 5. Test/emulated dedicated pins

Symbol	I/O Voltage	I/O	Functions	TFBGA169
TCK	VDD_IOR5	I	JTAG test clock	G4
TDI	VDD_IOR5	I	JTAG test data in	G3
TDO	VDD_IOR5	O	JTAG test data out	H4
TMS	VDD_IOR5	I	JTAG test mode select	G1
TRSTn	VDD_IOR5	I	JTAG test circuit reset	G2
TP_IF_P	VRF12_IF	O	Diff. test point for IF – positive	H2
TP_IF_N	VRF12_IF	O	Diff. test point for IF – negative	J2

2.6 FSMC external memory interface pins

Table 6. FSMC memory interface pins

Symbol	I/O Voltage	I/O	Functions	TFBGA169
FSMC_Data[15:0]	VDD_IOR3	I/O	FSMC EMI data bus	C13, E10, B10, E11, A12, A11, G10, F10, A10, D11, C10, G9, C9, H10, B9, A9
FSMC_Add[23:0](1)(2)	VDD_IOR3	O	FSMC EMI address bus	F7, C7, D7, F6, E6, F5, B7, E7, F8, A7, B8, D8, F9, E9, C8, H9, A8, E8, A6, B6, C6, D6, A5, B5
FSMC _OutEN	VDD_IOR3	O	FSMC EMI output enable	E5
FSMC _WEN	VDD_IOR3	O	FSMC EMI write enable	D5
FSMC _WTn	VDD_IOR3	I	FSMC EMI wait (SNOR, CRAM)	C5
FSMC _BLn[0,1]	VDD_IOR3	O	FSMC EMI byte lane	B13, B12
FSMC _CLK	VDD_IOR3	O	FSMC EMI clk	D9
FSMC _ADV	VDD_IOR3	O	FSMC EMI address valid	D10
FSMC _CS0	VDD_IOR3	O	FSMC EMI chip select for external memory bank 0	D13
FSMC _CS1	VDD_IOR3	O	FSMC EMI chip select for external memory bank 1	D12
FSMC _CS2	VDD_IOR3	O	FSMC EMI chip select for external memory bank 2	C11
FSMC _CS3/ iopwrsel_r3	VDD_IOR3	O	FSMC EMI chip select for external memory bank 3 / I/O ring 3 power selection	C12

1. FSMC_Add[23:0] are multiplexed with P1[31:8] - see *Table 9*
2. In case of NAND memory usage the
   FSMC_Add16 is used as CLE
   FSMC_Add17 is used as ALE

2.7 SQI pins

Table 7. SQI pins

Symbol	I/O Voltage	I/O	Functions	TFBGA169
SQI_SIO3	VDD_IOR4	I/O	SQI Flash data I/O 3	N10
SQI_SIO2	VDD_IOR4	I/O	SQI Flash data I/O 2	L10
SQI_SIO1/SO	VDD_IOR4	I/O	SQI Flash data I/O 1 / ser. O	M10
SQI_SIO0/SI	VDD_IOR4	I/O	SQI Flash data I/O 0 / ser. I	N11

Table 7. SQI pins (continued)

Symbol	I/O Voltage	I/O	Functions	TFBGA169
SQI_SCK	VDD_IOR4	O	SQI Flash clock	L11
SQI_CEn/ iopwrsel_r4	VDD_IOR4	O	SQI Flash chip enable / I/O ring 4 power selection	M11

SQI pins are multiplexed with P0[13:10] and P0[19] (see *Table 8*).

2.8 Port 0 pins

Port 0 consists of a 32-bit bidirectional I/O port. It can be either used as general purpose input or output port, or configured according to the associated alternate functions.

Table 8. Port 0 pins

Symbol	I/O voltage	I/O	Mode	Functions	TFBGA169
P0.0	VDD_IOR1	I/O	Default	GPIO.0: general purpose I/O	J13
		I	A	PPS_IN: pulse per second input	
		O	B	PPS_Out: pulse per second output	
		O	C	SQI_CEn: SQI Flash chip enable	
P0.1	VDD_IOR1	I/O	Default	GPIO.1: general purpose I/O	F12
		O	A	RTC_CLKO: RTC clock out	
P0.2	VDD_IOR1	I/O	Default	GPIO.2: general purpose I/O	E12
		O	A	MMC2_CLK: MMC 2 clock line	
P0.3	VDD_IOR1	I/O	Default	GPIO.3: general purpose I/O	H12
		I/O	A	MMC2_CMD: MMC 2 command line	
P0.4	VDD_IOR1	I/O	Default	GPIO.4: general purpose I/O	F13
		I/O	A	MMC2_DATA3: MMC 2 data 3	
P0.5	VDD_IOR1	I/O	Default	GPIO.5: general purpose I/O	E13
		I/O	A	MMC2_DATA2: MMC 2 data 2	
P0.6	VDD_IOR1	I/O	Default	GPIO.6: general purpose I/O	H13
		I/O	A	MMC2_DATA1: MMC 2 data 1	
P0.7	VDD_IOR1	I/O	Default	GPIO.7: general purpose I/O	G13
		I/O	A	MMC2_DATA0: MMC 2 data 0	
P0.8	VDD_IOR5	O	Default	CAN1TX: CAN 1 transmit data output	B2
		I/O	A	GPIO.8: general purpose I/O	
		I/O	B	I2C_SD: I2C serial data	

Table 8. Port 0 pins (continued)

Symbol	I/O voltage	I/O	Mode	Functions	TFBGA169
P0.9	VDD_IOR5	I	Default	CAN1RX: CAN 1 receive data input	B3
		I/O	A	GPIO.9: general purpose I/O	
		O	B	I2C_SCLK: I2C clock	
P0.10	VDD_IOR4	I/O	Default	SQI_SIO0/SI: SQI Flash data I/O 0 / ser. I	N11
		I/O	A	GPIO10: general purpose I/O	
P0.11	VDD_IOR4	I/O	Default	SQI_SIO1/SO: SQI Flash data I/O 1 / ser. O	M10
		I/O	A	GPIO11: general purpose I/O	
P0.12	VDD_IOR4	I/O	Default	SQI_SIO2: SQI Flash data I/O 2	L10
		I/O	A	GPIO12: general purpose I/O	
P0.13	VDD_IOR4	I/O	Default	SQI_SIO3: SQI Flash data I/O 3	N10
		I/O	A	GPIO13: general purpose I/O	
P0.14	VDD_IOR1	O	Default	UART0_RTS: UART0 request to send	J12
		I/O	A	GPIO14: general purpose I/O	
		I	C	MSPIN_sclk: MSP serial clock input	
P0.15	VDD_IOR1	I	Default	UART0_CTS: UART0 clear to send	M12
		I/O	A	GPIO15: general purpose I/O	
		I	B	Timer_ICAPA: extended function timer - input capture A	
		I	C	MSPIN_lrclk: MSP left/right clock input	
P0.16	VDD_IOR1	I	Default	UART0_DSR: UART0 data set ready	M13
		I/O	A	GPIO16: general purpose I/O	
		O	B	Timer_OCMPA: extended function timer – output compare A	
		I	C	MSPIN_SD: MSP serial data input	
P0.17	VDD_IOR1	I	Default	UART0_DCD: UART0 data carrier detect	N12
		I/O	A	GPIO17: general purpose I/O	
		I	B	Timer_ICAPB: extended function timer - input capture B	
P0.18	VDD_IOR1	O	Default	UART0_DTR: UART0 data terminal read	L12
		I/O	A	GPIO18: general purpose I/O	
		O	B	Timer_OCMPB: extended function timer – output compare B	
P0.19	VDD_IOR4	O	Default	SQI_Cen/iopwrsel_r4: SQI Flash chip enable / I/O ring 4 power selection	M11
		I/O	A	GPIO19: general purpose I/O	

Table 8. Port 0 pins (continued)

Symbol	I/O voltage	I/O	Mode	Functions	TFBGA169
P0.20	VDD_IOR2	I/O	Default	MMC_DATA0: multimedia card data 0	E1
		I/O	A	GPIO20: general purpose I/O	
		O	B	MAG_0GNS: GNS 3bit coding output (MAG0)	
P0.21	VDD_IOR2	I/O	Default	MMC_DATA1: multimedia card data 1	E2
		I/O	A	GPIO21: general purpose I/O	
		O	B	MAG_1GNS: GNS 3bit coding output (MAG1)	
P0.22	VDD_IOR2	I/O	Default	MMC_DATA2: multimedia card data 2	E3
		I/O	A	GPIO22: general purpose I/O	
		I/O	B	MAG_0GGPS: GGPS 3bit coding output (MAG0)	
P0.23	VDD_IOR2	I/O	Default	MMC_DATA3: multimedia card data 3	E4
		I/O	A	GPIO23: general purpose I/O	
		I/O	B	MAG_1GGPS: GGPS 3bit coding output (MAG1)	
P0.24	VDD_IOR2	I/O	Default	MMC_DATA4: multimedia card data 4	F1
		I/O	A	GPIO24: general purpose I/O	
P0.25	VDD_IOR2	I/O	Default	MMC_DATA5: multimedia card data 5	F2
		I/O	A	GPIO25: general purpose I/O	
P0.26	VDD_IOR2	I/O	Default	MMC_DATA6: multimedia card data 6	F3
		I/O	A	GPIO26: general purpose I/O	
P0.27	VDD_IOR2	I/O	Default	MMC_DATA7: multimedia card data 7	F4
		I/O	A	GPIO27: general purpose I/O	
P0.28	VDD_IOR2	I/O	Default	MMC_CMD: multimedia card command line	D2
		I/O	A	GPIO28: general purpose I/O	
P0.29	VDD_IOR2	O	Default	MSPout_SDATA/iopwrsel_r2: MSP serial data output/ I/O ring 2 power selection	C3
		I/O	A	GPIO29: general purpose I/O	
P0.30	VDD_IOR2	O	Default	MSPout_LRCLK MSP left/right clock output	C2
		I/O	A	GPIO30: general purpose I/O	
P0.31	VDD_IOR2	O	Default	MSPout_SCLK: MSP serial clock output	C1
		I/O	A	GPIO31: general purpose I/O	
		O	B	PRNSEQ0	

2.9 Port 1 pins

Port 1 consists of a 32-bit bidirectional I/O port. It can be either used as general purpose input or output port, or configured according to the associated alternate functions.

Table 9. Port 1 pins

Symbol	I/O Voltage	I/O	Mode	Functions	TFBGA169
P1.0	VDD_IOR1	O	Default	SSP_CSN/iopwrsel_r1: SSP chip select active low / I/O ring 1 power selection	J11
		I/O	A	GPIO32: general purpose I/O	
		I/O	B	SignGGPS: GGPS 3bit coding output (Sign)	
		O	C	SQI_Cen: SQI Flash chip enable	
P1.1	VDD_IOR1	I/O	Default	SSP_CLK: SSP clock	F11
		I/O	A	GPIO33: general purpose I/O	
		I/O	B	Clock_GGPS: GGPS clock out	
		O	C	SQI_Clk: SQI Flash clock	
P1.2	VDD_IOR1	I	Default	SSP_DI: SSP serial data input	H11
		I/O	A	GPIO34: general purpose I/O	
		I/O	B	SignGNS: GNS 3bit coding output (Sign)	
		I/O	C	SQI_SIO0/SI: SQI Flash data I/O 0 / ser. I	
P1.3	VDD_IOR1	O	Default	SSP_DO: SSP serial data output	G11
		I/O	A	GPIO35: general purpose I/O	
		I/O	B	Clock_GNS: GNS clock out	
		I/O	C	SQI_SIO1/SO: SQI Flash data I/O 1 / ser. O	
P1.4	VDD_IOR1	I	Default	UART2_RX: UART 2 Rx data	K12
		I/O	A	GPIO36: general purpose I/O	
P1.5	VDD_IOR1	O	Default	UART2_TX: UART 2 Tx data / ARM Boot 0	K11
		I/O	A	GPIO37: general purpose I/O	
P1.6	VDD_IOR1	I	Default	UART0_RX: UART 0 Rx data	L13
		I/O	A	GPIO38: general purpose I/O	
		I/O	C	SQI_SIO2: SQI Flash data I/O 2	
P1.7	VDD_IOR1	O	Default	UART0_TX: UART 0 Tx data / ARM Boot 1	K13
		I/O	A	GPIO39: general purpose I/O	
		I/O	C	SQI_SIO3: SQI Flash data I/O 3	
P1.8	VDD_IOR3	O	Default	FSMC_Add0: FSMC EMI address bus 0	F7
		I/O	A	GPIO40: general purpose I/O	

Table 9. Port 1 pins (continued)

Symbol	I/O Voltage	I/O	Mode	Functions	TFBGA169
P1.9	VDD_IOR3	O	Default	FSMC_Add1: FSMC EMI address bus 1	C7
		I/O	A	GPIO41: general purpose I/O	
P1.10	VDD_IOR3	O	Default	FSMC_Add2: FSMC EMI address bus 2	D7
		I/O	A	GPIO42: general purpose I/O	
P1.11	VDD_IOR3	O	Default	FSMC_Add3: FSMC EMI address bus 3	F6
		I/O	A	GPIO43: general purpose I/O	
P1.12	VDD_IOR3	O	Default	FSMC_Add4: FSMC EMI address bus 4	E6
		I/O	A	GPIO44: general purpose I/O	
P1.13	VDD_IOR3	O	Default	FSMC_Add5: FSMC EMI address bus 5	F5
		I/O	A	GPIO45: general purpose I/O	
P1.14	VDD_IOR3	O	Default	FSMC_Add6: FSMC EMI address bus 6	B7
		I/O	A	GPIO46: general purpose I/O	
P1.15	VDD_IOR3	O	Default	FSMC_Add7: FSMC EMI address bus 7	E7
		I/O	A	GPIO47: general purpose I/O	
P1.16	VDD_IOR3	O	Default	FSMC_Add8: FSMC EMI address bus 8	F8
		I/O	A	GPIO48: general purpose I/O	
P1.17	VDD_IOR3	O	Default	FSMC_Add9: FSMC EMI address bus 9	A7
		I/O	A	GPIO49: general purpose I/O	
P1.18	VDD_IOR3	O	Default	FSMC_Add10: FSMC EMI address bus 10	B8
		I/O	A	GPIO50: general purpose I/O	
P1.19	VDD_IOR3	O	Default	FSMC_Add11: FSMC EMI address bus 11	D8
		I/O	A	GPIO51: general purpose I/O	
P1.20	VDD_IOR3	O	Default	FSMC_Add12: FSMC EMI address bus 12	F9
		I/O	A	GPIO52: general purpose I/O	
P1.21	VDD_IOR3	O	Default	FSMC_Add13: FSMC EMI address bus 13	E9
		I/O	A	GPIO53: general purpose I/O	
P1.22	VDD_IOR3	O	Default	FSMC_Add14: FSMC EMI address bus 14	C8
		I/O	A	GPIO54: general purpose I/O	
P1.23	VDD_IOR3	O	Default	FSMC_Add15: FSMC EMI address bus 15	H9
		O	A	TCXO_CLK	
P1.24	VDD_IOR3	O	Default	FSMC_Add16/CLE: FSMC EMI address bus 16/CLE	A8
		I/O	A	GPIO56: general purpose I/O	

Table 9. Port 1 pins (continued)

Symbol	I/O Voltage	I/O	Mode	Functions	TFBGA169
P1.25	VDD_IOR3	O	Default	FSMC_Add17/ALE: FSMC EMI address bus 17/ALE	E8
		I/O	A	GPIO57: general purpose I/O	
P1.26	VDD_IOR3	O	Default	FSMC_Add18: FSMC EMI address bus 18	A6
		I/O	A	GPIO58: general purpose I/O	
P1.27	VDD_IOR3	O	Default	FSMC_Add19: FSMC EMI address bus19	B6
		I/O	A	GPIO59: general purpose I/O	
P1.28	VDD_IOR3	O	Default	FSMC_Add20: FSMC EMI address bus 20	C6
		I/O	A	GPIO60: general purpose I/O	
P1.29	VDD_IOR3	O	Default	FSMC_Add21: FSMC EMI address bus 21	D6
		I/O	A	GPIO61: general purpose I/O	
P1.30	VDD_IOR3	O	Default	FSMC_Add22: FSMC EMI address bus 22	A5
		I/O	A	GPIO62: general purpose I/O	
P1.31	VDD_IOR3	O	Default	FSMC_Add23: FSMC EMI address bus 23	B5
		I/O	A	GPIO63: general purpose I/O	

2.10 RF front-end pins

Table 10. RF front-end pins

Symbol	I/O Voltage	I/O	Functions	TFBGA169
LNA_IN	VRF12_LNA	I	Low noise amplifier input	K1
LNA_OUT	VRF12_LNA	O	Low noise amplifier output	M1
RFA_IN	VRF12_RFA	I	RF amplifier input	N4
XTAL_In	VRF12_RFDig	I	Input side of crystal oscillator or TCXO input	N6
XTAL_Out	VRF12_RFDig	O	Output side of crystal oscillator	M6

3 General description

3.1 RF front-end

The RF front-end is able to down-convert both the GPS-GALILEO signal from 1575.42 MHz to 4.092 MHz (4 Fo, being F0 = 1.023 MHz) and GLONASS signal from 1601.718 MHz to 8.57 MHz.

It embeds high performance LNA minimizing external component count and an LDO to supply the internal core facilitating requirements for external power supply. A three bits ADC converts the IF signals to sign (SIGN) and magnitude (MAG0 and MAG1). They can be sampled or not by SPI. The magnitude bits are internally integrated in order to control the variable gain amplifiers. The VGA gain can be also set by the SPI interface.

The RF tuner accepts a wide range of reference clocks (10 to 52 MHz) and can generate 16 Fo, 32 Fo, 48 Fo and 64 Fo sampling clock (GALGPS_CLK and GNS_CLK) for the baseband.

3.2 GPS/Galileo/Glonass/QZSS Base Band (G3BB) processor

STA8088EX integrates G3BB proprietary IP, which is the ST last generation high-sensitivity baseband processor fully compliant with GPS, Galileo, Glonass and QZSS satellite systems. Please refer to GPS solution specification and release notes for more details.

The base band receives, from the embedded RF front-end, two separate IF signals codified in sign-magnitude digital format on 3 bits and the related clocks. The Galileo/GPS (GALGPS) and Glonass (GNS) signals at the base band inputs are centered on 4.092 MHz and 8.57 MHz respectively.

The baseband processes the two IF signals performing data codification, sample rate convertion and final frequency convertion to zero IF before acquisition and tracking correlations.

The base band processor has the capability to acquire and track the Galileo, GPS and Glonass signals in a simultaneous or single way, or a combination of the three. The number of tracking channels to be used is programmable; the unused tracking channels can be powered down.

A complete multi-OS software library is provided by ST to handle GPS processing, managing satellite acquisition, tracking, pseudo-range calculation and positioning, generating the output in the standard NMEA message format. The library includes support of ST Self-Trained Assisted GPS (ST-AGPS), a complete and scalable solution for assisting GPS start-up with autonomous and server-based ephemeris prediction and extension.

3.3 MCU subsystem

The implemented subsystem includes an AHB lite bus matrix.

An ARM946 core is embedded in the subsystem and masters the AHB bus. The totally available TCM SRAM is 256 KB. The amount of memory on ITCM and DTCM can be configured by the ARM946 (see *Table 11*). ITCM can be configured as 64 + Ni x 16 KB; DTCM can be configured as 64 + Nd x 16 KB, where Ni + Nd = 8, Ni ≥1.

Table 11. TCM configuration

TCMcfg[2]	TCMcfg[1]	TCMcfg[0]	ITCM	DTCM
0	0	0	80 KB	176 KB
0	0	1	96 KB	160 KB
0	1	0	112 KB	144 KB
0	1	1	128 KB	128 KB
1	0	0	144 KB	112 KB
1	0	1	160 KB	96 KB
1	1	0	176 KB	80 KB
1	1	1	190 KB	64 KB

3.3.1 AHB slaves

- G3 APB port that allows interfacing with the G3BB acquisition memory and control registers.
- 16 Kbytes ROM
- Vectored Interrupt Controller (VIC).
- FS USB OTG controller
- FSMC external memory interface with NOR FLASH support
- SQI Flash memory controller
- 2 x ARM946 APB peripheral bus (APB1, APB2).

Vectored Interrupt Controller (VIC)

This Vectored Interrupt Controller (VIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. There are up to 64 interrupt lines. The VIC uses a bit position for each different interrupt source.

The software can control each request line to generate software interrupts. Each interrupt line can be independently enabled and configured to trigger a non-vectored Normal Interrupt Request (IRQ) or Fast Interrupt Request (FIQ) to the ARM946 CPU. Sixteen interrupt lines can also be selected to trigger a vectored IRQ. The VIC has two operation modes: the user mode and the privilege mode, in order to have the possibility to set (or not) one level of protection during execution.

FS USB dual role controller

Full speed USB dual role with transceiver. It can work as an FS USB device if connected to a USB HOST or it can work as a USB HOST when connected to a USB device. It is an AHB slave. When active it requires a 48 MHz clock USB_CLK.

FSMC external memory interface

16-bit non-muxed memory interface for burst NOR Flash, SRAM and NAND.

SQI Flash interface

STA8088EX includes a high-performance interface to Serial Quad Interface (SQI) serial NOR Flash chips, to support a low-cost simple implementation. A proprietary code prefect and data write buffer architecture is provided to allow transparent read access to Serial NOR as if it was memory mapped fetchable code. The presence of L1 Instruction cache and the ability to allocate critical sections in zero-wait state TCMs minimize the access latency of this solution.

3.4 APB peripherals

3.4.1 CAN

The 2 CAN cores perform communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

CAN consists of the CAN core, message RAM, message handler, control registers and module. For communication on a CAN network, individual message objects are configured. The message objects and identifier masks for acceptance filtering of received messages are stored in the message RAM. All functions concerning the handling of messages are implemented in the message handler. These functions include acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the CAN can be accessed directly by the CPU through the module interface. These registers are used to control/configure the CAN core and the message handler and to access the message RAM.

CAN features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled automatic re-transmission mode for time triggered CAN applications
- Programmable loop-back mode for self-test operation
- 8-bit non-multiplex Motorola HC08 compatible module interface
- Two 16-bit module interfaces to the AMBA APB bus from ARM

3.4.2 EFT

The Extended Function Timer (EFT) consists of a 16-bit counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (input capture) or generation of up to two output waveforms (output compare and PWM). Pulse lengths and waveform periods can be modulated from a very wide range using the timer prescaler.

EFT features

- Programmable prescaler: fAPB divided from 1 to 256, prescaler register (0 to 255) value +1.
- Overflow status flag and maskable interrupts.
- Output compare functions with:
  - 2 dedicated 16-bit registers
  - 2 dedicated programmable signals
  - 2 dedicated status flags
  - 2 dedicated interrupt flags
- Input capture functions with:
  - 2 dedicated 16-bit registers
  - 2 dedicated active edge selection signals
  - 2 dedicated status flags
  - 2 dedicated interrupt flags
- Pulse Width Modulation mode (PWM).
- One Pulse Mode (OPM).
- PWM input mode.
- Timer global interrupt (5 internally ORed)
  - ICIA: timer input capture A interrupt
  - ICIB: timer input capture B interrupt
  - OCIA: timer output compare A interrupt
  - OCIB: timer output compare B interrupt
  - TOI: timer overflow interrupt

3.4.3 SSP

The SSP is a master or slave interface for synchronous serial communication with peripheral devices that have Motorola SPI, National Semiconductor MicroWire or Texas Instruments Synchronous Serial Interfaces.

The SSP performs serial-to-parallel conversion on data received from a peripheral device on SSPRXD pin, and parallel-to-serial conversion on data written by CPU for transmission on SSPTXD pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 32 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO.

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SSPCLK from the on-chip clock, SSPCLKI. One combined interrupt is delivered, which is asserted from several internal maskable events.

SSP features

In both master and slave configurations, the SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32 bits,
- Programmable clock bit rate and prescaler
- Programmable clock phase and polarity in SPI mode

3.4.4 UART

The UARTx (x = 0|1|2) performs serial-to-parallel conversion on data asynchronously received from a peripheral device on URXDx pin, and parallel-to-serial conversion on data written by CPU for transmission on UTXDx pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive.

UART Features

The UARTx (x = 0|1|2) are Universal Asynchronous Receiver/Transmitter that support much of the functionality of the industry-standard 16C650 UART. The main features are:

- Programmable baud rates up to UARTCLK / 16 (3.0 Mbps with UARTCLK at 48 MHz), or up to UARTCLK / 8 (6.0 Mbps with UARTCLK at 48 MHz), with fractional baud-rate generator
- 5, 6, 7 or 8 bits of data
- Even, odd, stick or no-parity bit generation and detection
- 1 or 2 stop bit generation
- Automatic extraction of UART setting for baud rate, character size (7 or 8-bit), parity configuration and number of stop bits
- Support of the modem control functions CTS, RTS (UART0 and UART1), plus DCD, DSR, RTS, DTS and RI (UART0 only)
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection
- Line break generation and detection
- Separate 8-bit wide, 64-deep transmit FIFO and 12-bit wide, 64-deep receive FIFO
- Programmable FIFO disabling for 1-byte depth data path

These UARTs vary from industry-standard 16C650 on some minor points which are:

- Receive FIFO trigger levels
- The internal register map address space, and the bit function of each register differ
- The deltas of the modem status signals are not available
- 1.5 stop bits is not supported
- Independent receive clock feature is not supported

3.4.5 I^2C

STA8088EX includes an I^2C interface configurable as master or slave.

3.4.6 SDMMC

STA8088EX features two SD/MMC interfaces. One 52 MHz/ 8-bit (iNand Interfaces) and one 26 MHz/ 4bit (SD card interface)

3.4.7 MTU

The Multi Timer Unit provides access to four interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs). The FRCs can have F0 as clock input, allowing the counters to run from a much slower clock than the system clock.

The FRC is the part of the timer that performs the counting. There are four instantiations of the FRC block in the MTU, allowing four counts to be performed in parallel. The 32-bit counter in the FRC is split up into two 16-bit counters.

3.4.8 WDT

The watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

3.4.9 GPIO

GPIO block provides up to sixty-four (63) programmable inputs or outputs. Each input or output can be controlled in two modes:

- Software mode through an APB bus interface
- Alternate mode, where GPIO becomes a peripheral input or output

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) triggers an interrupt.

3.4.10 ADC

10-bit SAR ADC operating at1.8 V analog supply. It can convert up to 8 single ended channels with analog input multiplexer at 500KSPS

3.4.11 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 8 Kbyte SRAM and supplied with a dedicated voltage regulator. The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features

- 48-bit counter clocked by 32768 kHz clock
- 32-bit for the integer part (seconds) and 16-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (16-bit)
- Load bit to transfer the content of the entire load register (integer + fractional part) to the 48-bit counter. Once set by the MCU this bits is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.4.12 MSP

The STA8088EX provides one MSP block.

- Phillips I^2S format: left aligned with one cycle between leading edge of frame
- Synchronization and first data bit, 16 or 24 bits per sample
- Sony format: right aligned, 48 cycles per frame, 16 or 24 bits per sample,
- Matsushita format: right aligned, 64 cycles per frame, 16 or 24 bits per sample,
- Programmable number of bit clock cycles per frame: 32, 48 and 64,
- Programmable polarity of bit clock and frame synchronization,
- Programmable number of bits per sample: 16, 18, 20 and 24 bits.

4 Electrical characteristics

4.1 Parameter conditions

Unless otherwise specified, all voltages are referred to GND.

4.2 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25°C and T_A = 85°C.

The 'limit values' data is explained and identified with a letter as listed below, and reported in the NOTE field of the following tables where applicable:

- <P>: data tested in production.
- <C>: data based on engineering characterization, not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).
- <V>: data based on design validation performed on three sample devices, not tested in production.
- <S>: data based on design guidelines and simulation, not tested in production.

4.3 Typical values

Unless otherwise specified, typical data are based on T_A = 25°C, V_{ddio} = 1.8 V, V_{dd} = 1.20 V. They are given only as design guidelines and are not tested.

4.4 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.5 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

Table 12 lists the absolute maximum rating for STA8088EX.

Table 12. Voltage characteristics

Symbol	Parameter	Limit values		Unit
		Min.	Max.	
V_{DD12_LPVR}	Power supply filter pins for the core logic and buffers of the always on section	V_{GND} - 0.3	V_{GND} + 1.32	V
V_{DDIO_r1}	Power supply pins for the IO buffers	V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r2}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r3}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r4}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DDIO_r5}		V_{GNDIO} - 0.3	V_{GNDIO} + 3.63	V
V_{DD12_MVR}	Power supply filtering pins for the core logic in the switchable section	V_{GND} - 0.3	V_{GND} + 1.32	V
V_{RF12_LNA}	Analog supply voltage for LNA.	V_{GND_LNA} - 0.3	V_{GND_LNA} + 1.32	V
V_{RF12_RFA}	Analog supply voltage for RFA.	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_MIX}	Analog supply voltage for mixer	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_IF}	Analog supply voltage for IF section	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_RFDIG}	Analog supply voltage for RF digital	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_RFVCO}	Analog supply voltage for VCO	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{RF12_RFADC}	Analog supply voltage for RF ADC	V_{GND_RF} - 0.3	V_{GND_RF} + 1.32	V
V_{DD18_MVR}	Main voltage regulator input supply	V_{GND} - 0.3	V_{GND} + 1.98	V
V_{DD_LPVR}	Low power voltage regulator input supply	V_{GND} - 0.3	V_{GND} + 3.60	V
V_{RF18_RFVR}	RF voltage regulator input supply	V_{GND_RF} - 0.3	V_{GND_RF} + 2.75	V
$V_{ESD\text{-}HBM}$	Electrostatic discharge, human body model	1000		V
$V_{ESD\text{-}CDM}$	Electrostatic discharge, charge device model	250(1)		V
		100(2)		

1. All pins except for ball K1,N4
2. For ball K1,N4

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 13. Thermal characteristics

Symbol	Parameter	Limit values		Unit
		Min.	Max.	
T_{oper}	Operative ambient temperature	-40	+85	°C
T_j	Operative junction temperature	-40	+125	°C

Table 13. Thermal characteristics (continued)

Symbol	Parameter	Limit values		Unit
		Min.	Max.	
T_{st}	Storage temperature	-55	150	°C
$R_{j\text{-}amb}$	Thermal resistance junction to ambient(1)		41	°C/W

1. According to JEDEC specification on a 2 layers board

Table 14. Frequency limits

Symbol	Parameter	Test condition	Limit values			Notes	Unit
			Min.	Typ.	Max.		
F_{CLK}	Operating ARM9 CPU frequency	V_{dd} = 1.2 V; T_C = 85 °C	—	—	208	V	MHz
F_{AHB}	AHB frequency		—	—	52	V	MHz

Table 15. Power consumption

Symbol	Parameter	Test condition	Limit values			Notes	Unit
			Min.	Typ.	Max.		
P_{RF}	RFIP power (total $V_{RF18RFVR}$)	GPS + GLONASS 25 °C $V_{RF18RFVR}$ = 1.8 V; LNA ON	—	51	TBD		mW
		GPS 25 °C $V_{RF18RFVR}$ = 1.8 V; LNA ON	—	32	TBD		mW
P_{MVR}	Switchable area power (total $V_{DD18MVR}$)	@52 MHz (no PLL, FSMC and UART active, other peripherals inactive) 25 °C $V_{DD18MVR}$ = 1.8 V	—	56	TBD		mW
P_{LPVR}	Always ON area power (total V_{DDLPVR})	@52 MHz, 25 °C V_{DDLPVR} = 1.8 V	—	2	TBD		mW
P_{IO}	IO rings power (total V_{DDIO_rx})	@52 MHz (FSMC and UART active, other peripherals inactive), 25 °C V_{DDIO_rx} = 3.3 V	—	17	TBD		mW
I_{DSLEEP}	STAND-BY mode supply current	RTC running @32.768 kHz, 25 °C V_{DDLPVR} = 1.8 V	—	60	TBD		µA

4.6 Recommended DC operating conditions

Table 16 lists the functional recommended operating DC parameters for STA8088EX.

Table 16. Recommended DC operating conditions

Symbol	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
V_{DDIO}(1)	1.8V I/O supply voltage	1.71	1.8	1.89	V
	3.3V I/O supply voltage	3.00	3.30	3.60	V
V_{DDIO_r5}	I/O supply voltage for ring 5	3.00	3.30	3.60	V
V_{DD18_MVR}	Main voltage regulator input supply	1.71	1.8	1.89	V
V_{RF18_RFVR}	RF voltage regulator input supply	1.71	1.8	1.89	V
V_{DD_LPVR}	Low power voltage regulator input supply	1.62		3.60	V
T_C	Operating case temperature	-40		85	°C

1. Applicable to V_{DDIO_r1}, V_{DDIO_r2}, V_{DDIO_r3}, V_{DDIO_r4}

4.7 DC characteristics

Table 17 specifies the low voltage detection thresholds

Table 17. Low voltage detection thresholds

Parameter		Min.	Typ.	Max.	Unit
Input LVD main VR	Upper voltage threshold	1.55	1.62	1.67	V
	Lower voltage threshold	1.50	1.57	1.62	V
	Hysteresis	40	51	56	mV
Output LVD Main VR	Upper voltage threshold	1.18(1)	-	1.21(1)	V
	Lower voltage threshold	1.05	1.11	1.15	V
Input LVD LowPower VR	Upper voltage threshold	1.55	1.59	1.67	V
	Lower voltage threshold	1.50	1.57	1.62	V
	Hysteresis	18	22	25	mV
Output LVD LowPower VR	Upper voltage threshold	1.18(1)	-	1.21(1)	V
	Lower voltage threshold	1.10(1)	-	1.13(1)	V

1. Parameter guaranteed by design.

Table 18 lists the DC characteristics for all the IO digital buffers expect for the following input buffers: STBYn (J6), STDBY_OUT (J5), WAKEUP (K7) and RSTn (K8).

Table 18. I/O buffers DC characteristics

Symbol	Parameter	Test condition	Limit values			Unit
			Min.	Typ.	Max.	
V_{IL}(1)	Logical input low level voltage	V_{ddio} = 1.8 V	-0.3		0.3 * V_{ddio}	V
		V_{ddio} = 3.3V	-0.3		0.8	V
V_{IH}(1)	Logical input high level voltage	V_{ddio} = 1.8 V	0.7 * V_{ddio}		V_{ddio} + 0.3	V
		V_{ddio} = 3.3V	2.0		V_{ddio} + 0.3	V
V_{HYST}(2)	Schmitt-trigger hysteresis	–	50			mV
V_{OL}	Low level output voltage	V_{ddio} = 1.8 V			0.4	V
		V_{ddio} = 3.3V			0.4	V
V_{OH}	High level output voltage	V_{ddio} = 1.8 V	V_{ddio} - 0.4			V
		V_{ddio} = 3.3V	V_{ddio} - 0.4			V

1. Excludes oscillator inputs RTC_XTI and XTAL_IN. Refer to oscillator electrical specifications.
2. Apply to all digital inputs unless specified otherwise.

Table 19 lists the DC characteristics for the 1.2V IO digital buffers input buffers: STBYn (J6), STDBY_OUT (J5), WAKEUP and RSTn (K8).

Table 19. 1.2V I/O buffers DC characteristics

Symbol	Parameter	Test condition	Limit values			Unit
			Min.	Typ.	Max.	
V_{IL}	Logical input low level voltage	V_{DD12_LPVR} = 1.2 V	-0.3	—	0.4 * V_{DD12_LPVR}	V
V_{IH}	Logical input high level voltage	V_{DD12_LPVR} = 1.2 V	0.7 * V_{ddio}	—	V_{DD12_LPVR} + 0.3	V
V_{OL}	Low level output voltage	V_{DD12_LPVR} = 1.2 V		—	0.2	V
V_{OH}	High level output voltage	V_{DD12_LPVR} = 1.2 V	V_{DD12_LPVR} - 0.2	—		V

4.8 AC characteristics

4.8.1 RF electrical specifications

Table 20. LNA

Symbol	Parameter	Note	Limit values			Unit
			Min.	Typ.	Max.	
S_{21}	Power gain		TBD	17	TBD	dB

Table 20. LNA (continued)

Symbol	Parameter	Note	Limit values			Unit
			Min.	Typ.	Max.	
NF	Noise Figure @ 25°C			1.3	TBD	dB
IP_{1dB}	Input compression point	In G3 band	TBD	-23		dBm

Table 21. RFA – MIXER G3 – GALGPS FILTER & VGA

Symbol	Parameter	Note	Limit values			Unit
			Min.	Typ.	Max.	
RFA_{GV}	RFA voltage gain	Max gain (not testable)		20		dB
		Min gain (not testable)		10		dB
		Delta gain		10		dB
f_{IF}	IF frequency			4.092		MHz
NF	RF-IF-VGA noise figure	For max gain		4.5(1)		dB
G_C	Conversion gain (from RFAin to ADC input)	VGA and RFA at max gain	TBD	100	TBD	dB
		VGA and RFA at min gain	TBD	50	TBD	
VGA	VGA dynamic range		TBD	50	TBD	dB
IP_{1dB}	RF-IF-VGA input compression point	In G3 band RFA max VGA min	TBD	-65		dBm
IRR	Image rejection ratio		TBD	20		dB
BW_{GPS}	-3dB IF bandwidth	GPS mode	TBD	2.4		MHz
BW_{GAL}		Galileo mode	TBD	4.8		MHz
ATT	Alias frequency rejection	F=12 MHz		20		dB
		F = 28 MHz (Galileo)	20			dB
T_{gGPS}	IF filter group delay variation	GPS mode, fc ±1023 kHz			200(1)	ns
T_{gGAL}		Galileo mode, fc ±2046 kHz			60(1)	ns

1. Parameter guaranteed by design.

Table 22. RFA – MIXER G3 – GLONASS FILTER & VGA

Symbol	Parameter	Note	Limit values			Unit
			Min.	Typ.	Max.	
RFA_{GV}	RFA voltage gain	Max gain (not testable)		20		dB
		Min gain (not testable)		10		dB
		Delta gain		10		dB
f_{IFGNS}	IF frequency			8.5		MHz

Table 22. RFA – MIXER G3 – GLONASS FILTER & VGA (continued)

Symbol	Parameter	Note	Limit values			Unit
			Min.	Typ.	Max.	
NF	RF-IF-VGA noise figure	For max gain		5(1)		dB
G_C	Conversion gain (from RFAin to ADC input)	VGA and RFA at max gain	TBD	95	TBD	dB
		VGA and RFA at min gain	TBD	45	TBD	
VGA	VGA dynamic range		TBD	50	TBD	dB
IP_{1dB}	RF-IF-VGA input compression point	In G3 band RFA max VGA min	TBD	-69		dBm
IRR	Image rejection ratio			20		dB
$BW_{GLONASS}$	-1dB IF bandwidth			10		MHz
ATT	Alias frequency rejection	F = 24 MHz		20		dB
T_{gGPS}	IF filter group delay variation	fc ± 4000 kHz			20(1)	ns

1. Parameter guaranteed by design.

Table 23. Synthesizer

Symbol	Parameter	Note	Limit values			Unit
			Min.	Typ.	Max.	
F_{TCXO_XTAL}	Input frequency for xtal amplifier	That amplifier can be used also like TCXO input buffer	10		52	MHz
R_{DIV}	Reference divider range		1		63	
N_{DIV}	Loop divider range		56		2047	
F_{LO}	LO operating frequency			3142.656		MHz

4.8.2 Oscillator electrical specifications

This device contains two oscillators:

- a 32.768 kHz oscillator/buffer for RTC circuit.
- a 26 MHz oscillator/buffer in the RF Front-End

When used in oscillator mode, each oscillator requires a specific crystal, with parameters that must be as close as possible to the following recommended values. When used in input buffer mode, an external clock source must be applied.

32.768 kHz OSCI32 oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 27pF, as shown on *Figure 2*.

OSCI32 is power supplied by an internal dedicated DC regulators (DCREG_OSCI) that outputs a regulated 1.4V (+/- 100mV) from the unregulated VDD_LPVR input. DCREG_OSCI is enabled by default and it can be powered down by setting bit20-DCREG_OSCI_PD of CLK_CTRL_BCK_REG0.

OSCI32 is disabled by default and must be enabled by setting bit21-OSCI_EN of CLK_CTRL_BCK_REG0 to have 32.768KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The recommended oscillator specifications are shown in *Table 24*:

Table 24. Crystal recommended specifications

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
F_{SXTAL}	Crystal frequency(1)	—	32.768	—	kHz
LM_{SXTAL}	Motion inductance(1)	—	11.8	—	kH
CM_{SXTAL}	Motional capacitance(1)	—	2.0	—	fF
RM_{SXTAL}	Motional resistance(1)	—	60	—	kΩ
CO_{SXTAL}	Shunt capacitance(1)	—	1.5	—	pF
CL_{SXTAL}	Load capacitance(1)	—	27	—	pF

1. Parameter guaranteed by design.

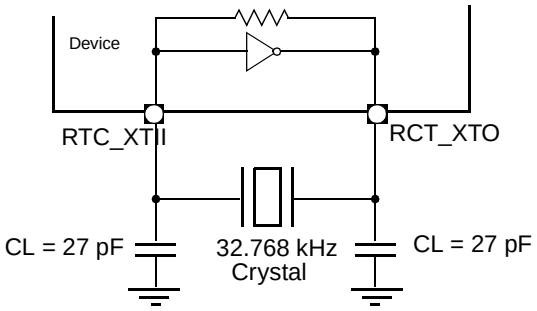
The oscillator amplifier specifications are shown in following table:

Table 25. Oscillator amplifier specifications

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
$V_{ILOSCI32}$	Low level input voltage(1)	—	—	0.3	V
$V_{IHOSCI32}$	High level input voltage(1)	1.04	—	—	V
V_{HYSTO}	Input hysteresis(1)	35	—	—	mV
T_S	Startup time(1)	0.5	15 x L_m/R_m	5	s
T_{RISE}	Rise time(2)	0.6	—	—	ns
T_{FALL}	Fall time(2)	0.6	—	—	ns
GM	Transconductance(3)	10	—	—	µA/V

1. Parameter guaranteed by design.
2. Oscillator in bypass mode.
3. The transconductance GM should be 3 times the transconductance calculated with the following formula, in worst case:
$GM_{min} = RM \cdot \omega^2 \cdot (CL + 2\ CO)^2$
where the CL and CO are the Load Capacitance and Shunt Capacitance of the actual crystal and ω is 2π by the oscillation frequency.

Figure 2. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit21-OSCI_EN = 0b in CLK_CTRL_BCK_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum. This also allows to drive RTC_XTI input even when a crystal is connected between RTC_XTI and RTC_XTO pins.
- Drive the RTC_XTI pin with a square signal that has low level $V_{ILOSCI32}$ and a high level $V_{IHOSCI32}$, or a sine wave (maximum amplitude: $V_{IHOSCI32}$ / 2, offset: $V_{IHOSCI32}$ / 2).

Table 26. Characteristics of external slow clock input

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
T_{JIT} (cc)	Cycle-to-cycle jitter	-70	—	70	ps
T_{JIT} (per)	Period jitter	-70	—	70	ps
	Variation	-500	—	500	ppm
T_{DUTY}	Duty cycle	45	—	55	%

4.8.3 26 MHz oscillator specifications

Refer to RF Front-End section for details.

4.8.4 System PLL specifications

This section gives the AC specification of System PLL embedded in STA8088EX device. As depicted in *Figure 3*, it receives, from the G3RF Front End, a buffered version of the external 26MHz clock source and generates a 624MHz clock used as clock reference for the clock generation block. Analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins. The SYSPLL is managed by the ARM MCU through APB Bridge 1.

Figure 3. System PLL block diagram

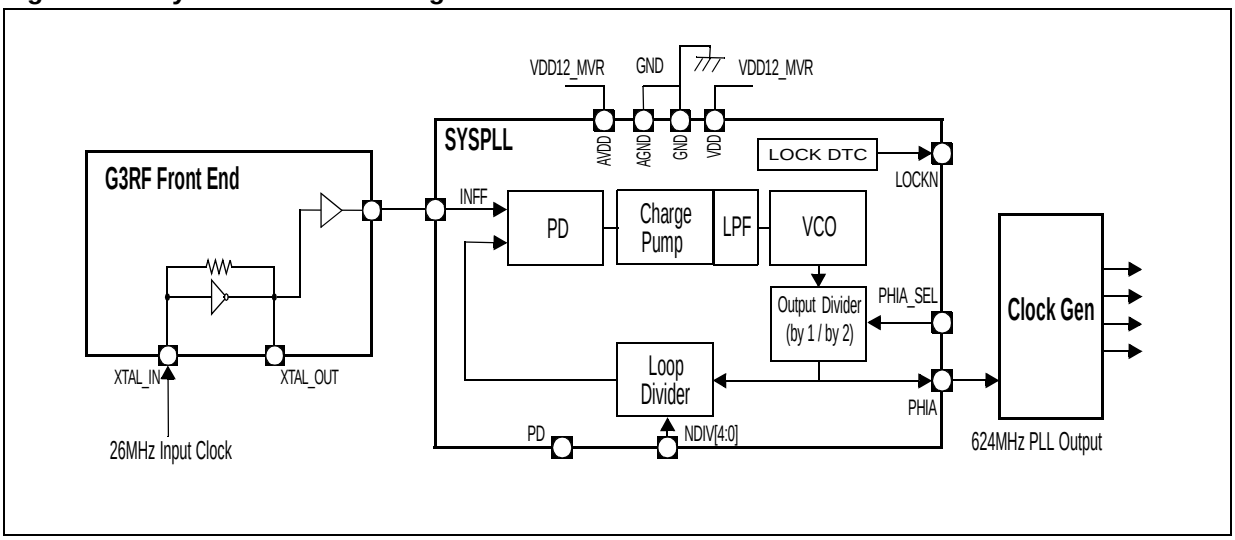


Table 27. SYSPLL specifications

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
F_{IN_RANGE}	INFF input clock frequency range(1)	4	—	65	MHz
δ_{INFF}	INFF input clock duty cycle(1)	40	—	60	%
$T_{R/F}$	INFF input clock rise/fall time(1)	—	—	0.1	ns
F_{VCO}	VCO frequency range(1)	240	—	650	MHz
F_{PLL}	PLL output PHIA frequency range(1)	120	—	650	MHz
T_{LOCK}	Lock time(1)	—	—	100	µs

1. Parameter guaranteed by design.

4.8.5 ADC specifications

This section gives the AC specification of the 10 bit Successive Approximation Register ADC embedded in STA8088EX device. It is controlled by the ARM9 MCU through a wrapper and an APB bridge as depicted in *Figure 4* and it has a maximum conversion rate of 1MSPS with 8 muxed analog input channels capability. An internal voltage reference is used and analog/digital power supplies connections are implemented inside the device without any needs of dedicated external pins.

Figure 4. SARADC connections

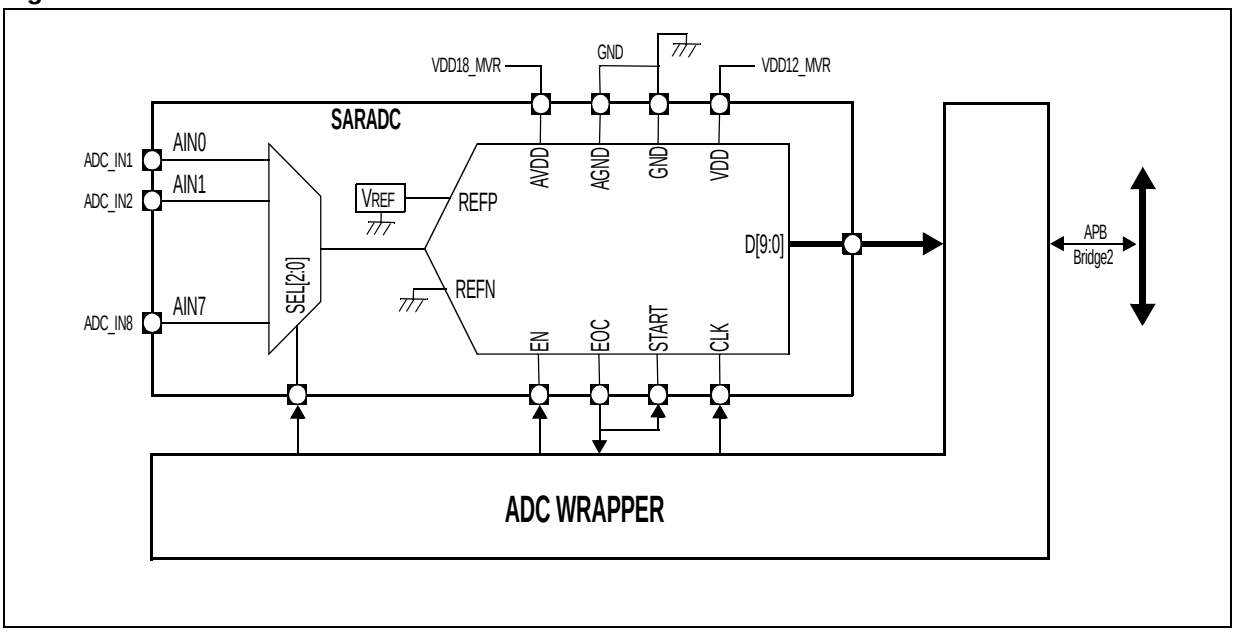


Table 28. SARADC specifications

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
V_{ADCIN}	ADC_IN input range(1)	V_{GND}-0.3	—	V_{DD18_MVR}+0.3	V
V_{ADCCR}	Conversion range(1)	V_{GND}	—	V_{REF}	V
V_{REF}	Voltage reference(1)	1.35	1.4	1.45	V
C_{IN}	Input capacitance(1)	5.5	7.0	8.5	pF
R_{IN}	Input mux resistance (total equivalent sampling resistance)(1)(2)	1.5	2.0	2.5	kΩ
F_{CLK}	Clock frequency(1)	2.5		15	MHz
δ_{CLK}	Clock duty cycle(1)	45	50	55	%
T_{SUP}	Start up time(1)(3)	—	—	20	µs
T_C	Conversion time(1)	—	14		cycles
T_S	Sampling time(1)	—	3		cycles
INL	Performance			< +/- 2	LSB
DNL				< +/- 2	LSB

1. Parameter guaranteed by design.
2. Pad input capacitance included.
3. From EN=1.

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 TFBGA169 9 x 9 mm package information

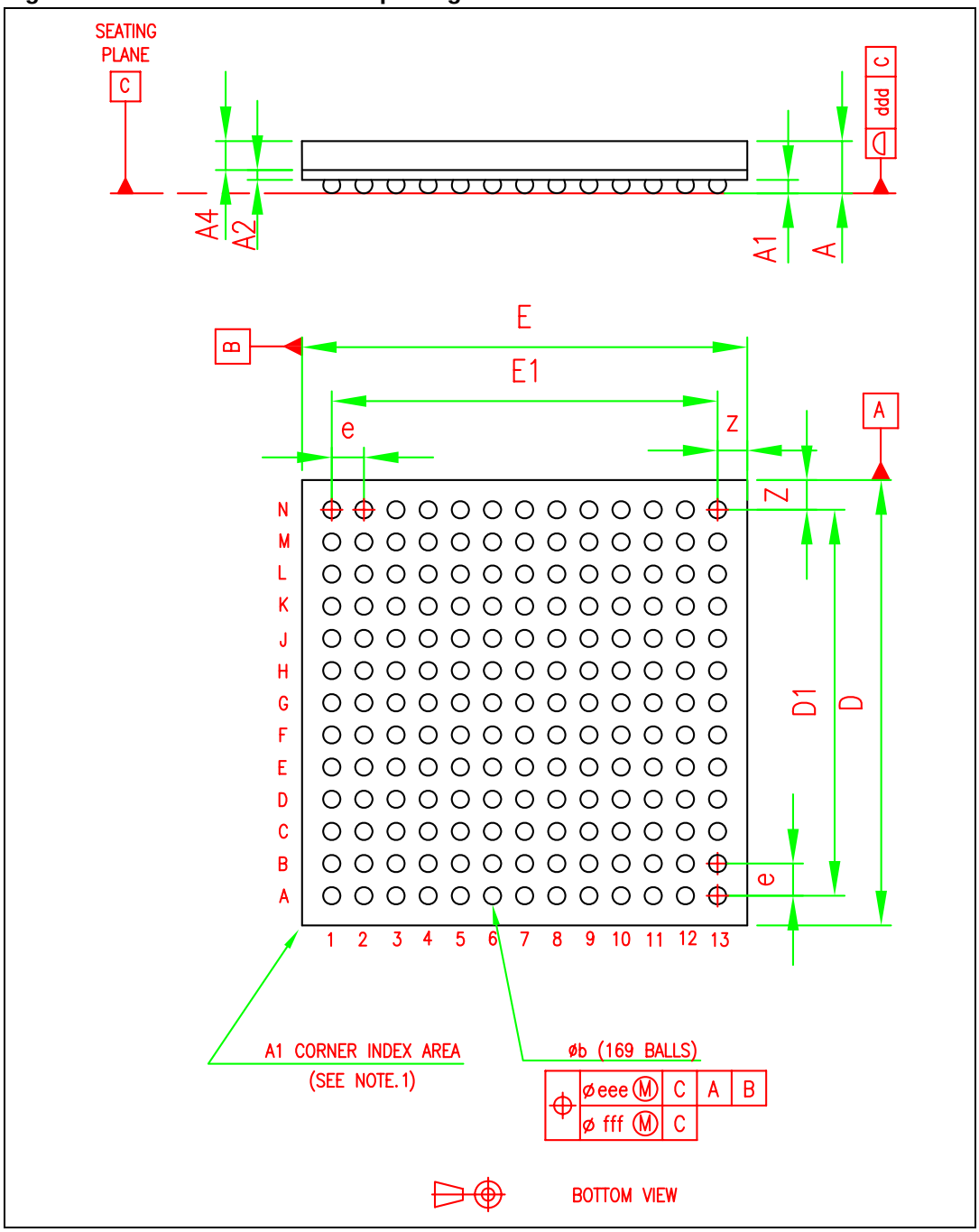
Table 29. TFBGA169 9 x 9 mm mechanical data

Ref. dim	Data book (mm)			Drawing (mm)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A(1)			1.20			1.07
A1(2)	0.21			0.22	0.27	0.32
A2		0.20		0.16	0.20	0.24
A4		0.585		0.57	0.585	0.60
b(3)	0.30	0.35	0.40	0.30	0.35	0.40
D	8.85	9.00	9.15	8.90	9.00	9.10
D1		7.80			7.80	
E	9.85	9.00	9.15	8.90	9.00	9.10
E1		7.80			7.80	
e		0.65			0.65	
Z		0.60			0.60	
ddd			0.08			0.08
eee(4)			0.15			0.15
fff(5)			0.05			0.05

1. TFBGA stands for Thin profile Fine Pitch Ball Grid Array.
   - The total profile height (Dim A) is measured from the seating plane to the top of the component
   - The maximum total package height is calculated by the following methodology:
   A Max = A1 Typ + A2 Typ + A4 Typ + $\sqrt{(A1^2 + A2^2 + A4^2}$ tolerance values)
   - Thin profile: 1.00 mm < A ≤ 1.20 mm / Fine pitch: e < 1.00 mm pitch.
2. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
   - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
3. The typical ball diameter before mounting is 0.35 mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

5. The tolerance of position that controls the location of the balls within the matrix with respect to each other.For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 5. TFBGA169 9 x 9 mm package dimension



1. - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
   - A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

6 Revision history

Table 30. Document revision history

Date	Revision	Changes
04-Jan-2010	1	Initial release.
25-Oct-2011	2	Updated *Features* list Updated following tables: – *Table 1: Device summary* – *Table 2: TFBGA169 ball out* – *Table 4: Main function pins* – *Table 8: Port 0 pins*: P0.0 – *Table 9: Port 1 pins*: P1.23 Updated following sections: – *Section 3.3.1: AHB slaves* – *Section 3.4.2: EFT* – *Section 3.4.3: SSP* – *Section 3.4.6: SDMMC* – *Section 3.4.7: MTU* – *Section 3.4.9: GPIO* Updated *Chapter 4: Electrical characteristics* Added *Section 5.3: TFBGA169 12 x 12 mm package information*
01-Dec-2011	3	Updated *Features* list Updated *Table 1: Device summary* Removed *Section 5.3: TFBGA169 12 x 12 mm package information*

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