VS6552

VGA Color CMOS Image Sensor Module

FEATURES

- Small physical size
- Ultra low power standby mode
- SmOP (Small Optical Package) technology featuring integrated lens
- Class leading low light performance
- VGA resolution sensor
- Compatible with STV0974 companion mobile processor
- High frame rate to minimize image distortion
- Low EMI link (VisionLink) to STV0974
- On-chip 10-bit ADC
- Automatic dark calibration
- I²C communications
- On-chip PLL

VS6552 offers an ultra low power standby mode that consumes less than 15 µW.
The SmOP lens has been designed to combine class leading low light performance with good depth of field to ensure excellent overall optical performance. The lens is a 2 element moulded plastic design.
The output data and qualification clock are transmitted over low noise, low voltage and fully differential links. VS6552 configuration registers are controlled via a private I²C interface to STV0974.

APPLICATIONS

- Mobile phone embedded camera system
- PDA embedded camera or accessory camera
- Wireless security camera

Table 1. Technical Specifications

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<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel resolution</td>
<td>644 x 484 (VGA)</td>
</tr>
<tr>
<td>Pixel size</td>
<td>5.6 µm x 5.6 µm</td>
</tr>
<tr>
<td>Exposure control</td>
<td>+81 dB</td>
</tr>
<tr>
<td>Analog gain</td>
<td>+24 dB (max)</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>60 dB (Typical)</td>
</tr>
<tr>
<td>Signal to noise at 50cd.m²</td>
<td>37 dB (Typical)</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>2.8 V (analog supply) 1.8 V (digital supply)</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;75 mW (@30 frame/s) 15 µW (standby mode)</td>
</tr>
<tr>
<td>Package size</td>
<td>10.7mm x 8.7mm x 6mm:SmOP1.5 9.5mm x 8.5mm x 6.1mm :SmOP2</td>
</tr>
<tr>
<td>Lens</td>
<td>45° HFOV, f# 2.8</td>
</tr>
<tr>
<td>Package type</td>
<td>14 pad SmOP</td>
</tr>
<tr>
<td>System attach</td>
<td>Socket or flexible circuit</td>
</tr>
</tbody>
</table>
Table 2. Order Codes

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Operating Temperature</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>VS6552V015/T2</td>
<td>[ -25; +55 ] °C</td>
<td>SmOP1.5</td>
</tr>
<tr>
<td>VS6552V02C/T2</td>
<td>[ -25; +55 ] °C</td>
<td>SmOP2M</td>
</tr>
<tr>
<td>VS6552V02D/T2</td>
<td>[ -25; +55 ] °C</td>
<td>SmOP2ME</td>
</tr>
</tbody>
</table>
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<td>13</td>
</tr>
<tr>
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1 OVERVIEW

1.1 Sensor Overview
The VS6552 VGA image sensor produces raw VGA digital video data at up to 30 frames per second. The image data is digitized using an internal 10-bit column ADC. The resulting 10-bit output data includes embedded codes for synchronization. The data is formatted and transmitted over a fully differential link. The data is accompanied by a qualifying clock that is transmitted over an identical fully differential link.
The sensor is fully configurable using an I²C interface.
The sensor is optimized for high volume mobile applications.

1.1.1 Typical Application - Mobile Application

The VS6552 is an image sensor, it should be used in conjunction with the STMicroelectronics STV0974 companion processor. The coprocessor and the sensor together form a complete imaging system.
The sensor’s main function is to convert the viewed scene into a data stream. The companion processor function is to manage the sensor so that it can produce the best possible data and to process the data stream into a form which is easily handled by upstream mobile baseband or MMP chipsets. The sensor supplies high speed clock signal to the processor and provides the embedded control sequences which allow the coprocessor to synchronize with the frame and line level timings. The processor then performs the color processing on the raw image data from the sensor before supplying the final image data to the host.

Figure 1. Camera System Using STV0974
## 2 SIGNAL DESCRIPTION

### Table 3. Signal Description

<table>
<thead>
<tr>
<th>Pad Number</th>
<th>Pad Name</th>
<th>I/O Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power supplies</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CEXT</td>
<td>PWR</td>
<td>Connection to capacitor&lt;br&gt;^a</td>
</tr>
<tr>
<td>2</td>
<td>AGND</td>
<td>PWR</td>
<td>Analog ground</td>
</tr>
<tr>
<td>3</td>
<td>AVDD</td>
<td>PWR</td>
<td>Analog power</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>PWR</td>
<td>Digital ground</td>
</tr>
<tr>
<td>11</td>
<td>VDD</td>
<td>PWR</td>
<td>Digital power</td>
</tr>
<tr>
<td><strong>System</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PDN</td>
<td>I</td>
<td>Power down control&lt;br&gt;^b</td>
</tr>
<tr>
<td>5</td>
<td>CLK</td>
<td>I</td>
<td>System clock input</td>
</tr>
<tr>
<td><strong>Control</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>MSCL</td>
<td>I</td>
<td>Serial communication clock</td>
</tr>
<tr>
<td>7</td>
<td>MSDA</td>
<td>I/O</td>
<td>Serial communication data</td>
</tr>
<tr>
<td><strong>Data</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>PCLKN</td>
<td>vLVDS output</td>
<td>Output qualifying clock</td>
</tr>
<tr>
<td>10</td>
<td>PCLKP</td>
<td>vLVDS output</td>
<td>Output qualifying clock</td>
</tr>
<tr>
<td>12</td>
<td>PDATAN</td>
<td>vLVDS output</td>
<td>Serial output data</td>
</tr>
<tr>
<td>13</td>
<td>PDATAP</td>
<td>vLVDS output</td>
<td>Serial output data</td>
</tr>
<tr>
<td><strong>Not connected</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Not connected</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>Not connected</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

^a. Internally generated voltage that needs to be externally decoupled with a 100 nF, 5 V capacitor
^b. Signal is active low

**Note:** The physical position of the signals on the package can be found by referring to the pinout information in Chapter 7: Package Mechanical Data.
3 FUNCTIONAL DESCRIPTION

The first sections of this chapter detail the main blocks in the device:

- Analog video block
- Digital video block

The later sections of this chapter describe other functional aspects of the device. Device level operating modes, including suspend, are detailed.

3.1 Analog Video Block

3.1.1 Features

- ADC: 10-bit A/D converter - SRAM readout
- Dynamic range 60 dB (typical)
- SNR 37 dB @ 50 cd.m\(^2\) (typical)

3.2 Digital Video Block

3.2.1 Features

- Frame rate: 30 frame/s max. (VGA) can be reduced down to less than 3 frame/s (VGA)
- Automatic dark calibration to ensure consistent video level over varying scenes

3.2.2 Dark Calibration Algorithm

VS6552 runs a dark calibration algorithm on the raw image data to control the video offsets caused by dark current. This ensures that a high quality image is output over a range of operating conditions. First frame dark level is correctly calibrated, for subsequent frames the adjustment of the dark level is damped by a leaky integrator function to avoid possible frame to frame flicker.
3.2.3 Image Statistics

VS6552 generates image statistics which can be used by STV0974 as an input to an auto exposure controller (AEC), automatic gain controller (AGC) and automatic white balance (AWB).

3.3 Device Operating Modes

3.3.1 Standby

This is the lowest power consumption mode. I^2C communications to STV0974 are not supported in this mode. The clock input pad, PLL and the video blocks are powered down.

3.3.2 Sleep Mode

Sleep mode preserves the contents of the I^2C register map. I^2C communications to STV0974 are supported in this mode. The sleep mode is selected via a serial interface command sent by STV0974. The data pads go high at the end of the current frame. At this point the video block and PLL power down. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers like exposure and gain are preserved. The system clock must remain active to allow communication with the sensor.

3.3.3 Clock Active Mode

This mode is similar to ‘sleep mode’ except that the PLL is now powered up to permit a PCLKP/PCLKN signal to be delivered to STV0974. The PDATAP/PDATAN pads remain inactive. The video block is powered down.

3.3.4 Idle Mode

VCAP is generated. The analog video block is now powered up but the array is held in reset and the output PDATAP/PDATAN pads remain high.

3.3.5 Video

The VS6552 streams live video to the STV0974.

Table 4. VS6552 Power-up Sequence

<table>
<thead>
<tr>
<th>Mode</th>
<th>Design block powered down</th>
<th>Video data inhibit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>I^2C</td>
<td>Digital</td>
</tr>
<tr>
<td>Standby (PDN low)</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Sleep</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Clock active</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Idle</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Video</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

^a.PLL (Phase Locked Loop) generates fast system clock for STV0974
^b.PLL, PCLKP and PCLKN pins

3.4 Power Management

VS6552 requires a dual power supply. The analog circuits are powered by a nominal 2.8 V supply while the digital logic and digital I/O are powered by a nominal 1.8 V supply.

3.4.1 Power-up, Power-down Procedures

The power up and power down procedures are detailed in the following Figure 3.
3.4.2 Active Signals with Unpowered VS6552
All signals going into the VS6552 must be either at a low state or high impedance when power is removed from the device. The exceptions to this rule are the I2C lines which may be at a low or high state and the clock which can be active.

3.5 Clock and Frame Rate Timing

3.5.1 Video Frame Rate Control
The output frame rate of VS6552 can be reduced by extending the frame length. The extension is achieved by adding 'blank' video lines to act as timing padding. This is advantageous as it does not reduce the pixel readout rate and therefore does not introduce unwanted motion distribution effects to the image. The frame rate can be reduced from the default 30 frame/s at VGA resolution to less than 3 frame/s at VGA resolution.

3.5.2 PLL and Clock Input
A PLL IP block is embedded. This block generates all necessary internal clocks from an input range defined in Table 5. The input clock pad accepts up to 26 MHz signals.

Table 5. System Input Clock Frequency Range

<table>
<thead>
<tr>
<th>System clock frequency⁴</th>
<th>Min. (MHz)</th>
<th>Max. (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.5</td>
<td>26</td>
<td></td>
</tr>
</tbody>
</table>

³The standard supported input frequencies (in MHz) are as follows: 6.5, 8.4, 9, 9.6, 9.72, 12, 13, 16.8, 18, 19.2, 19.44, 26.

3.5.3 Clock Input Type
VS6552 can receive the following clock types:
- Single ended CMOS
- Single ended Sine wave
- Clock can be AC or DC coupled
The clock is fail-safe.
3.6 Control and Video Interface Formats

3.6.1 Overview
Data is transferred from VS6552 to STV0974 via a high speed serial link (VisionLink). The serial data link comprises of two pairs of wires. The serial control data is transferred between the VS6552 to STV0974 via a private I2C bus.

3.6.2 VisionLink Physical Layer
Data signals (PDATAP and PDATAN) and clock signals (PCLKP and PCLKN) are transferred from VS6552 to STV0974 via 2 pairs of balanced 100 Ω impedance transmission lines. The transmission line pairs and custom transmitters/receivers realize a very low voltage differential (vLVDS) signalling scheme that can transfer information in a potentially noisy environment. As implemented in VS6552, VisionLink supports the transmission of raw Bayer data at VGA resolution up to 30 frame/s.

3.6.3 Serial I2C Control Bus
The internal registers in VS6552 can be configured by STV0974 via a private I2C bus. STV0974 is the bus master and VS6552 is the single slave. VS6552 sends and receives commands over this bus at up to 400 kHz.

4 ELECTRICAL CHARACTERISTICS

Table 6. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDIG</td>
<td>Digital power supply</td>
<td>-0.5 to 3.0</td>
<td>V</td>
</tr>
<tr>
<td>VANA</td>
<td>Analog power supply</td>
<td>-0.5 to 3.6</td>
<td>V</td>
</tr>
<tr>
<td>MSCL,</td>
<td>CCI Signals</td>
<td>-0.3 to VDIG + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>MSDA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PDN,</td>
<td>Power Down Control, System Clock Input</td>
<td>-0.3 to VDIG + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>CLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSTO</td>
<td>Storage temperature</td>
<td>-40 to + 85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: Caution: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Digital power supply voltage</td>
<td>1.7</td>
<td>-</td>
<td>1.9</td>
<td>V</td>
</tr>
<tr>
<td>AVDD</td>
<td>Analog power supply voltage</td>
<td>2.5</td>
<td>-</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>TAF</td>
<td>Temperature (functional operating)</td>
<td>-30</td>
<td>-</td>
<td>+70</td>
<td>°C</td>
</tr>
<tr>
<td>TAN</td>
<td>Temperature (normal operating)</td>
<td>-25</td>
<td>-</td>
<td>+55</td>
<td>°C</td>
</tr>
<tr>
<td>TAO</td>
<td>Temperature (optimal operating)</td>
<td>+5</td>
<td>-</td>
<td>+30</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: 1. Storage temperature: Camera has no permanent degradation
2. Functional operating temperature: Camera is electrically functional
3. Normal operating temperature: Camera produces ‘acceptable’ images
4. Optimum performance temperature: Camera produces optimal optical performance
4.1 DC Electrical Characteristics

Note: Typical values quoted for nominal voltage and temperature. Maximum values quoted for worse case operating conditions unless otherwise specified.

Table 8. Power Supply VDIG, VANA

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Digital</td>
<td>Analogue</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Standby</td>
<td>1</td>
<td>5</td>
<td>N/A</td>
<td>&lt;2</td>
<td>µA</td>
</tr>
<tr>
<td>Video, 30fps</td>
<td>15</td>
<td>20</td>
<td>9</td>
<td>15</td>
<td>mA</td>
</tr>
</tbody>
</table>

a. Not Measurable - current is below the minimum calibrated measurement capabilities of the test system (1 µA)

Table 9. System Clock

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Leakage current</td>
<td>g</td>
<td>2g</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

a. With DC coupled square wave clock
b. With DC 1V9 signal level applied

c. Not applicable - current is below the minimum calibrated measurement capabilities of the test system (1 µA)

d. For external clock frequencies <19.2MHz, the maximum frequency is 200kHz

Table 10. I2C Interface - MSDA, MSCL

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Low level input voltage</td>
<td>-</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>High level input voltage</td>
<td>0.7</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Low level output voltage</td>
<td>-</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Low level input current</td>
<td>-</td>
<td>-10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>IH</td>
<td>High level input current</td>
<td>-</td>
<td>10</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>f</td>
<td>Operating frequency range</td>
<td>0</td>
<td>400</td>
<td>kHz</td>
<td></td>
</tr>
</tbody>
</table>

a. For positive electrostatic discharges above 500 V, a shift of VIH may happen. However, the device remains fully functional even for a stress up to 2000 V included, and VIH<0.9 VDIG. Refer to the STV0974 datasheet for recommendations on MSCL/MSDA usage.
b. VOH not valid for CCI
c. 1 mA drive strength
d. For external clock frequencies <19.2MHz, the maximum frequency is 200kHz

4.2 AC Electrical Characteristics

Table 11. System Clock

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCL</td>
<td>DC coupled square wave (low level)</td>
<td>-</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VCH</td>
<td>DC coupled square wave (high level)</td>
<td>0.7</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCAC</td>
<td>AC coupled sine wave</td>
<td>0.5</td>
<td>1.0</td>
<td>1.2</td>
<td>V</td>
</tr>
</tbody>
</table>
Table 12. Timing Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fCLK</td>
<td>Clock frequency input(^a)</td>
<td>6.5 - 1(^%)(^a)</td>
<td>-</td>
<td>26 + 1(^%)(^b)</td>
<td>MHz</td>
</tr>
</tbody>
</table>

\(^a\)Nominal frequencies are 6.5 to 26MHz with a 1\(^%\) center frequency tolerance

\(^b\)The VS6552 maximum I2C frequency of 400 kHz is only valid for external clock frequencies at or above 19.2 MHz. Due to a design issue, for external clock frequencies below 19.2MHz, the maximum guaranteed I2C frequency is limited to 200 kHz.

Figure 4. CCI AC characteristics

Note: The VS6552 maximum I2C frequency of 400 kHz is only valid for external clock frequencies at or above 19.2 MHz. Due to a design issue, for external clock frequencies below 19.2MHz, the maximum guaranteed I2C frequency is limited to 200 kHz.
Table 13. vLVDS Interface AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{od}$</td>
<td>Differential voltage swing$^{a,b}$</td>
<td>100</td>
<td>150</td>
<td>200</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{cm}$</td>
<td>Common mode voltage (self biasing)</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>$R_O$</td>
<td>Output Impedance</td>
<td>40</td>
<td></td>
<td>140</td>
<td>W</td>
</tr>
<tr>
<td>$I_{DR}$</td>
<td>Drive current range (internally set by bias circuit)</td>
<td>0.5</td>
<td>1.5</td>
<td>2</td>
<td>mA</td>
</tr>
</tbody>
</table>

$a$: Supplies of $VDIG = 1.8$ V and $VANA = 2.8$ V, Temperature = 25 °C  
$b$: Measured over a 100 Ohm load

Table 14. vLVDS Timing Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{PCLKP/PCLKN}$</td>
<td>PCLKP/PCLKN clock frequency</td>
<td>-</td>
<td>-</td>
<td>120</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PCLKP/PCLKN}$</td>
<td>PCLKP/PCLKN clock period</td>
<td>8.3</td>
<td>-</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{LOW}$</td>
<td>Low period of PCLKP/PCLKN</td>
<td>1.66</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{HIGH}$</td>
<td>High period of PCLKP/PCLKN</td>
<td>1.66</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{RISE}$</td>
<td>Rise time of PDATAP/PDATAN, PCLKP/PCLKN</td>
<td>0.3</td>
<td>-</td>
<td>0.5</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{FALL}$</td>
<td>Fall time of PDATAP/PDATAN, PCLKP/PCLKN</td>
<td>0.3</td>
<td>-</td>
<td>0.5</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{HD;DAT}$</td>
<td>Data hold time</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>$I_{SU;DAT}$</td>
<td>Data set-up time</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

Figure 5. VisionLink AC timing
4.3 ESD Handling Characteristics

Table 15. ESD Handling Limits

<table>
<thead>
<tr>
<th>Test</th>
<th>Method</th>
<th>Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Human Body Model</td>
<td>JESD22 A114A</td>
<td>2kV</td>
</tr>
<tr>
<td>ESD Machine Model</td>
<td>JESD22 A115A</td>
<td>200V</td>
</tr>
<tr>
<td>Latch Up</td>
<td>JESD78</td>
<td>1.5 * Vddmax, 150mA</td>
</tr>
</tbody>
</table>

5 OPTICAL SPECIFICATION

The small amount of lens relative illumination effects (field darkening) is corrected by the STV0974.

Table 16. Optical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective Focal Length</td>
<td>4 mm ± 0.15 mm</td>
</tr>
<tr>
<td>Aperture</td>
<td>F2.8 aperture</td>
</tr>
<tr>
<td>Horizontal Field of View</td>
<td>45° ± 2°</td>
</tr>
<tr>
<td>TV Distortion (pin, cushion &amp; barrel)</td>
<td>-3% to 3%</td>
</tr>
<tr>
<td>MTF (Figure 6)</td>
<td>On axis: 45 %</td>
</tr>
<tr>
<td></td>
<td>Horizontal field: 30%</td>
</tr>
<tr>
<td></td>
<td>Diagonal field: 30%</td>
</tr>
</tbody>
</table>

Figure 6. MTF Points on the Image Field

6 DEFECT CATEGORIZATION

6.1 Pixel Defects

A packaged CMOS image sensor will display visual imperfections caused either by electrical faults or optical blemishes which can be introduced in the product at various stages of the manufacturing process. These impurities can result in pixel defects, that is a pixel whose output is not consistent with the level of incident light falling on the image sensor. The ability to identify and correct these defects is central to both the design requirements and quality certification, via test of STMicroelectronics sensor products.

The STMicroelectronics STV0974 co-processor implements defect correction algorithms which screens the presence of these defects in the final images. The defect correction algorithms ensure that the VS6552 sensor in conjunction with the STV0974 co-processor will produce a high quality final image.

7 PACKAGE MECHANICAL DATA

7.1 SmOP1.5 Module Outline

– Figure 7
– Figure 8
– Figure 9

7.2 SmOP2 M Module Outline

– Figure 10
– Figure 11
– Figure 12

7.3 SmOP2 ME Module Outline

– Figure 13
– Figure 14
– Figure 15
Notes:
1. Mass of module 0.50 grammes
2. Volume of Module 278 mm^3
3. Maximum draft angle on all moulded components unless otherwise stated.
4. Edge of ceramic and glue bead will not protrude past edge of lensholder.
5. Dimensions enclosed thus are inspection dimensions.
6. Minimum breaking torque between lensholder and barrel is 40 Nmm.
7. Surface finish on external moulded surfaces is RA 16 (Charmille 24).
8. Surface finish on base of ceramic is TBD.
9. All gates on moulded parts will be sub flush.
10. All mouldings to be free from visible flash or mismatch.
11. Uniformly distributed load of 20N may be applied to datum surfaces A & B.
12. These numbers denote tool No. and cavity.
13. These 3 depressions contain gates or are used for cavity & tool identification and ejector pin locations.

All dimensions in mm

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Figure 8. SmOP1.5 Module Outline

Field of View Data.

Edges of circular holes in customer's equipment must not intrude into the Cone. Edges of rectangular holes must not protrude into the Pyramid.

Material

Makrolon: 2405 Colour Black
COP: Zeonex E48R
E Glass Coated with IR Filter Material
Silicon
Ceramic: Alumina Dark Grey

Tolerances, unless otherwise stated

Linear

+0.10  Place Decimals 0  ±1.01  Place Decimals 0.0  ±0.10  Place Decimals 0.00  ±0.07

Angular

±0.25 degrees

Diameter

+0.10  Place Decimals 0

Position

0.10

Surface Finish 1.6 microns
Figure 9. SmOP1.5 Module Outline

Part Marking in Hatched areas. Refer to Spec. TBD for details.

Pad material is 0.30 microns gold on 2 microns nickel.

Underside of module showing connector and test pad layout.

Interpret drawing per BS308, 3rd Angle Projection.

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Figure 10. Module Outline (SmOP 2M)

Gate Location

These cavities may contain glue.

Notes:
1. Mass of module: <0.5 grammes.
2. 2 deg max draft angle on all moulded components unless otherwise stated.
3. Surface finish on all external moulded surfaces is Charmille 30 MAX.
4. Surfaces shown in silver to be conductively plated. See sheet 2 for plating information.
5. All gates to be sub flush.
6. All mouldings to be free from flash or mismatch.
7. Uniformly distributed load of 20N to be applied to datum surfaces A & B.
8. These numbers denote tool number and cavity.
9. These depressions may be used to indicate lens type, tool number and cavity.
10. These cavities may contain glue.

Notes:
11. Breaking torque between lens barrel and holder > 20 Nmm.
12. Corners of the substrate will not protrude past the rectangular footprint of the lens holder.
13. Glue bead will not protrude past edge of substrate.
14. All dimensions in mm. Do Not Scale.

Material: TPR

Surface Finish: 1.6 microns

Tolerances, unless otherwise stated:
- All Dimensions: ±0.10 mm
- Angular Position: ±0.1 degrees
- Surface Finish: 1.6 microns

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Part No.

Date

Initial

Consumer & Micro Group - Imaging Division

Drawn

Material

Finish

All dimensions in mm

Interpret drawing per BS308, 3RD Angle Projection
Figure 11. SmOP2 Module Outline

1. 4 point probe to be used to check resistance of the metalization.
2. Probe to must not contact the lens mount in the scalloped areas.
3. Probe to contact the cylindrical section of the lens mount between any 2 of the 3 equi-spaced points around the diameter.
4. Plating Options:
   a. 1 micron Copper, 0.1 micron MIN Stainless Steel
   b. 1 micron Copper, 0.1 micron MIN Nickel Chrome
   c. 1 micron Copper, 0.1 micron MIN TBD
5. Resistance to be less than 1 ohm.
6. Contact force to be 2N.

Tolerances, unless otherwise stated:

- All Dimensions: ±0.03
- Plan Dimensions: 0.05, 0.06
- Angular: ±0.5 degrees

Plating Notes:
- "Class A" Surface (Top face of barrel)
- Scalarps may contain welding marks.
- Weld will not protrude past cylindrical surface.
- These cavities may contain glue.
- 0.5 Cosmetics not guaranteed outside this area.
- Probe points to contact inside dotted lines.
- "Class A" Surface (Top face of barrel)

Sections A-A and B-B

Scale 5:1

Exclusion Zones:
- Edges of circular holes in customer's equipment must not protrude into the cone.
- Edges of rectangular holes must not protrude into the pyramid.

Note:
- If an upgrade path from 5.6 micron VGA to 4 micron SVGA is required then the 4 micron SVGA data should be used.

MAX Exclusion Zones Dimensions

<table>
<thead>
<tr>
<th>Module</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.6 micron VGA</td>
<td>61</td>
<td>50.36</td>
<td>39.06</td>
<td>4</td>
<td>3.2</td>
<td>2.4</td>
</tr>
<tr>
<td>4 micron SVGA</td>
<td>64</td>
<td>53.12</td>
<td>41.1</td>
<td>4.15</td>
<td>3.32</td>
<td>2.49</td>
</tr>
</tbody>
</table>

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Interpret drawing per BS308, 3RP Angle Projection

Material

All Dimensions in mm

Finish

This drawing is the property of STMicroelectronics and will not be copied or loaned without the written permission of STMicroelectronics.

See Plating Notes 2 and 3

These surfaces to be plated

SECTION A-A

SCALE 5:1

Exclusion Zones,
- Edges of circular holes in customer's equipment must not intrude into the cone.
- Edges of rectangular holes must not protrude into the pyramid.

Dimensions shown are maximums.

Note: If an upgrade path from 5.6 micron VGA to 4 micron SVGA is required then the 4 micron SVGA data should be used.
Underdside of module showing connector and test pad layout.

Area for test pads, additional tracks and part marking. No conductive contact or force allowed in this area.

Note:
Minimum size shown for pad. Pad spacing will be maintained. Actual pad outlines may be extended. Refer to individual product substrate drawings.

**Tolerances**, unless otherwise stated:
- All Dimensions: ±0.1
- Surface Finish: 1.6 microns
- Material:
  - Pad Material is 0.3 microns minimum gold on 5 microns minimum nickel.
- Position: ±0.10
- Angular: ±0.5 degrees

**Material**
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**Drawn**
DBS

**Date**
18/06/03

**Part No.**
7540020

**Title**
SMOP2-M OUTLINE DRAWING

**Scale**
3 of 3
Notes:
1. Mass of module: <0.5 grammes.
2. Volume of module: 384.7 mm^3.
3. 2 deg max draft angle on all moulded components unless otherwise stated.
4. Surface finish on all external moulded surfaces is Charmille 30 MAX.
5. Surfaces shown in silver to be conductively plated. See sheet 2 for plating information.
6. All gates to be sub flush.
7. All mouldings to be free from flash or mismatch.
8. Uniformly distributed load of 20N to be applied to datum surfaces A & B.
9. These numbers denote tool number and cavity. Text will be sub flush with surface.
10. These depressions may be used to indicate lens type, tool number and cavity.
11. Dimensions enclosed ( ) are inspection dimensions.
12. Breaking torque between lens barrel and holder > 20 Nmm.
13. All translational and rotational placement tolerances are included in this area.
14. Glue bead will not protrude past edge of Lens Holder.

Tolerances, unless otherwise stated:
- All Decimals: ±0.1
- Surface Finish: ±0.5 degrees
- Angular Position: ±0.1
- Surface Finish: ±0.5 microns

Material
- All dimensions in mm
- Interpreted drawing per BS308, 3RD Angle Projection

Finish
- All dimensions in mm
- This drawing is the property of STMicroelectronics and will not be reproduced without the written permission of STMicroelectronics.

Drawn
- DBS
- Date: 30/06/03
- Title: SMOP2-ME OUTLINE DRAWING

Sheet 1 of 3
Figure 14. SmOP2 Module Outline

**Pyramid**

See Table Dim A

**Cone**

See Table Dim B

Noryl N110, COP or PC

Noryl N110, COP or PC

E Glass with IR filter Material

Silicon

Substrate: Glass/epoxy pre-peg

---

**Plating Notes**

1. A point probe to be used to check resistance of the metalisation.
2. Probe to must not contact the lens mount in the scalloped areas.
3. Probe to contact the cylindrical section of the lens mount between any 2 of the 3 equi-spaced points around the diameter.

4. Plating Options:
   - a. 1 micron Copper, 0.1 micron MIN Stainless Steel
   - b. 1 micron Copper, 0.1 micron MIN Nickel Chrome
   - c. 1 micron Copper, 0.1 micron MIN TBO
5. Resistance to be less than 1 ohm.
6. Contact force to be 2N.

-exclusion Zones.

Edges of circular holes in customer's equipment must not intrude into the cone.
Edges of rectangular holes must not protrude into the pyramid.
Dimensions shown are maximums.

Note: If an upgrade path from 5.6 micron VGA to 4 micron SVGA is required then the 4 micron SVGA data should be used.

---

**MAX Exclusion Zones Dimensions**

<table>
<thead>
<tr>
<th>Module</th>
<th>A</th>
<th>B</th>
<th>C</th>
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<th>F</th>
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<tbody>
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<td>39.06</td>
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<td>64</td>
<td>53.12</td>
<td>41.1</td>
<td>4.15</td>
<td>3.32</td>
<td>2.49</td>
</tr>
</tbody>
</table>

---

**Material**

- 1 micron Copper, 0.1 micron MIN Stainless Steel
- 1 micron Copper, 0.1 micron MIN Nickel Chrome
- 1 micron Copper, 0.1 micron MIN TBD

**Interpretation**

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Figure 15. SmOP2 Module Outline

Underneath of module showing connector and test pad layout.

Notes:
B1. Notes and 10 connected Top edge radius charged from 0.005mm.
B2. Surface finish charged to charmele 30 MAX.
B3. Pad diameter reduced to charmele 30 MAX.
B4. Surface finish charged to charmele 30 MAX.

---

Any force applied to the topside of the substrate should be balanced by a counter force directly opposite on the underside of the substrate and vice versa.
8 APPLICATION INFORMATION

8.1 Socket
ST has developed a low-profile socket for the SmOP 1.5 package, which is suitable for reflow soldering and manual / automatic insertion of the camera module. The socket has been designed to withstand mobile phone grade reliability tests (temperature, shocks, vibration, salt mist). Please contact ST for details on ST P/N XS0015. See Figure 16 for recommended PCB layout and mechanical footprint of the XS0015 socket.

8.2 EMC and Shielding
The VS6552 is a low noise device and is highly tolerant of high levels of radio frequency (RF) radiation. However if this device is closely mounted to a sensitive receiver it is recommended that the VS6552 is shielded to prevent reducing the sensitivity or channel masking of the receiver.
Recommended maximum field strength: 1kV/m. Maximum radiated power transferred from the VS6552 into a GSM monopole antenna mounted 15 mm away from the VS6552 has peaks of interference at around -90 dBm. This is dependent on system design and layout.

To minimized the coupling between the GSM antenna and the sensor the following guide lines should be observed.
Camera should be positioned as far away from the GSM antenna as possible. The distance between the low frequency (below 1GHz) resonant antenna elements and the camera should also be maximized.
The VS6552 and its associated decoupling capacitors should NOT be connected together using the antenna reference ground. The ground connections in the sub circuit should be connected either:
- by a dedicated ground trace network, that is connected by a single point to the main ground of the system
- by an internal ground plane, which is entirely covered and single point connected to a protective ground.
The PCLKP and PCLKN lines can be filtered to reduce the induced noise.
The protective ground should be flooded around the sensor socket pads to reduce the radiation aperture in the protective ground plane.
Figure 16. SmOP1.5 Socket Mechanical Data
9 REVISION HISTORY

Table 17. Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description of Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>May 2004</td>
<td>1</td>
<td>First Release of Product Preview</td>
</tr>
<tr>
<td>21 October 2004</td>
<td>2</td>
<td>Second Release - Document status changed to datasheet. to reflect the product maturity level. Changes applied in Electrical Characteristics and Package Information with the addition of two packages (SmOP2M and SmOP2ME).</td>
</tr>
</tbody>
</table>