FEATURES

- **25, 35, 45 ns Read Access & R/W Cycle Time**
- **Unlimited Read/Write Endurance**
- **Automatic Non-volatile STORE on Power Loss**
- **Non-Volatile STORE Under Hardware or Software Control**
- **Automatic RECALL to SRAM on Power Up**
- **Unlimited RECALL Cycles**
- **1 Million STORE Cycles**
- **100-Year Non-volatile Data Retention**
- **Single 5V ±10% Power Supply**
- **Commercial, Industrial, Military Temperatures**
- **32-Pin 300 mil SOIC (RoHS-Compliant)**
- **32-pin CDIP and LCC Packages**

DESCRIPTION

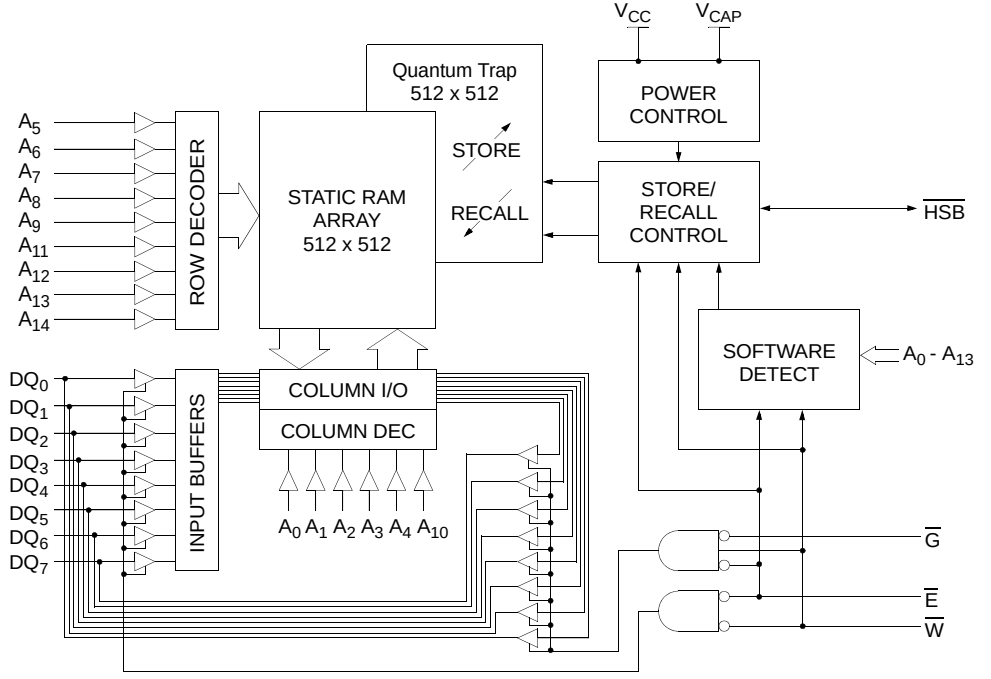
The Simtek STK14C88 is a 256Kb fast static RAM with a non-volatile Quantum Trap storage element included with each memory cell.

The SRAM provides the fast access & cycle times, ease of use and unlimited read & write endurance of a normal SRAM.

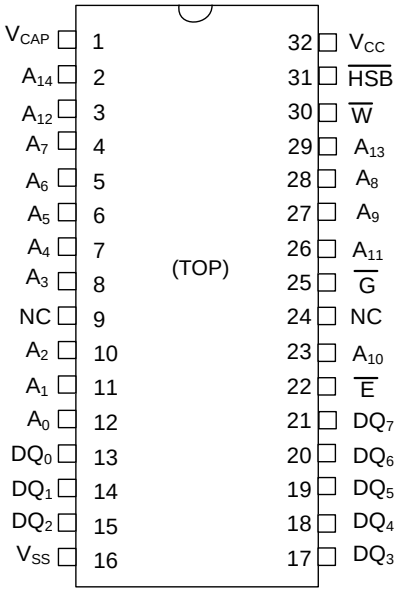
Data transfers automatically to the non-volatile storage cells when power loss is detected (the STORE operation). On power up, data is automatically restored to the SRAM (the RECALL operation). Both STORE and RECALL operations are also available under software control.

The Simtek nvSRAM is the first monolithic non-volatile memory to offer unlimited writes and reads. It is the highest performance, most reliable non-volatile memory available.

BLOCK DIAGRAM

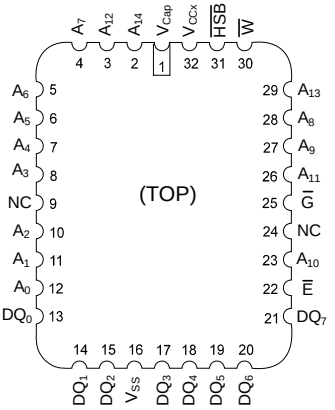


PIN CONFIGURATIONS



32-Pin 300 mil SOIC

32-Pin 300 mil CDIP



32-Pin 450 mil LCC

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{14}-A_0	Input	Address: The 15 address inputs select one of 32,768 bytes in the nvSRAM array
DQ_7-DQ_0	I/O	Data: Bi-directional 8-bit data bus for accessing the nvSRAM
$\overline{E}$	Input	Chip Enable: The active low $\overline{E}$ input selects the device
$\overline{W}$	Input	Write Enable: The active low $\overline{W}$ enables data on the DQ pins to be written to the address location latched by the falling edge of $\overline{E}$
$\overline{G}$	Input	Output Enable: The active low $\overline{G}$ input enables the data output buffers during read cycles. De-asserting $\overline{G}$ high caused the DQ pins to tri-state.
V_{CC}	Power Supply	Power: 5.0V, ±10%
$\overline{HSB}$	I/O	Hardware Store Busy: When low this output indicates a Store is in progress. When pulled low external to the chip, it will initiate a nonvolatile STORE operation. A weak pull up resistor keeps this pin high if not connected. (Connection Optional).
V_{CAP}	Power Supply	AutoStore Capacitor: Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile storage elements.
V_{SS}	Power Supply	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to Ground . . . . . –0.5V to 7.0V
Voltage on Input Relative to V_{SS} . . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ . . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias. . . . . –55°C to 125°C
Storage Temperature . . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)[e]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL/ Military		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}[b]	Average V_{CC} Current		97 80 70		100 85 70	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC2}[c]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC4}[c]	Average V_{CAP} Current during AutoStore Cycle		2		2	mA	All Inputs Don't Care
I_{SB1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30 25 22		31 26 23	mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA except $\overline{HSB}$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA except $\overline{HSB}$
V_{BL}	Logic "0" Voltage on $\overline{HSB}$ Output		0.4		0.4	V	I_{OUT} = 3mA
T_A	Operating Temperature	0	70	-40/-55	85/125	°C	

Note b: I_{CC1} and I_{CC3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC2} and I_{CC4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.
Note e: V_{CC} reference levels throughout this datasheet refer to V_{CC} if that is where the power supply connection is made, or V_{CAP} if V_{CC} is connected to ground.

AC TEST CONDITIONS

Input Pulse Levels . . . . . 0V to 3V
Input Rise and Fall Times. . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE[f] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

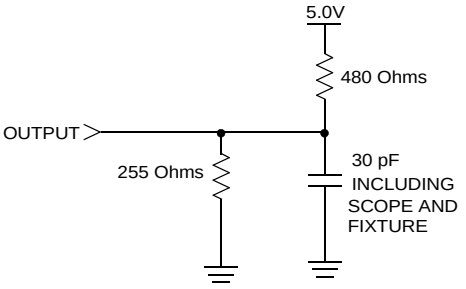


Figure 1: AC Output Loading

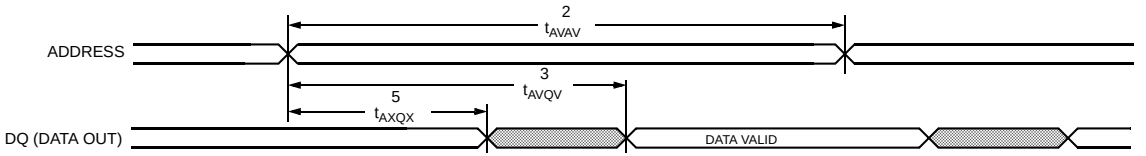
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[e]

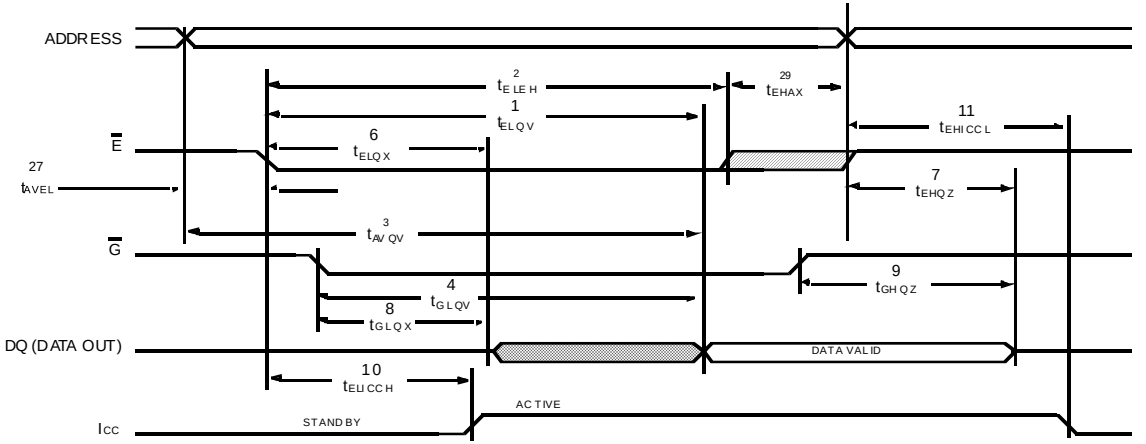
NO.	SYMBOLS		PARAMETER	STK14C88-25		STK14C88-35		STK14C88-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[g], t_{ELEH}[g]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[h]	t_{OH}	Output Hold after Address Change	5		5		5		ns
6	t_{ELQX}	t_{LZ}	Address Change or Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[i]	t_{HZ}	Address Change or Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[f]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[f]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note g: $\overline{W}$ and $\overline{HSB}$ must be high during SRAM READ cycles.
Note h: I/O state assumes $\overline{E}$ and $\overline{G} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$; device is continuously selected.
Note i: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[g, h]



SRAM READ CYCLE #2: $\overline{E}$ and $\overline{G}$ Controlled[g]



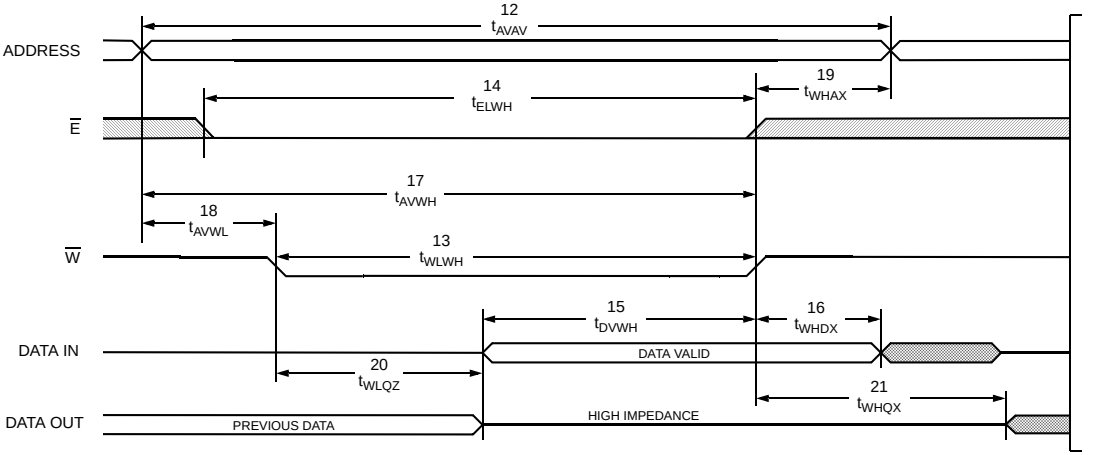
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[e]

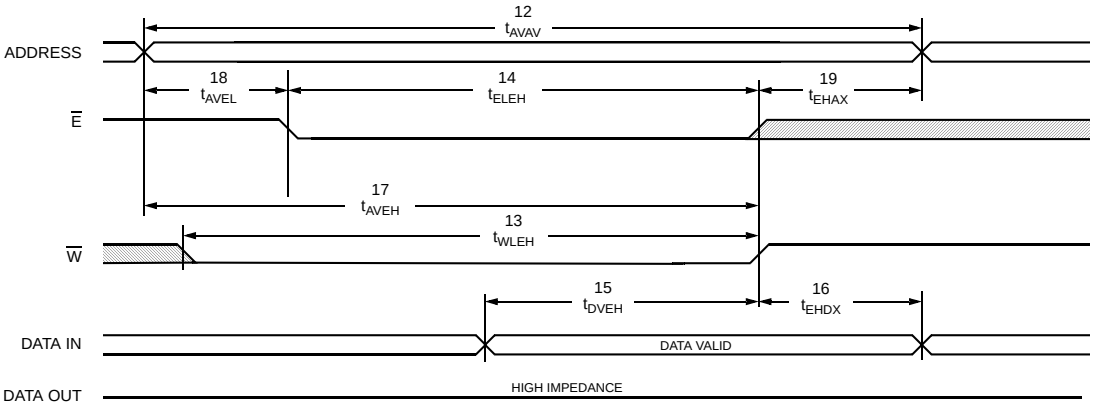
NO.	SYMBOLS			PARAMETER	STK14C88-25		STK14C88-35		STK14C88-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[i, j]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		ns

Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note l: $\overline{HSB}$ must be high during SRAM WRITE cycles.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[k, l]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[k, l]



HARDWARE MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A_{13} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	t
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile *STORE*	Output High Z	I_{CC2}	m

Note m: $\overline{HSB}$ *STORE* operation occurs only if an SRAM WRITE has been done since the last nonvolatile cycle. After the *STORE* (if any) completes, the part will go into standby mode, inhibiting all operations until $\overline{HSB}$ rises.

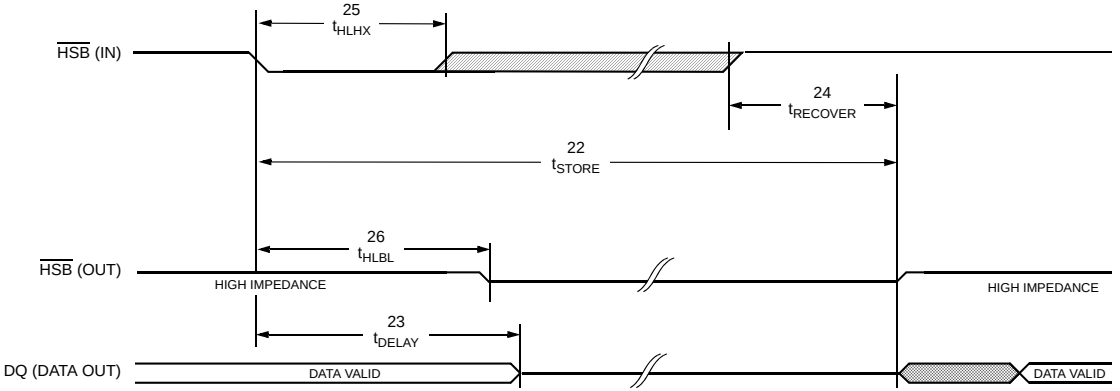
HARDWARE *STORE* CYCLE

(V_{CC} = 5.0V ± 10%)[e]

NO.	SYMBOLS		PARAMETER	STK14C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	n
23	t_{DELAY}	t_{HLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	n
24	$t_{RECOVER}$	t_{HHQX}	Hardware *STORE* High to Inhibit Off		700	ns	n, o
25	t_{HLHX}		Hardware *STORE* Pulse Width	15		ns	
26	t_{HLBL}		Hardware *STORE* Low to *STORE* Busy		300	ns	

Note n: $\overline{E}$ and $\overline{G}$ low and $\overline{W}$ high for output behavior.
Note o: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE *STORE* CYCLE



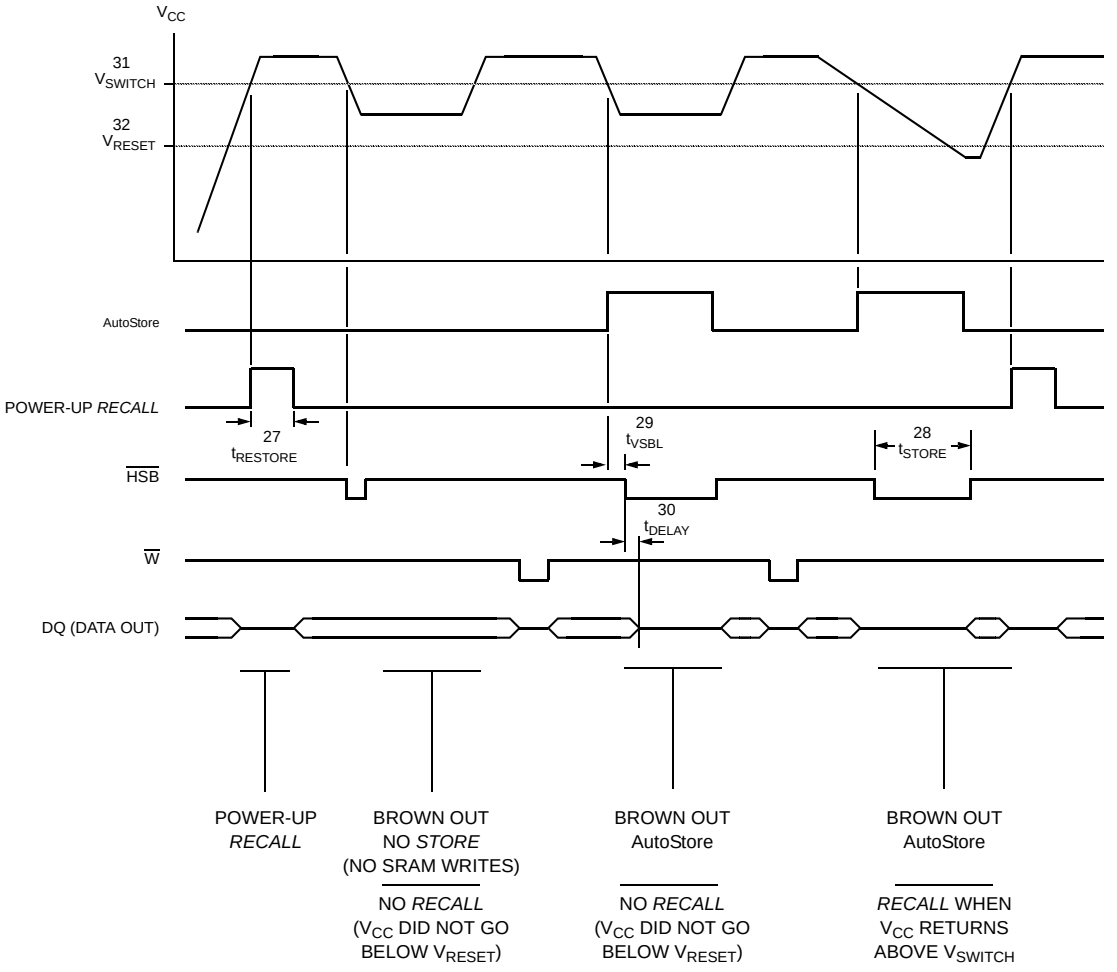
AutoStore™/POWER-UP *RECALL*

(V_{CC} = 5.0V ± 10%)[e]

NO.	SYMBOLS		PARAMETER	STK14C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	$t_{RESTORE}$		Power-up *RECALL* Duration		550	µs	p
28	t_{STORE}	t_{HLHZ}	*STORE* Cycle Duration		10	ms	n, q
29	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ Low		300	ns	l
30	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	n
31	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
32	V_{RESET}		Low Voltage Reset Level		3.6	V	

Note p: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note q: HSB is asserted low for 1µs when V_{CAP} drops through V_{SWITCH}. If an SRAM WRITE has not taken place since the last nonvolatile cycle, $\overline{HSB}$ will be released and no *STORE* will take place.

AutoStore™/POWER-UP *RECALL*



SOFTWARE *STORE*/*RECALL* MODE SELECTION

$\overline{E}$	$\overline{W}$	A_{13} - A_0 (hex)	MODE	I/O	POWER	NOTES
L	H	0E38	Read SRAM	Output Data	Active	n, r, s, t
		31C7	Read SRAM	Output Data		
		03E0	Read SRAM	Output Data		
		3C1F	Read SRAM	Output Data		
		303F	Read SRAM	Output Data		
		0FC0	Nonvolatile *STORE*	Output High Z	I_{CC2}	
L	H	0E38	Read SRAM	Output Data	Active	n, r, s, t
		31C7	Read SRAM	Output Data		
		03E0	Read SRAM	Output Data		
		3C1F	Read SRAM	Output Data		
		303F	Read SRAM	Output Data		
		0C63	Nonvolatile *RECALL*	Output High Z		

SOFTWARE-CONTROLLED *STORE*/*RECALL* CYCLE[v] (V_{CC} = 5.0V ± 10%)[e]

NO.	SYMBOLS		PARAMETER	STK14C88-25		STK14C88-35		STK14C88-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
33	t_{AVAV}	t_{RC}	*STORE*/*RECALL* Initiation Cycle Time	25		35		45		ns	n
34	t_{AVEL}	t_{AS}	Address Set-up Time	0		0		0		ns	u,v
35	t_{ELEH}	t_{CW}	Clock Pulse Width	20		25		30		ns	u,v
36	t_{ELAX}		Address Hold Time	20		20		20		ns	u, v
37	t_{RECALL}		*RECALL* Duration		20		20		20	µs	

Note r: The six consecutive addresses must be in the order listed. $\overline{W}$ must be high during all six consecutive $\overline{E}$ controlled cycles to enable a nonvolatile cycle.

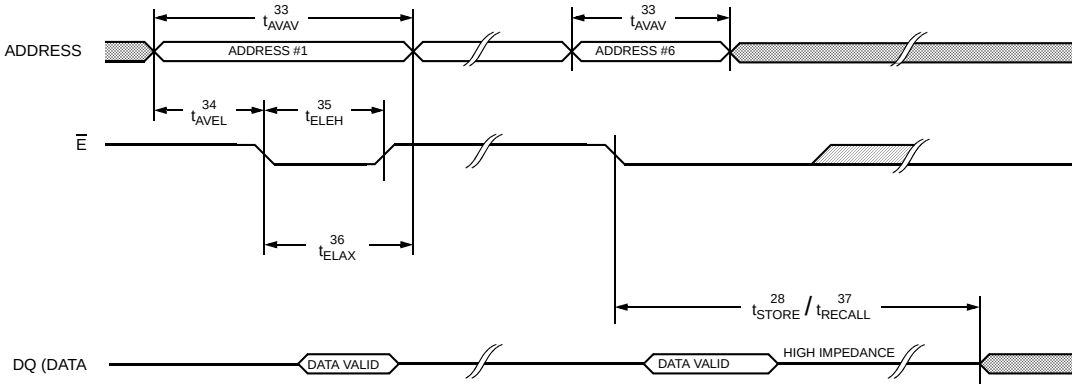
Note s: While there are 15 addresses on the STK14C88, only the lower 14 are used to control software modes.

Note t: I/O state assumes $\overline{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on state of $\overline{G}$.

Note u: The software sequence is clocked on the falling edge of $\overline{E}$ controlled READs without involving $\overline{G}$ (double clocking will abort the sequence). See application note: MA0002 http://www.simtek.com/attachments/appNote02.pdf.

Note v: The six consecutive addresses must be in the order listed in the Software *STORE*/*RECALL* Mode Selection Table: (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a *STORE* cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE*/*RECALL* CYCLE: $\overline{E}$ CONTROLLED[v]



nvSRAM OPERATION

The STK14C88 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to nonvolatile elements (the *STORE* operation) or from nonvolatile elements to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

NOISE CONSIDERATIONS

The STK14C88 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK14C88 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

POWER-UP *RECALL*

During power up, or after any low-power condition (V_{CAP} < V_{RESET}), an internal *RECALL* request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK14C88 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

SOFTWARE NONVOLATILE *STORE*

The STK14C88 software *STORE* cycle is initiated by executing sequential $\overline{E}$ controlled READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0FC0 (hex)	Initiate *STORE* cycle

The software sequence must be clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of $\overline{E}$ controlled READ operations must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0C63 (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the nonvolatile elements. The nonvolatile data can be recalled an unlimited number of times.

AutoStore MODE

The STK14C88 can be powered in one of three modes.

During normal AutoStore operation, the STK14C88 will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single *STORE* operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC} and initiate a *STORE* operation.

Figure 1 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of between 68μF and 220μF (± 20%) rated at 6V should be provided.

In system power mode, both V_{CC} and V_{CAP} are connected to the + 5V power supply without the 68μF capacitor. In this mode the AutoStore function of the STK14C88 will operate on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10ms *STORE* cycle.

If an automatic *STORE* on power loss is not required, then V_{CC} can be tied to ground and + 5V applied to V_{CAP} (Figure 2). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the STK14C88 is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, *STORE* operations may be triggered through software control or the $\overline{HSB}$ pin. To enable or disable AutoStore using an IO port pin, see “PREVENTING STORES” on page 12.

In order to prevent unneeded *STORE* operations, automatic *STORE*s as well as those initiated by externally driving $\overline{HSB}$ low will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle. Software-initiated *STORE* cycles are performed regardless of whether a WRITE operation has taken place.

If the power supply drops faster than 20 μs/volt before V_{CC} reaches V_{SWITCH}, then a 2.2 ohm resistor should be inserted between V_{CC} and the system supply to avoid momentary excess of current between Vcc and Vcap.

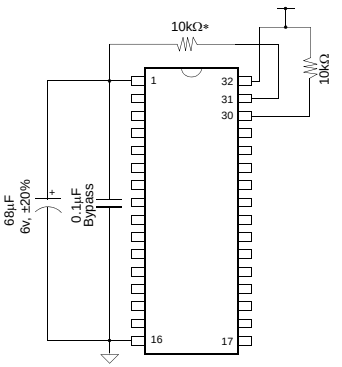


Figure 1: AutoStore Mode

AutoStore INHIBIT MODE

If an automatic *STORE* on power loss is not required, then V_{CC} can be tied to ground and system power applied to V_{CAP} (Figure 2). This is the AutoStore Inhibit Mode, in which the AutoStore function is disabled. If the STK14C88 is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, STORE operations may be triggered through software control. It is not permissible to change between these three options “on the fly.”

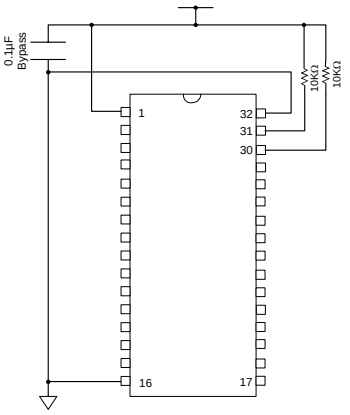


Figure 2: AutoStore Inhibit Mode

HSB OPERATION

The STK14C88 provides the $\overline{HSB}$ pin for controlling and acknowledging the *STORE* operations. The $\overline{HSB}$ pin can be used to request a hardware *STORE* cycle. When the $\overline{HSB}$ pin is driven low, the STK14C88 will conditionally initiate a *STORE* operation after t_{DELAY}; an actual *STORE* cycle will only begin if a WRITE to the SRAM took place since the last *STORE* or *RECALL* cycle. The $\overline{HSB}$ pin has a very resistive pullup and is internally driven low to indicate a busy condition while the *STORE* (initiated by any means) is in progress. Pull up this pin with an external 10K ohm resistor to V_{CAP} if $\overline{HSB}$ is used as a driver.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the *STORE* operation is initiated. After $\overline{HSB}$ goes low, the STK14C88 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

The $\overline{HSB}$ pin can be used to synchronize multiple STK14C88s while using a single larger capacitor. To operate in this mode the $\overline{HSB}$ pin should be connected together to the $\overline{HSB}$ pins from the other STK14C88s. An external pull-up resistor to + 5V is required since $\overline{HSB}$ acts as an open drain pull down. The V_{CAP} pins from the other STK14C88 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK14C88s detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin will cause all parts to request a *STORE* cycle (a *STORE* will take place in those STK14C88s that have been written since the last nonvolatile cycle).

During any *STORE* operation, regardless of how it was initiated, the STK14C88 will continue to drive the $\overline{HSB}$ pin low, releasing it only when the *STORE* is complete. Upon completion of the *STORE* operation the STK14C88 will remain disabled until the $\overline{HSB}$ pin returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

BEST PRACTICES

nvSRAM products have been used effectively for over 15 years. While ease-of-use is one of the product’s main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The non-volatile cells in an nvSRAM are programmed on the test floor during final test and quality assurance. Incoming inspection routines at customer or contract manufacturer’s sites will sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product’s firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, etc. should always program a unique NV pattern (e.g., complex 4-byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.

- Power up boot firmware routines should rewrite the nvSRAM into the desired state (autostore enabled, etc.). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently (program bugs, incoming inspection routines, etc.).
- The V_{cap} value specified in this datasheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the max V_{cap} value because the nvSRAM internal algorithm calculates V_{cap} charge time based on this max Vcap value. Customers that want to use a larger V_{cap} value to make sure there is extra store charge and store time should discuss their V_{cap} size selection with Simtek to understand any impact on the V_{cap} voltage level at the end of a t_{RECALL} period.

PREVENTING STORES

The *STORE* function can be disabled on the fly by holding $\overline{HSB}$ high with a driver capable of sourcing 30mA at a V_{OH} of at least 2.2V, as it will have to overpower the internal pull-down device that drives $\overline{HSB}$ low for 20µs at the onset of a *STORE*. When the STK14C88 is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the STK14C88 will attempt to pull $\overline{HSB}$ low; if $\overline{HSB}$ doesn't actually get below V_{IL}, the part will stop trying to pull $\overline{HSB}$ low and abort the *STORE* attempt.

HARDWARE PROTECT

The STK14C88 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CAP} < V_{SWITCH}$, all externally initiated *STORE* operations and SRAM WRITEs will be inhibited.

AutoStore can be completely disabled by tying V_{CC} to ground and applying + 5V to V_{CAP}. This is the AutoStore Inhibit mode; in this mode *STORE*s are only initiated by explicit request using either the software sequence or the $\overline{HSB}$ pin.

LOW AVERAGE ACTIVE POWER

The STK14C88 draws significantly less current when it is cycled at times longer than 50ns. Figure 3 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 4 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK14C88 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{cc} level; and 7) I/O loading.

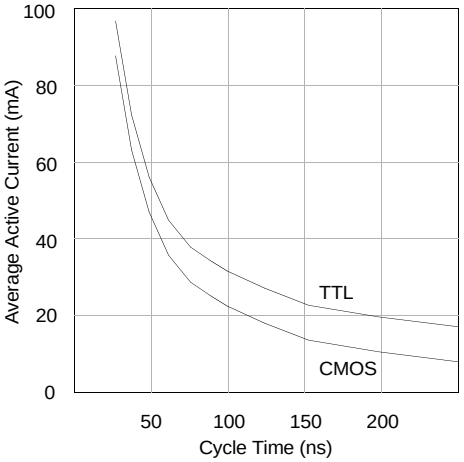


Figure 3: I_{cc} (max) Reads

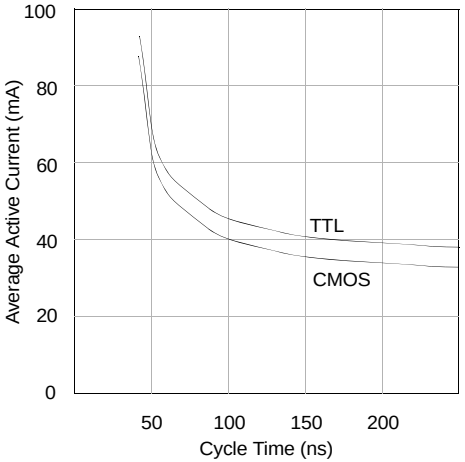
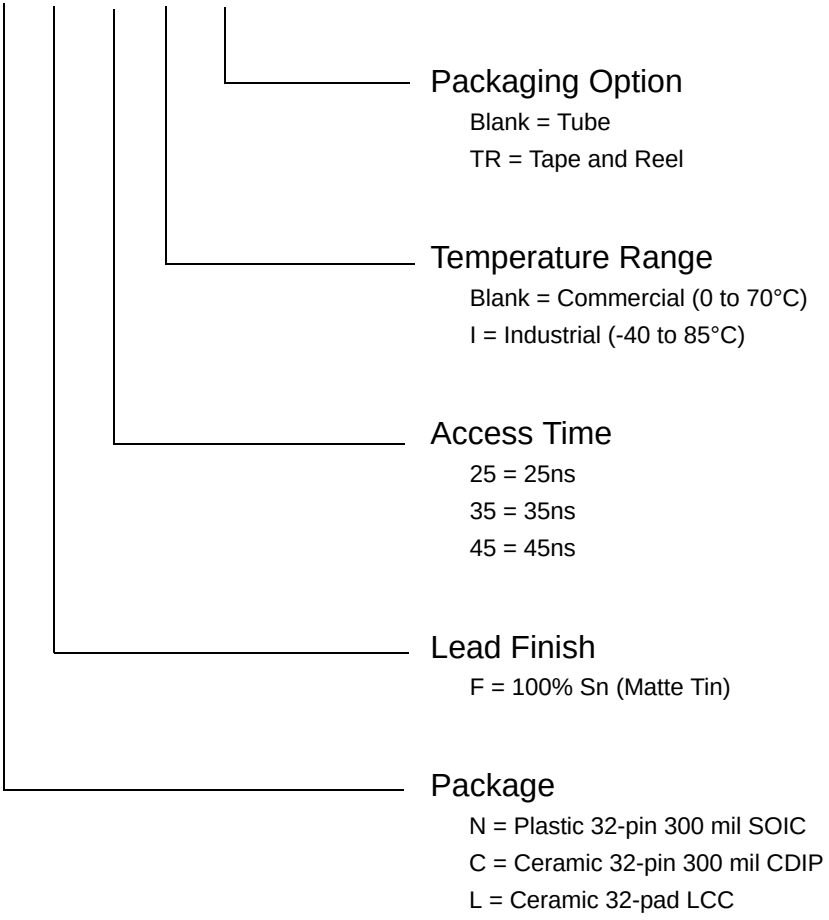


Figure 4: I_{cc} (max) Writes

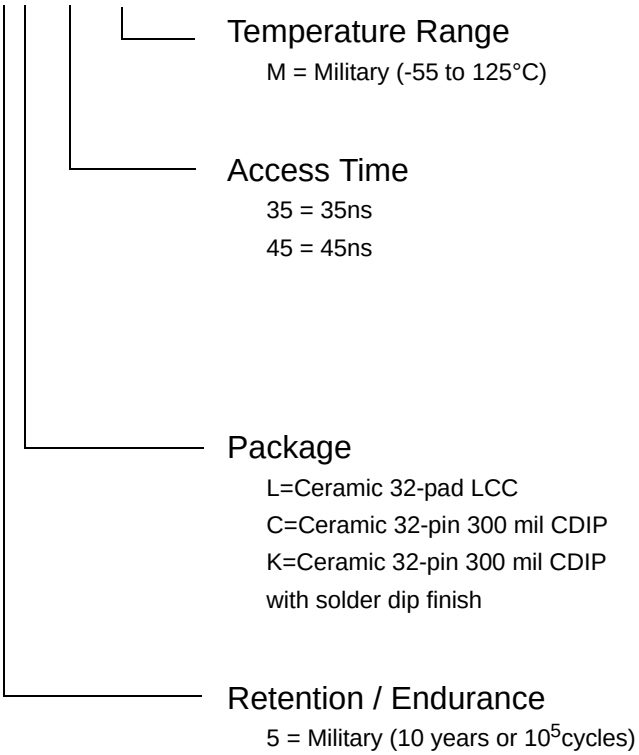
Commercial and Industrial Ordering Information

STK14C88 - N F 45 I TR



Military Ordering Information

STK14C88 - 5 C 45 M

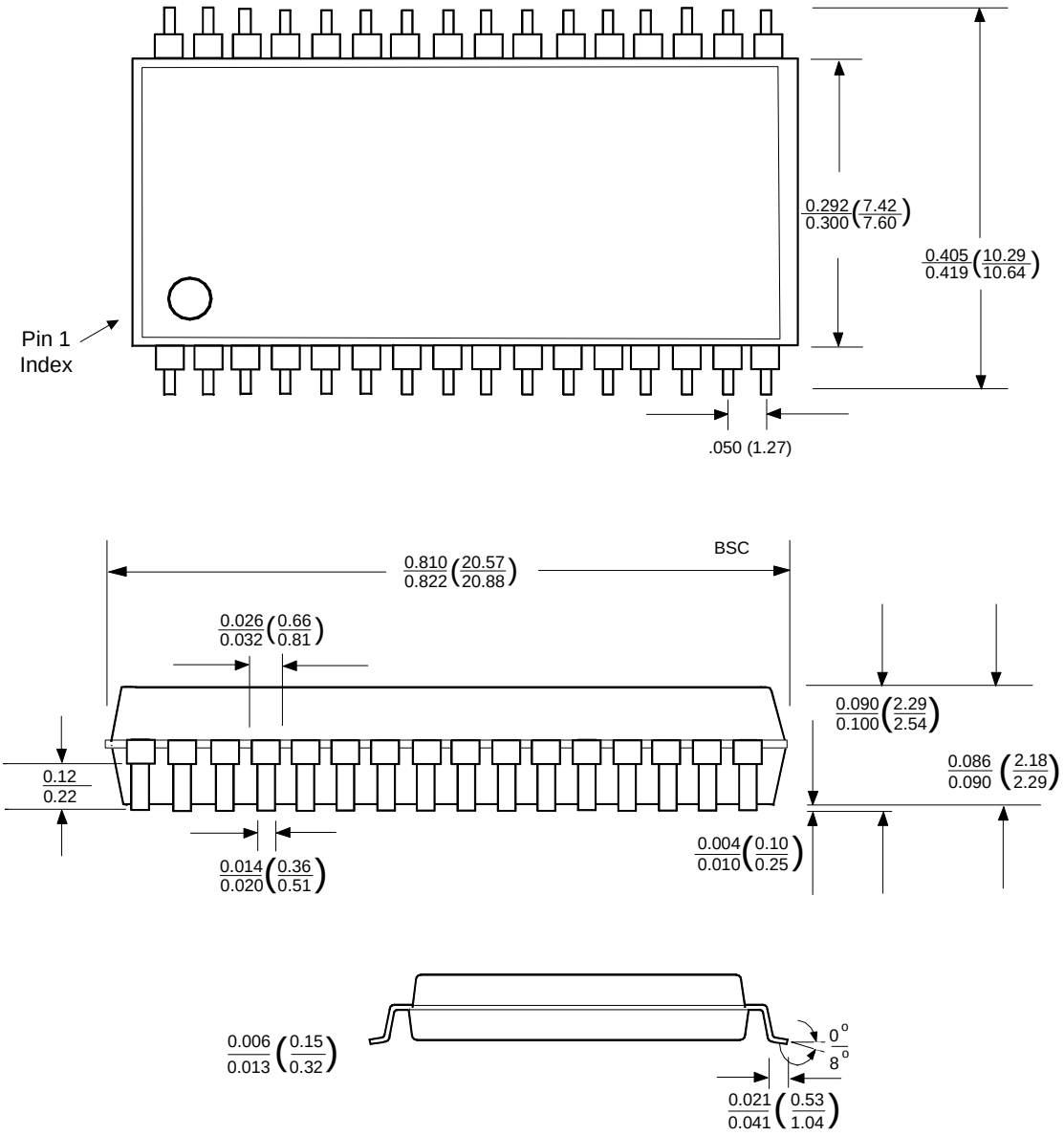


Ordering Information

Part Number	Description	Access Times	Temperature
STK14C88-NF25	5V 32Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Commercial
STK14C88-NF35	5V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Commercial
STK14C88-NF45	5V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Commercial
STK14C88-NF25TR	5V 32Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Commercial
STK14C88-NF35TR	5V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Commercial
STK14C88-NF45TR	5V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Commercial
STK14C88-NF25I	5V 32Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Industrial
STK14C88-NF35I	5V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Industrial
STK14C88-NF45I	5V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Industrial
STK14C88-NF25ITR	5V 32Kx8 AutoStore nvSRAM SOP32-300	25 ns access time	Industrial
STK14C88-NF35ITR	5V 32Kx8 AutoStore nvSRAM SOP32-300	35 ns access time	Industrial
STK14C88-NF45ITR	5V 32Kx8 AutoStore nvSRAM SOP32-300	45 ns access time	Industrial
STK14C88-C45I	5V 32Kx8 AutoStore nvSRAM CDIP32-300	45 ns access time	Industrial
STK14C88-5L35M	5V 32Kx8 AutoStore nvSRAM LCC32-450	35 ns access time	Military
STK14C88-5L45M	5V 32Kx8 AutoStore nvSRAM LCC32-450	45 ns access time	Military
STK14C88-5C35M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	35 ns access time	Military
STK14C88-5C45M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	45 ns access time	Military
STK14C88-5K35M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	35 ns access time	Military
STK14C88-5K45M	5V 32Kx8 AutoStore nvSRAM CDIP32-300	45 ns access time	Military

Package Diagrams

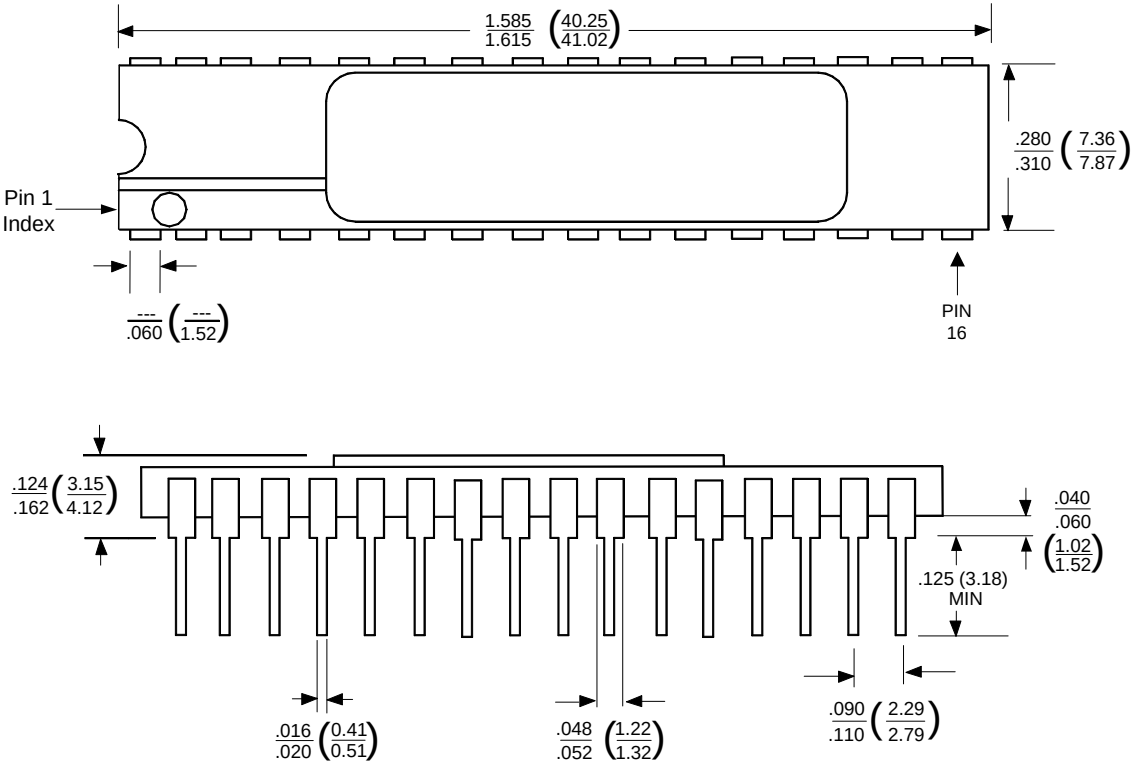
32 Lead 300 mil SOIC Gull Wing



DIM = INCHES MIN / MAX

DIM = mm (MIN / MAX)

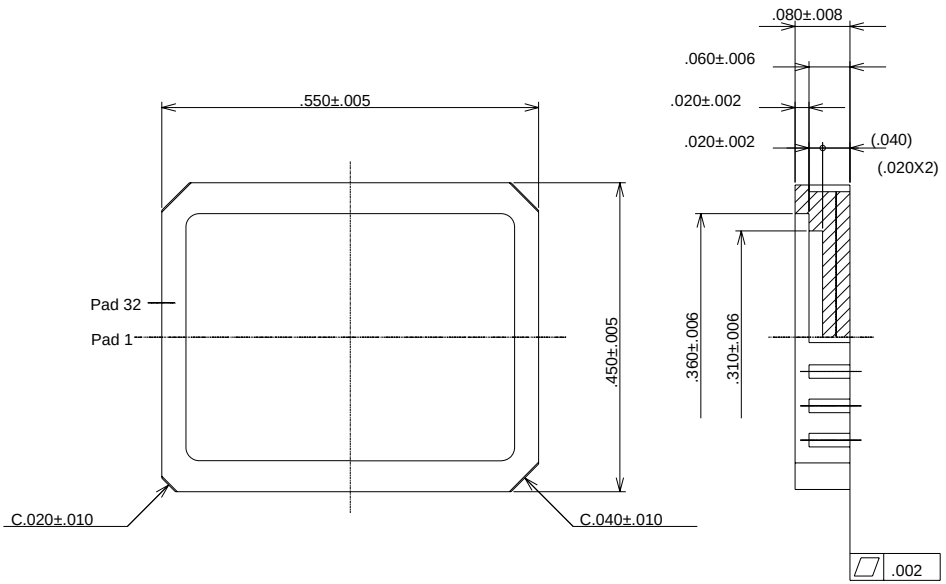
32 Lead 300 mil Side Braze DIL

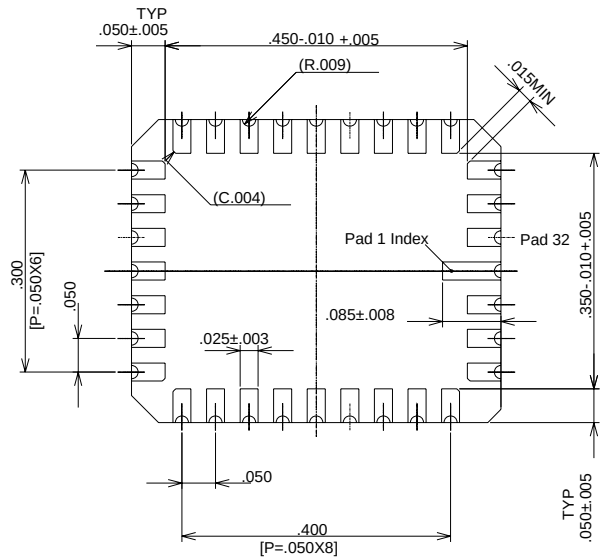


DIM = INCHES MIN / MAX

DIM = mm (MIN / MAX)

32 Lead 450 mil Ceramic LCC





NOTES:
1. GOLD PLATE 85~220, INCHES OVER 50~350 INCHES NICKEL.
2. PADS "A" AND "B" ELECTRICALLY CONNECTED TO THE DIE ATTACH PAD.
3. SEAL RING TO BE ELECTRICALLY ISOLATED FROM ALL LEADS.
4. LEAD RESISTANCE : 800mƒ MAX.
5. LEAD TO LEAD CAPACITANCE NOT TO EXCEED 3pf (1MHz).
6. BLACK ALUMINA CERAMIC.

Document Revision History

Revision	Date	Summary
0.0	December 2002	Removed 20 nsec device; Combined commercial, industrial and military; current limit resistor added for extreme power-off slew rate.
0.1	September 2003	Added lead-free lead finish
0.2	March 2003	Removed Commercial/Industrial Leaded Lead Finish, Removed “W” DIP package
0.3	February 2007	Add Tape Reel Ordering Options Add Product Ordering Code Listing Add Package Drawings Reformat Entire Document
0.4	July 2007	extend definition of t_{HZ} (#7) update fig. SRAM READ CYCLE #2, SRAM WRITE CYCLE #1, Note r, Note u and Note v to clarify product usage
2.0	February 2008	In the block diagramand elsewhere in the document, removed the “x” from V_{CCX}. Page 4: in Note g below the SRAM Read Cycles #1 and #2 table, revised note g by deleting “and low during SRAM WRITE cycles; in SRAM Read Cycles #1 & #2 table, revised description for t_{ELQX} and changed Symbol #2 to t_{ELEH} for Read Cycle Time; updated SRAM Read Cycle #2 timing diagram and changed title to add $\overline{G}$ controlled. Page 6: in Hardware Store Cycle table, removed footnote i for notes 22 and 23. Page 8: in Software Store/Recall Mode Selection table, added footnote n to both rows. Page 11: added best practices section. Under $\overline{HSB}$ Operation, revised first paragraph to read “The $\overline{HSB}$ pin has a very resistive pullup...” Page 15: added access times column to the Ordering codes; removed STK14C88-L45I row from the Ordering Information page.