SG901-1203 Intelligent Wi-Fi Module

Overview

The SG901-1203 is an 802.11b/g/n WLAN module including an integrated 802.11 Wi-Fi radio and microcontroller for easy integration of 802.11 into existing and new products.

The SG901-1203 includes a single-chip 802.11 transceiver, 32-bit microcontroller, flash and RAM. The module also includes a micro 2.45GHz ISM Band antenna. The module implements all levels of the 802.11 and TCP/IP Stack.

The on board 802.11 radio conforms to the IEEE 802.11 protocols operating in the 2.45GHz ISM frequency band supporting OFDM data rates from 6 to 65Mbps. It also supports CCK and legacy rates from 1 to 11Mbps.

The Module is housed in a 28-pin LGA. No external timing clocks or voltage regulators are required.

In addition to standard UART serial communications interfaces up to 2Mbps, a future software upgrade will offer SPI, I2C and I2S support.

The system is shipped running the Sagrad IWM OS ready for customer use.
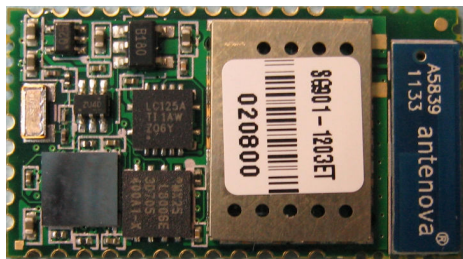
Features

• FCC Certified 802.11 solution currently in process
• All Popular Encryptions supported
• Simple AT command Set
• Variety of Standard Communications Interfaces
  - UART ports (TTL/CMOS Levels)
  - 1 SPI port
• Small, low-profile footprint
• Low current consumption
• Fully compliant with IEEE 802.11b/g and n WLAN standards including security features
• RoHs Compliant

Installed Software

• Sagrad AT commands
• Web Server/Client
• DHCP client

Applications

• iPad/Android remote control
• Deeply embedded wireless
• Industrial data acquisition
• Temperature control
• Home/Industrial automation
• Security systems
• Wireless serial port replacement
• Wireless sensors

Ordering Information

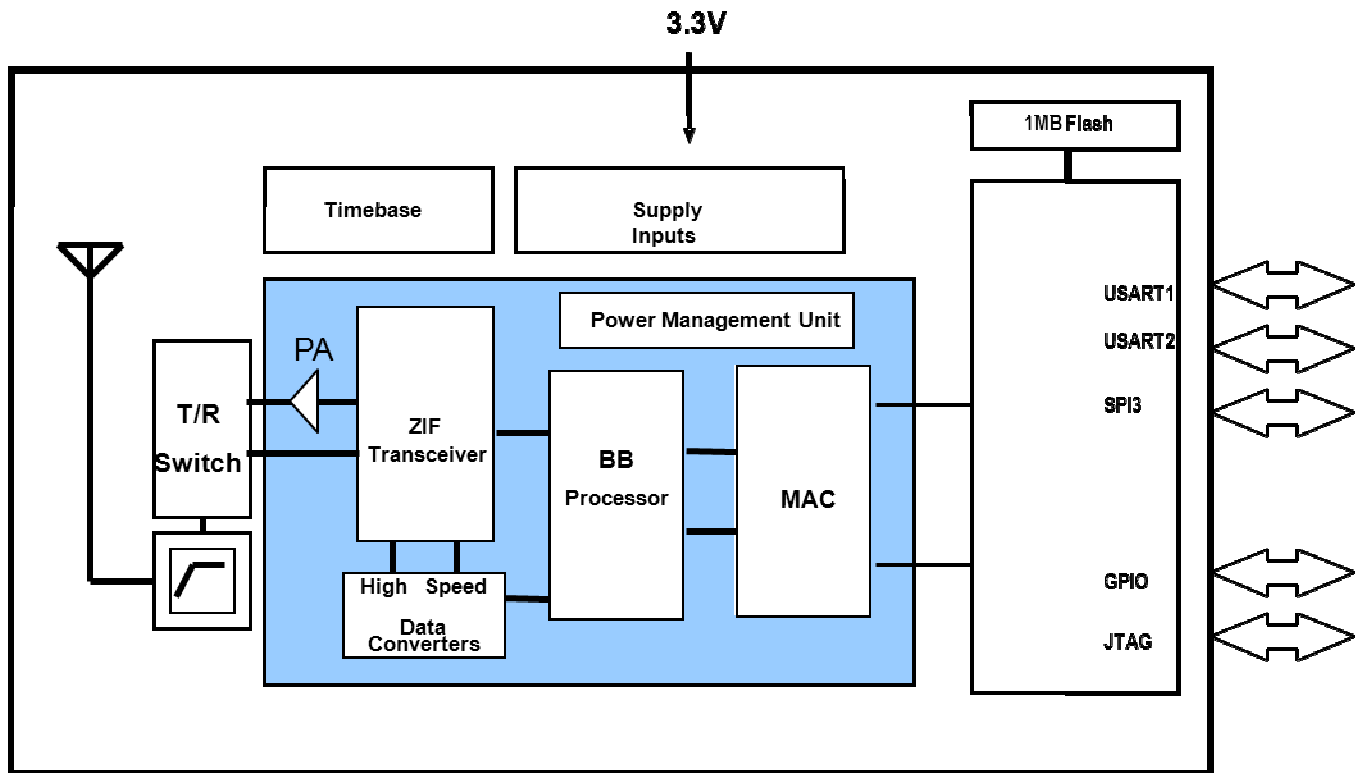| Package	Order Number	Temp Range
Cut tape/TR	SG901-1203-CT	0° to 70°C
Cut tape/TR	SG901-1203-ET	-40° to 85°C
Note: For orders less than 500 units, Sagrad ships in cut tape, otherwise Tape and Reel (TR) packaging is used.		

Evaluation KIT Available

Order Number	Description
SG923-0011	1203-EVK

SG901-1203 Block Diagram

3.3V

Timebase	Supply Inputs

Power Management Unit

1MB Flash

PA

T/R Switch

ZIF Transceiver

BB Processor

MAC

High Speed Data Converters

USART1
USART2
SPI3
GPIO
JTAG

Certifications

		Comment
FCC ID		In progress
ETSI ID		In progress

General Electrical Specifications

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Absolute Maximum Ratings						
3.3V Supply			-0.3		4.0	V
Vin for 5V tolerant pins			-0.3		5.5	V
Vin for all other pins			-0.3		2.8	V
Operating Conditions and Input Power Specifications						
Operating Temperature Range		Commercial	0		70	°C
		Extended Temperature	-30		85	°C
3.3V Supply	Input Supply Voltage	3.3V Supply input	3.1	3.3	3.6	V
	Standby Mode Current	3.3V, 25°C, SDRAM data retained		15		mA
	Power Save Mode Current	100mS beacon period, 75 byte beacons @ 1Mbps, short Preamble, DTIM = 3		20		mA
	Sleep Current	3.3V 25°C, no data retention, wakeup on events		200		uA
	Active RX w/power save (Note1)	DTIM 1, All beacons Received, no active data (average value)		900		uA
	Idle	Wireless disabled, running full-speed		45		mA
	Average TX Current	Peak, transmitting packets, 3.3V, 25°C		330		mA
	Average RX Current	Peak, Receiving packets, 3.3V, 25°C		125		mA

Note1: Calculated from measurements of each subsection

Digital Interface Specifications

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Digital Interface Specifications, I/O pins						
Inputs	VIH		1.4			V
	VIL		0.6			V
Outputs	VOH	IOH = 4mA	1.8			V
	VOL	IOL = 4mA			.4	V
Programmable Pull Up or Down Resistors		When turned on	80		120	Kohms

RF Characteristics

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
RX Sensitivity (note 2)	11b, 1Mbps			-96		dBm
	11b, 2 Mbps			-93		dBm
	11b, 5.5 Mbps			-91		dBm
	11b, 11 Mbps			-87		dBm
	11g, 9Mbps			-89.5		dBm
	11g, 18Mbps			-86		dBm
	11g, 36Mbps			-80		dBm
	11g, 54Mbps			-74.5		dBm
	11n, MCS1, 13Mbps			-86.5		dBm
	11n, MCS3, 26Mbps			-81.5		dBm
	11n, MCS5, 52Mbps			-74		dBm
	11n, MCS7, 65Mbps			-71		dBm
Channel to Channel De-sensitivity	CH1 to 14	11g, 54Mbps 10% PER		1		dB
Maximum Input Signal	CH7	11g, 54Mbps		-20		dBm
Adjacent Channel Rejection	11Mbps			38		dBc
	9Mbps			20		dBc
	54Mbps			4		dBc
	MCS1			24		dBc
	MCS7			3		dBc
TX Output Power (Note 2)	11b, 1Mbps	@802.11b spectral mask		18.3		dBm
	11b, 11Mbps			18.3		dBm
	11g, 9Mbps	@802.11g spectral mask		18.3		dBm
	11g, 54Mbps	EVM = -27dB, 4.5%		13.7		dBm
	802.11n MCS1	@802.11n spectral mask		18.3		dBm
	802.11n MCS7	EVM = -27dB		13.5		dBm
Antenna Gain		Average		-1.2		dBi

Note 2: Output Power and sensitivities are measured with a 50 ohms connection at the antenna port, antenna removed.

LGA Pin Out and Description

SIGNAL NAME	PIN NUMBER	DESCRIPTION	NOTES
GPIO Pins and alternate SPI functions			
GPIO0_MISO	16	Alternate SPI MISO pin	Input pull down and 5V tolerant
GPIO1_MOSI	17	Alternate SPI MOSI	Input pull down and 5V tolerant
GPIO2_SPICS	19	Alternate SPI Chip Select	Floating and 5V tolerant
GPIO3_SCLK	1	Alternate SPI Clock	Input pull down and 5V tolerant
Reserved Pins for future use			
GPIO4_RXD3	18		
GPIO5_TXD3	20		
GPIO6_ADC0	22		
GPIO7_ADC1	13		
GPIO8_ADC2	4		
GPIO9_ADC3	7		
GPIO11_SCL	11		
GPIO12_SDA	12		
GPIO15_DAC	21		
General purpose with no alternate function			
GPIO10	5	General purpose	Floating and 5V tolerant
GPIO13	15	General purpose	Input pull down and 5V tolerant
GPIO14	14	General purpose	
UART Pins			
RXD1	8	UART Receive data input	5V tolerant
TXD1	6	UART Transmit data output	5V tolerant
CTS1_DN	9	UART Clear to Send input	Active low, 5V tolerant
RTS1_DP	10	UART Request to send output	Active low, 5V tolerant
RESET			
RESETn	3	Reset input (See firmware load description)	Active low for 5ms with pull up to 2.5VDC. Not 5V tolerant.
JTAG Test Pins (NOTE)			
TRST_MISO3	28	JTAG TRST_N, Used for 1M Flash	5V tolerant
TDI	27	JTAG TDI	5V tolerant
TMS	26	JTAG TMS	5V tolerant
TCK	29	JTAG TCK	5V tolerant
TDO_SCK3	30	JTAG TDO, Used for 1M Flash	5V tolerant
SUPPLY Pins and paddle			
3.3V	24	Voltage supply	Decouple with 10uF capacitor
Ground	23	Ground	
Ground Paddle (NOTE)	25	Ground	Add plenty of ground vias for thermal dissipation and ground return
Firmware load Pin access			
BOOT0	2	(See firmware load description)	

NOTE: Pins 26 to 30 and the Module Paddle, labeled Pin 25 are additional pins when compared to available Bluetooth Modules in the market.

Firmware loading pin description

To enable the firmware download, Pin BOOT0 needs to be high during power up. RESETn pin need to be pulled low at least 5ms to initiate the firmware download sequence.
Note: The latest firmware is available at www.sagrad.com for download. Please refer to SG922-0008 document for full description.

Software Features

Contact Sagrad for features that are under development

Supported features
802.11 Stack with WPA
Serial Port Firmware update
Web client
Web Server with dynamic content
DHCP Client
TCP/IP

Features under development
Wireless Firmware update
SSL
Advanced Power Save Modes
Advanced AT Command Set
Note: Updated software releases occur in 4-8 week cycles.

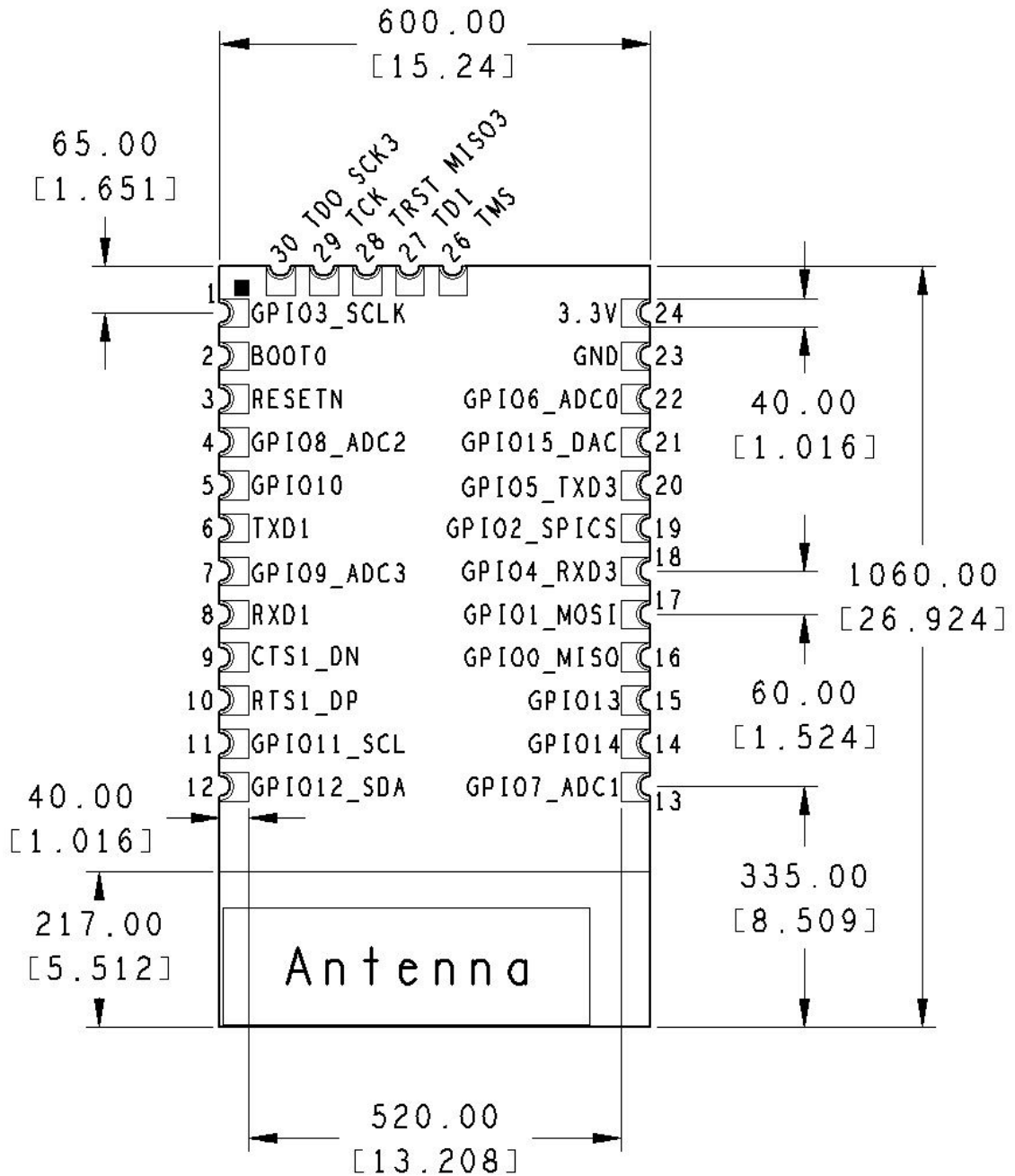| List of available support documents |
| --- |
| SG922-0007 User Manual and Command Reference |
| SG922-0008 Firmware Update Application Note |
| Note: These documents are available at www.sagrad.com for download. |

SW Architecture
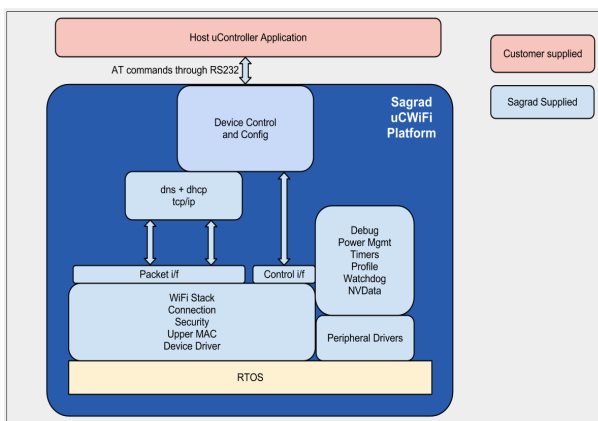
Top View

Dimensions: L: 26.92mm W: 15.24mm H: 2.35mm

NOTE: An antenna area of 217X520 mils need to be free of any ground metallization or traces under the unit. The area extending away from the antenna should be free from metal on the PCB and housing to meet expected performance. Pin 25 is the required paddle ground and is not shown in this diagram.

Recommended Layout
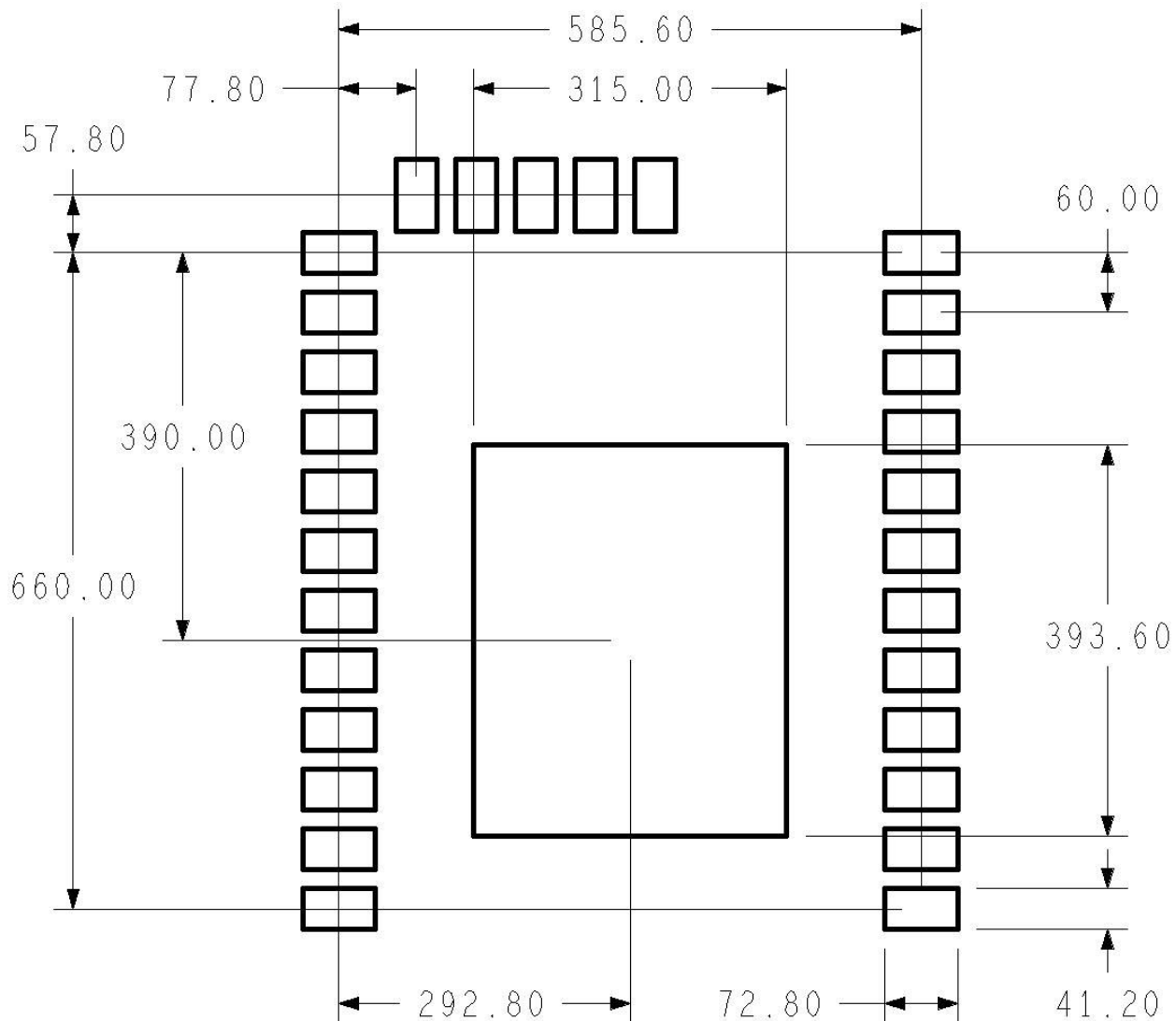
PCB design requires detailed review of center exposed pad. This pad requires good thermal conductivity. Soldering coverage should be maximized and checked via x-ray for proper design. There is a trade off in providing enough soldering for conductivity and too much which allows the module to "float" on the paddle creating reliability issues. Sagrad recommends two approaches, a large center via that allows excess soldering to flow down into the host PCB with smaller vias arount it. Or many smaller vias with just enough space for the viscosity of the chosen solder/flux to allow some solder to flow into the smaller vias. Each of these approaches need to result in 60% or more full contact solder coverage on the paddle after reflow. Sagrad strongly encourages PCB layout teams to work with their EMS providers to ensure vias and solder paste designs will result in satisfactory performance.
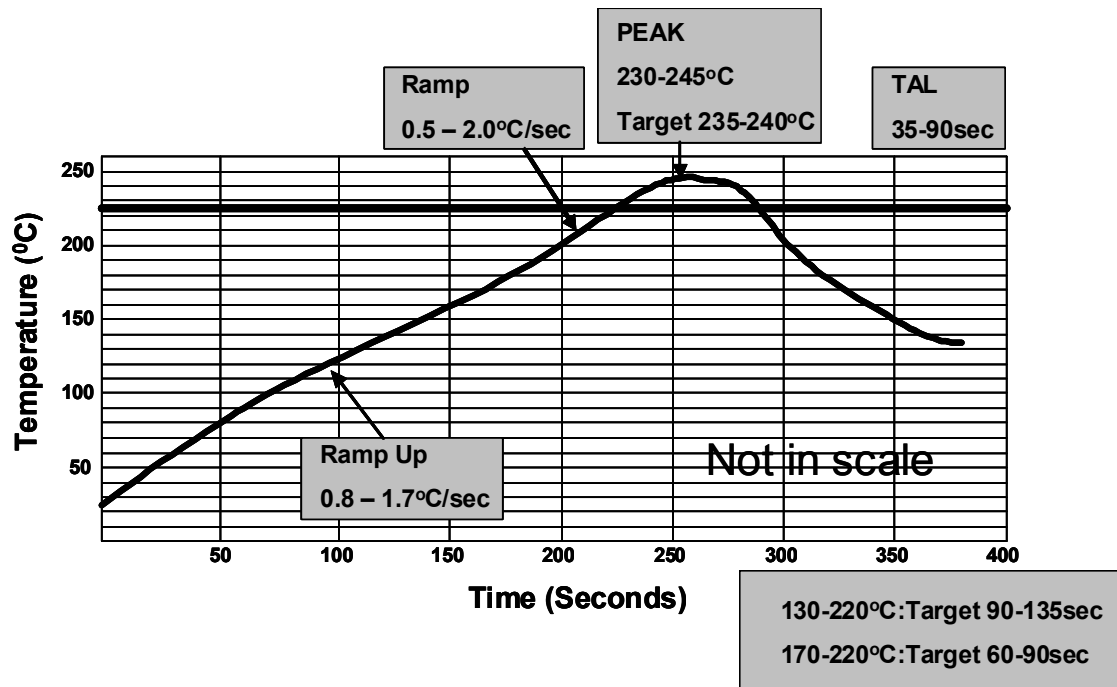
Note: Pin 1 is on the top left corner of this diagram. **See note on the Top View Pin out for antenna to PCB interference requirements for the layout.**

This view is viewed from the top.

Mechanical

- Maximum Peak Reflow Temperature: 240°C
- Recommended Reflow Profile:

Moisture Level Sensitivity: 3

Limiting component for moisture is the PCB used in the module.

Packaging

The part comes packaged in Tape and Reel

4mm   **24mm**   **8mm**

36m   **44mm**

Cover Tape

Media