



SG901-1091 Miniature Wi-Fi Radio

Overview

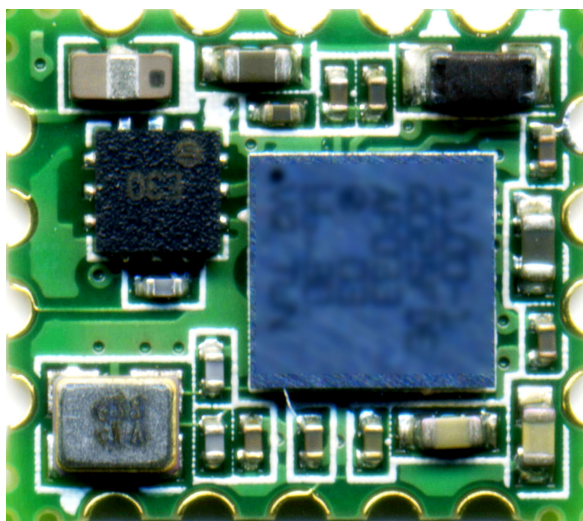
The SG901-1091 WiFi module is optimized to simplify successful integration into systems requiring the latest performance with small size. This module is a highly integrated single chip based 802.11b/g/n WLAN radio for embedded, low-power and extremely small form factor mobile applications. The product conforms to the IEEE 802.11b, g, and n protocols operating in the 2.45GHz ISM frequency band supporting 802.11g/n modulations from 6 to 65Mbps, and 802.11b modulations.

The SG901-1091 is a fully integrated wireless radio including RF Synthesizer/VCO, high-speed data converters, digital baseband processor, onboard MAC and PHY processors, Power Management, and Power Amplifier.

On-chip auto-calibration eliminates unit specific and customer calibration.

An on-board crystal and filter simplify system integration. The addition of 2.3 to 4.8V and 1.8V supplies, Antenna, and host communication provides a complete WiFi solution.

Host control is provided by either an SDIO or SPI interface at 1.8V.



Features

- Ultra Low Current Consumption
- Very Small Footprint (8.5 x 9.5mm)
- Self Calibrated
- Supports SPI and SDIO Interfaces
- RoHs Compliant
- Fully Integrated 802.11 System Solution
- Fully Compliant with the IEEE 802.11 WLAN Standards
- Support for 802.11g/n Modulations up to 65Mbps, and Mandatory 802.11b Modulations
- Intelligent Power Control, Including 802.11 Power Save Mode
- Factory Support for Linux /Android
- Source Code Available for porting to RTOS or Custom OS
- Industrial Temperature -40 to +85C
- Contact Factory for Regulatory compliant applications

Applications

- Hand-held Devices
- Embedded Systems
- Portable Systems
- Point of Sale terminals
- Personal Digital Assistants (PDA)
- Cameras
- Cable Replacement

Ordering Information

Packaging	Temp Range	Part Number
Tape and Reel	Industrial	SG901-1091-ET-TR
Bulk	Industrial	SG901-1091-ET-BLK
Tape and Reel	Commercial	SG901-1091-CT-TR
Bulk	Commercial	SG901-1091-CT-BLK

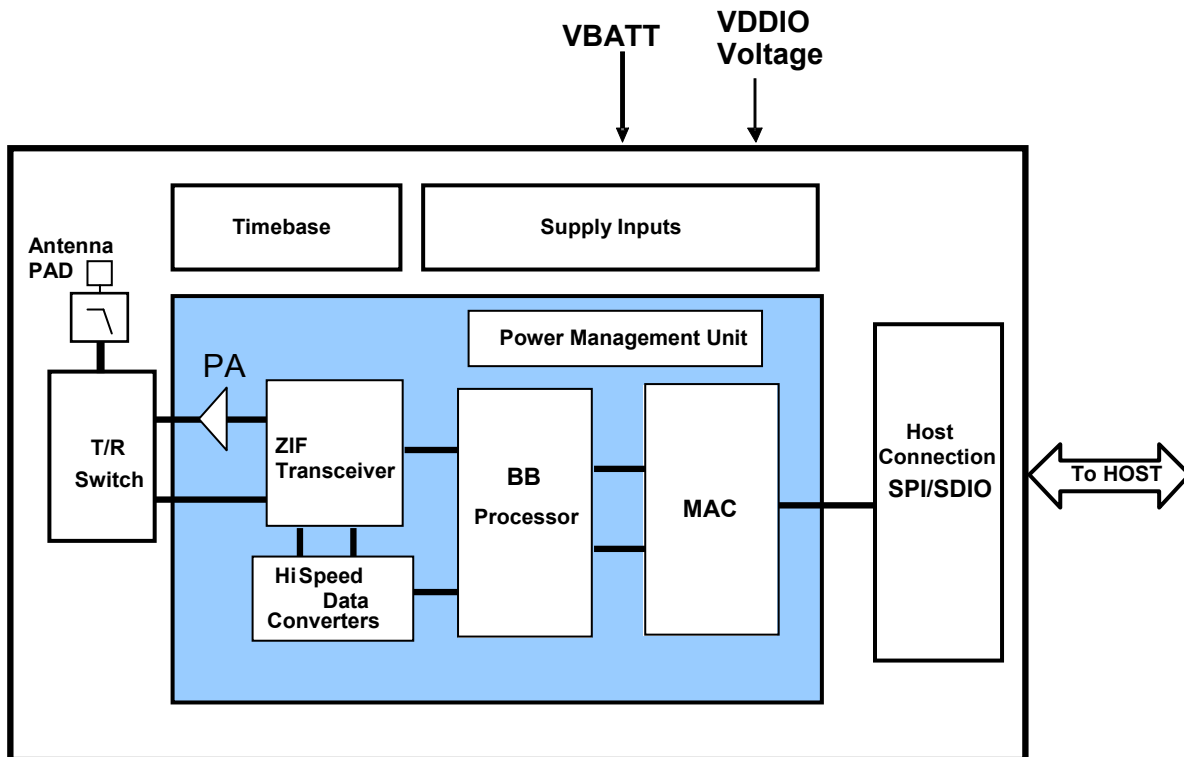
Evaluation Kit Available

This EVK supports embedded software development.

EVK for 1091	SG923-0010
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Block Diagram



Standards Performance

Standards Support	
Modulations	b/g/n Modulations
Power Save	802.11e/WMM/WMM-PS
Encryption	802.11i/WPA/WPA2
Resources	802.11k
Regulatory Support	802.11d
Fast BSS Transition	802.11r
Protected Frames	802.11w
Direct Connect	Wi-Fi Direct



General Electrical Specifications

Parameter	Test Condition / Comment	Min.	Typ.	Max.	Units	
Absolute Maximum Ratings						
VBAT Supply		-0.3		5.5	V	
VDDIO Supply		-0.3		2.5	V	
Operating Conditions and Input Power Specifications						
Operating Temperature Range		-40		85	°C	
VBAT Supply	Input Supply Voltage	2.3	3.6	4.8	V	
	Sleep Mode Current		80		uA	
	Power Save Mode Current	DTIM = 1	0.87		mA	
	Peak TX Current	14.5dBm		294	mA	
	Peak RX Current	Processing OFDM		75	mA	
VDDIO Supply	Input Supply Voltage	VHIO input supply determines Host CMOS logic levels	1.65	1.8	1.95	V
	Input Supply Current	RX Active, processing OFDM		0.87	mA	
	Sleep Mode Current			25	uA	
Input Voltage Levels	VIL			0.35VDDIO	V	
	VIH		0.625VDDIO		V	
Output Voltage Levels	VOL	IOL = 100uA		0.2	V	
	VOH	IOH = -100uA	VDDIO-0.2	VDDIO	V	

RF Characteristics

Parameter	Test Condition / Comment	Min.	Typ.	Max.	Units
Antenna Port Impedance			50		Ohms
Antenna Input Return Loss	CH1 to CH14		-11		dB
RX Sensitivity	11b, 1Mbps		-96		dBm
	11b, 2 Mbps		-93		dBm
	11b, 5.5 Mbps		-91		dBm
	11b, 11 Mbps		-87		dBm
	11g, 9Mbps		-89.5		dBm
	11g, 18Mbps		-86		dBm
	11g, 36Mbps		-80		dBm
	11g, 54Mbps		-74.5		dBm
	11n, MCS1, 13Mbps		-86.5		dBm
	11n, MCS3, 26Mbps		-81.5		dBm
	11n, MCS5, 52Mbps		-74		dBm
11n, MCS7, 65Mbps		-71		dBm	
Channel to Channel De-sensitivity	CH1 to 14	11g, 54Mbps 10% PER	1		dB
Maximum Input Signal	CH7	11g, 54Mbps	-20		dBm



RF Characteristics cont,

Parameter		Test Condition / Comment	Min.	Typ.	Max.	Units
Adjacent Channel Rejection	11Mbps			38		dBc
	9Mbps			20		dBc
	54Mbps			4		dBc
	MCS1			24		dBc
	MCS7			3		dBc
TX Output Power	11b, 1Mbps	@802.11b spectral mask		18.3		dBm
	11b, 11Mbps			18.3		dBm
	11g, 9Mbps	@802.11g spectral mask		18.3		dBm
	11g, 54Mbps	EVM = -27dB, 4.5%		13.7		dBm
	802.11n MCS1	@802.11n spectral mask		18.3		dBm
	802.11n MCS7	EVM = -27dB		13.5		dBm

Pinout List

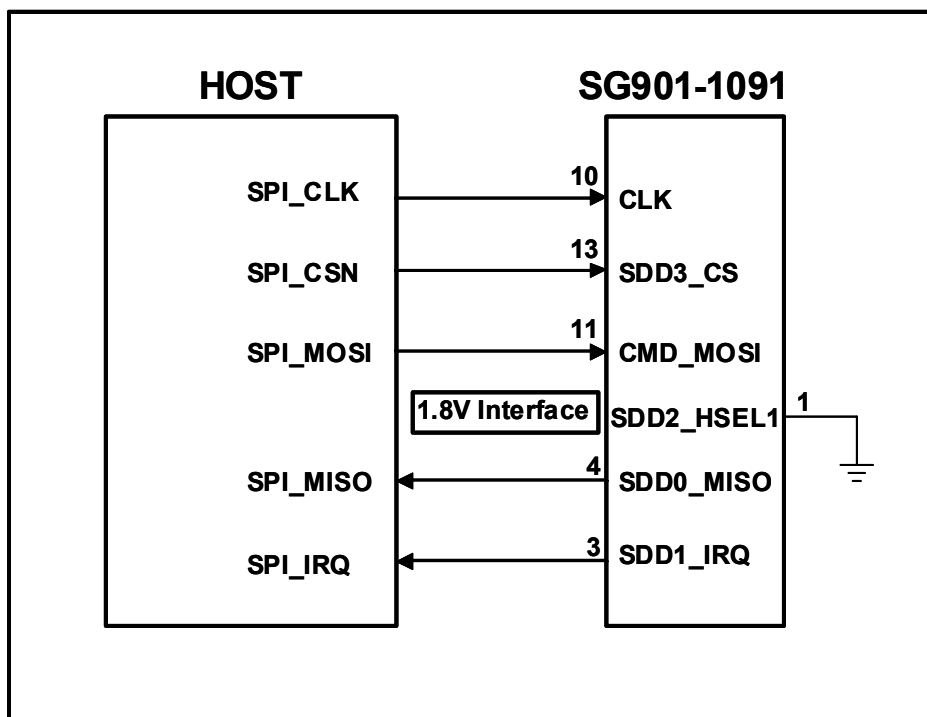
SIGNAL NAME	PIN NUMBER	DESCRIPTION	NOTES
RF Pin			
2G4_RF	6	Wi-Fi / Bluetooth Antenna Port, 50 ohms	Careful RF design is needed for this and nearby ground
Serial Interface Pins (VDDIO Domain, logic levels compatible with the VDDIO (Pin 18) input voltage)			
CMD_MOSI	11	SPI MOSI (input)	SDIO CMD VDDIO Domain
CLK	10	SPI Clock Input	SDIO CLK VDDIO Domain
SDD0_MISO	4	SPI MISO (output)	SDIO Data 0 VDDIO Domain
SDD1_IRQ	3	SPI: Interrupt Output	SDIO Data 1 VDDIO Domain, Push-Pull. Indicates an interrupt on the going rising edge
SDD2_HSEL1	1		SDIO Data 2 VDDIO Domain- at reset, low selects SPI, high SDIO
SDD3_CS	13	SPI Chip Select Input	SDIO Data 3 VDDIO Domain, Active Low
Control Pins			
POWERUP	14	Power Up Enable (from Host)	VDDIO Domain with internal pull up High = operating, Low = off
RSTn	2	Reset Input	VDDIO Domain – Active Low reset. At power up , RSTn must be held LOW until at least 2 cycles of the SLEEPCLK have been initiated.
SLEEPCLK	16	32.768 kHz Sleep Clock Input	VDDIO Domain, Required for proper operation
FEM_CTRL1	12	programmable	diversity switch control
FEM_CTRL2	9	programmable	diversity switch control
DBG_RXD	15	Debug UART	VDDIO Domain, Factory tests only
DBG_TXD	17	Debug UART	VDDIO Domain, Factory tests only
Power and Ground Pins			
VDDIO	18	Supply Voltage for I/O's	1.8V, Internally decoupled with a 0.1uF capacitor
VBAT	8	RF supply	2.3 to 4.8V, Internally decoupled with a 4.7uF capacitor
GND	5, 7, 19	Ground Connections	
SPI functions in MODE 3. Clock data in and out at the rising edge. CLK is idle at HIGH.			



SG901-1091 SPI/SDIO Interfaces

The SPI/SDIO interface for the SG901-1091 is a 5-wire low voltage interface depicted in figure 1. SDD2_HSEL1 pin High/Active or grounded defines the interface type.

Figure 1: Host Interfacing Block Diagram



SPI Interface

The five signals of the SG901-1091 SPI interface are as follows:

- SDD3_CS: Device select allows the use of multiple slaves from a Host. (1 device select per slave). This signal is active low. Signal is mandatory, even with only one slave because the Host must drive this signal to indicate SPI frames.
- CLK: Clock signal, active for multiple data length cycles during a SPI transfer (SDD3_CS active). The clock is allowed to be active when SDD3_CS is not active, in order to serve other possible slaves.
- SDD0_MISO: Data transfer from SG1091 to Host. Data is generated on the negative edge of CLK by the SG1091 and sampled on the positive edge of CLK. When SDD3_CS is inactive, SDD0_MISO is in Tri-state mode.
- CMD_MOSI: Data transfer from Host to SG1091. Data is generated on the negative edge of CLK by the Host and sampled on the positive edge of CLK.
- SDD1_IRQ: Interrupt from the SG1091, used to request a SPI transfer to the Host. This signal is active High (Host input must be level sensitive).



The SG901-1091 SPI interface has the following characteristics:

- Maximum operating frequency of 52MHz.
- The SPI interface operates in Half Duplex Mode.
- Host is the Master and the SG1091 is the slave
- The SPI data length, endianness and flow control are configurable. The Host can change the configuration by writing in the SPI configuration register
- 16 and 32 bits word lengths are supported including the following configurable modes, where [bn] is the bit transmission order from left to right:
 - 32-bit Mode0:[b15-b8], [b7-b0], [b31-b24], [b23-b17]
 - 32-bit Mode1:[b31-b24], [b23-b17], [b15-b8], [b7-b0]
 - 32-bit Mode2:[b7-b0], [b15-b8], [b23-b17], [b31-b24]
 - 16-bit Mode0:[b15-b8], [b7-b0]
 - 16-bit Mode1:[b7-b0], [b15-b8]
- The rising clock edge is used for sampling. Active clock edge for shifting is configurable (rise/fall)
- Supports automatic indirect addressing of device internal memory via fixed address SPI register to facilitate bulk DMA transfer
- Support Host wake up of the WLAN block by SPI register access
- The default WLAN configuration is: (refer to figures 2 and 3)
 - 32 bit data length
 - Most significant byte First, default is little Endian
 - Most significant bit First
 - Flow control on SDD0_MISO and in a register

Figure 2: Default SPI transfer from Host to the SG901-1091

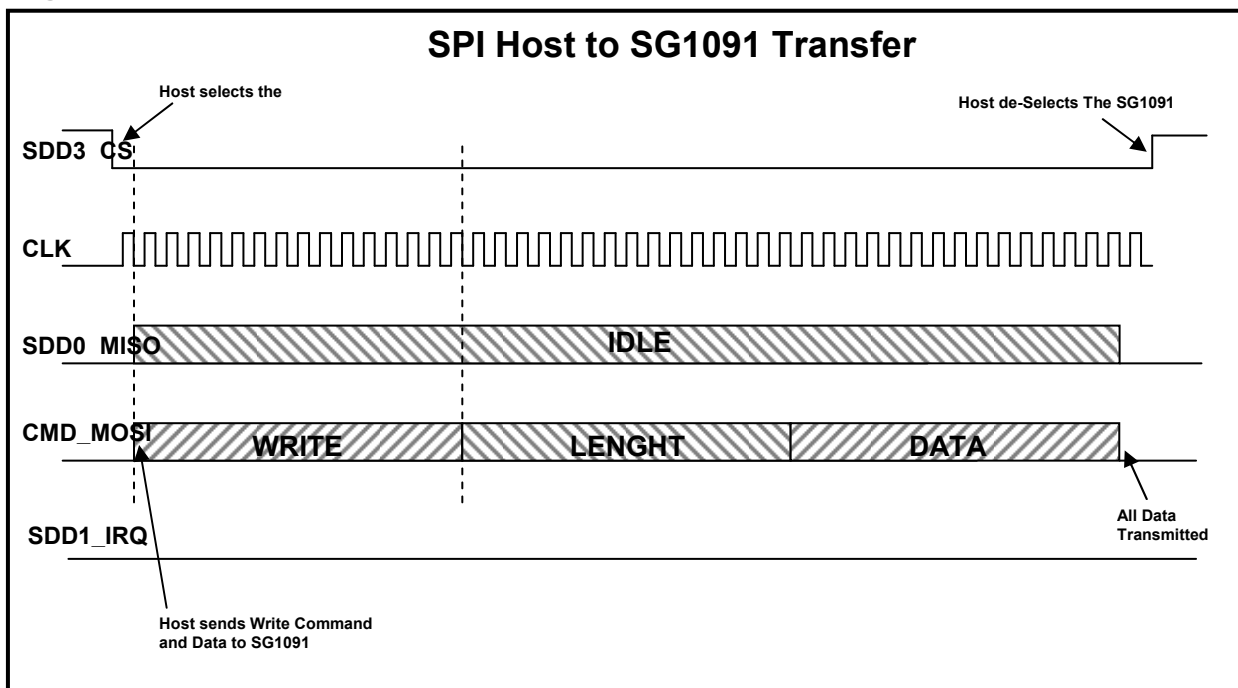
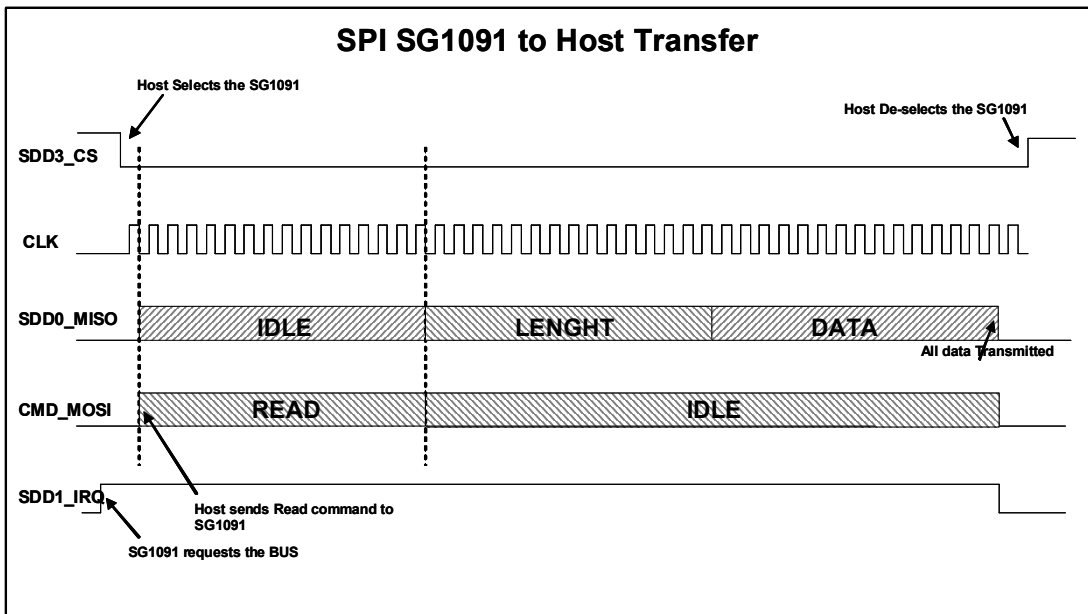




Figure 3: Default SPI data transfer form the SG901-1091 to the Host



SPI Timing Parameters. Refer to figure 4

Symbol	Description	Min.	Typ.	Max.	Units
T1	Clock Period	19.23			ns
T2, T3	Clock High and Low duration	$(0.45 \cdot T1) - T4$		$(.55 \cdot T1) - T4$	ns
T4, T5	Clock rise and fall time (10 TO 90%)	1		2.5	ns
T6	Input Set Up time (CMD_MOSI TO CLK active edge)	5		-	ns
T7	Input Hold time (CLK active edge to CMD_MOSI Invalid)	5			ns
T8	Output Set Up time (CLK active edge to SDD0_MISO Valid)			14.23	ns
T9	Output Hold time (CLK active edge to SDD0_MISO Invalid)	5			ns
T10	SDD3_CS to CLK (SDD3_CS fall to 1 st CLK rising edge)	5			ns
T11	CLK to SDD3_CS (Last falling edge of CLK to SDD3_CS rising edge)	1			ns

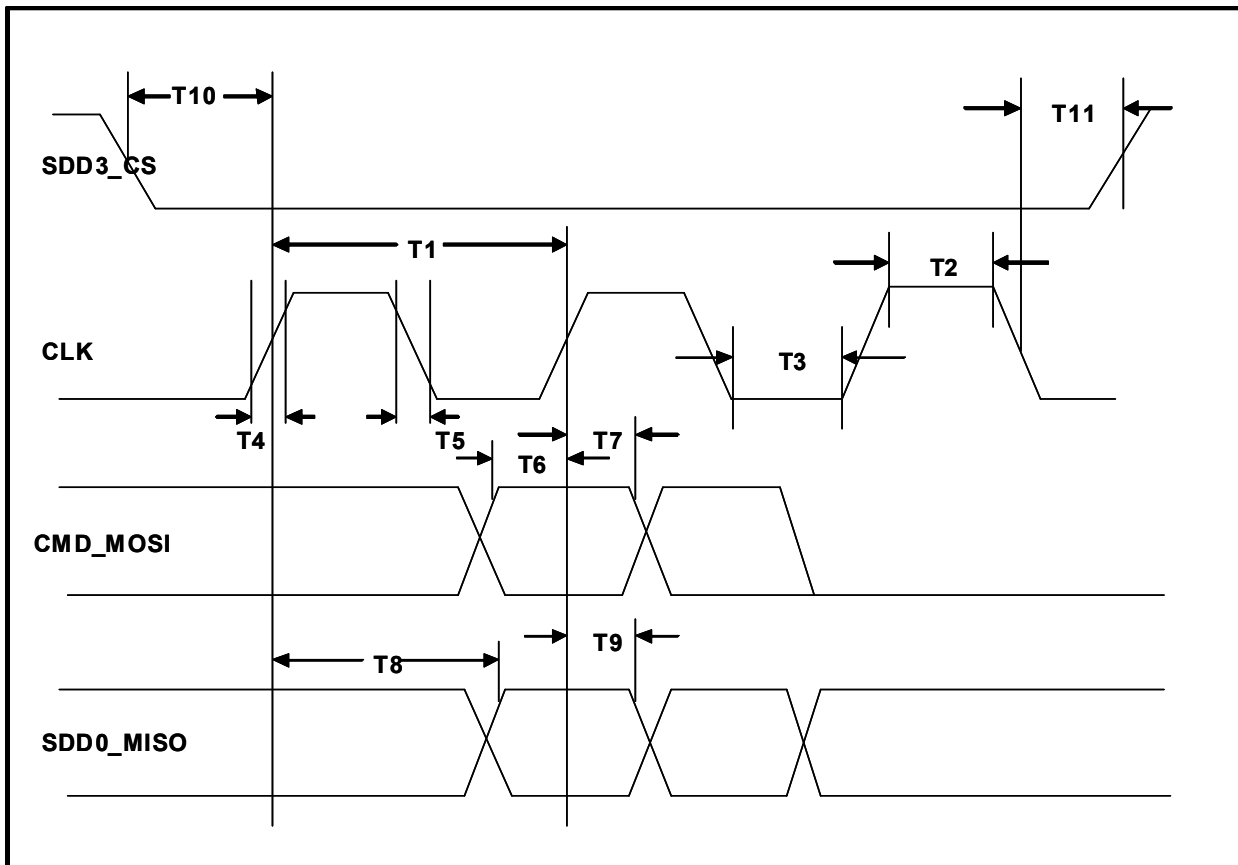


Figure 4: SPI Timing diagrams

SDIO Interface

The SG901-1091 SDIO interface has the following characteristics:

- Maximum operating frequency of 26MHz.



- The SDIO interface is a 4 to 6 wire data interface
- Compatible with the SDIO specification Version 1.10, except that the voltage range is not SD compatible, but is compatible with the standard I/O levels defined in this data sheet
- Interrupt may be generated to the host in 4 bit SDIO mode even without the SDIO clock.
- The SDIO is master at the Host side and Slave at the 1091 side
- Operation in SD mode from 1 to 4 data bits
- The 6 signals are as follows:

CLK: clock signal

CMD_MOSI: Bidirectional SDIO command line

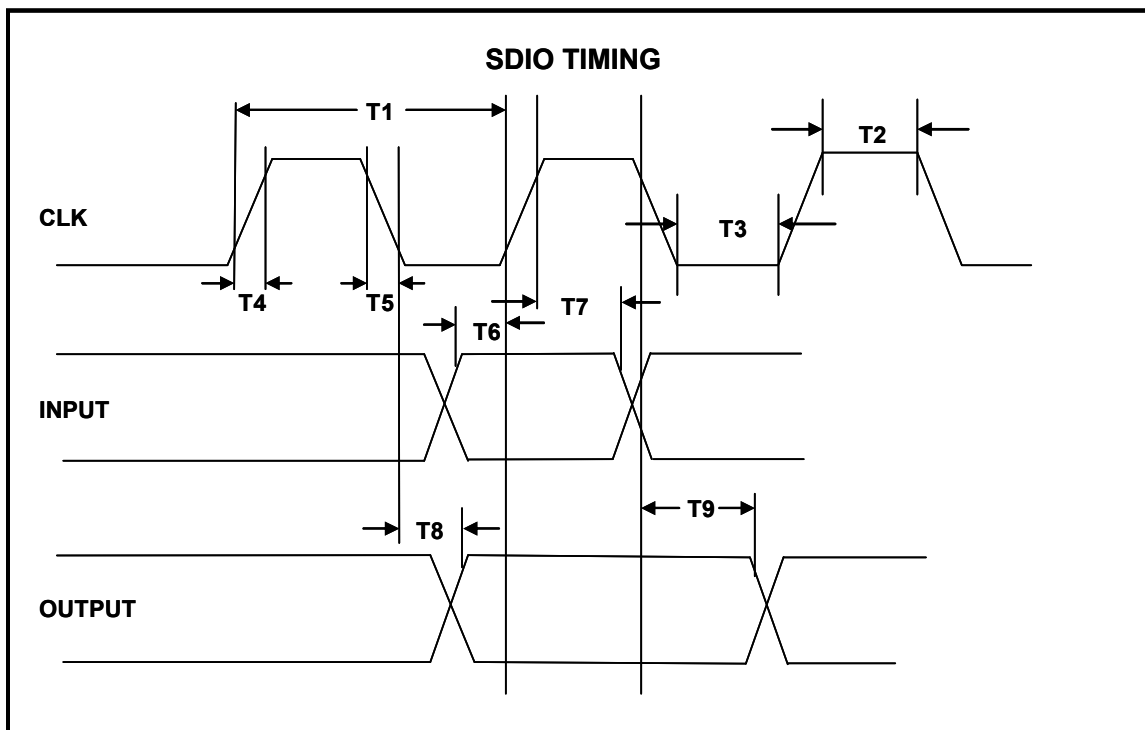
SDD0_MISO: Bidirectional data line

SDD1_IRQ: Bidirectional data line. When no data is present on this line, it is used as an interrupt from the 1091, used to request an SDIO transfer from the 1091 to the host

SDD2_HSEL1: Optional Bidirectional data line

SDD3_CS: Optional Bidirectional data line

Figure 5: SDIO Timing Diagram



SDIO Interface timing. Refer to figure 5

Symbol	Description	Min.	Typ.	Max.	Units



T1	Clock Period	38.46			ns
T4, T5	Clock Rise and Fall Time (10 to 90%)			9	ns
T2, T3	Clock High and Low Time	10			ns
T6, T7	Input Set Up and Hold Time (CMD_MOSI TO CLK active edge)	5		-	ns
T8, T9	Output Delay Time during data transfer mode			14	ns

WLAN Power Up/Down Sequence

The 1091 Power up sequencing is as follows:

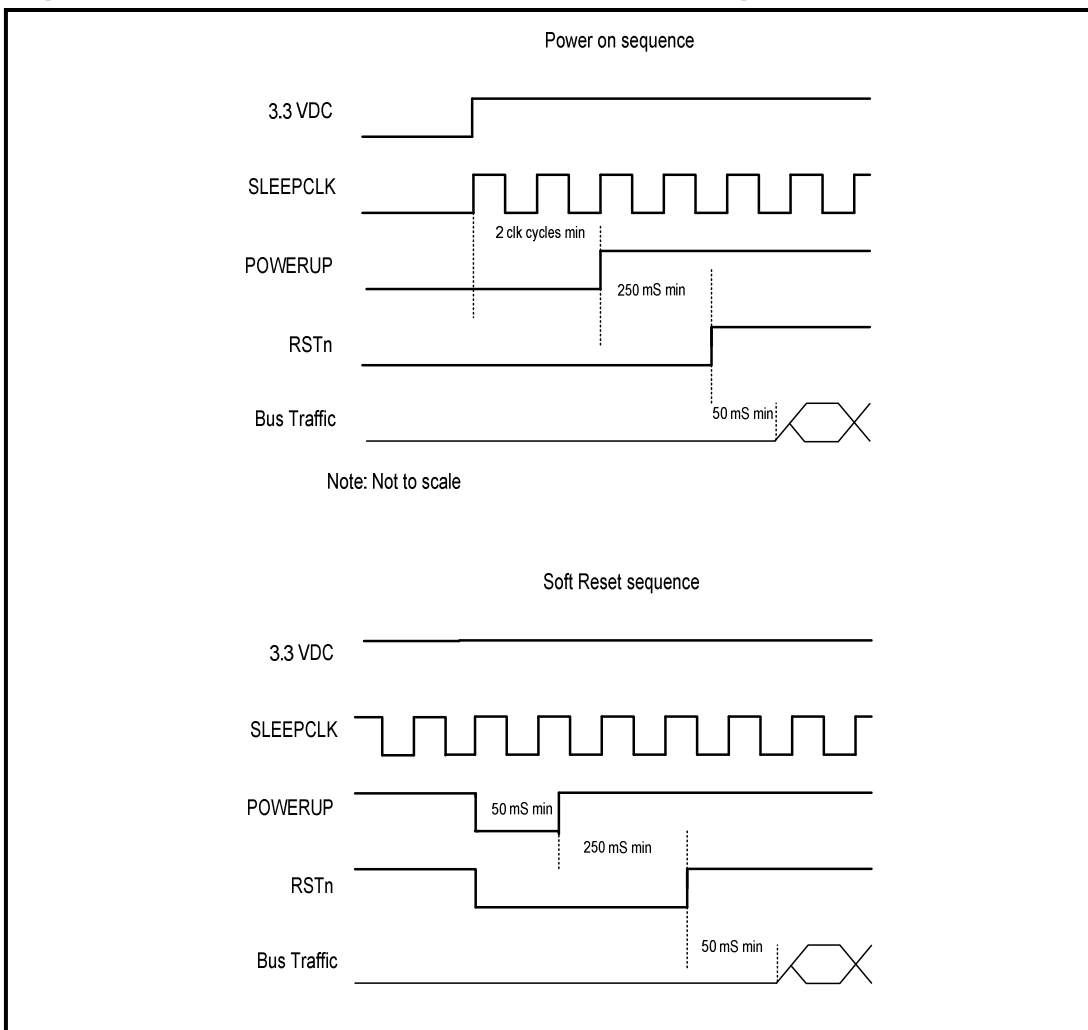
- VDDIO is applied
- SLEEPCLK (low power clock) is stable
- RSTn pin is released after at least two SLEEPCLK cycles
- POWERUP is asserted. Internal supplies stabilize within 20ms
- The Host must wait 30ms after RSTn release for all internal supplies to stabilize
- The device is then in sleep mode
- The Host shall then wake the module by writing over the Host interface, SPI or SDIO the WUP bit
- The module requests the reference clock already running
- The module will assert the RDY bit and assert the interrupt request to the Host
- The Host can now download the firmware and release the by further SPI/SDIO write
- The Host will wait for the Module to initialize and can clear the WUP bit
- Once initialized including a series of messages between the Host and the module, the Module may not have anything further to do and will enter the sleep state

The 1091 power down has no constraints. It is recommended that the Host activates the RSTn at least 2 cycles of the SLEEPCLK before powering off the supplies.

Figure 6 depicts the power up and down timing diagrams.



Figure 6. Power On and Off sequence diagrams



Software Support

The Wi-Fi module is supported via two different software stacks: 1) a Linux device driver (GPL License) that integrates with the Linux mac80211 layer and existing usermode tools, and 2) a phone-handset-oriented chipset-vendor supplied software stack that is available for customers with non-GPL requirements.

In both cases a license is required to distribute the chipset MAC firmware binary.

Linux Stack Features:

- Client mode
- Mini-AP mode (max 5 clients)
- Security: All standard modes (note: all packet encryption handled in MAC hardware)
 - Open System,
 - WEP,
 - WPA (TKIP) PSK and Enterprise, and
 - WPA2 (AES) PSK and Enterprise



- QoS
- OS Support: Linux v2.6 and 3.0, Android
- License: GPL

Vendor Stack Features:

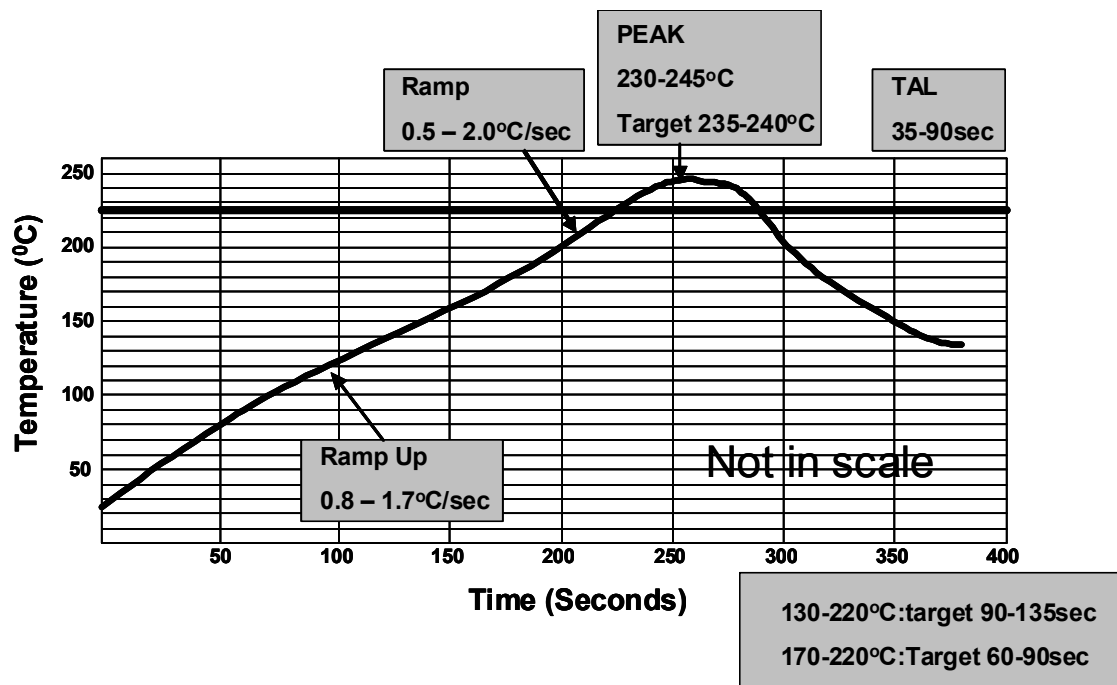
- Client mode
- Mini-AP mode (max 5 clients)
- Security: All standard modes (note: all packet encryption handled in MAC hardware)
 - Open System,
 - WEP,
 - WPA (TKIP) PSK and Enterprise, and
 - WPA2 (AES) PSK and Enterprise
- QoS
- OS Support: Linux v2.6, Android, portable codebase
- License: chipset-vendor SLA

The complete 802.11 stack requires about 350KB of space for the implementation of the entire specification. Extremely small versions can be created by knowledgeable customers but is a considerable task and requires detailed understanding of 802.11.

As a service to customers, Sagrad offers extended technical support on a fee basis.

Mechanical

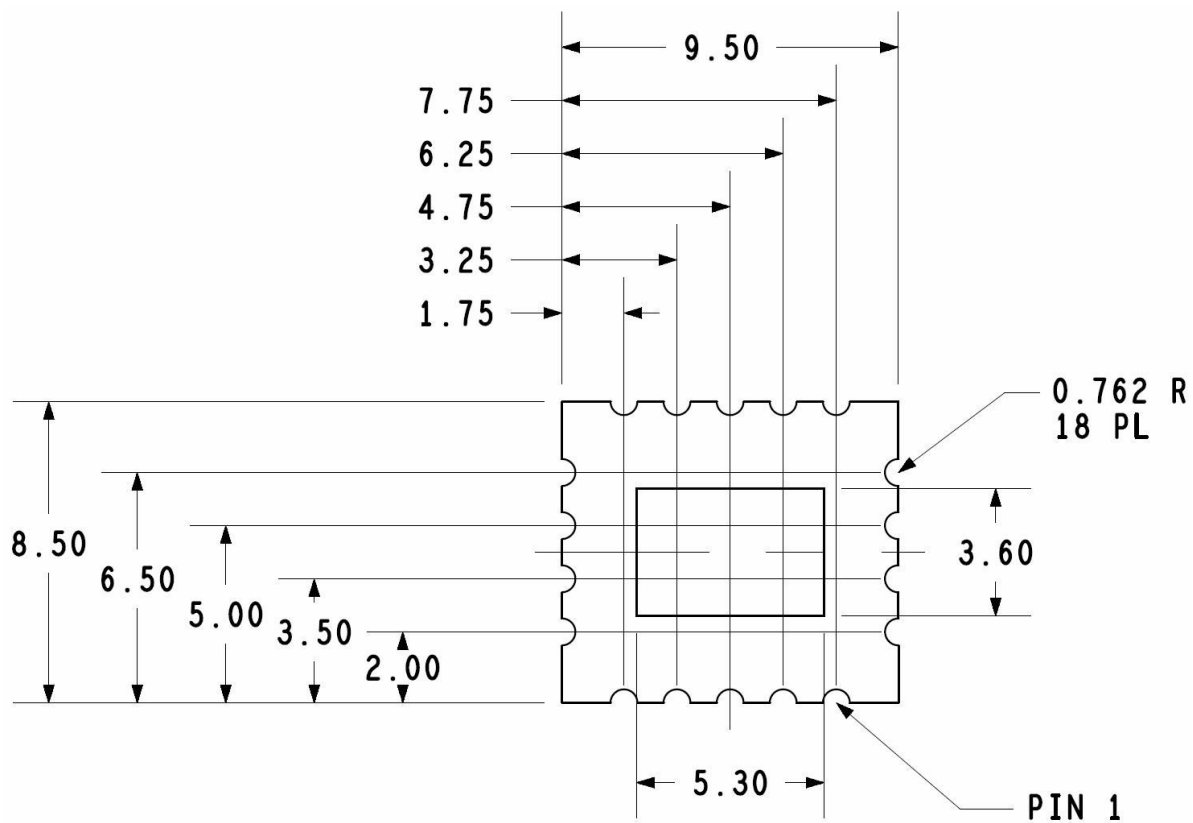
- Maximum Peak Reflow Temperature: 240°C
- Recommended Reflow Profile:



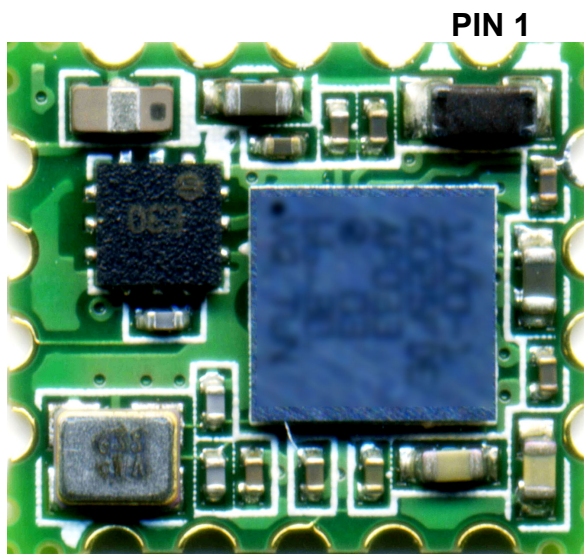
Moisture Level Sensitivity : 3



Mechanical (Bottom View)

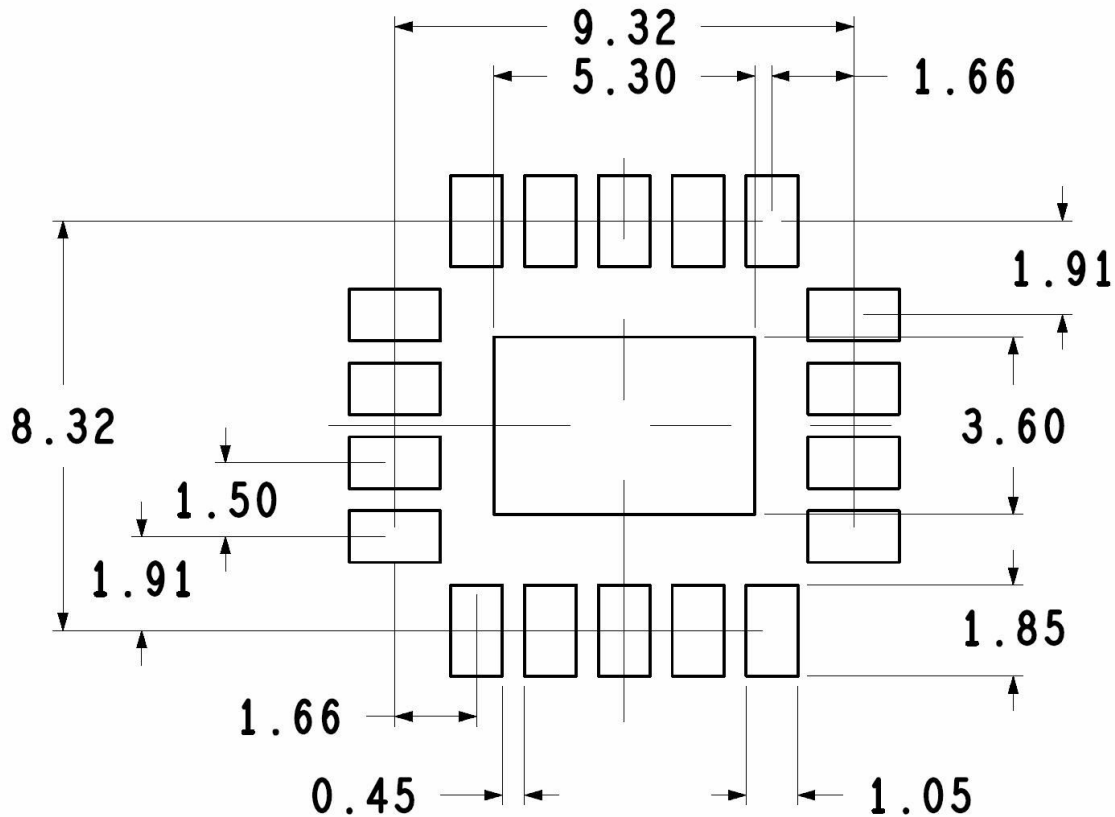


The nominal size of the part is 8.5x9.5mm with a height of 1.3 mm
Pin 1 is identified by a white silkscreen mark around the cut out in the top view of the device





Recommended Layout Pads (Top View)



PCB design requires detailed review of the center exposed pad. This pad requires good thermal conductivity. Soldering coverage should be maximized and checked via x-ray for proper design. There is a trade off in providing enough solder for conductivity, and too much which allows the module to "float" on the paddle creating reliability issues. Sagrad recommends two approaches, a large center via that allows excess soldering to flow down into the host PCB with smaller vias around it. Or many smaller vias with just enough space for the viscosity of the chosen solder/flux to allow some solder to flow into the smaller vias. Each of these approaches need to result in 60% or more full contact solder coverage on the paddle after reflow. Sagrad strongly encourages PCB layout teams to work with their EMS providers to insure vias and solder paste designs will result in satisfactory performance.

Packaging

The part comes packaged in Tape and Reel or Bulk.