3A, 18V, 800kHz Synchronous Step-Down Converter

General Description

The RT7297C is a high efficiency, monolithic synchronous step-down DC/DC converter that can deliver up to 3A output current from a 4.5V to 18V input supply. The RT7297C's current mode architecture and external compensation allow the transient response to be optimized over a wide input voltage range and loads. Cycle-by-cycle current limit provides protection against shorted outputs, and soft-start eliminates input current surge during start-up. The RT7297C also provides under voltage protection and thermal shutdown protection. The low current (<3μA) shutdown mode provides output disconnection, enabling easy power management in battery-powered systems. The RT7297C is available in an SOP-8 (Exposed Pad) package.

Marking Information

RT7297Cx ZSPYMDNN •	RT7297CxZSP : Product Number x : H or L YMDNN : Date Code

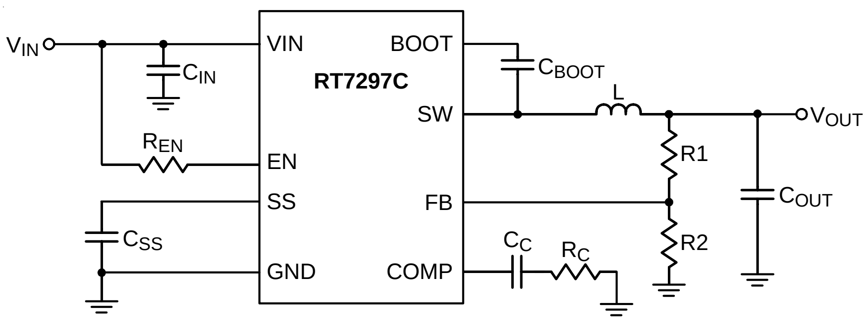
Features

- **±1.5% High Accuracy Reference Voltage**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **Integrated N-MOSFET Switches**
- **Current Mode Control**
- **Fixed Frequency Operation : 800kHz**
- **Output Adjustable from 0.8V to 12V**
- **Up to 95% Efficiency**
- **Programmable Soft-Start**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection**
- **Thermal Shutdown Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Wireless AP/Router
- Set-Top-Box
- Industrial and Commercial Low Power Systems
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation of High-Performance DSPs

Simplified Application Circuit



Ordering Information

RT7297C□□□

Package Type
SP : SOP-8 (Exposed Pad-Option 2)

Lead Plating System
Z : ECO (Ecological Element with Halogen Free and Pb free)

H : UVP Hiccup
L : UVP Latch-Off

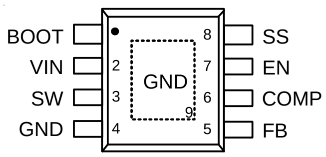
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)

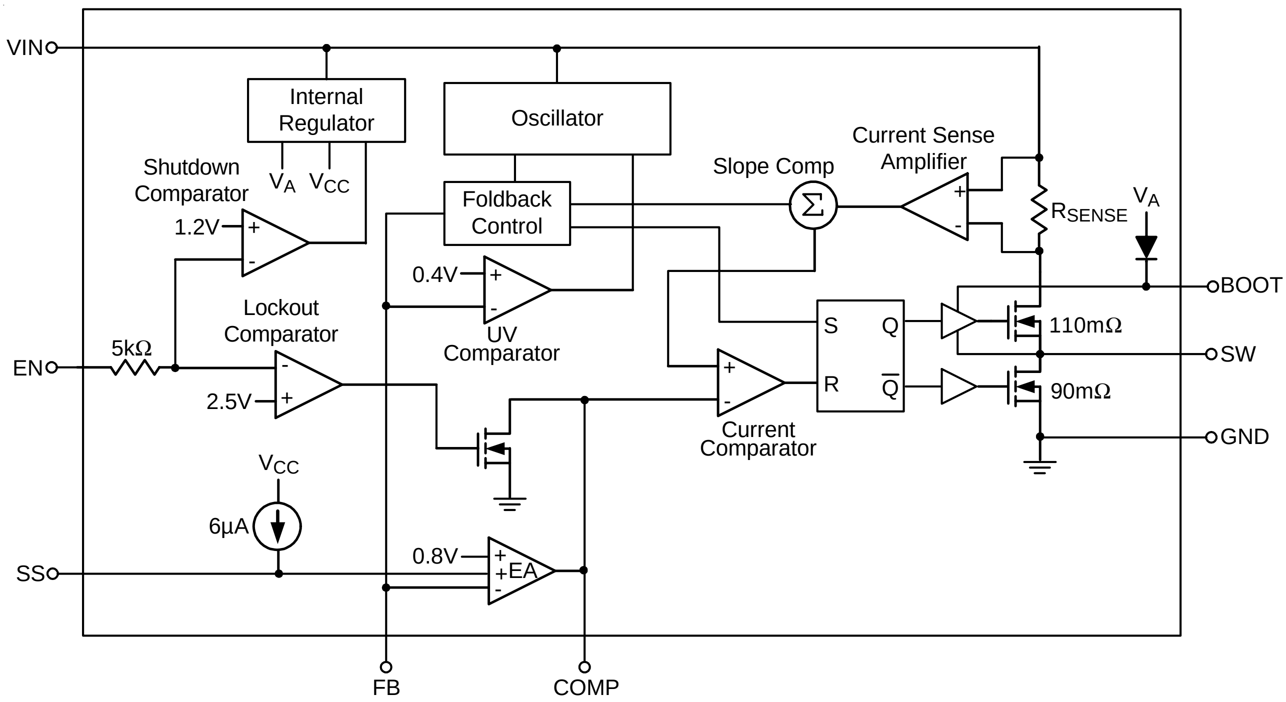


SOP-8 (Exposed Pad)

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
2	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitable large ceramic capacitor.
3	SW	Switch Node. Connect this pin to an external L-C filter.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	FB	Feedback Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input. A logic high enables the converter; a logic low forces the converter into shutdown mode reducing the supply current to less than 3μA. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 13.5ms.

Function Block Diagram



Operation

Shutdown Comparator

Activate internal regulator once EN input level is larger than the target level. Force IC to enter shutdown mode when the EN input level is lower than 0.4V.

Internal Regulator

Provide internal power for logic control and switch gate drivers.

Lockout Comparator

Activate the current comparator, release lock-out logic, and enable the switches as EN input level is larger than lockout voltage. Otherwise, the switches still locks out.

Oscillator

The oscillator provides internal clock and controls the converter's switching frequency.

Foldback Control

Dynamically adjust the internal clock. It provides a slower frequency as a lower FB voltage.

UV Comparator

As FB voltage is lower than the UV voltage, it will activate a UV protect scheme.

Error Amplifier

The output voltage COMP of the error amplifier is adjusted comparing FB signal with the internal reference voltage and SS signal.

Current Sense Amplifier

R_{SENSE} detects the peak current of the high side switch. This signal is amplified by the current sense amplifier and added with a slope compensation signal. Then, It controls the switches by comparing this signal with the COMP voltage.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- $-0.3V$ to $20V$
- Switch Voltage, SW ---------- $-0.3V$ to $(V_{IN} + 0.3V)$
- $V_{BOOT} - V_{SW}$ ---------- $-0.3V$ to $6V$
- Other Pins Voltage ---------- $-0.3V$ to $20V$
- Power Dissipation, P_D @ $T_A = 25°C$
  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- $-65°C$ to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- $-40°C$ to 125°C
- Ambient Temperature Range ---------- $-40°C$ to 85°C

Electrical Characteristics

($V_{IN} = 12V$, $T_A = 25°C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current		$V_{EN} = 0V$	--	0.5	3	μA
Supply Current		$V_{EN} = 3V$, $V_{FB} = 0.9V$	--	0.8	1.2	mA
Reference Voltage	V_{REF}	$4.5V \le V_{IN} \le 18V$	0.788	0.8	0.812	V
Error Amplifier Transconductance	G_{EA}	$\Delta I_C = \pm 10\mu A$	--	940	--	μA/V
High Side Switch On-Resistance	$R_{DS(ON)1}$		--	110	--	mΩ
Low Side Switch On-Resistance	$R_{DS(ON)2}$		--	90	--	mΩ
High Side Switch Leakage Current		$V_{EN} = 0V$, $V_{SW} = 0V$	--	0	10	μA
Upper Switch Current Limit		Min. Duty Cycle, $V_{BOOT} - V_{SW} = 4.8V$	--	5.1	--	A
COMP to Current Sense Transconductance	G_{CS}		--	5.1	--	A/V
Oscillation Frequency	f_{OSC1}		--	800	--	kHz
Short Circuit Oscillation Frequency	f_{OSC2}	$V_{FB} = 0V$	--	270	--	kHz
Maximum Duty Cycle	D_{MAX}	$V_{FB} = 0.7V$	--	84	--	%
Minimum On-Time	t_{ON}		--	100	--	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Enable Threshold (Rising)	V_{EN_H}		2.3	2.52	2.7	V
Output Enable Hysteresis	V_{EN_Hys}		--	210	--	mV
Input Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	3.8	4.2	4.5	V
Input Under Voltage Lockout Hysteresis	ΔV_{UVLO}		--	320	--	mV
Soft-Start Current	I_{SS}	V_{SS} = 0V	--	6	--	μA
Soft-Start Period	t_{SS}	C_{SS} = 0.1μF	--	13.5	--	ms
Thermal Shutdown	T_{SD}		--	150	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

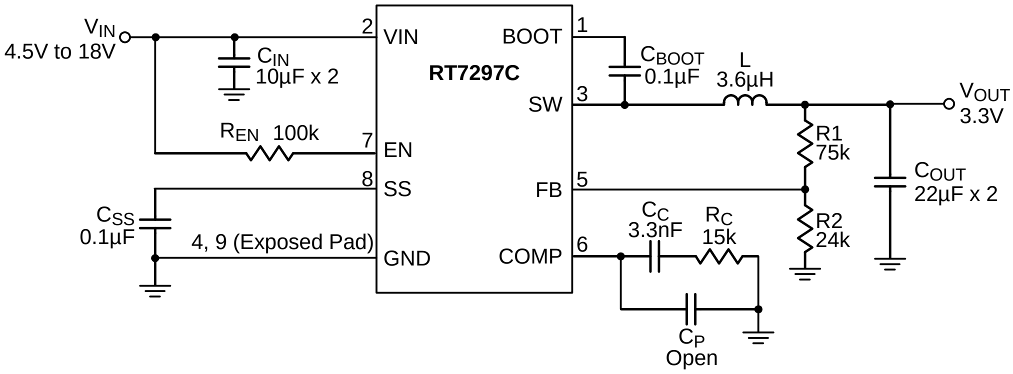
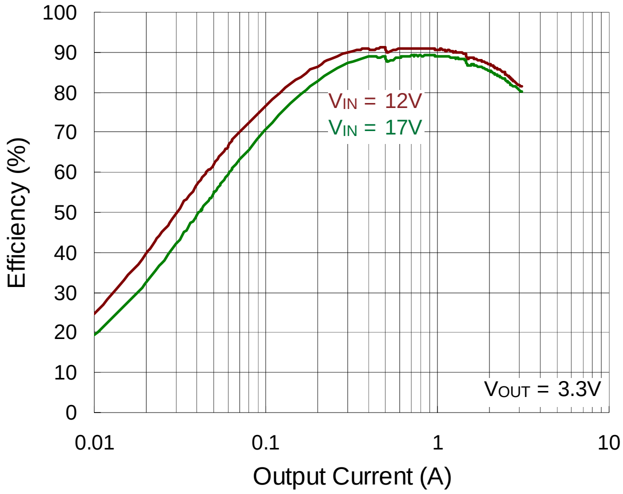


Table 1. Suggested Component Selection

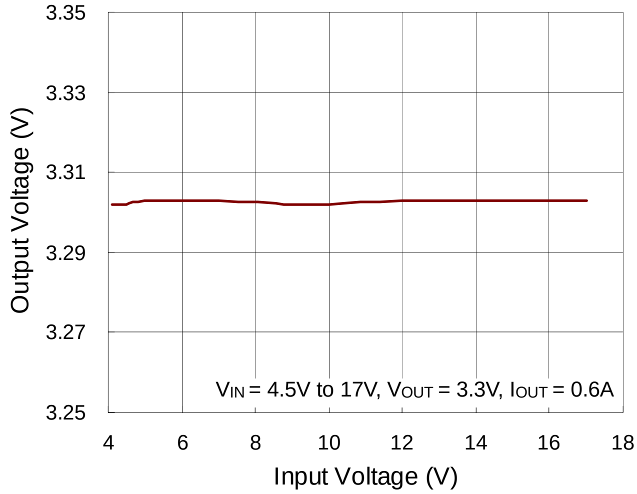
V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L (µH)	C_{OUT} (µF)
8	27	3	35	3.3	10	22 x 2
5	62	11.8	20	3.3	6.8	22 x 2
3.3	75	24	15	3.3	3.6	22 x 2
2.5	25.5	12	10	3.3	3.3	22 x 2
1.8	15	12	7	3.3	2.2	22 x 2
1.2	12	24	5	3.3	1.5	22 x 2
1	3	12	4	3.3	1.5	22 x 2

Typical Operating Characteristics

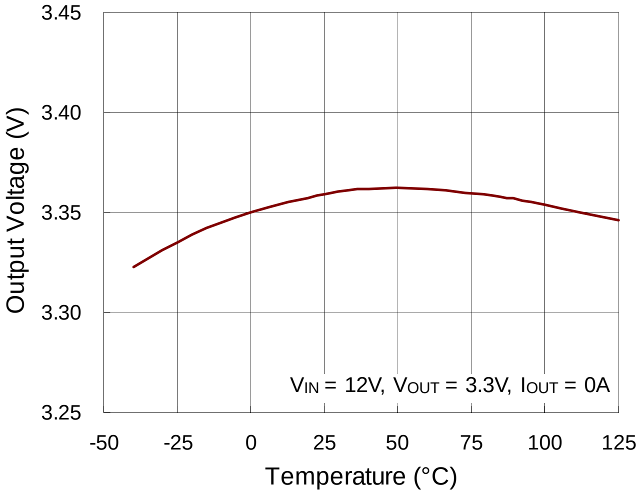
Efficiency vs. Output Current



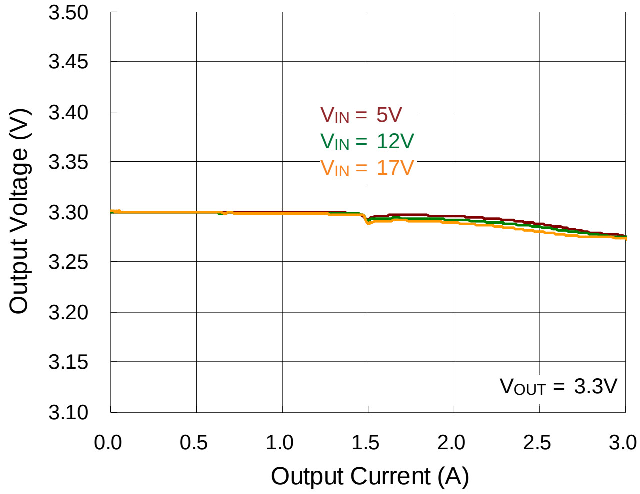
Output Voltage vs. Input Voltage



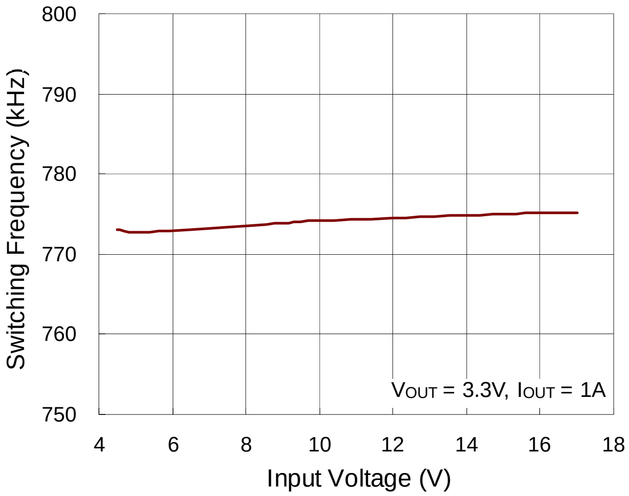
Output Voltage vs. Temperature



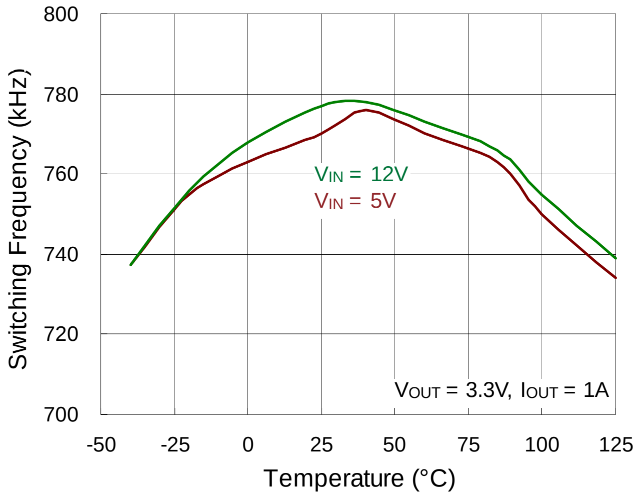
Output Voltage vs. Output Current



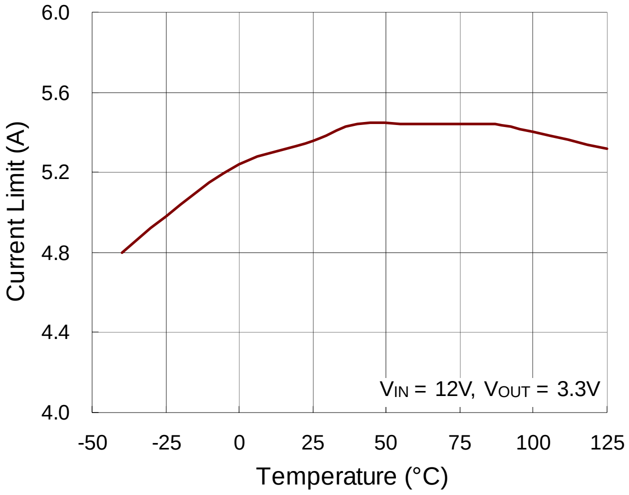
Switching Frequency vs. Input Voltage



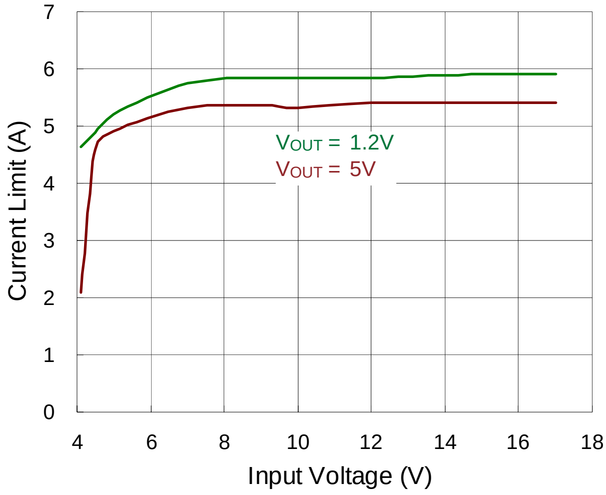
Switching Frequency vs. Temperature



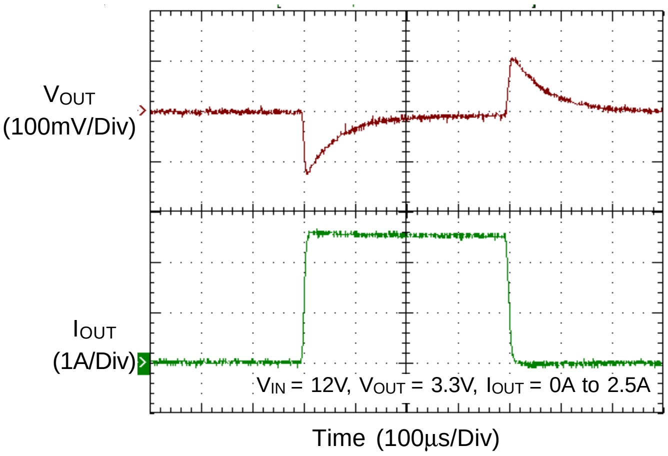
Current Limit vs. Temperature



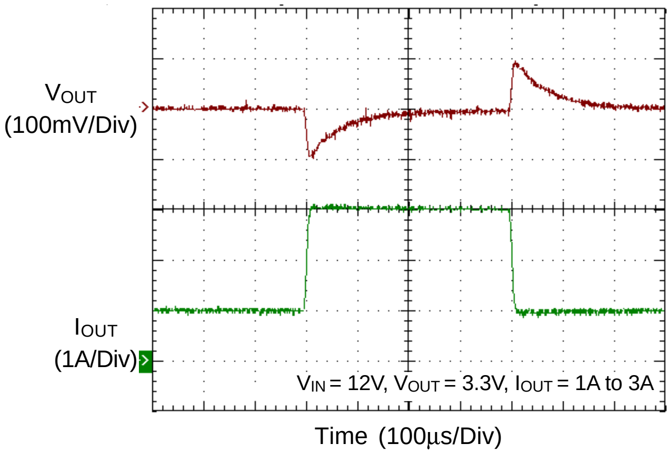
Current Limit vs. Input Voltage



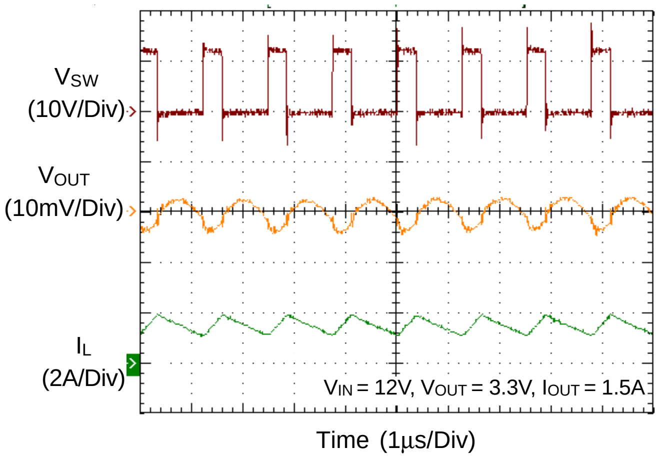
Load Transient Response



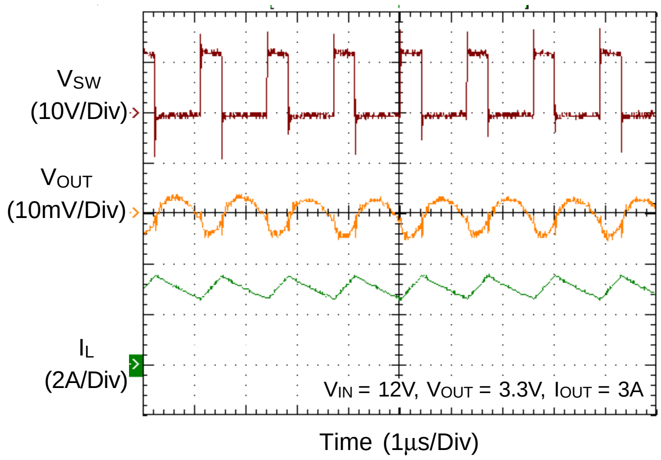
Load Transient Response



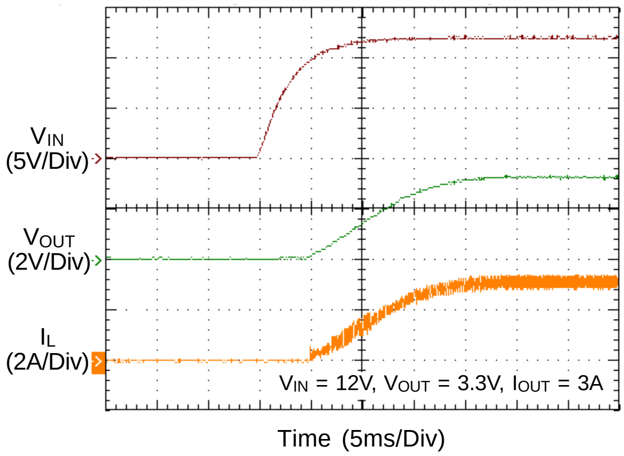
Output Ripple Voltage



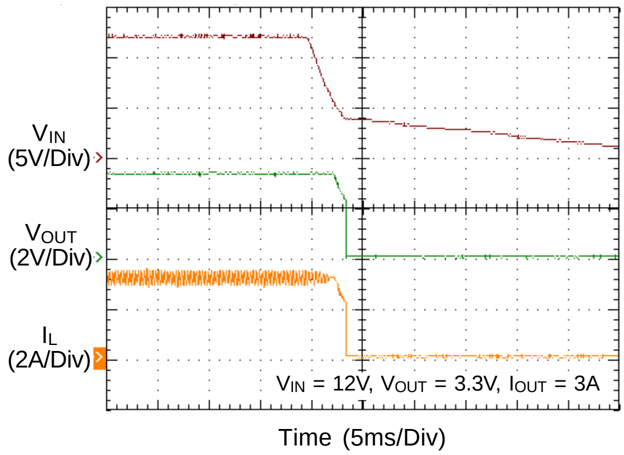
Output Ripple Voltage



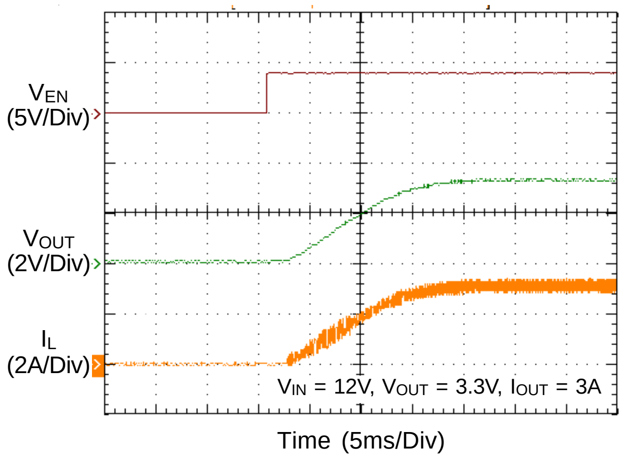
Power On from V_{IN}



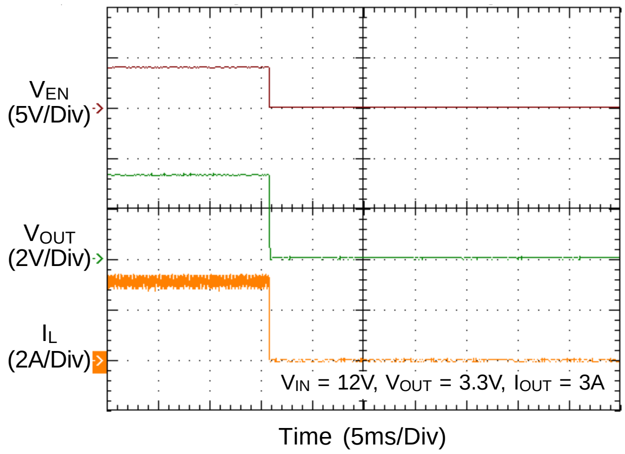
Power Off from V_{IN}



Power On from EN



Power Off from EN



Application Information

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

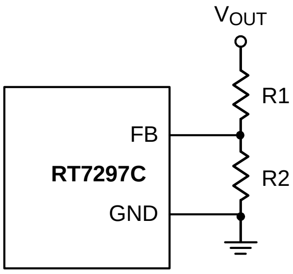


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right)$$

Where V_{REF} is the reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 0.1µF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7297C. Note that the external boot voltage must be lower than 5.5V

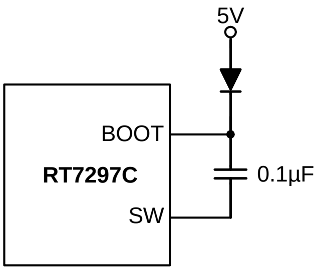


Figure 2. External Bootstrap Diode

Soft-Start

The RT7297C provides soft-start function. The soft-start function is used to prevent large inrush current while converter is being powered-up. The soft-start timing can be programmed by the external capacitor between SS and GND. An internal current source I_{SS} (6µA) charges an external capacitor to build a soft-start ramp voltage. The V_{FB} voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is calculated as follows :

Soft-Start time $t_{SS} = \frac{0.8 \times C_{SS}}{I_{SS}}$, if C_{SS} capacitor is 0.1μF, then soft-start time = $\frac{0.8 \times 0.1\mu}{6\mu} \fallingdotseq 13.5\text{ms}$

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT7297C quiescent current drops to lower than 3µA. Driving the EN pin high (>2.5V, <18V) will turn on the device again. For external timing control, the EN pin can also be externally pulled high by adding a R_{EN} resistor and C_{EN} capacitor from the VIN pin (see Figure 3).

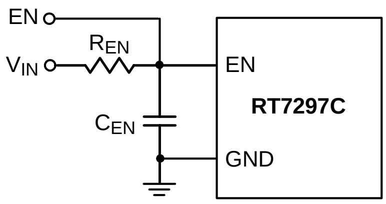


Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 4. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

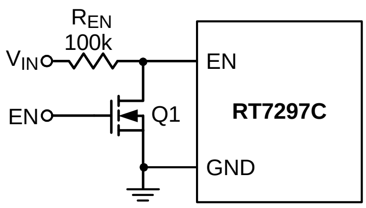


Figure 4. Digital Enable Control Circuit

Under Voltage Protection

Hiccup Mode

For the RT7297CH, it provides Hiccup Mode Under Voltage Protection (UVP). When the V_{FB} voltage drops below 0.4V, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT7297CH will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

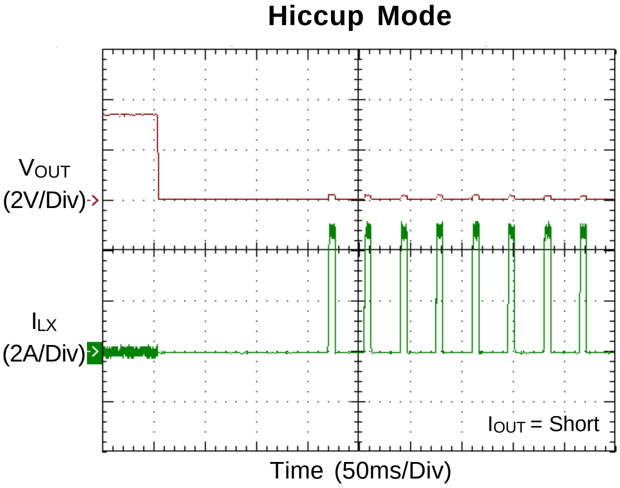


Figure 5. Hiccup Mode Under Voltage Protection

Latch-Off Mode

For the RT7297CL, it provides Latch-Off Mode Under Voltage Protection (UVP). When the FB voltage drops below half of the feedback reference voltage, V_{FB}, UVP will be triggered and the RT7297CL will shut down in Latch-Off Mode. In shutdown condition, the RT7297CL can be reset by EN pin or power input VIN.

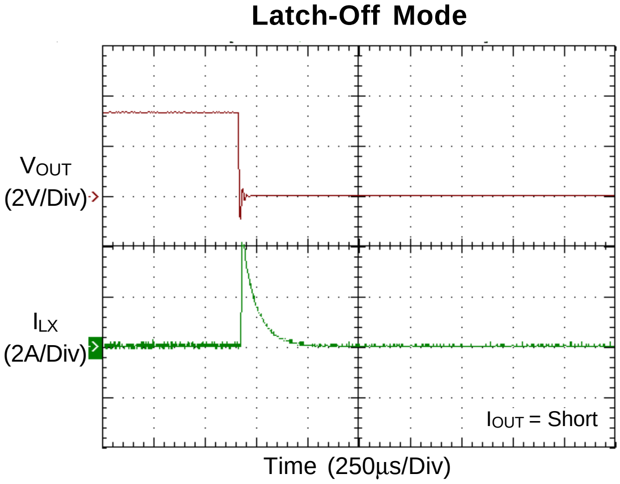


Figure 6. Latch-Off Mode Under Voltage Protection

Over Temperature Protection

The RT7297C features an Over Temperature Protection (OTP) circuitry to prevent from overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current is given :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For the input capacitor, two 10μF low ESR ceramic capacitors are suggested. For the suggested capacitor, please refer to Table 3 for more details. The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple. Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be the highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (75°C/W) = 1.333W (min.copper area PCB layout)

$P_{D(MAX)}$ = (125°C − 25°C) / (49°C/W) = 2.04W (70mm^{2}copper area PCB layout)

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 7, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 7.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 7.b) reduces the θ_{JA} to 64°C/W. Even further, increasing the copper area of pad to 70mm^2 (Figure 7.e) reduces the θ_{JA} to 49°C/W.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

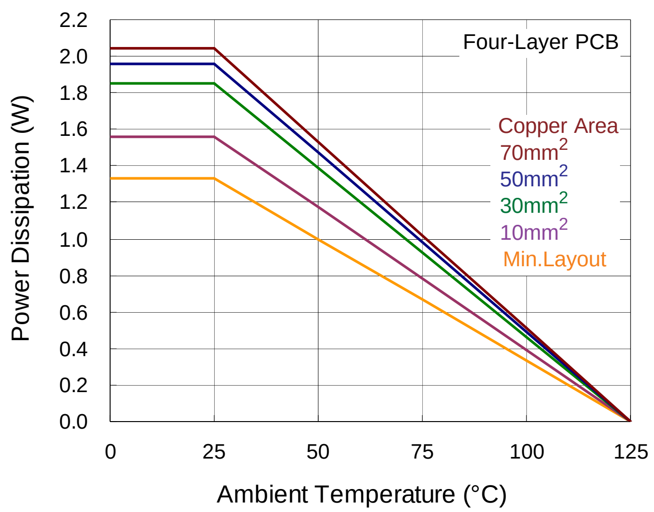
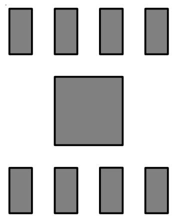
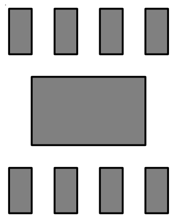


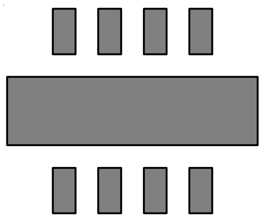
Figure 8. Derating Curve of Maximum Power Dissipation



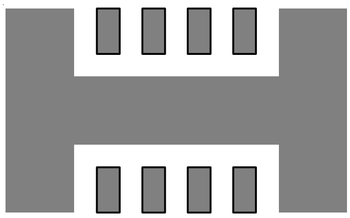
(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} = 75°C/W



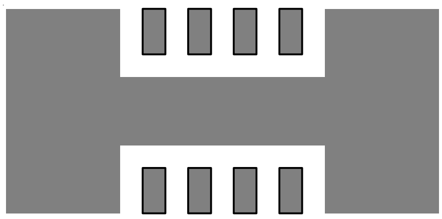
(b) Copper Area = 10mm^2, θ_{JA} = 64°C/W



(c) Copper Area = 30mm^2 , θ_{JA} = 54°C/W



(d) Copper Area = 50mm^2 , θ_{JA} = 51°C/W



(e) Copper Area = 70mm^2 , θ_{JA} = 49°C/W

Figure 7. Thermal Resistance vs. Copper Area Layout Design

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT7297C.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT7297C.
- An example of PCB layout guide is shown in Figure 9 for reference.

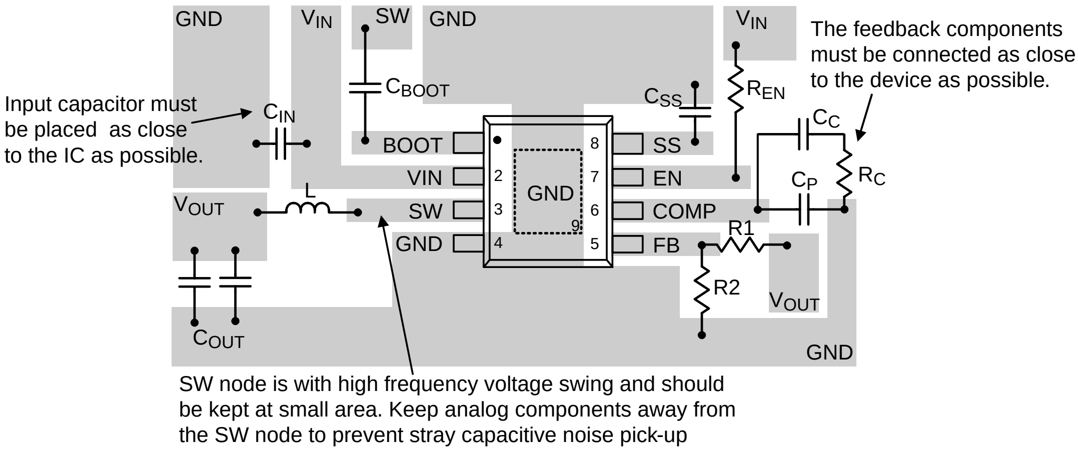
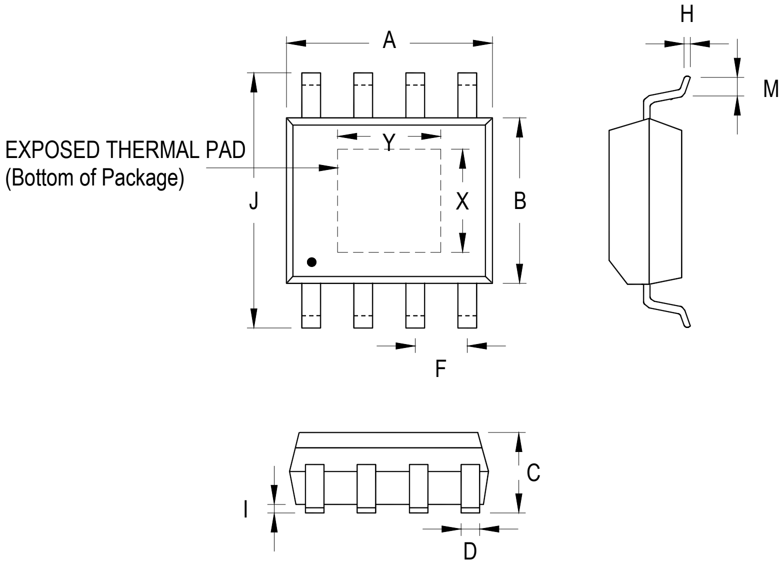


Figure 9. PCB Layout Guide

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (µF)	Case Size
C_{IN}	MURATA	GRM31CR61E106K	10	1206
C_{IN}	TDK	C3225X5R1E106K	10	1206
C_{IN}	TAIYO YUDEN	TMK316BJ106ML	10	1206
C_{OUT}	MURATA	GRM31CR60J476M	47	1206
C_{OUT}	TDK	C3225X5R0J476M	47	1210
C_{OUT}	MURATA	GRM32ER71C226M	22	1210
C_{OUT}	TDK	C3225X5R1C22M	22	1210

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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