# RAA489250B

5-Cell Battery Front End

## Description

The RAA489250B is a 5-Cell Battery Front End (BFE) with both autonomous protection functions and battery health monitoring for packs with MCU control (see Figure 1).

The RAA489250B monitors each cell for overvoltage and undervoltage, pack temperature, and charge and discharge current. This device includes internal self tests to confirm its own health, and system checks to confirm the system state.

The $I^2C$ interface includes an optional CRC to reliably communicate with an MCU. The device has a charge pump to drive a high-side CFET. The RAA489250B has a low typical Idle current consumption of 98µA to maximize operational time.

The RAA489250B is offered in an efficient 32 Ld 4mm×4mm QFN package.

## Features

- Sleep current: 1.6µA
- VPACK voltages: 5V to 30V
- $V_{CELL}$ accuracy (Over Temp): ±10mV
- $I_{PACK}$ Resolution: 13.16µV
- Open wires and self tests
- Autonomous detection and actions
- High-side charge FET control

## Applications

- Power tools
- Hand held electronics
- Battery protector

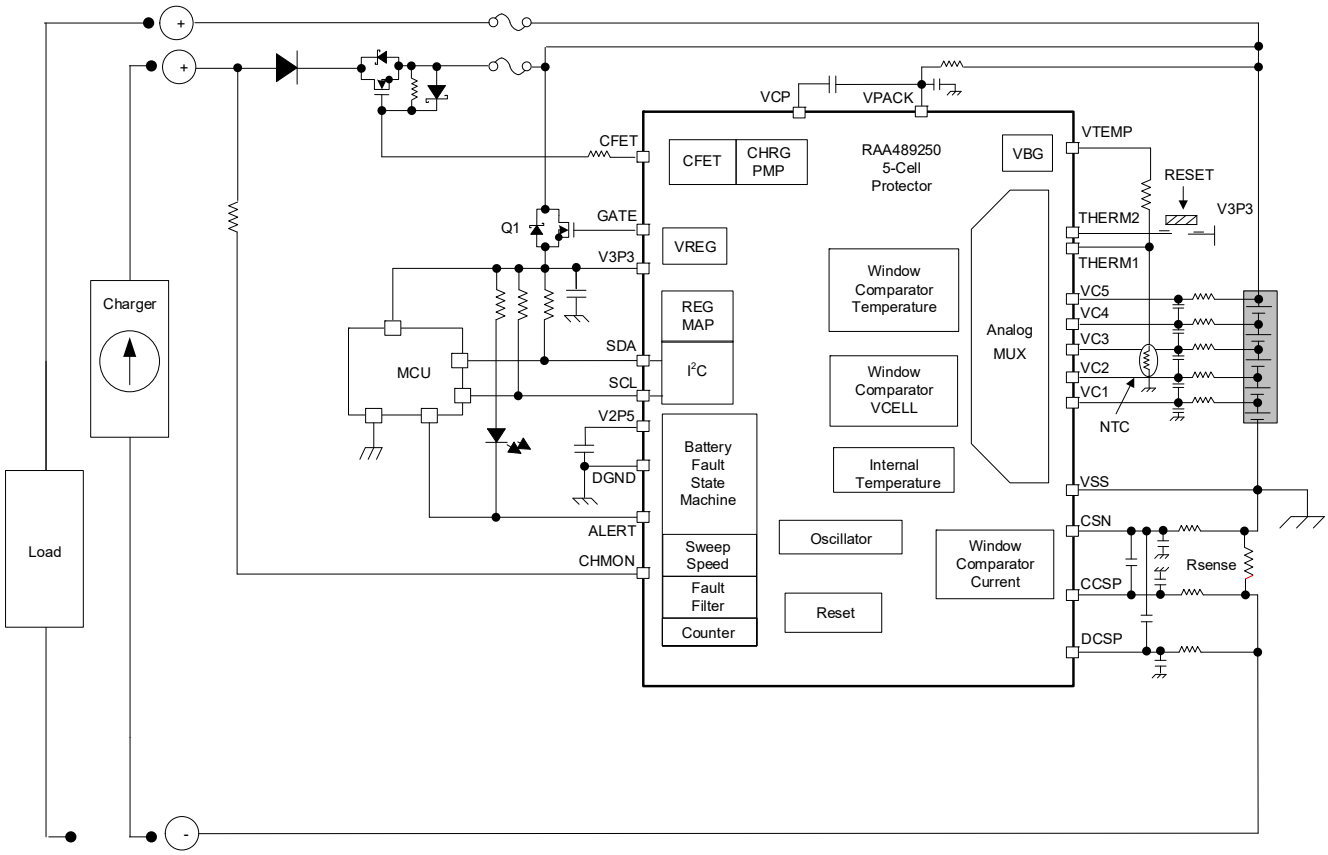



**Figure 1. BFE with Shared Rsense**

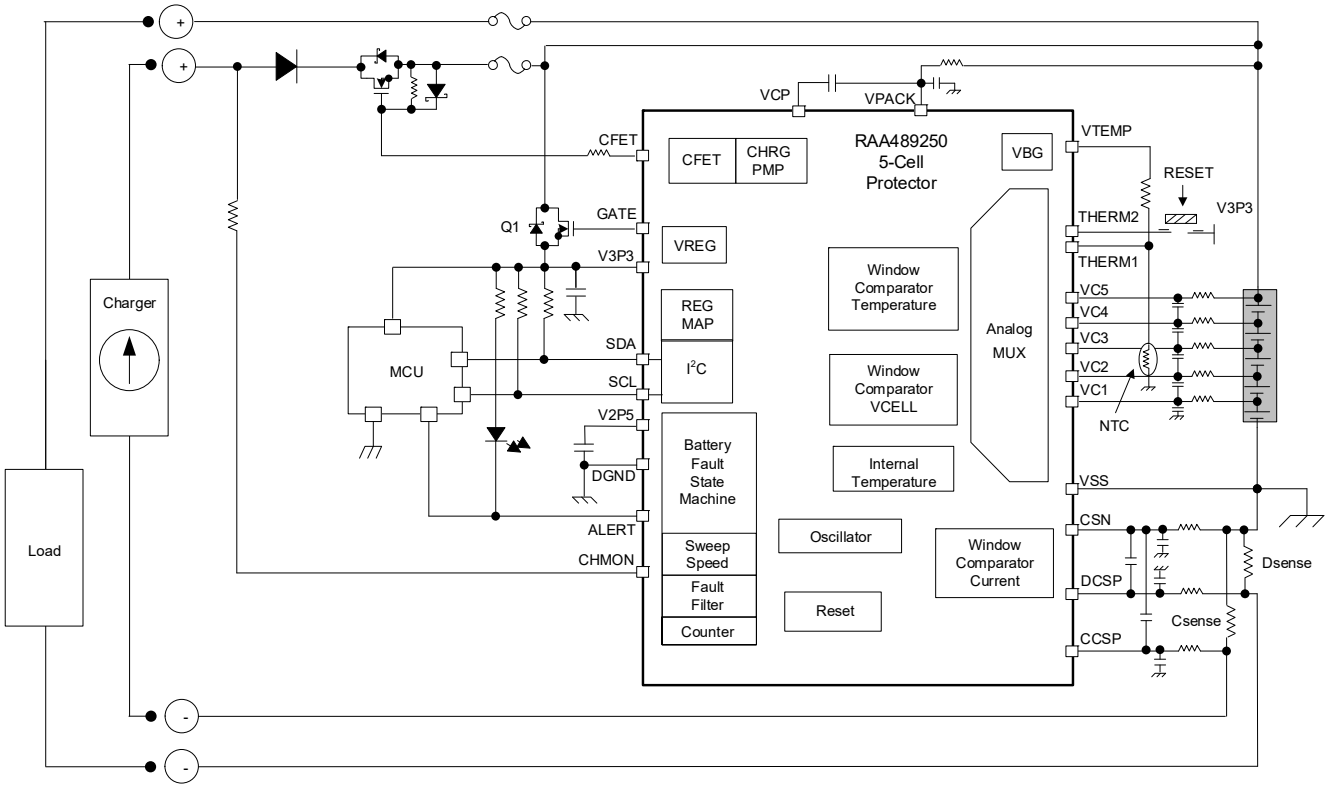



**Figure 2. BFE with Split Rsense**

# Contents

# 1. Overview

## 1.1 Block Diagram

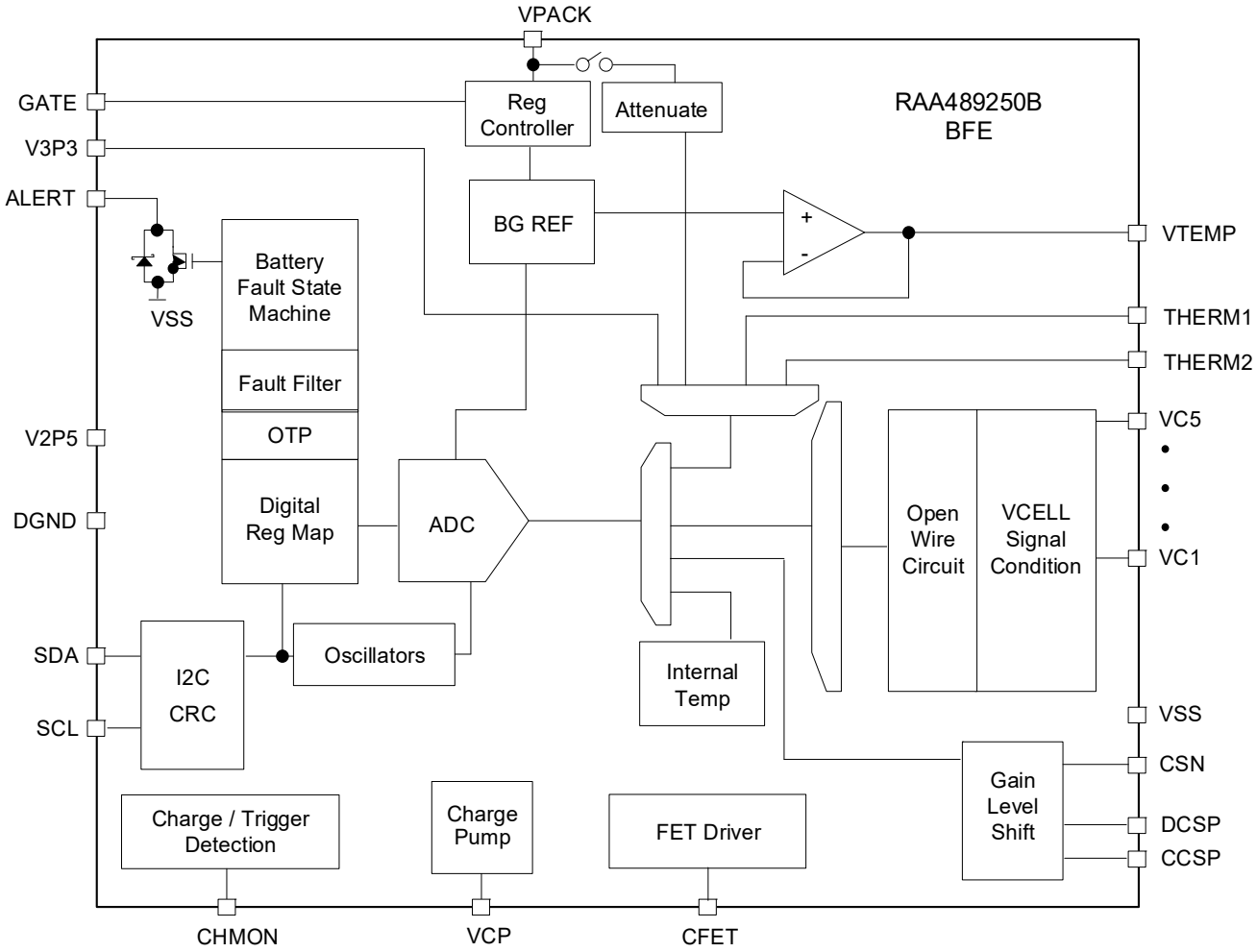



**Figure 3. Block Diagram**

# 2. Pin Information

## 2.1 Pin Assignments

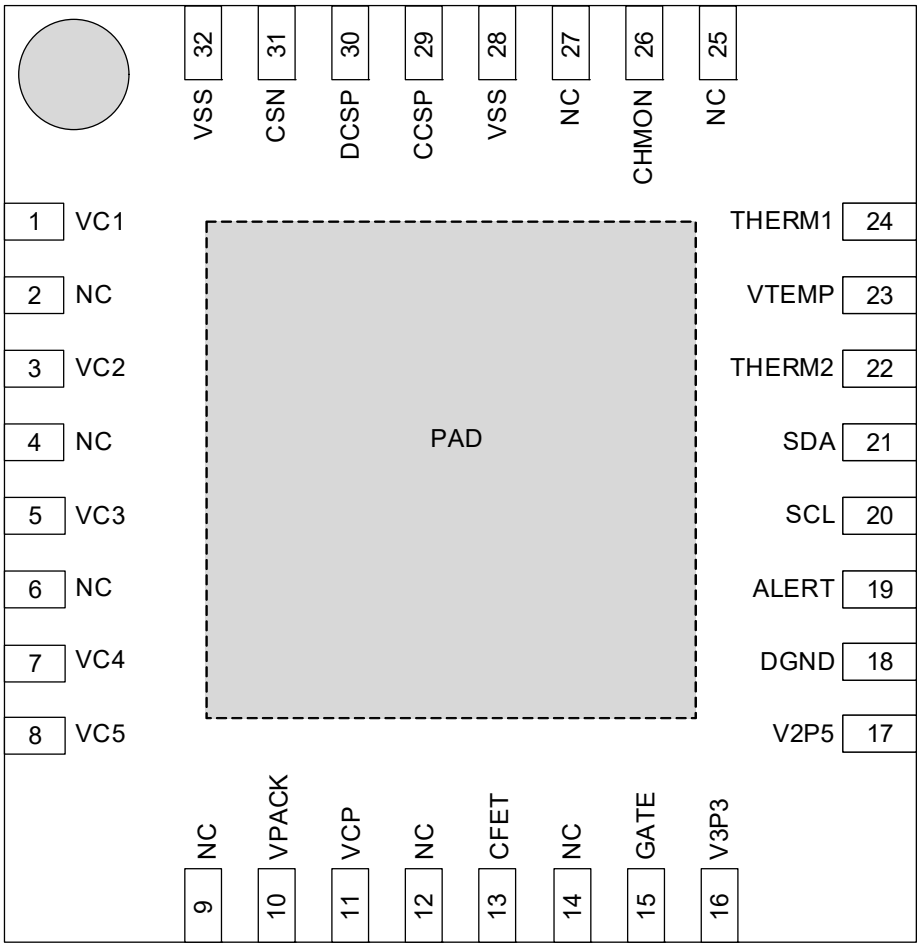



**Figure 4. Pin Assignments - Top View**

## 2.2 Pin Descriptions

| Pin Number | Pin Name | Description |
|---|---|---|
| 1, 3, 5, 7, 8 | VCn (n = 1 to 5) | **Battery cell voltage inputs.** For applications with a 5-cell battery string, where cell number 1 connects to the lowest voltage and cell number 5 connects to the highest voltage, VCn connects to the positive terminal of cell n. The negative terminal of cell n connects to VC n-1. All connections from cell to pin are made as a kelvin sense route and through a low pass filter network. |
| 10 | VPACK | **VPACK Pin.** Connect this pin to the pack voltage. A voltage at this pin powers the IC. Connect a 10µF capacitor from pin to VSS. |
| 11 | VCP | **Charge pump output voltage.** Place a capacitor between VCP and VPACK. The charge pump provides power to CFET driver. Connect a minimum of 0.1µF capacitor between this pin and VPACK. |
| 13 | CFET | **High side charge FET control pin.** Connect to the gate of a NMOS that connects to the charge path of the battery pack. When CFET is enabled, this pin is connected to the charge pump to turn the NMOS on. |
| 15 | GATE | **Regulator control pin.** Connect this pin to the gate of an external NMOS for high current regulation. Connect the pin to V3P3 pin for low current regulation. Connect a capacitor that is ~1/8 to 1/10 of the V3P3 cap value between this pin and VSS. |
| 16 | V3P3 | **3.3V supply voltage input.** Connect directly to the source of the external NMOS FET, Connect a 10µF capacitor between this pin and VSS. |

| Pin Number | Pin Name | Description |
|---|---|---|
| 17 | V2P5 | **Internal 2.5V supply decoupling pin.** Connect a 1µF capacitor between V2P5 and DGND. |
| 18 | DGND | **Digital Ground**. If separate digital and analog ground planes are used connect them together at the VSS pin. |
| 19 | ALERT | **ALERT pin.** This pin is the fault and status change indicator for the pack. The Fault and Status bits can change the state of the $\overline{\text{ALERT}}$ pin. The pin is an open drain NMOS. The pin asserts to the VSS level when an unmasked fault or status bit is set. Otherwise, the pin is in a high impedance state. A pull-up resistor greater than 10kΩ to MCU voltage is required. |
| 20 | SCL | **Serial Clock pin.** This pin is the clock signal for the $I^2C$ communication interface. An optional pull-up resistor greater than 4.7kΩ to 3.3V can be attached depending on the MCU pin driving this node. |
| 21 | SDA | **Serial Data pin.** This is an open-drain serial data I/O for the $I^2C$ communication interface. A pull-up resistor greater than 4.7kΩ to 3.3V is required |
| 23 | VTEMP | **VTEMP pin.** Connect this pin through a pull-up resistor to the thermistor circuits. |
| 24, 22 | THERM1,2 | **Thermistor pins.** Connect a thermistor to each of these pins. COTn, CUTn, DOTn, and DUTn thresholds are compared to the measurement of the respective thermistor. Reset the device by connecting the THERM2 pin to V3P3 pin. |
| 25 | NC | **NC or Analog ground.** This pin is not connected internally, it can be floated or it can be connected to analog ground to be compatible with another device. |
| 26 | CHMON | **Charge Monitor pin.** When the voltage on CHMON pin rises above the $V_{CHTHR}$, the CH PRESI bit transitions from 0 to 1. Connect this pin to the top of the charger. This pin requires an external pull down resistor for operation to VSS. |
| 29 | CCSP | **Charge Current Sense Positive.** Connect a current sense resistor between this pin and the CSN pin to detect charge current. |
| 30 | DCSP | **Discharge Current Sense Positive.** Connect a current sense resistor between this pin and the CSN pin to detect discharge current. |
| 31 | CSN | **Current Sense Negative.** Connect this pin to the PCB ground and the negative terminal of the battery pack. |
| 28, 32 | VSS | **Analog ground.** VSS is the negative reference voltage for the IC and must be connected to GND. This pin also serves as the negative reference pin for cell1 voltage measurement. |
| 2, 4, 6, 9, 12, 14, 27 | NC | **No Connect pins.** Do not connect these pins to ground, together, or any other node. |
| - | EPAD | **Electrical Pad.** Connect to VSS |

# 3. Specifications

## 3.1 Absolute Maximum Ratings

***Caution***: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| VPACK | -0.3 | +30 | V |
| CFET, VCP | VPACK - 0.3 | VPACK +12 | V |
| CHMON | -0.3 | +30 | V |
| VPACK - VC5 | -30 | +30 | V |
| VC5 | -0.3 | +30 | V |
| VC4 | -0.3 | +25 | V |
| VC3 | -0.3 | +19 | V |
| VC2 | -0.3 | +13 | V |
| VC1 | -0.3 | +6.5 | V |
| VCn - VC(n-1) (n = 2 to 5) | -0.3 | 6.5 | V |
| DGND | -0.3 | 0.5 | V |
| GATE | -0.3 | 12.5 | V |
| V3P3 | -0.3 | 6.5 | V |
| V2P5 | -0.3 | 2.9 | V |
| CCSP, DCSP, CSN, THERM1, VTEMP, THERM2 | -0.3 | 6.5 | V |
| SDA, SCL, $\overline{\text{ALERT}}$ | DGND -0.3 | 6.5 | V |
| $\overline{\text{ALERT}}$, SDA | -10 | 0 | mA |
| CFET | 0 | 5 | mA |
| Maximum Junction Temperature | - | +125 | °C |
| Maximum Storage Temperature Range | -65 | +150 | °C |
| Human Body Model (Tested per JS-001-2023) | - | 1.5 | kV |
| Charged Device Model (Tested per JS-002-2022) | - | 750 | V |
| Latch-Up (Tested per JESD78E; Class 2, Level A) | - | 100 | mA |

## 3.2 Recommended Operating Conditions

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| Supply Voltage, VPACK | 5 | 18 | 22.5 | V |
| Ambient Temperature | -40 | 25 | +85 | °C |
| VCn - VC(n-1) (n = 2 to 5); VC1 - VSS | 1.5 | 3.6 | 4.5 | V |
| CCSP - CSN, DCSP - CSN (CSN = VSS) | -200 | - | 200 | mV |
| VCP, CFET (pin - VPACK) | 0 | 10 | 11 | V |
| CHMON | 0 | - | VPACK | V |
| $\overline{\text{ALERT}}$, SDA, SCL | 0 | 3.3 | V3P3 | V |
| THERM1, THERM2 (as thermistor inputs) | 0 | 0.68 | 2.09 | V |
| THERM2 (as RESET) | 0 | - | V3P3 | V |
| DGND-VSS, CSN - VSS | -0.1 | - | 0.1 | V |

## 3.3 Thermal Information

| Parameter | Package | Symbol | Conditions | Typical Value | Unit |
|---|---|---|---|---|---|
| Thermal Resistance | 32 Ld 4x4 QFN Package | $\theta_{JA}$[1] | Junction to ambient | 38 | °C/W |
| | | $\theta_{JC}$[2] | Junction to case | 2.5 | °C/W |

1. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For $\theta_{JC}$, the case temperature location is the center of the exposed metal pad on the package underside.

## 3.4 Electrical Specifications

$T_A$ = +25°C, VPACK = 18V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS. External component values per Section 9.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Power-On Reset Voltage at VPACK (Device Enters/Exits Reset State) | $V_{PORf}$ | Falling Edge | 3.5 | 3.8 | 4.1 | V |
| | $V_{PORr}$ | Rising Edge | | 4.6 | 5 | V |
| Power-On Hysteresis | $V_{PORhys}$ | | | 0.8 | | V |
| Power-Up Time | $t_{PwrUp}$ | Power Applied to IDLE Mode | | 20 | 35 | ms |
| Power-On Reset Time | $t_{RESET}$ | VPACK > $V_{POR}$, Hard or Soft RESET | | 8 | | ms |
| Wakeup Startup Time | $t_{WakeUp}$ | Low Power to IDLE Mode | | 1 | | ms |
| Current Consumed by the IC | $I_{VPACK}$ | Operating, CFET ON, during SCAN | | 800 | 900 | µA |
| | | IDLE Mode | | 98 | 140 | µA |
| | | LOW POWER Mode, LP Reg = 1 | | 31 | 45 | µA |
| | | LOW POWER Mode, LP Reg = 0 | | 1.6 | 5 | µA |
| **$V_{CELL}$** | | | | | | |
| Cell Measurement Error (Triggered Celln Measurement) | $V_{CELL\_ME}$ | T = 0°C to 60°C; RS = 1kΩ, CS = 0.1µF, $V_{CELL}$ = 1.0V to 4.25V | -10 | | 10 | mV |
| $V_{CELL}$ Leakage Current OFF | $V_{Cell\_IbOff}$ | Cell measure off | | | 200 | nA |
| $V_{CELL}$ Bias Current ON | $V_{Cell\_IbOn}$ | During measure | | 3 | | µA |
| $V_{CELL}$ Bias Current Match ON | $V_{Cell\_Ios}$ | During measure | | ±0.3 | | µA |
| **$I_{PACK}$ (xCSP - CSN)** | | | | | | |
| $I_{PACK}$ Vos | $I_{PACK\_VOS}$ | xCSP = CSN = 0V | 0 | 110 | | µV |
| $I_{PACK}$ Vos TC | $I_{PACK\_VOSTC}$ | xCSP = CSN = 0V, 0C to 60C | | 0.4 | | µV |
| IPACK Bias Current | $I_{PACK\_BC}$ | | | -1.2 | | µA |
| IPACK Bias Current Offset | $I_{PACK\_IOS}$ | | | ±500 | | nA |
| IPACK Gain Error | $I_{PACK\_GE}$ | VDischarge = 10mV to 50mV; VCharge = -10mV to -50mV | -3 | -0.5 | 3 | % |
| $I_{PACK}$ Charge Detect (CHRGI) | $I_{CHRGI}$ | Code > 0x012E | | -0.6 | | mV |
| $I_{PACK}$ Discharge Detect (DCHRGI) | $I_{DCHRGI}$ | Code > 0x012E | | 0.6 | | mV |
| **$I_{PACK}$ Threshold (xCSP - CSN)** | | | | | | |
| DSC Hysteresis (DCSP-CSN) | $DSC_{Hys}$ | | | 20 | | mV |
| Charge Short-Circuit Voltage (CCSP-CSN) | CSC | | | -200 | | mV |

$T_A$ = +25°C, VPACK = 18V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS. External component values per Section 9. (Cont.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| CSC Hysteresis (CCSP-CSN) | $CSC_{Hys}$ | | | 20 | | mV |
| CSC Delay (CCSP-CSN) | $CSC_{dly}$ | | | 0.1 | | ms |
| **$V_{PACK}$** | | | | | | |
| VPACK Attenuation | $V_{PACKAttn}$ | | | 15 | | V/V |
| VPACK Measurement Error | $V_{PACK\_ME}$ | 7.5V < VPACK < 21.25V | | ±0.5 | | % |
| VPACK Measurement Error TC | $V_{PACKME\_TC}$ | | | ±100 | | ppm/°C |
| **$V_{TEMP}$** | | | | | | |
| $V_{TEMP}$ Voltage Accuracy | - | 0 to 0.5mA load | 2.037 | 2.064 | 2.091 | V |
| $V_{TEMP}$ Measurement Error | $V_{VTEMP\_ME}$ | | | ±4.5 | | mV |
| Settling Time for VTEMP before a THERM1, THERM2 Measurement | $t_{VTEMP}$ | VTEMP Turn ON to single triggered thermistor measurement | | 18 | | ms |
| $V_{TEMP}$ Max Threshold | $V_{TEMP\_max}$ | Code > 0x06CC = OWF | | 2.253 | | V |
| $V_{TEMP}$ Min Threshold | $V_{TEMP\_min}$ | Code < 0x0533 = OWF | | 1.843 | | V |
| **Thermistor** | | | | | | |
| Thermistor Leakage Current | - | | -1 | | 1 | µA |
| Open Wire Threshold | $OW_{VTHERM}$ | Code > 0x0FD7 = OWF | | 1.9 | | V |
| RESET Voltage Threshold (THERM2) | $RST_{VTHERM}$ | Threshold voltage above V2P5. | | 0.4 | | V |
| RESET Time (THERM2) | $t_{RESET}$ | The time the THERM2 pin is above $RST_{VTHERM}$ before the device resets | | 500 | | ms |
| RESET Exit Time (THERM2) | $t_{RST\_Exit}$ | The time between the THERM2 pin falling below 2.6V and the state machine transitioning to POWER UP (pin must not read OW or DOT) | | 2 | | ms |
| Thermistor Measurement Error | $THERM_{ME}$ | VTHERMx = 1V | | ±4 | | mV |
| **Internal Over-Temperature Sensor** | | | | | | |
| Internal Temperature Sensor Code | - | 25°C (HEX) | | 0x0636 | | LSBs |
| Internal Over-Temperature Threshold | IOT | Analog comparator | | 100 | | °C |
| **V3P3 and V2P5 Regulators** | | | | | | |
| Regulation Voltage Accuracy | $V3P3_V$ | At V3P3 Pin, 0-30mA load | 3.22 | 3.32 | 3.42 | V |
| Pin Measurement Error | $REG_{ME}$ | | | ±7.5 | | mV |
| GATE Pin Drive Current | $I_{Gate\_drv}$ | Device maintains regulation under load | | 10 | | µA |
| **V3P3 and V2P5 Thresholds** | | | | | | |
| V3P3 Overvoltage Threshold | $dV3P3_{OV}$ | Digital Comparator (0xBE0) (self test) | | 3.553 | | V |
| V3P3 Undervoltage Threshold | $dV3P3_{UV}$ | Digital Comparator (0x999) (self test) | | 2.97 | | V |
| V3P3 Power Good OV Threshold | $PG_{V3P3\_OV}$ | Analog comparator | | 3.8 | | V |
| V3P3 Power Good UV Threshold | $PG_{V3P3\_UV}$ | Analog comparator | | 2.51 | | V |

$T_A$ = +25°C, VPACK = 18V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS. External component values per Section 9. (Cont.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| V2P5 Overvoltage Threshold | $dV2P5_{OV}$ | Digital comparator (self test) (0x8BD) | | 2.75 | | V |
| V2P5 Undervoltage Threshold | $dV2P5_{UV}$ | Digital comparator (self test) (0x6CA) | | 2.25 | | V |
| V2P5 Power Good OV Threshold | $PG_{V2P5\_OV}$ | Analog comparator | | 2.8 | | V |
| V2P5 Power Good UV Threshold | $PG_{V2P5\_UV}$ | Analog comparator | | 2.0 | | V |
| **VCP (Charge Pump)/CFET** | | | | | | |
| VCP Voltage ($V_{CP}$ - VPACK) | - | CFET EN = 1; CGS = 10nF | | 10 | | V |
| | | 5V<VPACK<10V | 8 | | | V |
| CFET On-State Output Resistance | $R_{HCFON}$ | Resistance from CFET to VCP | | 3.5 | | kΩ |
| Charge Pump Rising Voltage Threshold (To clear CPF) | $V_{pmpMin}$ | | | 7.5 | | V |
| Charge Pump Falling Voltage Threshold (To set CPF) | $V_{pmpFall}$ | | | 5.0 | | V |
| CFET Off-State Output Resistance | $R_{HCFOFF}$ | Resistance from CFET to VPACK | | 2.0 | | kΩ |
| Charge Pump External Current Capacity | $I_{pmp}$ | CFET_EN = 1, VCP = VPACK+9V | | 5 | 10 | µA |
| CFET ON-Time | - | 10nF pin capacitance; 10% to 90%, Riso = 1k | | 240 | | µs |
| CFET OFF-Time | - | 10nF pin capacitance; 10% to 90%, Riso = 1k | | 130 | | µs |
| Charge Pump Start-Up Time | $t_{strt}$ | $C_{pmp}$ = 100nF; the time it takes to charge the $C_{pmp}$ | | | 30 | ms |
| **Charge Detection Monitor (CHMON)** | | | | | | |
| Charge Detection Threshold | $V_{CHTHR}$ | Rising Edge, $V_{CHMON}$ - $V_{ss}$ | 0.9 | 1.2 | 1.6 | V |
| Charge Detection Hysteresis | $V_{CHHys}$ | | | 100 | | mV |
| CHMON Detection Current | CHDC | CHMON ON (>3V), into pin | | 3 | | µA |
| CHMON Internal Pull-Down Resistor | RCHPD | 0V to VPACK; CHMON Off | | 15 | | MΩ |
| Charge Monitor Enable Delay Time | $t_{CHEN}$ | Power FET(s) off to CHMON Detect | | 100 | | ms |
| **Open Wire** | | | | | | |
| Open-Wire Current | $I_{OW}$ | VCn pin to VSS (n = 1 to 5) | | 400 | | µA |
| Open-Wire Detection Time | $t_{OWON}$ | Open-wire current source on-time | | 15 | | ms |
| Open-Wire ADC Read time | | Reference to OW assertion. Time to first compare | | 10 | | ms |
| Detection Threshold (Cells) | $V_{OWth1}$ | All $V_{CELLs}$ (ADC code 0x0058) | | 0.45 | | V |
| Detection Threshold (VSS) | $V_{OWth2}$ | VSS - VC1 | | 0.25 | | V |
| Detection Threshold (VPACK) | $V_{OWth3}$ | VC5 - VPACK | | 0.5 | | V |
| **Cell Balancing** | | | | | | |
| Internal Cell Balance Resistance VCn to VCn-1 (n = 1 to 5) | RCB_OFF | CBn Off (n = 1 to 5) | | 4 | | MΩ |
| | RCB_ON | CBn On (n = 1 to 5) | | 50 | | Ω |

$T_A$ = +25°C, VPACK = 18V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS. External component values per Section 9. (Cont.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **System** | | | | | | |
| 4MHz Oscillator Accuracy | - | | -5 | ±1.25 | 5 | % |
| 32kHz Oscillator Accuracy | - | | -15 | ±5 | 15 | % |
| **$\overline{\text{ALERT}}$** | | | | | | |
| $\overline{\text{ALERT}}$ Low Level Output Voltage | $AT_{VOL}$ | $I_{sink}$ = 2mA | | 0.2 | 0.6 | V |
| $\overline{\text{ALERT}}$ Leakage Current | $AT_{LIH}$ | $\overline{\text{ALERT}}$ = 0 V to 3.3V | | | 1 | µA |
| **I²C Interface Specifications** | | | | | | |
| SDA and SCL Input Buffer LOW Voltage | $V_{IL}$ | | -0.3 | | 0.3xV3p3 | V |
| SDA and SCL Input Buffer HIGH Voltage | $V_{IH}$ | | $0.7xV_{3p3}$ | | V3p3+0.3 | V |
| SDA and SCL Input Buffer Hysteresis | $I2C_{Hysteresis}$ | | | 0.05xV3p3 | | V |
| SDA Output Buffer LOW Voltage | $V_{OL}$ | Sinking 2mA | 0 | 0.2 | 0.6 | V |
| Pin Leakage Current for SDA and SCL Pins | $I_{leak}$ | | -1 | | 1 | µA |
| SCL Frequency | $f_{SCL}$ | | | | 400 | kHz |
| Pulse Width Suppression Time at SDA and SCL Inputs | $t_{IN}$ | Any pulse narrower than the max spec is suppressed | | | 50 | ns |
| SCL Falling Edge to SDA Output Data Valid | $t_{AA}$ | SCL falling edge crossing 30% of $V_{DD}$, until SDA exits the 30% to 70% of $V_{DD}$ window | | | 900 | ns |
| Time the Bus Must be Free Before the Start of a New Transmission | $t_{BUF}$ | SDA crossing 70% of $V_{DD}$ during a STOP condition, to SDA crossing 70% of $V_{DD}$ during the following START condition | 1300 | | | ns |
| Clock LOW Time | $t_{LOW}$ | Measured at the 30% of $V_{DD}$ crossing | 1300 | | | ns |
| Clock HIGH Time | $t_{HIGH}$ | Measured at the 70% of $V_{DD}$ crossing | 600 | | | ns |
| SDA Low Timeout I²C communication is reset bus released | $t_{TIMEOUT}$ | | 25 | 32 | | ms |
| 8th Bit to ACK Bit Delay (Applies to reading ADC Output Data Only) | $I^2C\_t_{WAIT}$ | Time between the rising edge of the clock pulse corresponding to the last bit of any byte, and the falling edge of the clock pulse corresponding to the Acknowledge bit | 7 | | | µs |
| START Condition Setup Time | $t_{SU:STA}$ | SCL rising edge to SDA falling edge. Both crossing 70% of $V_{DD}$ | 600 | | | ns |
| START Condition Hold Time | $t_{HD:STA}$ | From SDA falling edge crossing 30% of $V_{DD}$ to SCL falling edge crossing 70% of $V_{DD}$ | 600 | | | ns |
| Input Data Setup Time | $t_{SU:DAT}$ | From SDA exiting the 30% to 70% of $V_{DD}$ window, to SCL rising edge crossing 30% of $V_{DD}$ | 100 | | | ns |
| Input Data Hold Time | $t_{HD:DAT}$ | From SCL falling edge crossing 30% of $V_{DD}$ to SDA entering the 30% to 70% of $V_{DD}$ window | 20 | | 900 | ns |

$T_A$ = +25°C, VPACK = 18V; VCell = 3.6V, DGND = VSS = 0V, unless otherwise specified. All voltages are with respect to VSS. External component values per Section 9. (Cont.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| STOP Condition Setup Time | $t_{SU:STO}$ | From SCL rising edge crossing 70% of $V_{DD}$, to SDA rising edge crossing 30% of $V_{DD}$ | 600 | 17 | | ns |
| STOP Condition Hold Time | $t_{HD:STO}$ | From SDA rising edge to SCL falling edge. Both crossing 70% of $V_{DD}$ | 600 | 45 | | ns |
| Output Data Hold Time | $t_{DH}$ | From SCL falling edge crossing 30% of $V_{DD}$, until SDA enters the 30% to 70% of $V_{DD}$ window | 0 | 150 | | ns |
| SDA and SCL Rise Time | $t_R$ | From 30% to 70% of $V_{DD}$ | 20+0.1xCb | | 300 | ns |
| SDA and SCL Fall Time | $t_F$ | From 70% to 30% of $V_{DD}$ | 20+0.1xCb | | 300 | ns |

# 4. Typical Performance Curves

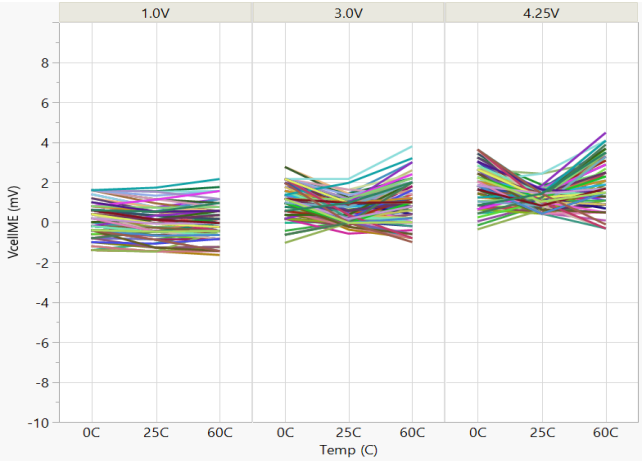



Figure 5. Cell 1 ME vs Voltage

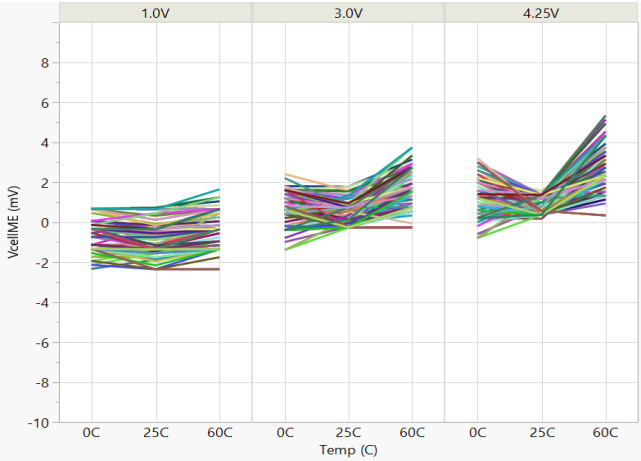



Figure 6. Cell 2 ME vs Voltage

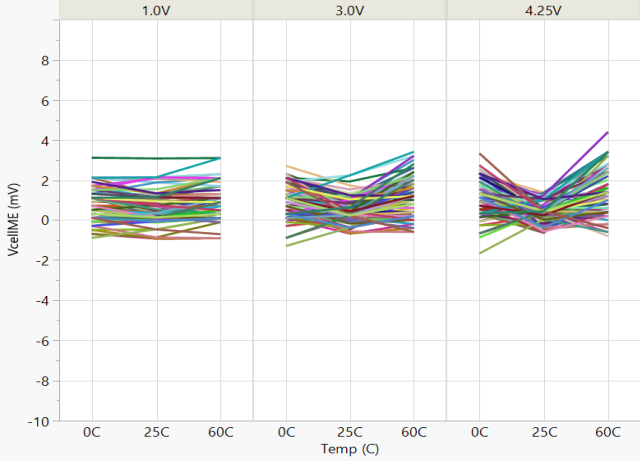



Figure 7. Cell 3 ME vs Voltage

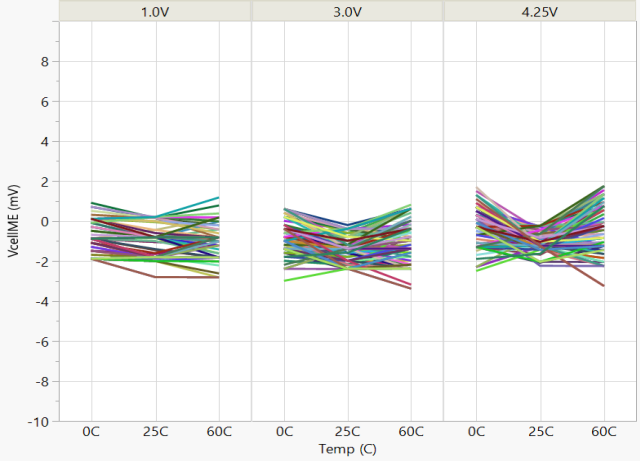



Figure 8. Cell 4 ME vs Voltage

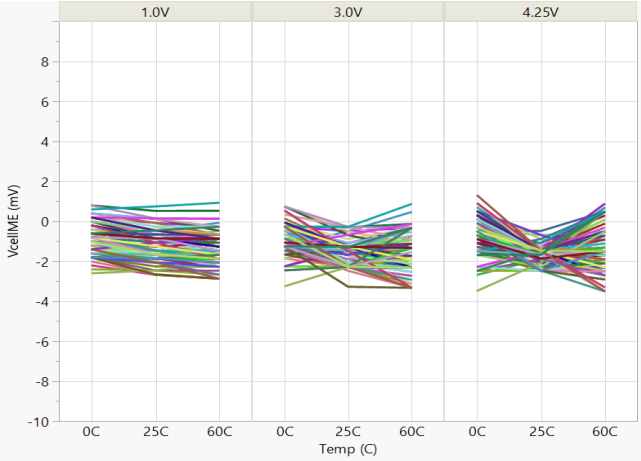



Figure 9. Cell 5 ME vs Voltage

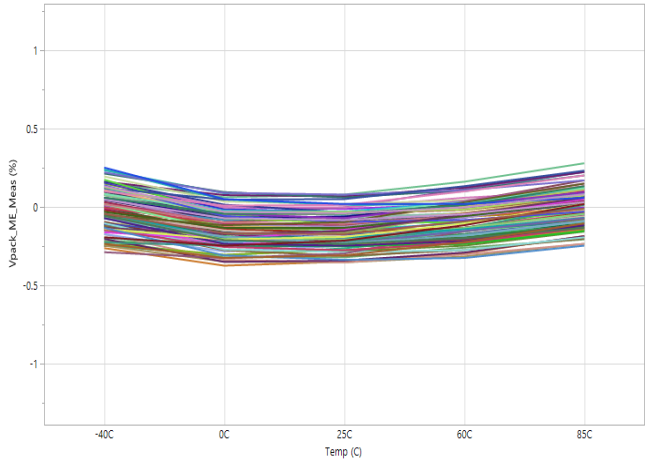



Figure 10. VPACK Pin Voltage ME

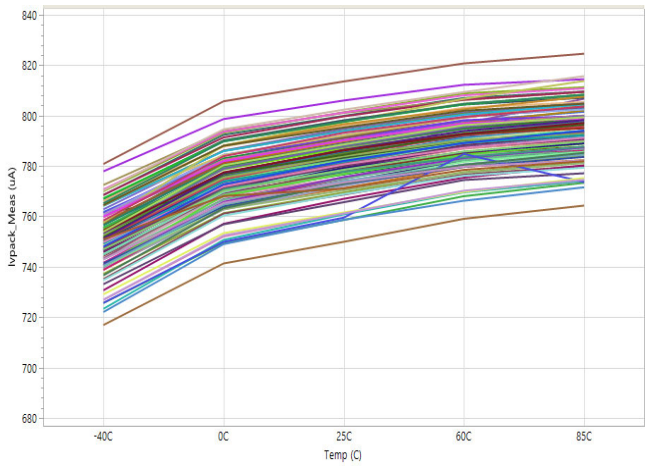



Figure 11. VPACK Current (SCAN, CFET on)

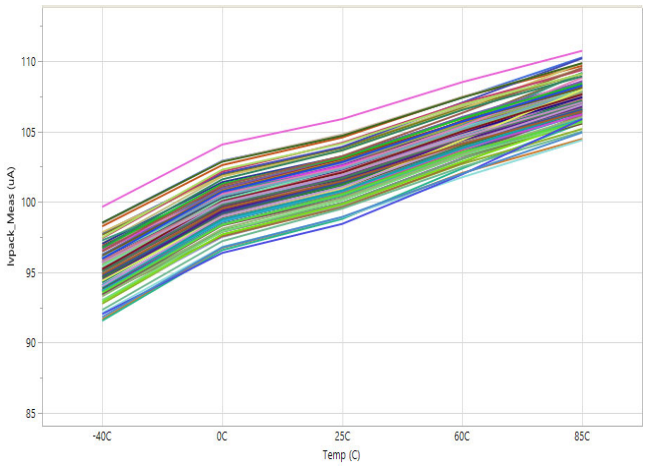



Figure 12. VPACK Current (IDLE, CFET off)

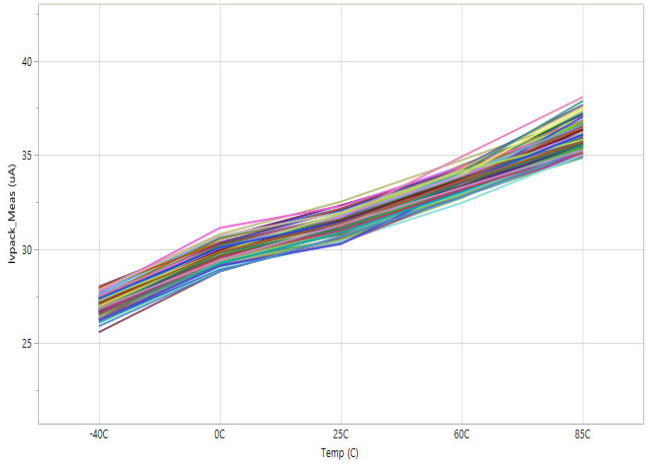



Figure 13. VPACK Current (SLEEP)

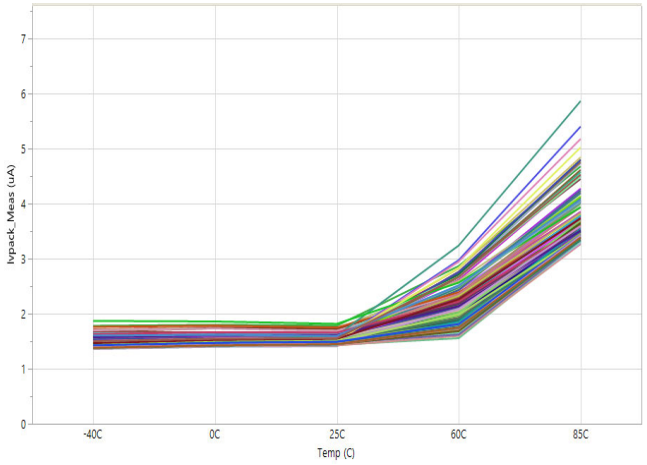



Figure 14. VPACK Current (SHIP)

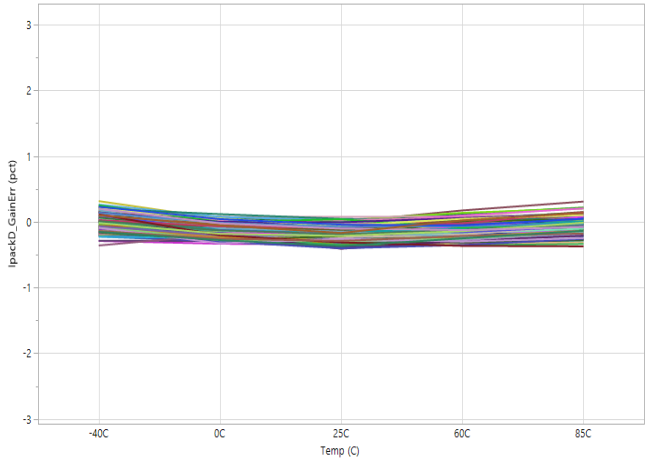



Figure 15. Discharge Current GE

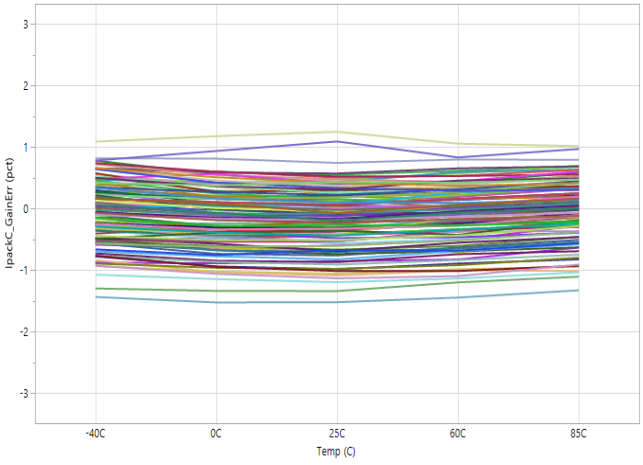



Figure 16. Charge Current GE

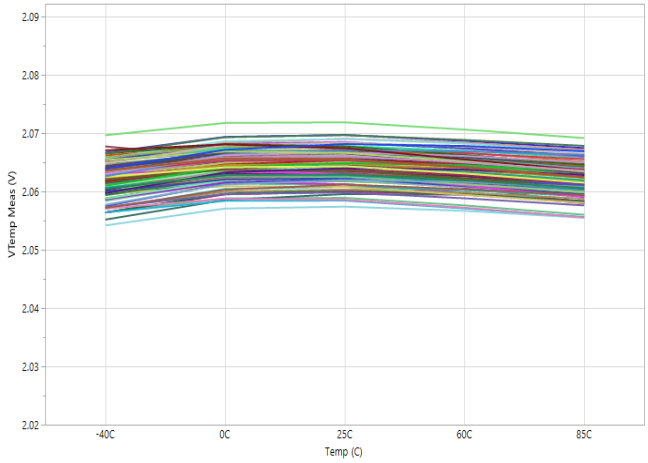



Figure 17. VTEMP Pin Voltage

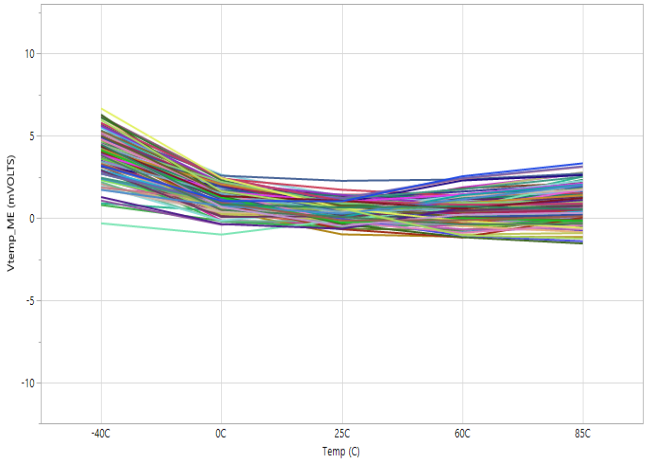



Figure 18. VTEMP Pin Voltage ME

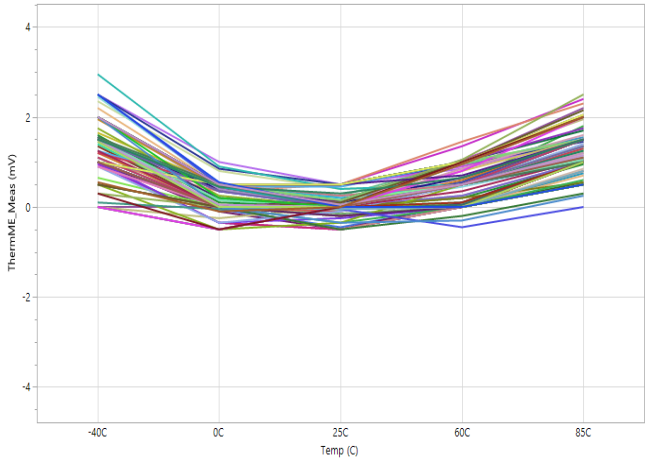



Figure 19. THERM Pins Voltage ME at 1V

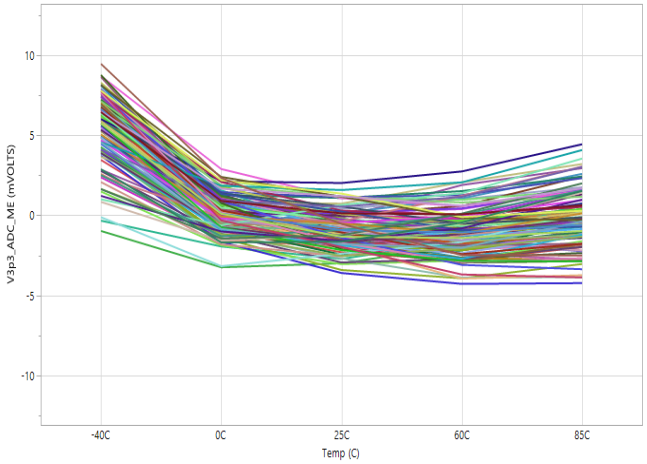



Figure 20. V3P3 Pin ME

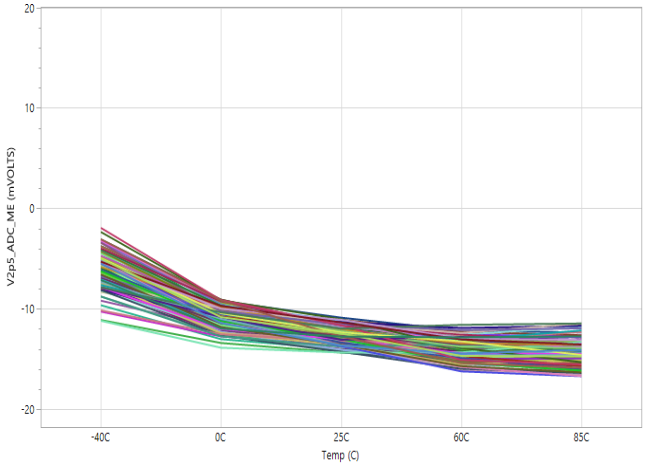



Figure 21. V2P5 Pin ME

# 5. State Machine Overview

## 5.1 System Modes

The State Machine flow diagram in Figure 22 shows the relationships between the device states and modes. A state executes its function then moves to the next state or mode, while modes can loop or remain static until another function or status change forces a transition out of the mode.

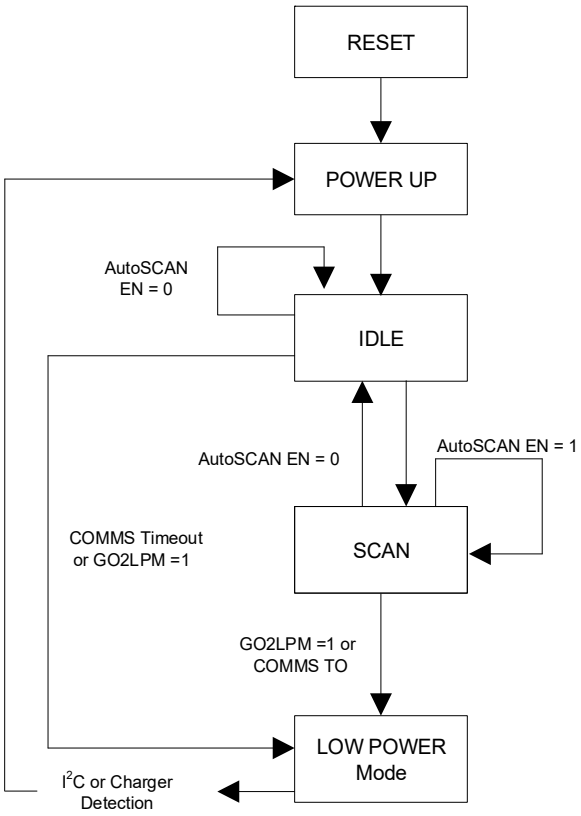



**Figure 22. State Machine Flow Diagram**

### 5.1.1 Reset State

At initial device power-up, the RAA489250B enters the RESET State. This state has the highest priority and is also initiated by a momentary connection of the THERM2 pin to the V3P3 pin (Hard RESET) or a VPACK voltage lower than $V_{POR}$ or the V2P5 or V3P3 voltages falling below their Power-On Reset (POR) thresholds. A RESET interrupts any action the device is performing.

The device turns off all regulators and oscillators when entering this state from a Hard RESET. On completion of RESET, the device transitions to the Power-Up State.

### 5.1.2 Power-Up State

The Power-Up State is entered from the RESET State. This state prepares the device for normal operation in IDLE Mode by executing device initialization followed by analog self test that checks the status of the IC.

On exiting the RESET State, the device turns on and checks the 4MHz oscillator and initializes logic states. It then reads trim/fuse settings, powers the monitor pins, powers the analog comparators and measurement amps, enables the FET driver (not the charge pump) and the ADC. An oscillator failure detected in the Power-Up State sets bit 0x10.10 OSCF and forces the device to transition to LOW POWER Mode.

If exiting from LOW POWER Mode, the device turns on and checks the 4MHz oscillator, which is followed by an analog self test that checks the status of the IC. Then, it powers the analog comparators, measurement amps, and the ADC.

On successful completion of initialization and analog self checks, the device transitions to IDLE Mode.

### 5.1.3 IDLE Mode

By default the MCU is in control of the system with the device in IDLE Mode (bit 0x80.8 AutoSCAN En is clear, unless otherwise noted). The MCU is responsible for triggering device measurements, enabling/disabling the power FET, and fault reaction. Faults detected in this state do not automatically turn off the power FET, except for short-circuit detections.

In IDLE Mode, the device executes commands from the MCU. The MCU is responsible for the state of the power FET and acts on faults or status changes. Section Fault Detection and Recovery lists the analog and digital faults. The $\overline{\text{ALERT}}$ pin asserts for faults and can assert for status bits provided the respective mask bit is cleared (0x11 Status).

Communication timeout in IDLE Mode is controlled by bits 0x80.[14:13] Communication TO. If the SDA pin does not make a high-to-low transition while the SCL pin is high within the selected period of time, the device transitions to LOW POWER Mode. Setting bit 0x40.5 Go2LPM to 1 also transitions the device to LP Mode.

Executing 0x41.7 Trigger Measurement causes a temporary transition to SCAN Mode to execute the 0x41.[4:0] Measurement Selection. When completed, the device transitions back to IDLE Mode to await the next MCU instruction.

Setting bit 0x80.8 AutoSCAN En to 1 causes the device to transition to SCAN Mode. Renesas recommends setting the 0x40.6 Clear All Faults to 1 before enabling AutoSCAN to initialize counters to 0.

### 5.1.4 SCAN Mode

SCAN Mode operation is dependent on the setting of control bits. If the 0x80.8 AutoSCAN En bit is clear (default), the device enters SCAN from IDLE when a measurement is triggered, and remains in SCAN Mode until the triggered measurement completes, then it transitions back to IDLE. If the AutoSCAN En bit is set to 1, the device continuously loops through the system scan sequence and remains in SCAN Mode (Figure 23). The only exceptions to these two cases is a fault or Go2LPM instruction causes a transition to LP Mode.

With AutoSCAN Enabled, the device continuously performs a scan sequence that measures the pack current, pack and cell voltages during each scan (Normal Loop). Every 4 scans, the thermistor voltages are measured. Every 100 scans, a series of self tests are executed if 0x42.14 Self Test En is set to 1. Measurement results are compared to the relevant thresholds during each scan they are executed. The sequence and timing of a complete system scan cycle is detailed in Figure 24. The time between scans is set by the 0x80.[12:11] Scan Delay bits.

If a fault is detected during AutoSCAN that requires CFET to turn OFF, the device asserts $\overline{\text{ALERT}}$ to signal the MCU to read the fault and status registers, then transitions to LP Mode after a 100µs delay. During the transition, no other functions are allowed. See 0x42.12 FETCON to enable or disable automatic FET control in AutoSCAN.

After exiting LP back to IDLE Mode, the MCU should issue a 0x40.6 Clear All Faults to initialize counters to 0.

Communications Timeout is active in both IDLE and SCAN Modes. The MCU has to initiate communication with the device within the selected time period. Allowing the communication timer to expire causes a transition from IDLE or SCAN to LOW POWER Mode.

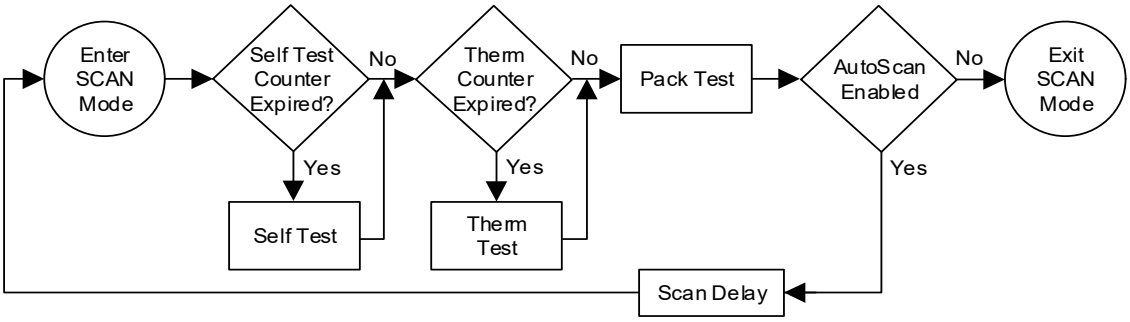



**Figure 23. System Scan Sequence**

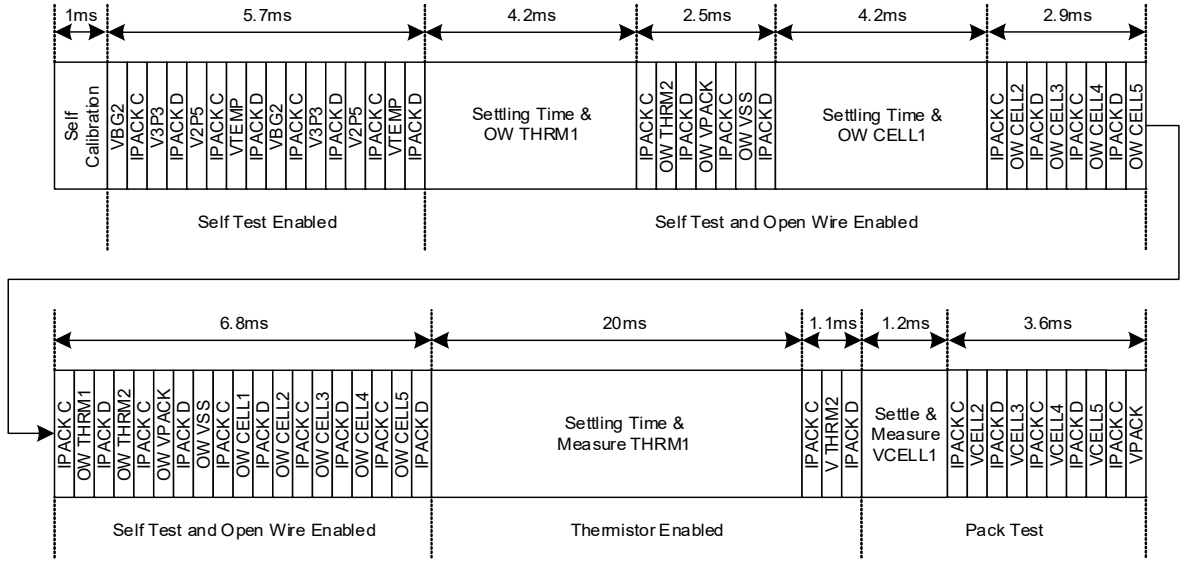



**Figure 24. Scan Sequence Timing**

## 5.1.5 LOW POWER Mode

The RAA489250B consumes the lowest current in LOW POWER (LP) Mode. Power FETs and all non-essential circuitry are OFF. In LP Mode, the device waits for a 0x11.3 CH PRESI bit transition from low to high to exit. Asserting the SDA pin while the SCL pin is high also exits this state.

The device transitions to LP Mode when a communication timeout occurs or when the bit 0x40.5 Go2LPM is set to 1 or if either IOTF or OSCF faults are set (see Table 3). Entry into LP Mode turns off CFET and stops the communication timeout timer.

Following a communications timeout, the $\overline{\text{ALERT}}$ pin is asserted and then the state does nothing for 100µs before proceeding to turn OFF the remainder of the sub blocks. The 100µs time delay allows the MCU to prepare itself for LP Mode. No other functions are allowed during this period. After the 100µs, the $\overline{\text{ALERT}}$ pin transitions to Hi-Z. On wakeup following a communications timeout, the $\overline{\text{ALERT}}$ pin is reasserted.

The regulator has two possible settings in this Mode determined by the setting of bit 0x42.13 LP Regulator, one setting keeps it fully enabled, and the other reduces current consumption to a minimum. The lowest powered state of the device is selected by setting LP Reg bit to 0, see Table 1.

The register values are retained in LP Mode with the LP Reg bit set to 1. If the LP Reg bit is clear, only the weak regulator is enabled so register values may or may not be retained. The weak regulator has limited drive capability. If the V3P3 node is overloaded, the regulator voltage might drop below the POR threshold causing the device to reset on wakeup.

After exiting LOW POWER back to IDLE Mode, the MCU should issue 0x40.6 Clear All Faults to initialize counters to 0.

**Table 1. LP Mode Settings**

| LP REG Bit (0x42.13) | Result |
|---|---|
| 0 | Weak Regulators; Register values are retained if Regulators remain above VPOR |
| 1 | Strong Regulator; Register and counter values are retained; VTEMP can be Active |

# 6. Faults

## 6.1 Fault Detection and Recovery

A fault is reported when the related fault threshold is exceeded for consecutive readings. For digital comparisons, fault delay is implemented with counters that are incremented for consecutive faulty readings; for analog comparisons fault delay is accomplished with timers. These counters/timers are cleared if the fault condition clears before they reach their limits.

A counter is incremented each time the device detects a fault while in SCAN Mode. If the fault counter exceeds the threshold, the device sets the respective fault bit.

When an analog comparison threshold is exceeded, a timer is started. If the timer also exceeds its threshold, the device sets the respective fault bit.

If a fault is reported, action can be taken to turn OFF the CFET. Table 2, Table 3, Table 4, and Table 5 show the power FET action related to specific fault conditions. These tables list the number of consecutive faults required before setting the fault bit.

Faults that turn OFF the CFET have recovery thresholds. Recovery thresholds are compared to the most recent measurement as long as the fault is present. Cell over/undervoltage, and charge over/under-temperature faults have separate recovery thresholds. The recovery threshold is fixed relative to the fault detection threshold voltage plus/minus a hysteresis. Overvoltage and charge over-temperature recovery thresholds are defined as the original threshold minus the respective hysteresis threshold. Under-temperature and undervoltage recovery thresholds are defined as the original threshold value plus the respective hysteresis value. If a measurement parameter does not have a recovery threshold, the fault detection threshold is also used for the recovery limit.

During the first and every 100th scan that follows, the SELF TEST Loop is executed if bit 0x42.14 Self Test En is set. A Self Test fault requires two consecutive detections to set. The device executes the SELF TEST Loop twice to determine if a fault is present. If a fault is present with each check, the fault bit is set and $\overline{\text{ALERT}}$ is asserted, then the device continues in SCAN mode unless the MCU commands otherwise.

## 6.2 Power FET Fault Response

The following tables show the FET reaction for each specific fault. Table 2 details the system fault response for digital compare faults that have no dependency on the power FET configuration bit 0x82.7 CPWR. Digital Compares require a Triggered System Scan or AutoSCAN measurement. Table 3 details the system fault response for analog compare faults that have no dependency on the power FET configuration bit CPWR. Analog compares do not require ADC measurements.

**Table 2. Digital Fault Response**

| Fault (Fault Flag) | CFET State | Compare Type | Seq Count | Comments |
|---|---|---|---|---|
| V3P3 (REGF) | OFF | Digital[1] | 2 | Device only controls FETs in SCAN Mode with 0x80.8 AutoSCAN En and FETCON enabled.<br>MCU controls FETs in IDLE Mode, and in SCAN Mode if AutoSCAN = 0 OR 0x42.12 FETCON = 0<br>Seq Count refers to the number of consecutive failures within a Scan, not the number of scans. |
| V2P5 (REGF) | OFF | Digital[1] | 2 | |
| VBG2 (REGF) | OFF | Digital[1] | 2 | |
| VTMPF | OFF | Digital[1] | 2 | |
| OWF | OFF | Digital[2] | 2 | |
| OW THERM | OFF | Digital[1] | 2 | |
| DOCF | OFF | Digital | 8 | |
| COCF | OFF | Digital | 8 | |

1. 0x42.14 Self Test En must be enabled.
2. 0x42.14 Self Test En and 0x80.15 Open Wire En must be enabled.

**Table 3. Analog Fault Response**

| Fault Flag | CFET State | Compare Type | Debounce Rise/Fall Time (ms) | Comments |
|---|---|---|---|---|
| OSCF | OFF | Analog | 0.5/0.002 | Device controls FETs in SCAN and IDLE Modes, these faults force the device to transition to LOW POWER Mode |
| IOTF | OFF | Analog | 1/1 | |
| COMMTO | OFF | Timer | 0x80.[13:12] | |
| CPF | OFF | Analog | 0.1/ 0.1 | Device controls FETs in SCAN and IDLE Modes |
| DSCF (SCF) | OFF | Analog | 0x83.[15:14] | |
| CSCF (SCF) | OFF | Analog | 0.1/ 0.1 | |

**Table 4. Parallel FET Fault Response**

| CPWR = 1<br>Fault Flag | CFET State | Number of Faults | Comments |
|---|---|---|---|
| DOT (OTF) | OFF | 2 | Device controls FETs in SCAN Mode with 0x80.8 AutoSCAN En and FETCON enabled.<br>MCU controls FETs in IDLE Mode, and in SCAN Mode if AutoSCAN = 0 OR 0x42.12 FETCON = 0<br>All Digital Compares |
| COT (OTF) | OFF | 2 | |
| CUT (UTF) | OFF | 2 | |
| DUT (UTF) | OFF | 2 | |
| OVLO (OVF, LOF) | OFF | 2 | |
| OV (OVF) | OFF | 2 | |
| UV (UVF) | ON | 2 | |
| UVLO (UVF, LOF) | OFF | 2 | |

**Table 5. Series FET Fault Response**

| CPWR = 0 | Charge Direction | | CFET State | Number of Faults | Comments |
|---|---|---|---|---|---|
| Fault Flag | CHRGI | DCHRGI | | | |
| DOT (OTF) | X | X | OFF | 2 | Device controls FETs in SCAN Mode with 0x80.8 AutoSCAN En and FETCON enabled.<br><br>MCU controls FETs in IDLE Mode, and in SCAN Mode if 0x42.12 FETCON = 0<br><br>All Digital Compares |
| COT (OTF) | X | 0 | OFF | 2 | |
| CUT(UTF) | X | 0 | OFF | 2 | |
| DUT (UTF) | X | X | OFF | 2 | |
| OVLO (OVF, LOF) | X | X | OFF | 2 | |
| OV (OVF) | X | 0 | OFF | 2 | |
| UV (UVF) | X | X | ON | 2 | |
| UVLO (UVF, LOF) | X | X | OFF | 2 | |

The power FET fault response for the CPWR = 1 parallel FET configuration setting is shown in Table 4 while the response for CPWR = 0 series FET setting is shown in Table 5. For CPWR dependent faults, the RAA489250B controls the CFET when bits 0x80.8 AutoSCAN En and 0x42.12 FETCON are enabled, otherwise the MCU is expected to control the power FETs.

# 7. System Registers

**Table 6. System Register List**

| Addr (Hex) | Register Name | Pg# | Register Description[1] | Default (Hex) |
|---|---|---|---|---|
| **Measurement Results (RO)** | | | | |
| 00 | Pack Voltage | 24 | [11:0] Step: 7.5mV; Range: POR to 28.8V | 0000 |
| 01 | Cell Max Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 02 | Cell Min Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 03 | Thermistor 1 | | [11:0] Step 0.5mV; Range -0.128V to 1.92V | 0000 |
| 04 | Thermistor 2 | | [11:0] Step 0.5mV; Range -0.128V to 1.92V | 0000 |
| 05 | Discharge Current | | [11:0] Step 13.16µV; Range -3.368mV to 50.526mV | 0000 |
| 06 | Charge Current | | [11:0] Step 13.16µV; Range -50.526mV to 3.368mV | 0000 |
| 20 | VTEMP | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 21 | Cell 1 Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 22 | Cell 2 Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 23 | Cell 3 Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 24 | Cell 4 Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |
| 25 | Cell 5 Voltage | | [11:0] Step: 1mV; Range: 0.512V to 4.608V | 0000 |

**Table 6. System Register List (Cont.)**

| Addr (Hex) | Register Name | Pg# | Register Description[1] | Default (Hex) |
|---|---|---|---|---|
| **Faults And Status** | | | | |
| 10 | Faults (RO) | 27 | [15] REGF<br>[14] OWF<br>[13] IOTF<br>[12] VTMPF<br>[11] CPF<br>[10] OSCF<br>[9] RSV<br>[8] COMMTO<br>[7] LOF<br>[6] OVF<br>[5] UVF<br>[4] OTF<br>[3] UTF<br>[2] SCF<br>[1] DOCF<br>[0] COCF | 0000 |
| 11 | Masks & Status<br>([15:8] R/W; [7:0] RO) | 31 | [15] Busy Mask (**1**)<br>[14] RSV (**1**)<br>[13] RSV (**0**)<br>[12] RSV (**0**)<br>[11] CH PRESI Mask (**1**)<br>[10:9] RSV (**11**)<br>[8] CPSSD (**0**)<br>[7] Busy (**0**)<br>[6] VTEMP Status (**0**)<br>[5] V3P3OK (**1**)<br>[4] RSV (**0**)<br>[3] CH PRESI (**0**)<br>[2] RSV (**0**)<br>[1] DCHRGI (**0**)<br>[0] CHRGI (**0**) | CE20 |
| **Set Up** | | | | |
| 40 | System Config 1<br>([15:8] RO; [7:0] R/W) | 33 | [15:11] RSV (**00000**)<br>[10] ALERT Status; 1 - Asserted, **0 - Clear**<br>[9] RSV (**0**)<br>[8] CFET Status; 1- CFET ON, **0- CFET OFF**<br>[7] Soft Reset; 1- Reset, **0- No Action**<br>[6] Clear All Faults; 1- clear All Faults and Counters, **0- No Action**<br>[5] GO2LPM; 1- Go to LOW POWER Mode, **0- No Action**<br>[4] CP_En; 1- Enable Charge Pump, **0- Disable charge pump**<br>[3] RSV (**0**)<br>[2] ALERT Pin Assert; 1- Assert, **0- Deassert**<br>[1] RSV (**0**)<br>[0] CFET_En; 1- CFET ON, **0- CFET OFF** | 0000 |
| 41 | Measure Select<br>([15:8] RO; [7:0] R/W) | 34 | [15] Trigger Busy; 1- Busy, **0- No Action**<br>[7] Trigger Measurement; 1- Trigger, **0- No Action**<br>[4:0] Measurement Select (**00000**) | 0000 |
| 42 | System Config 2<br>(R/W) | 36 | [15] VTEMP_En; 1- ON, **0- OFF**<br>[14] Self Test En; **1 - Enable**, 0 - Disable<br>[13] LP Reg; 1- Strong Regulator, **0- Weak Regulator**<br>[12] FETCON; 1- Enable auto FET control, **0- MCU FET control**<br>[11] Config Lock; **1- Regs 0x8n Locked**, 0- Regs 0x8n unlocked<br>[10:5] RSV (**000000**)<br>[4:0] CB_EN; 1- ON, **0- OFF** | 4800 |

**Table 6. System Register List (Cont.)**

| Addr (Hex) | Register Name | Pg# | Register Description[1] | Default (Hex) |
|---|---|---|---|---|
| **Thresholds (R/W with Key)** | | | | |
| 80 | System Config 3 | 37 | [15] OW En Cells; **0- Disable**, 1 - Enable<br>[14:13] Comm Timeout; 00- OFF, 01- 0.1s, 10- 1s, **11- 5s**<br>[12:11] Scan Delay; **00- 0s**, 01- 0.1s, 10- 0.5s, 11- 1s<br>[10:9] RSV (**00**)<br>[8] AutoSCAN En; **0- Disable**, 1 - Enable<br>[7:0] RSV (**0000 0000**) | 6000 |
| 81 | OV Thresholds | 38 | [15:8] Cell OV; Step 10mV; 2V to 4.55V; **Default 4.29V**;<br>[7:5] Cell OV Hysteresis; Step -50mV; Range: -50mV to -400mV **Default -150mV**<br>[4:0] Cell OVLO Step 50mV; 3.05V to 4.6V **Default 4.6V** | E55F |
| 82 | UV Thresholds | 39 | [15:8] Cell UV; Step 10mV, Range 0.512V to 3.06V, **Default (0.642 ---> 1.002V)**<br>[7] CPWR; 0- Serial Power FET Config, **1- Parallel Power FET Config**<br>[6:4] Cell UV Hysteresis; Step 100mV, Range 100mV to 800mV, **Default 300mV**<br>[3:0] Cell UVLO; Step 100mV, 0.512V to 2.01V, **Default 0.512V** (0x84.15 SUVLO = 0) | 31A0 |
| 83 | SC, OT & UT Thresholds | 40 | [15:14] SSC Delay: 00- OFF, 01- 0.1ms, **10- 1ms**, 11- 10ms<br>[13:11] DOT; Range 0.268V to 0.107V, **Default 0.157V**<br>[10:8] DUT; Range 1.804V to 1.18V **Default 1.583V**<br>[7:6] Therm Enable; 00- Off, 01- THERM1, **10- Both**, 11- Both (no faults for Therm2)<br>[5:3] COT; Range 0.528V to 0.205V, **Default 0.307V**<br>[2:0] CUT; Range 1.583V to 0.866V, **Default 1.18V** | A3A4 |
| 84 | Current Thresholds | 44 | [15] SUVLO; 1- Add 1.002V to UVLO Threshold, **0- No Action**<br>[14:12] SSC; 000- 12.5mV, 001- 25mV, 010- 50mV, 011- 100mV, **100- 200mV**<br>[11:6] DOC; Step 1mV, 1mV to 51mV, **Default 50mV**<br>[5:0] COC; Step -1mV, -1mV to -51mV, **Default -50mV** | 4C71 |
| **Product Information (Read Only Bits)** | | | | |
| FD | Die Revision | | [3:0] Die Revision | 0006 |
| FE | Manufacturing ID | | [7:0] Manufacturing ID | 0049 |
| FF | Device ID | | [7:0] Device ID | 0014 |

1. Bold text indicates default value.

# 7.1 Calculating Thresholds and Readings

## 7.1.1 Measurement Reads

The RAA489250B stores the results of 13 measurements (VPACK, $V_{CELL}$ Max, $V_{CELL}$ Min, Thermistor 1, Thermistor 2, $I_{PACK}$ Discharge, $I_{PACK}$ Charge, VTEMP, and VCELL1-5) with every complete scan sequence. Additional measurements are accessible by executing a single triggered scan (see 0x41.[4:0] Measurement Selection).

**Table 7. Measurement Registers**

| Register Name | Bit Function | | | | | | | | Default Value (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) | |
| Measurement (Upper Byte) | RSV | RSV | RSV | RSV | Bit11 | Bit10 | Bit9 | Bit8 | 00 |
| Measurement (Lower Byte) | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00 |

Use Equation 1 to calculate the decimal result from the register value.

**(EQ. 1)** $$MEAS = (RegVal) \cdot MEAS_{Step} + MEAS_{Min}$$

Table 8 shows the constants used in Equation 1 to calculate the voltage for each of the 10 possible measurement result by type.

**Table 8. Measurement Constants**

| Measured Parameter | Electrical Spec pg# | Coefficients | | Max Val ADC Code 0xFFF | Min Val ADC Code 0x000 | Unit | Comments |
|---|---|---|---|---|---|---|---|
| | | $MEAS_{Step}$ | $MEAS_{Min}$ | | | | |
| VPACK | 10 | 0.0075 | -1.92 | 28.8 | -1.92 | V | Usable Range: POR to 28.8V |
| $V_{CELL}$ | 9 | 0.001 | 0.512 | 4.608 | 0.512 | V | |
| Thermistors | 10 | 0.0005 | -0.128 | 1.92 | -0.128 | V | Usable range begins at 0V (0x100) |
| $I_{PACK}$ | 9 | 0.0132 | -3.368 | ±50.5266 | -3.368 | mV | Usable range begins at ±200µV |
| VTEMP | 10 | 0.001 | 0.512 | 4.608 | 0.512 | V | |
| V3P3 | 10 | 0.001 | 0.512 | 4.608 | 0.512 | V | |
| V2P5 | 10 | 0.001 | 0.512 | 4.608 | 0.512 | V | |
| VBG2 | N/A | 0.0005 | -0.128 | 1.92 | -0.128 | V | Usable range begins at 0V (0x100) |

#### 7.1.1.1 Internal Temperature

The Internal temperature sensor is not calibrated and is only intended for comparisons to the internal over-temperature fault threshold. This sets bit 0x10.13 IOTF to shut down the device at extreme high temperature. The sensor is not provided to indicate die temperature significantly below the IOTF threshold.

### 7.1.2 Digital Thresholds

Digital Thresholds are compared to the relevant ADC measurement results at the time they are made. Single triggered measurements (0x41.7 Trigger Measurement) executed in IDLE Mode sets the related fault bit if a threshold is violated but does not shut off the CFET. Threshold violations in AutoSCAN (0x80.8 AutoSCAN En) can shut off the CFET in specific cases. The power FET response and the conditions required to set the fault are found in Fault Detection and Recovery.

The faults related to these thresholds are automatically cleared when a subsequent measurement indicates the voltage has moved to within the allowed range determined by the threshold combined with its hysteresis. See Recovery Threshold for more information. Not all thresholds have settable hysteresis.

#### 7.1.2.1 $V_{CELL}$ Thresholds

The RAA489250B has programmable thresholds to monitor cell voltages. Cell Overvoltage Lockout (0x81.[4:0] $V_{CELL}$ OVLO), Cell Overvoltage (0x81.[15:8] $V_{CELL}$ OV), Cell Undervoltage (0x82.[15:8] $V_{CELL}$ UV), Cell Undervoltage Lockout (0x82.[3:0] $V_{CELL}$ UVLO), and Delta Cell Overvoltage (0x82.[15:8] $V_{CELL}$ UV) thresholds are digitally compared after every cell voltage measurement. The device has two levels of thresholds for overvoltage and undervoltage detection.

OV and OVLO threshold violations set bit 0x10.6 OVF to 1 when a cell voltage reading is above either threshold. Conversely, UV and UVLO threshold violations set bit 0x10.5 UVF to 1 when a cell voltage reading is below either threshold. Bit 0x10.7 LOF also sets if the OVLO or UVLO thresholds are violated.

#### 7.1.2.2 Temperature Thresholds

Discharge Over-Temperature (0x83.[13:11] DOT), Charge Over-Temperature (0x83.[5:3] COT), Charge Under-Temperature (0x83.[2:0] CUT) and Discharge Under-Temperature (0x83.[10:8] DUT) thresholds are compared to THERM pin measurements. The thresholds assume a negative temperature coefficient thermistor, see VTEMP, THERMn Pins.

The over-temperature and under-temperature thresholds are digitally compared to each THERM pin measurement. If the voltage measurement at the pin is lower than the over-temperature threshold, the bit 0x10.4 OTF is set to 1. If the voltage measurement at the pin is higher than the under-temperature threshold, the bit 0x10.3 UTF is set to 1.

For 0x82.7 CPWR = 0; if bit 0x11.0 CHRGI is set, the voltages are compared to the Charge thresholds. If bit 0x11.1 DCHRGI is set, the voltages are compared to the Discharge thresholds. For 0x82.7 CPWR = 1, both charge and discharge thresholds are compared, see Setting OT/UT Thresholds.

#### 7.1.2.3 $I_{PACK}$ Thresholds

The discharge overcurrent threshold (0x84.[11:6] DOC) is digitally compared to the discharge current measurement. Results are greater than this threshold set bit 0x10.1 DOCF to 1.

The charge overcurrent threshold (0x84.[11:6] DOC) operates in a similar manner as the discharge overcurrent threshold. The device detects when a charge current measurement is below the threshold and sets bit 0x10.0 COCF to 1.

#### 7.1.2.4 Threshold Equations

Use Equation 2 to calculate the decimal threshold value from the digital value.

**(EQ. 2)** $$THRESHOLD = (RegVal) \cdot THRESHOLD_{Step} + THRESHOLD_{MIN}$$

Use Equation 3 to calculate the digital threshold value from the decimal value.

**(EQ. 3)** $$REGVal = Integer\left[\frac{(THRESHOLD_{Value} - THRESHOLD_{MIN})}{THRESHOLD_{STEP}}\right]$$

Table 9 lists the constants to be used in Equation 2 and Equation 3 for each threshold.

**Table 9. Threshold Constants**

| Threshold | Reg Val (Hex) | # of Bits | Coefficients | | Max Val ADC Code | Min Val ADC Code | Unit |
|---|---|---|---|---|---|---|---|
| | | | $Threshold_{Step}$ | $Threshold_{Min}$ | | | |
| OVLO | 81.[4:0] | 5 | 0.05 | 3.05 | 4.6 | 3.05 | V |
| OV | 81.[15:8] | 8 | 0.01 | 2.0 | 4.55 | 2.0 | V |
| UV | 82.[15:8] | 8 | 0.01 | 0.512 | 3.06 | 0.512 | V |
| UVLO (SUVLO=0) | 82.[3:0] | 4 | 0.1 | 0.512 | 2.01 | 0.512 | V |
| UVLO (SUVLO=1) | 82.[3:0] | 4 | 0.1 | 1.514 | 3.012 | 1.514 | V |
| DOC | 84.[11:6] | 6 | 1 | -1 | 50 | 1 | mV |
| COC | 84.[5:0] | 6 | -1 | -1 | -1 | -50 | mV |

#### 7.1.2.5 Recovery Threshold

Thermistor temperature (COT, CUT), cell overvoltage (OV) and undervoltage (UV) thresholds have recovery threshold hysteresis settings. When a thermistor or cell voltage reading exceeds its respective threshold, the device signals by setting the related fault bit. After detecting the fault, the device compares subsequent readings to the threshold with hysteresis before clearing the fault.

The remaining thresholds do not have adjustable hysteresis, the recovery voltage to clear the faults is set by the threshold alone.

#### 7.1.2.6 Hysteresis Setting

The hysteresis setting is a value added to or subtracted the original threshold to set a voltage recovery level. Use Equation 4 to calculate the recovery threshold value. $OV_{hys}$ (0x81.[7:5] $V_{CELL}$ OV Hysteresis) and $UV_{hys}$

(0x82.[6:4] $V_{CELL}$ UV Hysteresis) have programmable hysteresis settings while COT and CUT hysteresis is a fixed value of ~5C based on the threshold selection.

**(EQ. 4)** $$HystersisThresh = THRESHOLD + HysteresisVal$$

Use Equation 5 and the constants listed in Table 9 to calculate the digital hysteresis value.

**(EQ. 5)** $$REGVal = Integer\left[\frac{(Hysteresis_{Value} - Hysteresis_{MIN})}{Hysteresis_{STEP}}\right]$$

Use Equation 6 and the constants listed in Table 9 to calculate the decimal hysteresis value.

**(EQ. 6)** $$Hysteresis_{Value} = (RegVal) \cdot Hysteresis_{Step} + Hysteresis_{MIN}$$

For an OV threshold setting of 4.2V and a hysteresis setting of -100mV, the recovery threshold becomes 4.1V. Following an OVF, the device uses the recovery threshold of 4.1V to compare each cell voltage until the maximum cell voltage reads below the 4.1V threshold, which then clears the OVF bit.

**Table 10. Hysteresis Constants**

| Hysteresis Threshold | Reg Val Hex | # Of Bits | Constants | | Max Val ADC Code | Min Val ADC Code | Unit |
|---|---|---|---|---|---|---|---|
| | | | $Hysteresis_{Step}$ | $Hysteresis_{Min}$ | | | |
| OV | 81.[6:4] | 3 | -0.05 | -0.05 | -0.4 | -0.05 | V |
| UV | 82.[6:4] | 3 | +0.1 | +0.1 | 0.8 | 0.1 | V |

## 7.2 Register Definitions

RAA489250B operation is controlled by configuration registers and monitored by measurement result, status, and fault registers. Default values for settings using multiple bits are highlighted in gray.

### 7.2.1 0x10 Faults

See Faults and ALERT Pin 19 for additional details on the device fault reactions. The $\overline{ALERT}$ pin is asserted when a fault bit is set. The $\overline{ALERT}$ pin is released on read of the Fault and Status registers but the fault bits are not cleared by this action.

If the 0x11.15 BUSY Mask bit is clear so the MCU can monitor device 0x11.7 BUSY status, the digital compare faults do not assert $\overline{ALERT}$. Fault and Status registers should be read following triggered measurements when the busy mask bit is clear. Analog compare faults are not blocked, see Faults.

The fault bits are cleared on reset, or on retest if the fault condition has cleared, or by setting the bit 0x40.6 Clear All Faults to 1.

**Table 11. Fault Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x10.[15:8] | REGF | OWF | IOTF | VTMPF | CPF | OSCF | RSV | COMMTO | 00 |
| 0x10.[7:0] | LOF | OVF | UVF | OTF | UTF | SCF | DOCF | COCF | 00 |

#### 7.2.1.1 0x10.15 REGF

The REG Fault bit reports under/overvoltage conditions at the V3P3 and V2P5 pins and the VBG2 block using digital comparators. VBG2 is the reference that generates the V3P3 voltage. These tests are performed in the SELF TEST loop of the system scan if 0x42.14 Self Test En is set.

The REGF bit is set to 1 when the voltage exceeds the digital threshold for two consecutive measurements. The device takes no other action for a REGF unless 0x42.12 FETCON and 0x80.8 AutoSCAN En are both enabled. Then, the device automatically shuts off the CFET.

The V3P3 and V2P5 regulators also have power-good analog comparators ($PG_{V3P3\_OV}$) that monitor the pin voltages. If a violation occurs, the device performs a power on reset. This action does not set the REGF bit.

#### 7.2.1.2 0x10.14 OWF

The Open-Wire Fault bit is set to 1 when VSS, VPACK or a VC# pin fails the Open-Wire digital thresholds for two consecutive measurements. The test is performed in the SELF TEST loop of the system scan if 0x42.14 Self Test En and 0x80.15 Open Wire En are both set. 0x42.12 FETCON and 0x80.8 AutoSCAN En must both be enabled for automatic shutoff of the CFET due to an OWF.

The VSS and VPACK OW comparators have debounce timers of ~100µs. Because these pins are compared to the cell sense input pins, the VPACK and VC# pin filters must have similar time constants.

#### 7.2.1.3 0x10.13 IOTF

The Internal Over-Temperature Fault bit is set when the device die temperature exceeds ~100°C. The device continuously monitors its temperature in IDLE and SCAN Modes. When IOTF sets, the device transitions to LP Mode.

The bit clears when the die temperature drops below ~75°C.

#### 7.2.1.4 0x10.12 VTMPF

The VTEMP Fault bit is set when the measured voltage exceeds the analog thresholds for two consecutive measurements or when at least one thermistor pin (THERM1 or THERM2) fails the open-wire test for thermistors. These tests are performed in the SELF TEST loop (if enabled) of the system scan and at least one of the thermistors must be enabled (0x83.[7:6] Thermistor Enable). 0x42.12 FETCON and 0x80.8 AutoSCAN En must both be enabled for automatic shutoff of the CFET due to an VTMPF.

#### 7.2.1.5 0x10.11 CPF

The Charge Pump Fault bit indicates the voltage between the VCP and VPACK pins is below the analog threshold required to drive the CFET. A 1 indicates that the charge pump is not ready for use. The CFET is disconnected from the charge pump if the CPF bit is set. The device clears the CPF bit automatically when the charge pump voltage reaches the acceptable range ($V_{pmpMin}$) and the CFET is reconnected to the charge pump if it was previously enabled.

This bit is set to 1 at power up until the voltage on the charge pump pin reaches ~7.5V, then the CPF bit is automatically cleared. If the voltage on the charge pump falls below ~5.0V ($V_{pmpFall}$), the CPF bit is set to 1.

#### 7.2.1.6 0x10.10 OSCF

The Oscillator Fault bit is set if the oscillator frequency shifts out of range. This is constantly monitored in IDLE and SCAN Modes. There is no enable bit to gate this monitor. An OSCF forces the device to transition to LP Mode.

The bit is automatically cleared to 0 when the fault condition has cleared.

#### 7.2.1.7 0x10.8 COMMTO

The Communication Timeout bit is set to 1 if the device has not received a valid serial communication from the MCU within the period set by 0x80.[14:13] Communication TO. A communication timeout fault forces the device to transition to LOW POWER Mode.

The bit is cleared to 0 when the device resets, when the Fault register is read, a valid serial communication has been received, or by setting the bit 0x40.6 Clear All Faults to 1. This bit is not latched, an attempt to read this bit clears it.

A valid serial communication is defined as when the SDA line is pulled low by the MCU while the SCL line is high.

#### 7.2.1.8 0x10.7 LOF

The Lockout Fault bit is set to 1 when either the 0x81.[4:0] $V_{CELL}$ OVLO or 0x82.[3:0] $V_{CELL}$ UVLO digital thresholds are violated. Reading this bit combined with bits 0x10.6 OVF and 0x10.5 UVF informs the system which lockout threshold was violated. The test is performed in the normal loop of the system scan.

The device does not disable the CFET for an LOF if a Single System Scan is triggered (0x41.[4:0] Measurement Selection). 0x42.12 FETCON and 0x80.8 AutoSCAN En must both be enabled for automatic shutoff of the CFET due to an LOF.

The LOF bit is cleared when the device resets, or on retest when all cell voltages are >UVLO and <OVLO thresholds, or by setting the bit 0x40.6 Clear All Faults to 1.

#### 7.2.1.9 0x10.6 OVF

The Overvoltage Fault bit is set when at least one cell voltage measurement exceeds the OV digital threshold. The device compares the maximum cell voltage to 0x81.[15:8] $V_{CELL}$ OV and 0x81.[4:0] $V_{CELL}$ OVLO thresholds for each system scan. The OVF bit setting is a logic OR of the two comparisons. An OVLO failure takes precedence over an OV failure. The test is performed in the normal loop of the system scan.

The OVF fault has a recovery threshold set by 0x81.[7:5] $V_{CELL}$ OV Hysteresis that enables the device to clear the fault after the measured cell voltages drop below the setting. See Recovery Threshold for more details.

The device does not disable the CFET for an OVF if a Single System Scan is triggered (0x41.[4:0] Measurement Selection). 0x42.12 FETCON and 0x80.8 AutoSCAN En must both be enabled for automatic shutoff of the CFET due to an OVF.

The OVF bit is cleared when the device resets, or when the maximum cell reading measures below both OV and OVLO thresholds, or by setting the bit 0x40.6 Clear All Faults to 1.

#### 7.2.1.10 0x10.5 UVF

The Undervoltage Fault bit is set when at least one cell voltage measurement falls below the UV digital threshold. The device compares the minimum cell voltage to 0x82.[15:8] $V_{CELL}$ UV and 0x82.[3:0] $V_{CELL}$ UVLO thresholds for each system scan. The UVF bit setting is a logic OR of the two comparisons. A UVLO failure takes precedence over an UV failure. The test is performed in the normal loop of the system scan.

The UVF fault has a recovery threshold set by 0x82.[6:4] $V_{CELL}$ UV Hysteresis that enables the device to clear the fault after the measured cell voltages rise above the setting. See Recovery Threshold for details.

The RAA489250B does not disable the CFET for a UVF regardless of 0x42.12 FETCON and 0x80.8 AutoSCAN En settings.

The UVF bit is cleared when the device resets, or when the minimum cell reading measures above both UV and UVLO thresholds, or by setting the bit 0x40.6 Clear All Faults to 1.

#### 7.2.1.11 0x10.4 OTF

The Over-Temperature Fault bit is set when an enabled thermistor voltage reading is below the OT threshold. This fault asserts $\overline{\text{ALERT}}$ regardless of the setting of bit 0x11.15 BUSY Mask. The device assumes a Negative Temperature Coefficient (NTC) thermistor on the THERM pin. Table 27 lists example threshold settings represented as pin voltages, ADC codes and temperature.

The device compares the voltage readings of the enabled THERM pin to the 0x83.[13:11] DOT and 0x83.[5:3] COT thresholds in the THERM loop of the system scan (Figure 23) and also when individual THERM pin's voltage measurement is triggered (Table 14). Single triggered THERM pin measurements are compared to the thresholds with one exception. If bits 0x83.[7:6] Thermistor Enable are set to 11, THERM2 is not compared.

If the device detects a discharge current (0x11.1 DCHRGI), the DOT threshold is used. If a charge current is detected (0x11.0 CHRGI), the COT threshold is used. A DOT failure takes precedence over a COT failure.

0x42.12 FETCON and 0x80.8 AutoSCAN En must both be enabled for automatic shutoff of the CFET due to an OTF.

The COT recovery threshold is a fixed hysteresis of approximately 5°C below the COT Threshold. The DOT threshold has no hysteresis.

The OTF bit is cleared when the device resets, or when the thermistor voltage measurement rises above the violated threshold, or by setting the bit 0x40.6 Clear All Faults to 1.

#### 7.2.1.12 0x10.3 UTF

The Under-Temperature Fault bit is set when the voltage reading of an enabled thermistor is above the UT threshold. This fault asserts $\overline{\text{ALERT}}$ regardless of the setting of bit 0x11.15 BUSY Mask. The device assumes an NTC thermistor on the THERM pin. Table 27 lists example threshold settings represented as pin voltages, ADC codes and temperature.

The device compares the voltage readings of the enabled THERM pin to the 0x83.[10:8] DUT and 0x83.[2:0] CUT thresholds in the THERM loop of the system scan (Figure 23) and also when individual THERM pin's voltage measurement is triggered (Table 14). Single triggered THERM pin measurements are compared to the thresholds with one exception. If bits 0x83.[7:6] Thermistor Enable are set to 11, THERM2 is not compared.

If the device detects a discharge current (0x11.1 DCHRGI), the DUT threshold is used. If a charge current is detected (0x11.0 CHRGI), the CUT threshold is used. A DUT failure takes precedence over a CUT failure.

0x42.12 FETCON and 0x80.8 AutoSCAN En must both be enabled for automatic shutoff of the CFET due to an OTF.

The CUT recovery threshold is a fixed hysteresis of approximately 5°C above the CUT Threshold. The DUT threshold has no hysteresis.

The UTF bit is cleared when the device resets, or when the thermistor voltage measurement drops below the violated threshold, or by setting the bit 0x40.6 Clear All Faults to 1.

#### 7.2.1.13 0x10.2 SCF

The Short-Circuit Fault bit is a logic OR of the analog short-circuit comparisons for both discharge (DCSP - CSN) and charge (CCSP-CSN) sense resistors. If the discharge voltage exceeds the Threshold 0x84.[14:12] DSC for the 0x83.[15:14] SCC Delay time, the SCF bit is set to 1. The charge current short-circuit threshold is fixed at -200mV, a violation of this threshold sets the SCF bit to 1 independent of the SCC Delay time setting (see Table 3).

The RAA489250B disables the CFET for a SCF regardless of 0x42.12 FETCON and 0x80.8 AutoSCAN En settings. On detection of an SCF, the MCU should clear bit 0x40.0 CFET En until the short-circuit is removed.

The bit clears if the device is reset, or by setting the bit 0x40.6 Clear All Faults to 1. If the fault condition is still present, this bit sets again.

#### 7.2.1.14 0x10.1 DOCF

The Discharge Overcurrent Fault bit reports the result of the discharge overcurrent digital comparison. If the $I_{PACK}$ discharge (DCSP-CSN) measurement result is above the 0x84.[11:6] DOC threshold for eight consecutive measurements (not scans), bit DOCF is set to 1. $I_{PACK}$ current is measured multiple times during each scan. The test is performed in the normal loop of a system scan (Figure 23). The eight consecutive measurements can be individual triggered measurements triggered eight consecutive times over a long period of time. The counter is reset by setting the 0x40.6 Clear All Faults bit to 1.

A DOCF disables the CFET if detected during AutoSCAN and bit 0x42.12 FETCON is set.

The device does not change Modes for a DOCF for single triggered scans, the Controller controls the CFET and Mode transitions.

The bit clears when the device resets, when the measurement reads below the DOC threshold, or by setting the bit 0x40.6 Clear All Faults to 1.

#### 7.2.1.15 0x10.0 COCF

The Charge Overcurrent Fault bit reports the result of the charge overcurrent digital comparison. If the $I_{PACK}$ charge (CCSP-CSN) measurement result magnitude is above the 0x84.[5:0] COC threshold for eight consecutive measurements (not scans), bit COCF is set to 1. $I_{PACK}$ current is measured multiple times during each scan. The test is performed in the normal loop of a system scan (Figure 23). The eight consecutive measurements can be individual triggered measurements triggered eight consecutive times over a long period of time. The counter is reset by setting the 0x40.6 Clear All Faults bit to 1.

A COCF disables the CFET if detected during AutoSCAN and bit 0x42.12 FETCON is set.

The device does not change Modes for a COCF while in IDLE Mode. The Controller controls the CFET and Mode transitions while in IDLE.

The bit clears when the device resets, when the measurement reads above the COC threshold, or by setting the bit 0x40.6 Clear All Faults to 1.

### 7.2.2 0x11 Status

The device STATUS register includes device status information and mask bits that if cleared, enables the related status bit to assert ALERT Pin 19.

**Table 12. Status Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x11.[15:8] **R/W** | BUSY Mask | RSV | RSV | RSV | CH PRESI Mask | RSV | RSV | CPSSD | CE |
| 0x11.[7:0] **RO** | BUSY | VTEMP | V3P3OK | RSV | CH PRESI | RSV | DCHRGI | CHRGI | 20 |

#### 7.2.2.1 0x11.15 BUSY Mask

The Busy Mask bit connects the 0x11.7 BUSY Bit status to the $\overline{\text{ALERT}}$ pin by asserting the pin to VSS when the device is making measurements. A mask bit setting of 0 connects the Busy bit status to the pin. A mask bit setting of 1 (default) disables this connection. The Busy Bit is only operational during continuous or single triggered system scans.

When set to 1, this mask does not block faults from asserting the $\overline{\text{ALERT}}$ pin. However, when set to 0, the $\overline{\text{ALERT}}$ pin follows the status of 0x11.7 BUSY. When the Busy status is routed to the $\overline{\text{ALERT}}$ pin, this blocks faults based on digital compares from asserting $\overline{\text{ALERT}}$. Fault and Status registers should be read following triggered measurements when the busy mask bit is clear. Analog compare faults are not blocked, see Faults.

#### 7.2.2.2 0x11.[14:12] RSV

These bits are set to 100 by default and return this value on read. The default value for these bits should be used when writing to this register.

#### 7.2.2.3 0x11.11 CH PRESI Mask

The Charger Present Mask bit connects the status of the 0x11.3 CH PRESI bit to the $\overline{\text{ALERT}}$ pin if set to 0. A mask bit setting of 1 (default) disables this connection.

With the mask bit setting of 0, a CH PRES bit transitioning from 0 to 1 results in the $\overline{\text{ALERT}}$ pin being asserted to VSS until the Controller reads faults and status from the device. When the read has occurred the status bit is cleared and the $\overline{\text{ALERT}}$ pin returns to a high-impedance state.

The Charger Present bit can change states freely for a Charger Present Mask bit setting of 1.

#### 7.2.2.4 0x11.[10:9] RSV

These bits are set to 11 by default and return this value on read. The default value for these bits should be used when writing to this register.

#### 7.2.2.5 0x11.8 CPSSD

The Charge Pump Soft-Start Done bit indicates the status of the soft-start function for the charge pump. Following the enable of the charge pump by setting bit CP_EN to 1, the soft-start masks the CPF bit until either the VCP pin voltage minimum ($V_{pmpMin}$) is reached or the timer reaches 50ms. A 1 indicates that the charge pump has completed soft-start and the CPF bit is active. The power FETs cannot be enabled if CPSSD is not set.

#### 7.2.2.6 0x11.7 BUSY

The Busy bit reports whether the device is busy measuring parameters or executing SELF TEST while the device is running single triggered system scans or 0x80.8 AutoSCAN En. The bit is set to 1 when the device is busy, 0 indicates that device is idle or between automatic scans during 0x80.[12:11] Scan Delay.

This bit status can be connected to the $\overline{\text{ALERT}}$ pin by clearing the 0x11.15 BUSY Mask.

#### 7.2.2.7 0x11.6 VTEMP Status

The VTEMP Status bit reports whether the VTEMP output is ON or OFF. A 1 indicates the VTEMP output is ON, otherwise the VTEMP output is OFF.

#### 7.2.2.8 0x11.5 V3P3OK

The V3P3 OK bit is set to 1 when the pin voltage falls within the normal range, or set to 0 if high or low. The voltage is monitored by an analog comparator when the device is in IDLE or SCAN Mode. The device takes no automatic action based on this bit. The normal range is defined by $PG_{V3P3\_UV}$ and $PG_{V3P3\_OV}$.

#### 7.2.2.9 0x11.4 RSV

This bit is set to 0 by default and returns this value on read. The default value for this bit should be used when writing to this register.

#### 7.2.2.10 0x11.3 CH PRESI

The Charge Present status bit is set to 1 (level triggered) when the voltage at the CHMON pin rises above the threshold $V_{CHTHR}$. The bit is not latched if the CH PRESI Mask bit is set to 1. A CH PRESI bit transition from 0 to 1 wakes the device from LP Mode (edge triggered). The device begins monitoring 100ms after CFET turns OFF. See CHMON Pin 26 for more about the charger detection circuit.

If the CH PRESI Mask bit is set to 0, the CH PRESI bit is latched until the Controller reads the Fault and Status registers. The latched bit results in the $\overline{\text{ALERT}}$ pin asserting until the register reads.

The CHMON Pin connects to the top of the positive charger terminal.

#### 7.2.2.11 0x11.2 RSV

This bit is set to 0 by default and returns this value on read. The default value for this bit should be used when writing to this register.

#### 7.2.2.12 0x11.1 DCHRGI

The Discharge Current Indicator bit sets if charge is being removed from the battery pack. If the current sense resistor voltage measurement is greater than approximately 600µV (IDCHRGI), the DCHRGI bit is set to 1.

The DCHRGI bit is set when there are two consecutive readings greater than the DCHRGI threshold, either with two single triggered discharge current measurements or a single triggered system scan. The bit is set to 0 when a single $I_{PACK}$ measurement falls below the DCHRGI threshold. This bit is not latched.

Some fault responses are gated by DCHRGI bit status and the bit 0x82.7 CPWR setting. The Power FET Fault Response lists the FET behavior versus faults.

#### 7.2.2.13 0x11.0 CHRGI

The Charge Current Indicator bit sets if charge is being added to the battery pack. If the current sense resistor voltage measurement is less than approximately -600µV (ICHRGI), the CHRGI bit is set to 1.

The CHRGI bit is set when there are two consecutive readings below the CHRGI threshold, either with two single triggered charge current measurements or a single triggered system scan. The bit is set to 0 when a single $I_{PACK}$ measurement rises above the CHRGI threshold. This bit is not latched.

Some fault responses are gated by CHRGI bit status and the bit 0x82.7 CPWR setting. The Power FET Fault Response lists the FET behavior versus faults.

## 7.2.3 0x40 System Config 1

The System Configuration 1 register includes control bits for resetting the device, clearing the faults register, Mode change, charge pump, and CFET. It also includes a bit to test the $\overline{\text{ALERT}}$ pin and status bits for the ALERT function and CFET.

**Table 13. System Config 1 Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x40.[15:8] **RO** | RSV | RSV | RSV | RSV | RSV | $\overline{\text{ALERT}}$ | RSV | CFET | 00 |
| 0x40.[7:0] **RW** | Soft Reset | Clear All Faults | GO2LPM | CP_En | RSV | $\overline{\text{ALERT}}$ Assert | RSV | CFET_EN | 00 |

### 7.2.3.1 0x40.[15:11] RSV

These bits are set to 00000 by default and return this value on read. The default value for these bits should be used when writing to this register.

### 7.2.3.2 0x40.10 $\overline{\text{ALERT}}$ Status

The read only $\overline{\text{ALERT}}$ status bit indicates the status of the $\overline{\text{ALERT}}$ function while in operation. A 1 indicates the device is busy measuring (0x11.15 BUSY Mask is clear) or signaling a fault or change in status. A 0 indicates no new faults or change in status have been detected since the MCU has read the Faults and Status registers (this action releases the $\overline{\text{ALERT}}$ pin).

### 7.2.3.3 0x40.9 RSV

This bit is set to 0 by default and returns this value on read. The default value for this bit should be used when writing to this register.

### 7.2.3.4 0x40.8 CFET Status

The read only CFET status bit confirms the CFET pin output is enabled. A 1 indicates the output is enabled while a 0 indicates it is disabled.

### 7.2.3.5 0x40.7 Soft RESET

Setting the Soft Reset bit to 1 forces the state machine to jump to the Reset State, that resets all register values to the factory defaults, including data registers. The device then proceeds through the Power-Up State before it enters IDLE Mode. The bit action is equivalent to a hard reset or a power-on reset (POR) event. All counters and state machines are set to their default states. This bit is self cleared when the registers are set to the factory defaults. The default bit setting is 0.

### 7.2.3.6 0x40.6 Clear All Faults

Write a 1 to the Clear ALL Faults bit to clear all faults, status bits, and counters. Other register settings are maintained with this command. On completion the bit is self cleared to 0 (the default).

The analog compared faults do not clear while the condition that sets them is present. Use this bit to reset the no current counter and other fault counters when exiting LOW POWER Mode.

#### 7.2.3.7 0x40.5 Go2LPM

Write a 1 to the Go to LOW POWER Mode bit to force the RAA489250B to transition to LOW POWER Mode. This bit function only executes when the device is in either IDLE or SCAN Mode. The default bit setting is 0 and the bit is automatically cleared when the device returns to IDLE Mode.

When this setting is executed, the device starts a timer and does not respond to another $I^2C$ instruction (or wake up) for ~200µs.

#### 7.2.3.8 0x40.4 CP_En

The Charge Pump Enable bit turns On and Off the Charge Pump in IDLE and SCAN Modes. A setting of 1 enables the Charge Pump while setting the bit to 0 (default) disables it. This bit has no effect in other modes.

If CP_EN is set and the device is running with 0x80.8 AutoSCAN En, the strong regulator (and CFET if also enabled) remains on during 0x80.[12:11] Scan Delay periods. If CP_EN is clear, the weak regulator is active during Scan Delay periods and external loads can not be supported by the V3P3 regulator.

Bit 0x11.8 CPSSD sets when the charge pump voltage reaches its operating range.

Cell balance current for Cell 5 is reduced if the charge pump is disabled.

#### 7.2.3.9 0x40.3 RSV

This bit is set to 0 by default and returns this value on read. The default value for this bit should be used when writing to this register.

#### 7.2.3.10 0x40.2 $\overline{\text{ALERT}}$ Pin Assert

Writing a 1 to this bit asserts the $\overline{\text{ALERT}}$ pin low. A internal NMOS is activated providing a low-impedance connection between the $\overline{\text{ALERT}}$ and VSS pins. Writing a 0 to this bit followed by reading the 0x10 Faults and 0x11 Status registers turns OFF the NMOS releasing the $\overline{\text{ALERT}}$ pin to a high-z state. The default setting of this bit is 0.

#### 7.2.3.11 0x40.1 RSV

This bit is set to 0 by default and returns this value on read. The default value for this bit should be used when writing to this register.

#### 7.2.3.12 0x40.0 CFET En

The CFET Enable bit turns ON and OFF the High-side Charge FET. Write a 1 to connect the CFET pin to the Charge Pump voltage to turn on the CFET. A 0 (default) setting disconnects the CFET pin from the charge pump.

The CFET is not enabled if either 0x40.4 CP_En or 0x11.8 CPSSD bit is not set.

### 7.2.4 0x41 Measure Select

The Measure Select register enables full MCU control over which device measurement functions are executed.

**Table 14. Measure Select Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x41.[15:8] **RO** | Trigger Busy | RSV | RSV | RSV | RSV | RSV | RSV | RSV | 00 |
| 0x41.[7:0] **R/W** | Trigger Measurement | RSV | RSV | Measurement Selection | | | | | 00 |

#### 7.2.4.1 0x41.15 Busy

The read only Trigger Busy bit indicates the status of the measurement that was started by writing 1 to the trigger measurement bit. A 1 indicates that the device is performing a measurement.

This bit sets when the device detects and reacts to the Trigger Measurement bit transition from 0 to 1. The Trigger Busy and Trigger Measurement bits automatically clear on completion of the selected measurement.

Trigger commands are not stacked, do not attempt to trigger another measurement when this bit is set.

#### 7.2.4.2 0x41.[14:8,6:5] RSV

These bits are set to 0 by default and return this value on read. The default value for these bits should be used when writing to this register.

#### 7.2.4.3 0x41.7 Trigger Measurement

Write a 1 to this bit to trigger the measurement(s) selected with the Measurement Selection bits while in IDLE Mode. This bit automatically clears to 0 (default) after the measurement has completed. The bit is only active while in IDLE Mode.

All measurements are compared to their respective thresholds, but the device does not change Modes, turn OFF the power FET(s), or assert the $\overline{\text{ALERT}}$ pin when a fault is detected. The MCU is expected to check the results of triggered measurements in IDLE Mode and react accordingly. There are three exceptions:

- If the device does not receive communication from the MCU within the setting of 0x80.[14:13] Communication TO, the device transitions to LP Mode and the CFET turns OFF.
- If an analog fault occurs, the device transitions to LP Mode and the CFET turns OFF.
- If the Measurement Selection is Single System Scan, the $\overline{\text{ALERT}}$ pin asserts on a fault detection.

The $\overline{\text{ALERT}}$ pin is asserted for faults that result in the device transitioning to LOW POWER Mode. Faults are set based on the number of consecutive threshold violations. See Power FET Fault Response for details.

This function is edge triggered, the previously triggered measurement must complete and this bit must be clear before another measurement can be executed.

#### 7.2.4.4 0x41.[4:0] Measurement Selection

The Measurement Selection bits determine the action the device executes when the Trigger Measurement bit is set to 1. All measurement registers and fault/no current counters are updated following triggered measurements. Table 15 lists the actions the device can perform and the execution time. The default setting for these bits is 0. The measurement result is stored in the Thermistor 2 data register if a dedicated data register is not assigned. The VTEMP En bit has to be set to 1 before measuring VTEMP, THERM1, or THERM2. Bit settings not listed are not supported.

**Table 15. Measurement Selection Table**

| 0x41.4 | 0x41.3 | 0x41.2 | 0x41.1 | 0x41.0 | Selection | Execution Time | Description |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | System Scan | ~55ms | One Complete System Scan. |
| 0 | 0 | 0 | 0 | 1 | VTEMP | <420µs | Measure VTEMP pin voltage. |
| 0 | 0 | 0 | 1 | 0 | V3P3 | <420µs | Measure V3P3 pin voltage. |
| 0 | 0 | 0 | 1 | 1 | V2P5 | <420µs | Measure V2P5 pin voltage. |
| 0 | 0 | 1 | 0 | 0 | VBG2 | <420µs | Measure VBG2 voltage. |
| 0 | 0 | 1 | 0 | 1 | Internal Temp | <420µs | Measure the Internal temperature sensor voltage. |
| 0 | 0 | 1 | 1 | 0 | THERM1 | <420µs | Measure THERM1 Pin voltage. |
| 0 | 0 | 1 | 1 | 1 | THERM2 | <420µs | Measure THERM2 Pin voltage. |
| 0 | 1 | 0 | 0 | 0 | VPACK | <420µs | Measure VPACK pin voltage. |
| 0 | 1 | 0 | 0 | 1 | VCell 1 | <420µs | Measure VCell1 pin voltage. |
| 0 | 1 | 0 | 1 | 0 | VCell 2 | <420µs | Measure VCell2 pin voltage. |
| 0 | 1 | 0 | 1 | 1 | VCell 3 | <420µs | Measure VCell3 pin voltage. |
| 0 | 1 | 1 | 0 | 0 | VCell 4 | <420µs | Measure VCell4 pin voltage. |
| 0 | 1 | 1 | 0 | 1 | VCell 5 | <420µs | Measure VCell5 pin voltage. |
| 1 | 0 | 1 | 1 | 0 | IPACK (D) | <1.57ms | Measure the voltage between DCSP and CSN pins. |
| 1 | 0 | 1 | 1 | 1 | IPACK (C) | <1.57ms | Measure the voltage between CCSP and CSN pins. |

## 7.2.5 0x42 System Config 2

The System Configuration 2 register includes control bits for the MCU enable/disable device functions used during system scan or single triggered measurements. Configuration lock and cell balance controls are also included.

**Table 16. System Config 2 Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x42.[15:8] | VTEMP EN | Self Test En | LP Reg | FETCON | Config Lock | RSV | RSV | RSV | 48 |
| 0x42.[7:0] | RSV | RSV | RSV | CB5 EN | CB4 EN | CB3 EN | CB2 EN | CB1 EN | 00 |

### 7.2.5.1 0x42.15 VTEMP EN

The VTEMP Enable bit turns ON or OFF the VTEMP output. The default setting of 0 turns OFF the output while a setting of 1 turns it on. This bit is only functional in IDLE Mode.

In SCAN Mode, the device automatically controls the VTEMP output for Single System Scans and 0x80.8 AutoSCAN En. The state machine turns ON and OFF the VTEMP output while executing the THERM and SELF TEST Loops in system scan. The state machine does not change the state of this bit during scans.

Triggered measurements of the thermistor voltages executed from IDLE Mode using the Measurement Selection Table do not automatically enable the VTEMP output, the VTEMP EN bit must be set 18ms before the single trigger measurement of THERM pins and should be cleared following its completion.

If VTEMP_EN is set and the device transitions to Low Power mode with bit 0x42.13 LP Regulator set to ‘1 (strong regulator in LP Mode), the VTEMP regulator remains on. If 0x42.13 is set to 0, the VTEMP regulator does not remain on in LP Mode.

### 7.2.5.2 0x42.14 Self Test En

The Self Test Enable bit setting of 1 (default) includes the SELF TEST Loop tests during the System Scan Sequence. A setting of 0 bypasses SELF TEST during the system scan sequence.

This bit enables tests for THERM OW, VTMPF and 0x10.15 REGF.

Bit 0x80.15 Open Wire En must also be set to 1 to enable VCell tests for 0x10.14 OWF.

#### 7.2.5.3 0x42.13 LP Regulator

The LP Regulator bit sets regulator operation while in LOW POWER Mode. A setting of 1 enables the strong regulator in LP Mode. The power good comparators are enabled when the strong regulator is used. The current consumption of the device is more while this regulator is enabled. A setting of 0 (default) enables the weak regulator while in LP Mode reducing current consumption. The weak regulator has limited drive capability, if the V3P3 node is overloaded the regulator voltage might drop below the POR threshold causing the device to reset on wakeup.

The device transitions from LP to IDLE Mode on a RESET, POR, CHMON detection, or $I^2C$ transaction.

#### 7.2.5.4 0x42.12 FETCON

The FET Connect bit setting of 1 enables automatic FET control in response to a fault detection in AutoSCAN (0x80.8 AutoSCAN En = 1). A setting of 0 (default) disables this feature leaving the fault response up to the MCU. See Faults for FET control dependency of specific faults on this bit setting.

#### 7.2.5.5 0x42.11 Config Lock

The Configuration Lock bit locks out (prevent writing to) registers 0x80 through 0x84 when set to the default of 1. Set this bit to 0 before attempting to write to these registers, then set it back to 1 when the changes are complete.

#### 7.2.5.6 0x42.[10:5] RSV

These bits are set to 00 0000 by default and return this value on read. The default value for these bits should be used when writing to this register.

#### 7.2.5.7 0x42.[4:0] CBn En

A setting of 1 enables an internal Cell Balance transistor with its drain connected to pin VCn and its source connected to pin VC(n-1). The amount of cell balance current is determined by the cell voltage divided by the sum of the external filter resistances and the CB FET on resistance (RCB_ON). The CB current for cell 5 is slightly reduced if the charge pump is disabled. The default setting for these bits is 0. Cell balancing is blocked and these settings are ignored if bit 0x80.15 Open Wire En is set.

These bits must be cleared by the MCU as they do not self clear during Mode or State changes. They are cleared on RESET.

### 7.2.6 0x80 System Config 3

Register 0x84 requires the use of a key before writing is permitted, see 0x42.11 Config Lock.

**Table 17. System Config 3 Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x80.[15:8] | OW Enable | Communication Timeout | | Scan Delay | | RSV | RSV | AutoSCAN EN | 60 |
| 0x80.[7:0] | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV | 00 |

#### 7.2.6.1 0x80.15 Open Wire En

An Open-Wire Enable bit setting of 1 includes open-wire test for cell connections while executing the SELF TEST Loop within the System Scan Sequence. An open-wire test can be executed while in IDLE Mode by triggering the Single System Scan (0x41 Measure Select) with this bit previously set to 1. The default setting of 0 omits the open-wire test. 0x42.14 Self Test En must also be set to 1 because the open-wire test is a subset of SELF TEST.

#### 7.2.6.2 0x80.[14:13] Communication TO

The Communication Timeout bits set the maximum time between MCU communications with the RAA489250B before a 0x10.8 COMMTO fault forces a transition to LP Mode. If the SDA pin does not make a high-to-low transition while the SCL pin is high within the selected period of time, the device transitions to LOW POWER Mode.

When the MCU asserts the SDA pin low while the SCL pin is high, the communication timer resets to 0. Table 18 lists the selectable times with the default setting highlighted in gray.

**Table 18. Comm TO Selections**

| D[13:12] | Timeout Time (s) |
|---|---|
| 00 | OFF |
| 01 | 0.1 |
| 10 | 1 |
| 11 | 5 |

#### 7.2.6.3 0x80.[12:11] Scan Delay

The Scan Delay bits control the time delay between automatic system scans in SCAN Mode when a system scan is triggered while bit 0x80.8 AutoSCAN En is 1. Scan Delay is only functional while the device is in SCAN Mode with AutoSCAN_En = 1.

If CP_EN is set and the device is running in AutoSCAN, the strong regulator (and CFET if also enabled) remains on during Scan Delay periods. If CP_EN is clear, the weak regulator is active during Scan Delay periods then some external loads can not be supported by the V3P3 regulator.

Table 19 lists the selectable delays with the default setting highlighted in gray.

**Table 19. Scan Delay Selections**

| 0x80.[12:11] | Scan Delay Time (s) |
|---|---|
| 00 | 0 |
| 01 | 0.1 |
| 10 | 0.5 |
| 11 | 1 |

#### 7.2.6.4 0x80.[10:9] RSV

These bits are reserved and should be ignored on read and always set to 00 on write.

#### 7.2.6.5 0x80.8 AutoSCAN En

An AutoSCAN Enable bit setting of 0 (default) transitions the state machine to IDLE Mode after a triggered measurement is completed. For a bit setting of 1, the state machine stays in SCAN Mode after the system scan and 0x80.[12:11] Scan Delay has completed, then transitions back to the start of SCAN Mode where another system scan is performed. An AutoSCAN En bit setting of 1 places the device in a continuous scan loop until a fault is detected or the bit value is changed to 0 by the MCU. Fault reaction in some cases is dependent on the setting of 0x42.12 FETCON, also see Faults for additional details.

#### 7.2.6.6 0x80.[7:0] RSV

These bits are set to 0000 0000 by default and return this value on read. These bits can be written by the MCU but are cleared on device reset.

### 7.2.7 0x81 OV Thresholds

Register 0x81 requires the use of a key before writing is permitted, see 0x42.11 Config Lock. The settings in this register set the cell overvoltage thresholds. Each $V_{CELL}$ measurement is compared to these overvoltage limits.

**Table 20. OV Thresholds Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x81.[15:8] | $V_{CELL}$ OV Threshold | | | | | | | | E5 |
| 0x81.[7:0] | $V_{CELL}$ OV Hysteresis | | | $V_{CELL}$ OVLO Threshold | | | | | 5F |

#### 7.2.7.1 0x81.[15:8] $V_{CELL}$ OV

The $V_{CELL}$ Overvoltage threshold detector alerts the system to discontinue charging at the selected voltage. The threshold detector is a digital comparator that requires an ADC $V_{CELL}$ measurement to compare. If this threshold is exceeded, fault bit 0x10.6 OVF is set to 1.

The setting ranges from 2.0V to 4.55V with a 10mV step size and a default of 4.29V.

#### 7.2.7.2 0x81.[7:5] $V_{CELL}$ OV Hysteresis

The $V_{CELL}$ OV Hysteresis setting determines the cell voltage required to recover from and clear a $V_{CELL}$ OV Fault (0x10.6 OVF). The recovery voltage is the setting of this register subtracted from 0x81.[15:8] $V_{CELL}$ OV.

The setting ranges from 50mV to 400mV with a 50mV step size and a default of 150mV.

#### 7.2.7.3 0x81.[4:0] $V_{CELL}$ OVLO

The $V_{CELL}$ Overvoltage Lockout threshold detector alerts the system to discontinue charging at the selected voltage. The threshold detector is a digital comparator that requires an ADC $V_{CELL}$ measurement to compare. If this threshold is exceeded (VCell > Threshold), fault bits 0x10.6 OVF and 0x10.7 LOF are set to 1.

The setting ranges from 3.05V to 4.6V with a 50mV step size and a default of 4.6V.

### 7.2.8 0x82 UV Thresholds

Register 0x82 requires the use of a key before writing is permitted, see 0x42.11 Config Lock. The settings in this register set the cell undervoltage thresholds. Each $V_{CELL}$ measurement is compared to undervoltage limits.

**Table 21. UV Threshold Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x82.[15:8] | $V_{CELL}$ UV Threshold | | | | | | | | 31 |
| 0x82.[7:0] | CPWR | $V_{CELL}$ UV Hysteresis | | | $V_{CELL}$ UVLO Threshold | | | | A0 |

#### 7.2.8.1 0x82.[15:8] $V_{CELL}$ UV

The undervoltage threshold detector alerts the system to discontinue discharge at the selected voltage. The threshold detector is a digital comparator that requires an ADC $V_{CELL}$ measurement to compare. If this threshold is exceeded, fault bit 0x10.5 UVF is set to 1.

The setting ranges from 0.512V to 3.06V with a 10mV step size and a default of 1.002V. Setting this threshold to the minimum value disables UVF detection.

#### 7.2.8.2 0x82.7 CPWR

The Configure Power FET bit changes the power FET response versus the fault signaled. A bit setting of 0 is for series power FET configurations. The power FETs are dependent on the CHRGI and DCHRGI bit status with this setting. A bit setting of 1 (default) is for parallel power FET configuration.

The power FET automatic response versus fault is found in Power FET Fault Response.

#### 7.2.8.3 0x82.[6:4] $V_{CELL}$ UV Hysteresis

The $V_{CELL}$ UV Hysteresis setting determines the cell voltage required to recover from and clear a $V_{CELL}$ UV Fault (0x10.5 UVF). The recovery voltage is the setting of this register added to 0x82.[15:8] $V_{CELL}$ UV.

The setting ranges from 100mV to 800mV with a 100mV step size and a default of 300mV.

#### 7.2.8.4 0x82.[3:0] $V_{CELL}$ UVLO

During discharge, the undervoltage threshold detector alerts the system to discontinue discharge at the selected voltage. The threshold detector is a digital comparator that requires an ADC $V_{CELL}$ measurement to compare. If this threshold is exceeded ($V_{CELL}$ < Threshold), fault bit 0x10.5 UVF and 0x10.7 LOF are set to 1.

The minimum setting of 0.512V equals the minimum voltage result for a cell measurement. This setting disables the UVLO Threshold and LOF detection.

When bit 0x84.15 SUVLO is set to 0 (default), the UVLO Threshold setting ranges from 0.512V to 2.01V with a 100mV step size and a default of 0.512V. Setting bit SUVLO to 1 adds 1.002V to the selected UVLO threshold.

### 7.2.9 0x83 SCC, OT/UT Thresholds

Register 0x83 requires the use of a key before writing is permitted, see 0x42.11 Config Lock. The settings in this register set the pack operating temperature limits based on external thermistor voltages.

**Table 22. SCC and Therm Register**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x83.[15:8] | SCC Delay | | DOT | | | DUT | | | A3 |
| 0x83.[7:0] | Therm Enable | | COT | | | CUT | | | A4 |

See Setting OT/UT Thresholds on how to calculate the OT/UT thresholds and Faults for a detailed descriptions of the relationship between fault thresholds, delays and device reactions.

#### 7.2.9.1 0x83.[15:14] SCC Delay

The Short-Circuit Current Delay register sets the deglitch time requirement for short-circuit determination. If the short-circuit current remains, determined by applicable threshold (see 0x84.[14:12] DSC), after the delay has timed out the fault bit 0x10.2 SCF sets.

Table 23 lists the selectable delays with the default setting highlighted in grey.

**Table 23. SCC Delay**

| D[15:14] | Delay (Typ) |
|---|---|
| 00 | 30us |
| 01 | 0.1ms |
| 10 | 1ms |
| 11 | 5ms |

#### 7.2.9.2 0x83.[13:11] DOT

The Discharge Over-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is discharging (0x11.1 DCHRGI is set). The RAA489250B assumes NTC thermistors are in use, when the thermistor voltage is less than this threshold fault bit 0x10.4 OTF is set.

The selectable thresholds are listed in Table 26 with the default setting highlighted.

#### 7.2.9.3 0x83.[10:8] DUT

The Discharge Under-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is discharging (0x11.1 DCHRGI is set). The RAA489250B assumes NTC thermistors are in use, when the thermistor voltage is greater than this threshold fault bit Table 7.2.1.12 is set.

The selectable thresholds are listed in Table 26 with the default setting highlighted.

#### 7.2.9.4 0x83.[7:6] Thermistor Enable

The Thermistor Enable bits select the number of thermistors to measure and compare during System Scans. The bit selections are listed in Table 24 with the default setting highlighted in grey.

**Table 24. Thermistor Enable Selection**

| Thermistor Enable Bits: D[7:6] | | Thermistor Measurement |
|---|---|---|
| 0 | 0 | OFF (Not measured during System Scans) |
| 0 | 1 | THERM1 |
| 1 | 0 | THERM1 and THERM2 |
| 1 | 1 | THERM1 and THERM2 (no Faults) |

VTEMP does not turn ON for a bit selection OFF (00b) during System Scans. For all other selections, the VTEMP regulator turns ON 18ms (tVTEMP) before measuring the pin(s) during either AutoSCAN or a Triggered Single System Scan.

Single triggered measurements of the thermistor voltages alone requires the user to first enable the VTEMP output (0x42.15 VTEMP EN). If the thermistor enable bits are set to OFF, the device still compares the thermistor measurements to the temperature thresholds during single triggered scans.

Setting the Thermistor Enable bits to 11 selects a special mode where both thermistors are measured, but only THERM1 measurements are compared to the OT and UT limits. This mode is included for applications that use THERM2 to monitor devices other than batteries.

#### 7.2.9.5 0x83.[5:3] COT

The Charge Over-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is charging (0x11.0 CHRGI is set). The RAA489250B assumes NTC thermistors are in use, when the thermistor voltage is less than this threshold, fault bit 0x10.4 OTF is set.

The selectable thresholds to set COT are listed in Table 25 with the default setting highlighted. COT has a recovery hysteresis linked to each setting, also listed in the table, which clears OTF automatically.

#### 7.2.9.6 0x83.[2:0] CUT

The Charge Under-Temperature register sets the threshold of a digital comparator that monitors the thermistor voltages when the pack is charging (0x11.0 CHRGI is set). The RAA489250B assumes NTC thermistors are in use, which means that if the thermistor voltage is greater than this threshold, fault bit 0x10.3 UTF is set.

The selectable thresholds to set CUT are listed in Table 25 with the default setting highlighted. CUT has a recovery hysteresis linked to each setting, also listed in the table, which clears UTF automatically.

#### 7.2.9.7 Setting OT/UT Thresholds

The Thermistor Threshold register settings represent specific voltages to set cell temperature limits. Figure 25 illustrates the recommended thermistor circuit with RP typically set equal to 2x $R_{THERM}$. See VTEMP, THERMn Pins for other circuit details. Which thresholds are applied to the thermistor measurement results is dependent on the setting of bit 0x82.7 CPWR.

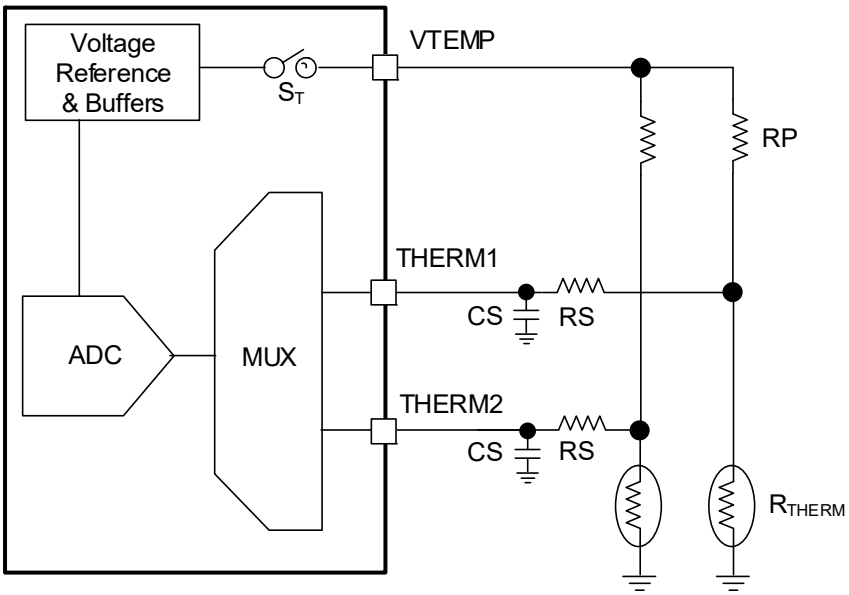



**Figure 25. Thermistor Circuit Configuration**

The selectable thermistor thresholds during charging are listed in Table 25 with the defaults highlighted.

**Table 25. Thermistor Thresholds (Charge)**

| Setting | COT (OTF Set) | | | COT (OTF Clear) | | | CUT (UTF Set) | | | CUT (UTF Clear) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Volts | Code | Temp | Volts | Code | Temp | Volts | Code | Temp | Volts | Code | Temp |
| 000 | 0.528 | 0x0520 | 35 | 0.601 | 0x05B2 | 30 | 1.583 | 0x0D5E | -20 | 1.492 | 0x0CA7 | -15 |
| 001 | 0.462 | 0x049B | 40 | 0.528 | 0x0520 | 35 | 1.491 | 0x0CA6 | -15 | 1.393 | 0x0BE1 | -10 |
| 010 | 0.404 | 0x0427 | 45 | 0.462 | 0x049C | 40 | 1.392 | 0x0BE0 | -10 | 1.283 | 0x0B0F | -5 |
| 011 | 0.352 | 0x03BF | 50 | 0.404 | 0x0428 | 45 | 1.287 | 0x0B0E | -5 | 1.181 | 0x0A39 | 0 |
| 100 | 0.307 | 0x0365 | 55 | 0.353 | 0x03C1 | 50 | 1.180 | 0x0A38 | 0 | 1.073 | 0x0962 | 5 |
| 101 | 0.268 | 0x0317 | 60 | 0.308 | 0x0367 | 55 | 1.073 | 0x0962 | 5 | 0.968 | 0x088F | 10 |
| 110 | 0.234 | 0x02D3 | 65 | 0.268 | 0x0318 | 60 | 0.967 | 0x088E | 10 | 0.867 | 0x07C5 | 15 |
| 111 | 0.205 | 0x0299 | 70 | 0.234 | 0x02D4 | 65 | 0.866 | 0x07C4 | 15 | 0.771 | 0x0706 | 20 |

The selectable thermistor thresholds during discharge are listed in Table 26 with the defaults highlighted. Discharge thermistor thresholds do not have hysteresis.

The OTF and UTF thresholds ignore the current direction bits (0x11.1 DCHRGI and 0x11.0 CHRGI) when 0x82.7 CPWR is set to 1, so the fault bit sets when the first threshold is crossed. In most cases, this is the selected charge threshold from Table 25.

**Table 26. Thermistor Thresholds (Discharge)**

| Setting | DOT | | | DUT | | |
|---|---|---|---|---|---|---|
| | Volts | Code | Temp | Volts | Code | Temp |
| 000 | 0.268 | 0x0317 | 60 | 1.804 | 0x0F18 | -35 |
| 001 | 0.234 | 0x02D3 | 65 | 1.740 | 0x0E98 | -30 |
| 010 | 0.205 | 0x0299 | 70 | 1.667 | 0x0E06 | -25 |
| 011 | 0.179 | 0x0265 | 75 | 1.583 | 0x0D5E | -20 |
| 100 | 0.157 | 0x0239 | 80 | 1.491 | 0x0CA6 | -15 |
| 101 | 0.138 | 0x0213 | 85 | 1.392 | 0x0BE0 | -10 |
| 110 | 0.122 | 0x01F3 | 90 | 1.287 | 0x0B0E | -5 |
| 111 | 0.107 | 0x01D5 | 95 | 1.180 | 0x0A38 | 0 |

Table 27 shows temperature versus ADC codes and pin voltages using the recommended circuit configuration (Figure 25) with an NCP18XH103F03RB thermistor and the typical VTEMP voltage.

**Table 27. Example Thermistor Thresholds**

| Thermistor Temperature (°C) | ADC Code (HEX) | Therm Pin Voltage (mV) |
|---|---|---|
| 105 | 1AA | 85 |
| 100 | 1C0 | 96 |
| 95 | 1D8 | 108 |
| 90 | 1F6 | 123 |
| 85 | 216 | 139 |
| 80 | 23E | 159 |
| 75 | 26A | 181 |
| 70 | 29C | 206 |
| 65 | 2D8 | 236 |
| 60 | 31C | 270 |
| 55 | 36A | 309 |
| 50 | 3C6 | 355 |
| 45 | 42E | 407 |
| 40 | 4A2 | 465 |
| 35 | 256 | 531 |
| 30 | 5BA | 605 |
| 25 | 65E | 687 |
| 20 | 710 | 776 |
| 15 | 7D0 | 872 |
| 10 | 89C | 974 |
| 5 | 970 | 1080 |
| 0 | A46 | 1187 |
| -5 | B20 | 1296 |
| -10 | BF2 | 1401 |
| -15 | CBA | 1501 |
| -20 | D72 | 1593 |
| -25 | E1A | 1677 |

#### 7.2.9.8 Thermistor Fault Response

The device response to a thermistor measurement result is dependent on the setting of 0x83.[7:6] Thermistor Enable and if the result was obtained using a single triggered measurement or from a system scan. Table 28 shows when the device makes a measurement and if it is compared to the relevant thresholds based on the settings and type of measurement executed.

**Table 28. Thermistor Fault response**

| Therm Enable | THERM1 | | | | THERM2 | | | |
|---|---|---|---|---|---|---|---|---|
| | System Scan | | Single Measure | | System Scan | | Single Measure | |
| | OTF/UTF | Measured | OTF/UTF | Measured | OTF/UTF | Measured | OTF/UTF | Measured |
| 00 | NO | NO | YES | YES | NO | NO | YES | YES |
| 01 | YES | YES | YES | YES | NO | NO | YES | YES |
| 10 | YES | YES | YES | YES | YES | YES | YES | YES |
| 11 | YES | YES | YES | YES | NO | YES | NO | YES |

### 7.2.10 0x84 Current Thresholds

Register 0x84 requires the use of a key before writing is permitted, see 0x42.11 Config Lock.

**Table 29. Current Thresholds**

| Register | Bit Function | | | | | | | | Default (Hex) |
|---|---|---|---|---|---|---|---|---|---|
| | 15/7 (MSB) | 14/6 | 13/5 | 12/4 | 11/3 | 10/2 | 9/1 | 8/0 (LSB) | |
| 0x84 (Upper Byte) | SUVLO | DSC Threshold | | | DOC Threshold | | | | 4C |
| 0x84 (Lower Byte) | DOC Threshold | | COC Threshold | | | | | | 71 |

See Faults for detailed descriptions of the relationship between fault thresholds, delays, and device reactions.

#### 7.2.10.1 0x84.15 SUVLO

If set to 1, the Shift UVLO threshold bit adds 1.002V to the setting 0x82.[3:0] $V_{CELL}$ UVLO. With the default bit setting of 0, the UVLO threshold is as defined by bits 0x82.[3:0].

#### 7.2.10.2 0x84.[14:12] DSC

The Discharge Short-Circuit Current threshold register sets the short-circuit threshold of the analog comparator for the Discharge path.

If the voltage across the discharge current-sense resistor (see DCSP, CCSP, and CSN Pins) is more negative than this threshold for more than 0x83.[15:14] SCC Delay, fault bit 0x10.2 SCF is set.

The bit selections are listed in Table 30 with the default setting highlighted in gray.

**Table 30. DSC Threshold**

| D[14:12] | Threshold |
|---|---|
| 000 | 12.5mV |
| 001 | 25mV |
| 010 | 50mV |
| 011 | 100mV |
| 100 | 200mV |

#### 7.2.10.3 0x84.[11:6] DOC

The Discharge Overcurrent threshold register sets the overcurrent threshold of a digital comparator. If the voltage across the discharge current-sense resistor (DCSP, CCSP, and CSN Pins) exceeds this threshold for more than eight sequential measurements, fault bit 0x10.1 DOCF is set. The device measures current multiple times within each system scan so this fault can be detected within one scan.

This fault only shuts off CFET if both 0x42.12 FETCON and 0x80.8 AutoSCAN En are set to 1.

The setting ranges from 1mV to 50mV with a step size of 1mV and a default of 50mV. Setting above 51mV disables DOC detection.

#### 7.2.10.4 0x84.[5:0] COC

The Charge Overcurrent threshold register sets the overcurrent threshold of a digital comparator. If the voltage across the charge current sense resistor (DCSP, CCSP, and CSN Pins exceeds this threshold for more than eight sequential measurements, fault bit 0x10.0 COCF is set. The device measures current multiple times within each system scan so this fault can be detected within one scan.

This fault only shuts off CFET if both 0x42.12 FETCON and 0x80.8 AutoSCAN En are set to 1.

The setting ranges from -1mV to -50mV with a step size of 1mV and a default of -50mV. Setting below -51mV disables COC detection.

# 8. I²C Serial Interface

The device includes a digital interface for users to configure the device operation and monitor parameters. The device is available to communicate to anytime the chip is not being reset. The device supports an I²C SMBus serial interface.

This device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the Controller. The device being controlled is the Target. The Controller always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the device operates as the Target device in all applications.

The device uses command codes to perform block reads. The device does not support random sequential reads. A command code read is a block read with the starting register address and the number of bytes to read back digitally encoded into the device. Command codes support register read backs with and without CRC.

## 8.1 I²C Target Address

The device can be can be used with any I²C host device. Each device must have its own unique serial address. The device supports packet error checking. Packet error checking is enabled by a separate Target address.

The Targets address for both CRC and non CRC packages are listed in Table 31.

**Table 31. I²C Address Value**

| Format | Address (7-bit Binary) |
|---|---|
| Packets without CRC | 0010 010 |
| Packets with CRC | 1010 110 |

## 8.2 Communication Packet Format.

The device communicates with a Controller that is complaint with the I²C protocol. The device processes read and write requests as word (2 byte) widths. A write action requires two bytes (word) of data to change the individual bits within the register. The minimum data width for a read command is two bytes. The device supports Command Codes in place of sequential reads.

The ordering of the bytes is compliant to a Little Endian standard. The Little Endian has the 1st data byte containing data bits 7 through 0 of the data byte word. The second data byte contain data bits 15 through 8. The most significant bit within the byte is data bit 7 for the first byte and data bit 15 for the second byte. The least significant bit for each byte is data bit 0 for the 1st bit and data bit 8 for the second bit. The device processes the packet in byte widths. Reading a 0x8008 from a register has the device to sending the data byte 0x08 as the first byte and 0x80 as the second byte (overall 0x0880). Similar to reading, the write byte is ordered in the same manner. A register value of 0x12FE is sent to the device as 0xFE12. It is responsibility of the Controller to reverse the order of the bytes. Figure 26 illustrates the order of the data bytes for a read command. Figure 27 illustrates the order of the data bytes for a write command. See I²C Target Address for more information on communicating to the device.

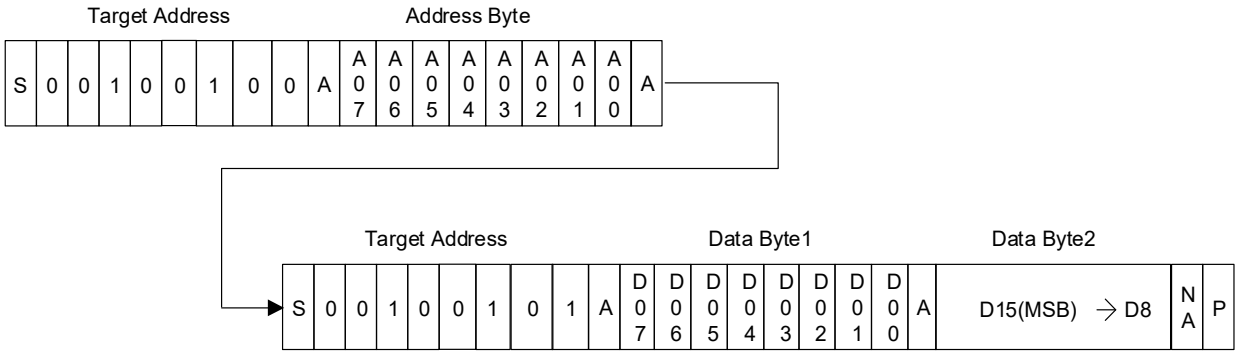



**Figure 26. I²C Read Data Format**

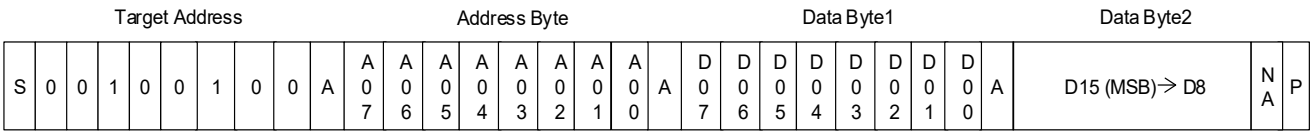



**Figure 27. I²C Write Data Format**

## 8.3 Cyclical Redundancy Check (CRC)

The device has a CRC (cyclical redundancy check) for securer communication between Controller and Target. The CRC code is a byte in length. The equation of the CRC is $X^8+X^2+X^1+1$. The CRC equation has a minimum Hamming Distance of 3 for payloads up to 247 bits.

For Write commands, the register of the device is changed when the transmitted CRC byte by the Controller is the same in value as the CRC byte calculated by the Target (the device). When the two CRC bytes agree, the Target transmits an acknowledge bit (ACK) to the Controller. If the byte values do not agree, a NACK is transmitted is set.

For Read commands, the Target sends CRC byte(s) as part of the read packet. It is the responsibility of the Controller to check the CRC byte versus the calculated CRC byte of the Controller. As part of the Read command, the Controller writes several bytes to indicate a Read command and to indicate which register value to reading from. For a read, the Target sends the Controller a CRC byte with the calculated value for the two Target address bytes, the address byte and the read word. Figure 33 and Figure 31, illustrate the read and write formats with a CRC byte.

## 8.4 Protocol Conventions

The logic state on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 28). At power-up, the SDA pin is in the input Mode.

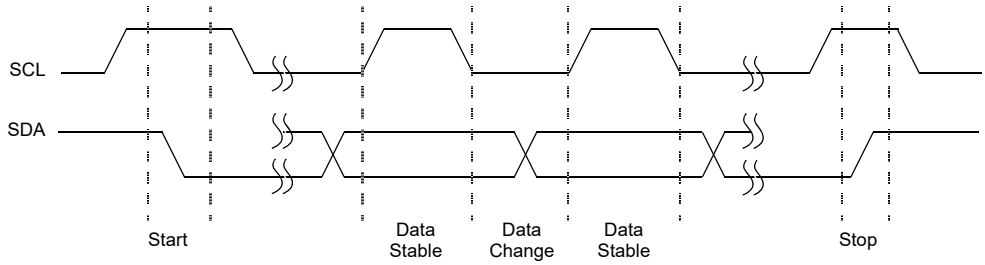



**Figure 28. Valid Data Changes, Start, and Stop Conditions**

All $I^2C$ interface operations must begin with a START condition that is a HIGH-to-LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 28). A START condition is ignored during the power-up sequence.

All $I^2C$ interface operations must be terminated by a STOP condition that is a LOW-to-HIGH transition of SDA while SCL is HIGH (see Figure 28). A STOP condition at the end of a Read operation, or at the end of a Write operation returns the $I^2C$ state machine to its initial state where it waits for the next START.

An Acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either Controller or Target, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 29). The device responds with an ACK after recognition of a START condition followed by a valid Target Address byte, and when again after a successful receipt of the Register Address Byte. The device responds with an ACK after receiving each data byte of a write operation. The device indicates that the maximum number bytes have been received for a write packet by sending a NACK to the Controller. The Controller then sends a Stop bit to terminate the packet.

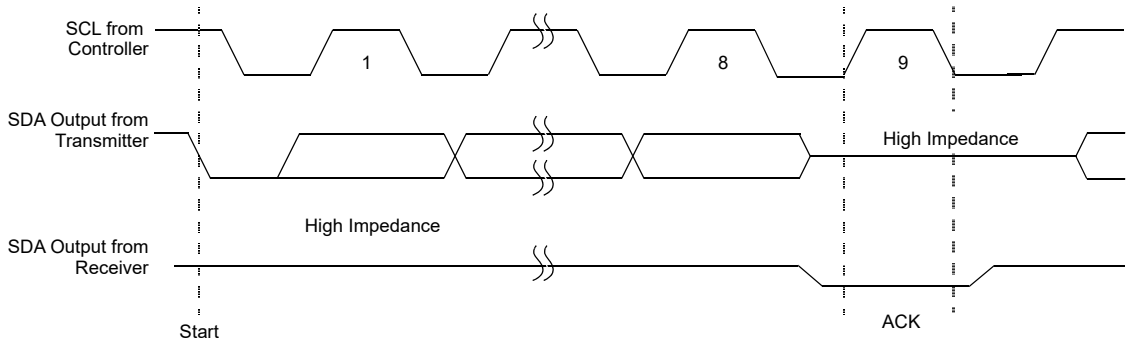



**Figure 29. Acknowledge Response from Receiver**

For a read packet, the device sends an ACK after each byte sent by the Controller. The Controller sends an ACK bit following every byte transmitted by the device. The Controller sends a NACK bit after the final read back byte. The Target then sends a Stop bit to terminate the packet.

The last bit of the Target Address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a 1, a Read operation is selected. A 0 selects a Write operation (see Figure 30).

After loading the entire Target Address byte from the SDA bus, the device compares it with the internal Target Address. On a correct compare, the device outputs an acknowledge on the SDA line.

### 8.4.1 Write Operation

A Write operation requires a START condition, followed by a Target Address byte, a Register Address byte, a word of Data, and a STOP condition (see Figure 30 and Figure 31). The Target device responds with an ACK after successfully receiving each of the four bytes. The content of the word of Data is transferred to the device register at the rising edge of the SCL pin during the ACK and a successful comparison of the CRC byte of the Controller versus the internally calculated CRC byte.

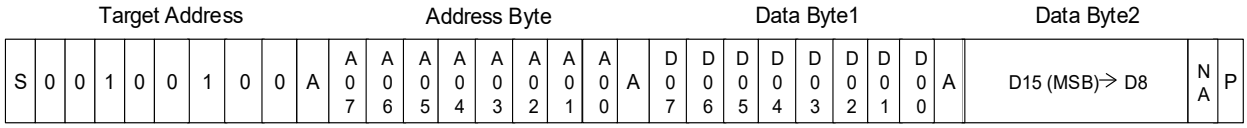



**Figure 30. I²C Write Format**

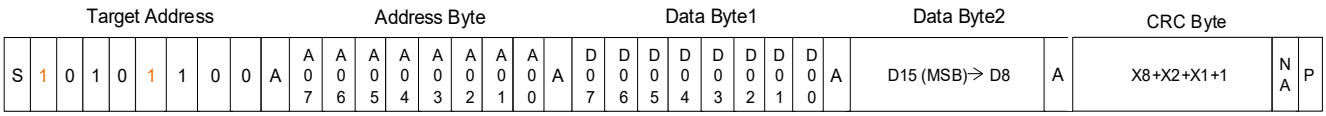



**Figure 31. I²C Write Format with CRC**

### 8.4.2 Read Operation

A Read operation consists of a three byte sequence, followed by one word of Data (see Figure 32 and Figure 33). The Controller initiates the read operation by sending the following sequence of bits: a START bit, the Target Address byte with the R/W bit set to 0, a Register Address byte, a second START bit, and a second Target Address byte with the same seven MSBs but with the R/W bit set to 1. After each of the four bytes, the device responds with an ACK. The device transmits the word of Data followed by a CRC byte (if enabled) for as long as the Controller responds with an ACK. The ACK bit occurs on the rising edge of the SCL pin for every 8 bits transmitted. The Controller terminates the Read operation by issuing a NACK, and then a STOP condition.

The Data words received from the Target are from the memory location indicated by an internal pointer. The initial value of the pointer is determined by the address byte in the Read operation instruction, and increments by one during transmission of each word of Data.


**Figure 32. I²C Read Format**

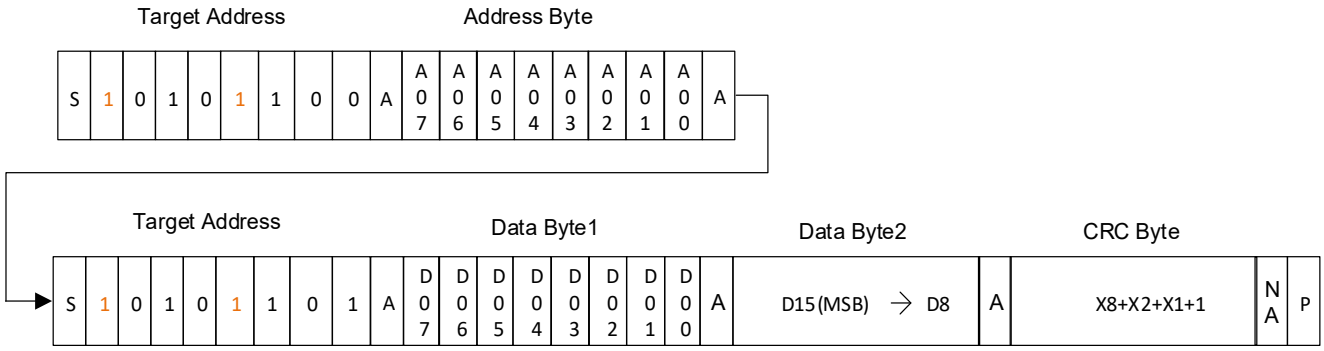



**Figure 33. I²C Read Format with CRC**

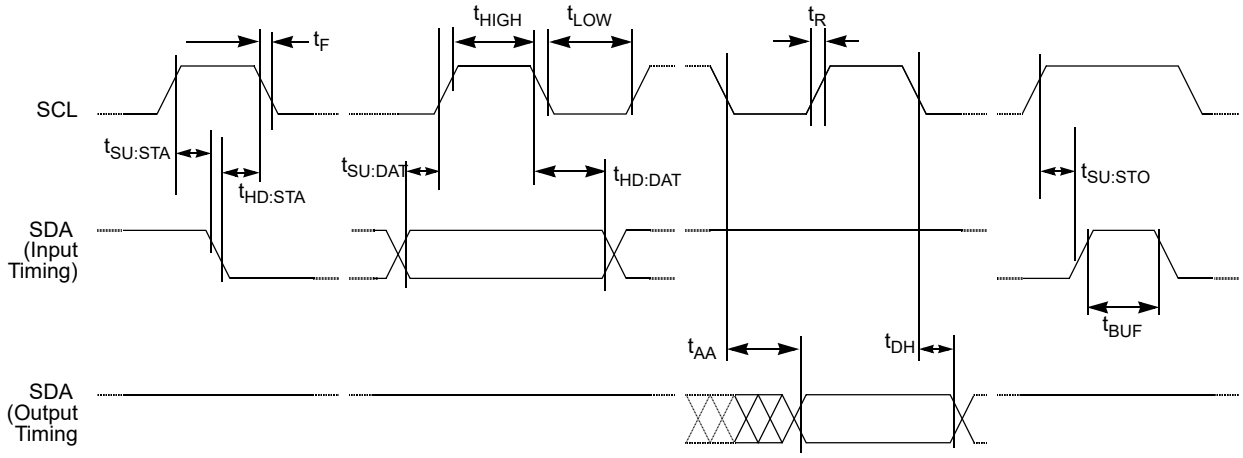



**Figure 34. I²C Timing**

## 8.4.3 Command Codes

Command codes are block reads that have the register addresses and the number of bytes to read back encoded into the device. Table 32 defines each command code, which register addresses are read back (Hex), and the read time at 400kbs (add ~30µs with CRC). The use of command codes is faster than individually reading each register.

A C1 Fault and Status command received by the device while the $\overline{\text{ALERT}}$ pin is asserted results in the $\overline{\text{ALERT}}$ pin able to change state freely. Read ALERT Pin 19 for more information on how the $\overline{\text{ALERT}}$ pin interacts with the Fault and Status command code.

**Table 32. Command Code Details**

| CMD | Reg Address | | Byte Count | Read Time (µs) | Register Data Returned |
|---|---|---|---|---|---|
| | Start | End | | | |
| C1 | 10 | 11 | 7 | 220 | Fault and Status |
| C2 | 00 | 06 | 17 | 530 | VPACK, $V_{Cell\_max}$, $V_{Cell\_min}$, THERM1, THERM2, $I_{discharge}$, and $I_{charge}$ |
| C3 | 05 | 06 | 7 | 220 | $I_{discharge}$ and $I_{charge}$ |
| C4 | 20 | 25 | 15 | 470 | VTEMP, Cell 1-5 Voltages |

Figure 35 and Figure 36 are the packet formats for command codes. The command codes support CRC. The CRC byte value is calculated from the value of each register word read back, the two Target addresses and the

command code. The calculation of the CRC is processed from the first Target address byte to the final byte that is read back.

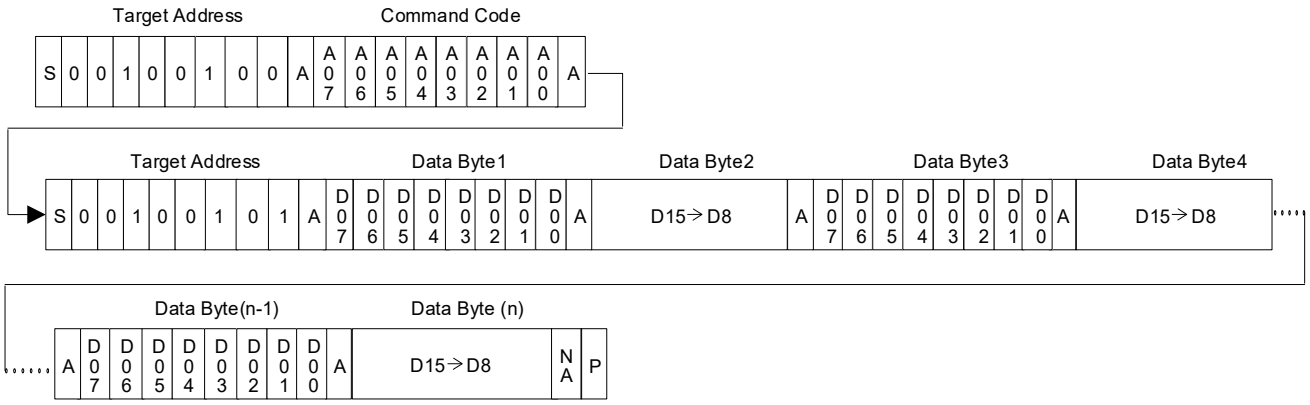



**Figure 35. I²C Command Code Read Format**

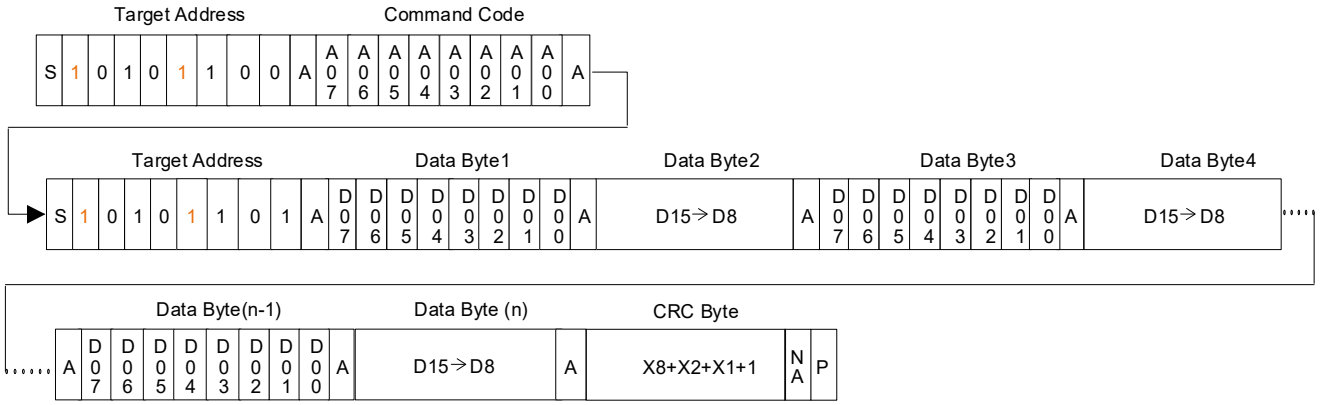



**Figure 36. I²C Command Code Read Format with CRC**

# 9. Pins

## 9.1 VC# Pins

The VC# pins (1, 3, 5, 7, 8) are the voltage sense inputs of the device that are connected in pairs to differentially measure each cell voltage. Positive pin $VC_n$ and negative pin $VC_{n-1}$ are connected to the ADC through a multiplexer. Each voltage sense input uses an external filter to protect against battery voltage transients. The basic input filter structure provides protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. Place any vias in line to the signal inputs so that the inductance of these forms a low-pass filter with the grounded capacitors.

The filtered battery cell voltages internally connects to the cell voltage monitoring system. The monitoring system contains a multiplexer to select a specific input, and an analog to digital converter.

Figure 37 illustrates a typical $V_{CELL}$ filter connection for the device. The differential capacitance ($C_{Diff}$) should be 0.1µF. The isolation resistance ($R_{ISO}$) should be 1kΩ. Deviation from these values can effect device performance, for example, cell measurement error or open-wire test.

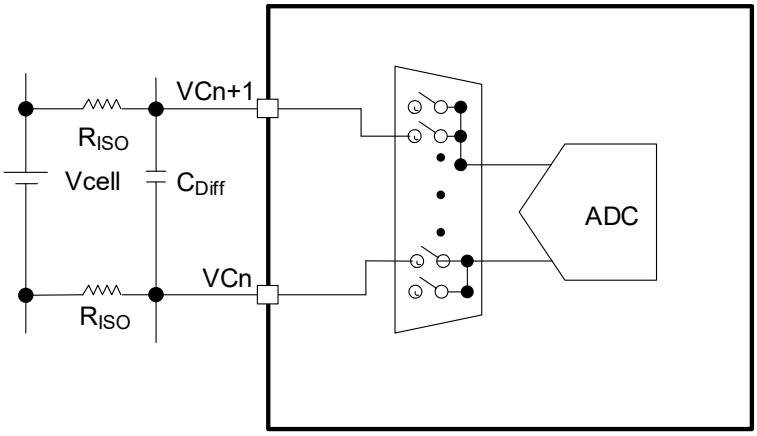



**Figure 37. Voltage Sense Pin Connections**

### 9.1.1 Open Wire on VC# Pins

The device performs an open-wire test by connecting a resistor to VSS for each VCn pin simultaneously. The current source on time is 10ms. After 7ms from turning ON the pin current, the device performs a VCell scan to measure the cell voltages of the pack while current is being drawn from the pin. The cells are measured starting at cell 1 and proceeding to the top cell of the pack. If a cell reading measures below 0.6V (0x058), an internal flag is set. The open-wire test has to fail two times consecutively before the bit 0x10.14 OWF is set 1. The open-wire test is performed in the SELF TEST Loop of the system scan. The open wire only reports if any of the cell open-wire tests fail. To specifically find the open-wire pin that failed, use bits 0x42.[4:0] CBn En to individually turn ON the pin current source and perform a VCell/VPACK read. A block diagram of the open-wire functions is shown in Figure 38.

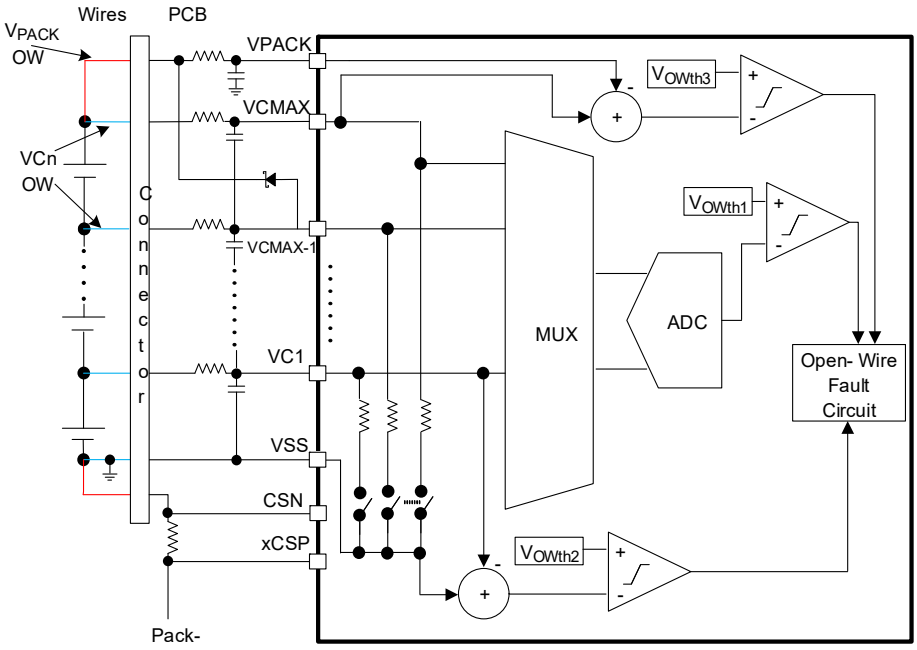



**Figure 38. Open-Wire Block Diagram**

## 9.2 VPACK Pin 10

The VPACK pin is the main power connection to the device. Connect a 10µF bypass cap to ground at the pin (Figure 39). This pin should have a series resistor of ~10Ω, which combined with the capacitor to ground filters out system noise.

## 9.3 VCP Pin 11

The VCP pin is the charge pump output connection to the charge pump capacitor that is connected between the VCP pin and VPACK pin. A charge pump capacitor value of approximately 10 times the sum of the gate capacitance (up to 0.1µF) connected to the CFET pin is recommended. Place the capacitor close to the device pins as shown in Figure 39.

The VCP pin is an analog output and should not be driven by an external source.

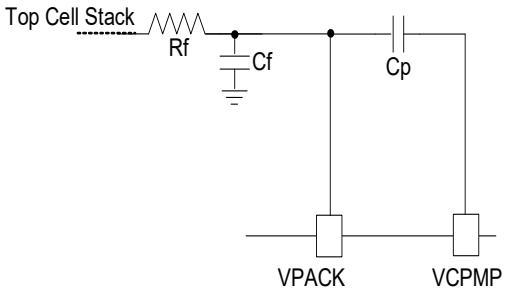



**Figure 39. VPACK and VCP Pins**

## 9.4 CFET Pin 13

The High-side Charge FET pin is pulled up to the charge pump voltage when the 0x40.4 CP_En bit is set to 1 and the charge pump is operational (0x10.11 CPF = 0 and 0x11.8 CPSSD = 1). When enabled, the VCP pin is connected internally to the CFET pin through ~3.5kΩ resistance ($R_{HCFON}$). When disabled, the CFET pin connects to VPACK through ~2kΩ resistance ($R_{HCFOFF}$). These resistances are composed of both physical resistors and the ON resistance of the internal switches.

## 9.5 Regulator and Supply Pins

The device has an internal regulator that uses an external power transistor to provide regulated voltages for its internal circuits. The output of this regulator also powers other system circuitry, including the microcontroller.

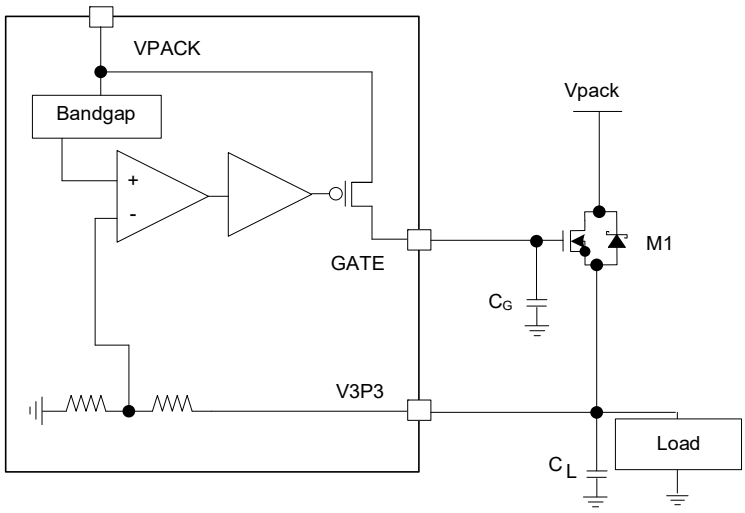



**Figure 40. External Power Supply Components**

### 9.5.1 V3P3 Pin 16

The V3P3 pin is the analog 3.3V power supply input. This pin is the analog feedback pin for the regulator control circuit. Connect a 10µF bypass capacitor between this pin and digital ground (DGND).

Connect a NMOS between the GATE pin and V3P3 pin. The device can power external circuitry from this pin.

Route the NMOS drain connection to the pack voltage separately to the battery pack from the high current load path to minimize any transient effects.

Choose an NMOS device that has a maximum VDS voltage rating greater than the maximum expected voltage transient. The NMOS device chosen should be within the safe operation curve (load current versus VDS voltage). Choose an NMOS that has a $V_{GS}$ ON threshold less than 2.5V. The chosen threshold reduces the minimum operational pack voltage. The minimum operational pack voltage is determined by the $V_{GS}$ ON, plus the V3P3 operating voltage.

### 9.5.2 GATE Pin 15

The GATE Pin drives the gate terminal of the external NMOS transistor in the loop of the register. The integrated controller with an external NMOS forms a LDO regulator.

A capacitor connected between the Gate pin and DGND is required for regulator stability. The value of the capacitor should be at least 1µF. This capacitance should be ~1/8 to 1/10 of the V3P3 load capacitance.

The ratio between the Gate and V3P3 capacitors determines the regulator response to load removal. A 1/8 ratio slows the regulator response while 1/10 enables the fastest response.

## 9.6 V2P5 Pin 17

The V2P5 pin is the internal 2.5V digital power supply. External connections must be limited to a 1µF decoupling capacitor to DGND. This pin is for internal use only. Do not load or drive this pin from an external source.

## 9.7 DGND Pin 18

DGND is the digital ground reference pin for the device. It must have a solid connection to the digital ground plane. If separate digital and analog ground planes are used, they should be connected together at the VSS pin.

## 9.8 $\overline{\text{ALERT}}$ Pin 19

The $\overline{\text{ALERT}}$ pin is an active low open-drain digital output pin that indicates either a fault or status bit change has occurred. A pull-up of >4.7kΩ to V3P3 or the MCU supply is necessary, a 499kΩ to V3P3 is used on the device evaluation board. Any fault that turns OFF CFET forces a transition to LP Mode ~200µs after asserting the $\overline{\text{ALERT}}$ pin low. This pin becomes high impedance while in LP Mode.

If more than one fault or status bit is asserted before reading the Fault and Status registers, the $\overline{\text{ALERT}}$ pin is released and then reasserted after the first read. The device requires the Fault and Status registers to be read a second time before releasing the $\overline{\text{ALERT}}$ pin. This is specific to cases with more than one fault/status bit assertion (0x10 Faults and 0x11 Status).

Figure 41 (A) and (B) are timing diagrams for different Fault or Status bit sequencing scenarios. Figure 41(A) is an example of two fault or status changes before a read. In this case, an OV detection sets OVF then the OV clears before a read. The OVF and the OV clear each cause separate $\overline{\text{ALERT}}$s. Figure 41(B) is an example of single persistent fault or status bit changes, each followed a read that releases $\overline{\text{ALERT}}$.

All fault and status bits that are connected to $\overline{\text{ALERT}}$ pin are logically OR'd. A Status bit that has a masked bit that is enabled prevents the bit connection to the $\overline{\text{ALERT}}$ pin.

Reading the Fault and Status registers individually does not release the $\overline{\text{ALERT}}$ pin, both must be read sequentially. A sequential read without starting at the fault register (0x10) does not release the $\overline{\text{ALERT}}$ pin.

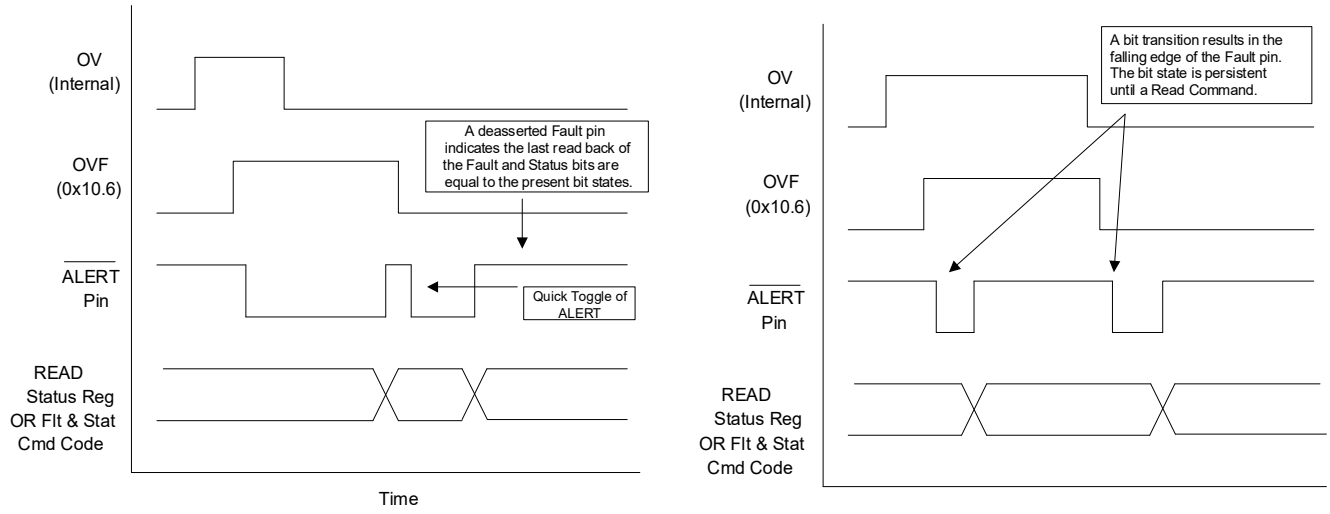



**Figure 41. (A) De-asserted Fault, (B) Persistent Fault**

## 9.9 SCL Pin 20

The SCL pin is the communications clock pin driven by the Controller for $I^2C$ communications protocol. Connect an optional minimum 4.7kΩ valued resistor from the pin to V3P3 to ensure it is pulled high in LP Mode so the wakeup with communication works properly. If the MCU has a push-pull output and ensures this is high, the resistor can be omitted to save power.

## 9.10 SDA Pin 21

The SDA pin is the serial data pin for bidirectional communications between Controller and Target for the $I^2C$ communications protocols. It is driven by the Controller for sending a Target address byte for write commands. In this Mode, the device pin is an open drain. The pin is driven by the Target for data reads. Connect a minimum 4.7kΩ valued resistor from the pin to V3P3.

## 9.11 VTEMP, THERMn Pins

THERM pins (22, 24) are analog voltage inputs that connect to external thermistor circuitry. These pins are optimized to work with an external NTC thermistors to monitor the temperature of the battery pack. The thermistors are biased by the VTEMP regulator pin (23), as shown in Figure 42.

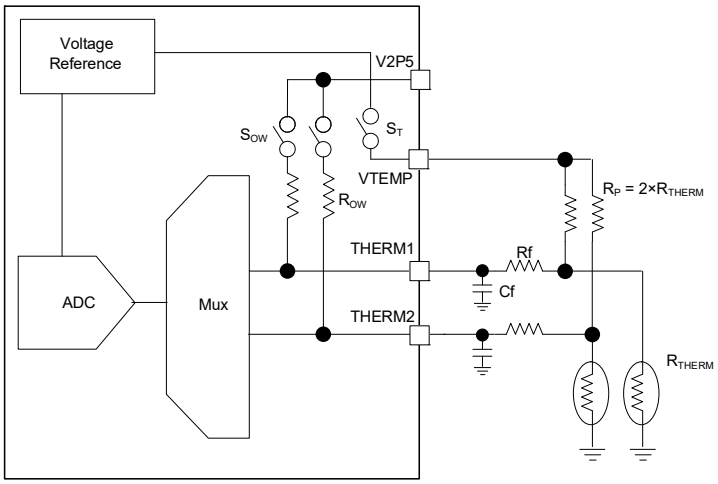



**Figure 42. Thermistor Pin Configuration**

The Thermistor inputs are sampled as part of system scan sequence (Figure 23). Before measuring the thermistors, the internal switch $S_T$ is closed, connecting the two pull-up resistors RP through the VTEMP pin to the reference voltage. This sets up a pair of voltage dividers consisting of RP and $R_{THERM}$. The voltage between these resistors is a function of the temperature ($R_{THERM}$). From the thermistor, an optional low pass filters consisting of Rf (10kΩ) and Cf (0.022µF) connects to each THERM pin. Each of these pins is then measured in sequence relative to VSS. Switches $S_{OW}$ are used only for Open-Wire test as part of the SELF TEST Loop.

Before the device performs a thermistor measurement during either AutoSCAN or a Triggered Single System Scan, the VTEMP output is turned on ~18ms before the ADC measures the THERM1 voltage. The time allows the voltage at the THERM pin to settle before measuring. The settling time at the THERM pin is dependent on the pin capacitance.

### 9.11.1 Hard RESET

A hard reset is initiated by connecting the THERM2 pin (22) above the reset threshold voltage ($RST_{VTHERM}$) for $t_{RESET}$ time. The Reset voltage threshold is defined with respect to (above) the voltage on the V2P5 pin. A switch with terminals connecting the THERM2 and the V3P3 pin is used on the evaluation boards. The Reset state is exited $t_{RST\_Exit}$ time after the falling edge on THERM2 pin occurs.

### 9.11.2 Thermistor Pins Open-Wire Test

The Thermistor pins are tested for open wires in the SELF TEST Loop of the system scan. If the measured result exceeds the threshold (~1.9V) for two consecutive tests, the device sets bit 0x10.12 VTMPF to 1. The thermistor divider network must be chosen to remain below the open-wire threshold over the range of operation.

## 9.12 CHMON Pin 26

The Charge Monitor pin detects a rising edge above the $V_{CHTHR}$ threshold. This pin is intended to be connected to the positive terminal of the charger for charger detection. A 1M internal pull-down resistor biases the voltage on the pin below the threshold.

The logic level of the pin is always available for read back (0x11.3 CH PRESI). A CH PRESI bit value of 1 indicates the voltage is above the $V_{CHTHR}$.

The device monitors for a rising edge, except for the 100ms period following shutoff of CFET. If the device is in LP Mode and a rising edge occurs, the device exits LP Mode.

Tie this pin to ground if unused.

## 9.13 DCSP, CCSP, and CSN Pins

Current is monitored by measuring the differential voltage across a current sense resistor connected between the CCSP (29) or DCSP (30) and CSN (31) pins (Figure 43). The current sense circuit individually monitors charge and discharge currents. Both charge (CCSP-CSN) and discharge (DCSP-CSN) currents are measured every system scan. Current measurements are interlaced with the other measurements during the system scan.

The Charge Current Sense Positive (CCSP) pin is connected CHARGE- terminal for split current sense (0x82.7 CPWR = 1) applications. The CCSP pin is connected to the Pack- node for shared current sense (CPWR = 0) applications.

The Discharge Current Sense Positive (DCSP) pin is connected to the Pack- node.

The Current Sense Negative (CSN) pin is connected to BAT- (VSS and ground), the most negative voltage of the pack.

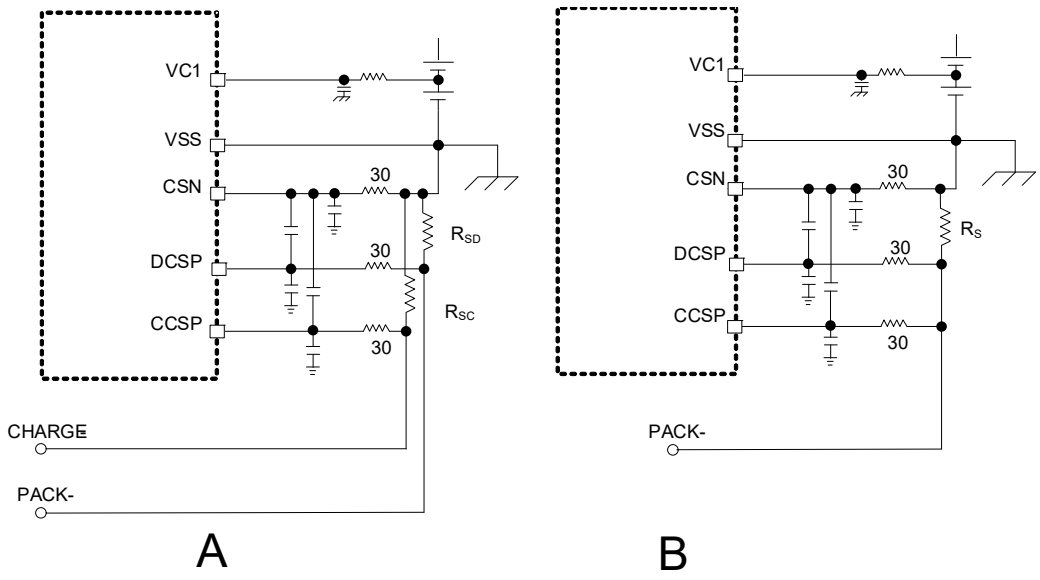



**Figure 43. Current Sense (A) Split (B) Shared**

The recommended filter configuration for the current monitor circuitry is shown in Figure 43. The 30Ω resistors along with the capacitors filter system noise to minimize measurement errors. The capacitors to ground are 1µF, and the capacitors across the input pins are 1000pF

The value of the current sense resistor is application specific and must be determined based on peak and nominal load currents, charge current and end of charge current detection (0x11.4 RSV).

Renesas does not recommend operating at the extreme limits of the inputs. In an application care should be taken to guard-band against additional noise and transients that can cause current levels to reach or exceed the maximum voltages.

## 9.14 VSS Pin

VSS is the analog ground pin (28, 32). It must have a solid connection to the ground plane(s). Connect the digital and analog ground planes together as close to the VSS pin as possible. Never connect the exposed pad to any other signal other than VSS. Multiple vias are recommended for good thermal conductivity. The PCB footprint should always have an EPAD landing. Soldering to the EPAD also provides mechanical stability.

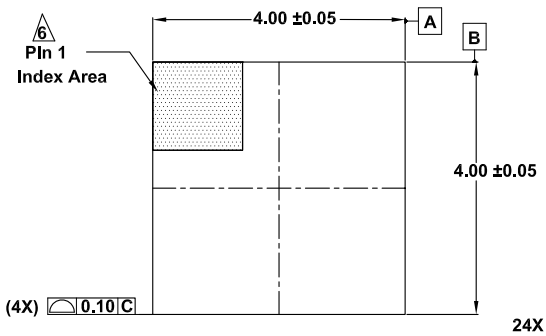
## 9.15 NC Pins

NC or No Connect pins (2, 4, 6, 9, 12, 14, 25, 27) must not be biased or connected to other system nodes including, but not limited to, ground. These pins PCB pads must be allowed to float.

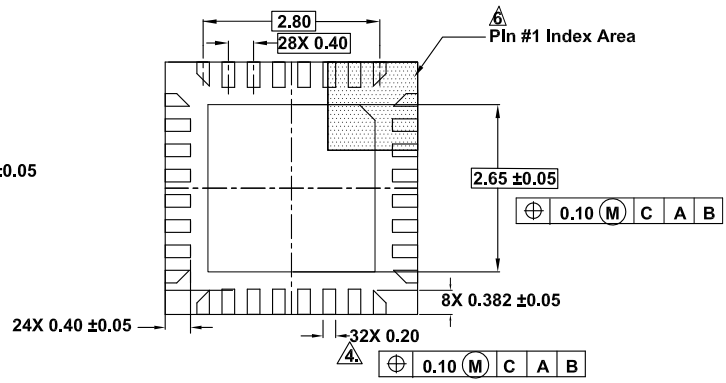
# 10. Package Outline Drawing

For the most recent package outline drawing, see L32.4x4C.

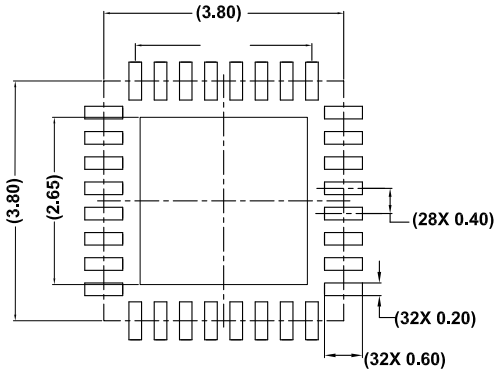
L32.4x4C
32 Lead Quad Flat No-Lead Plastic Package (QFN)
Rev 2, 4/2022



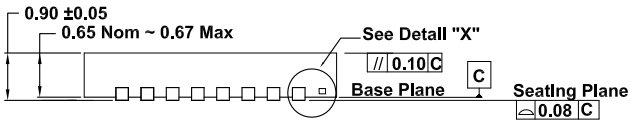

Top View



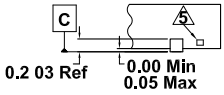

Bottom View




Typical Recommended Land Pattern




Side View




Detail "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

# 11. Ordering Information

| Part Number[1] [2] | Part Marking | Package Description[3] (RoHS Compliant) | Pkg. Dwg. # | Carrier Type[4] | Temp Range |
|---|---|---|---|---|---|
| RAA489250B2GNP#HA5 | 489250B 02GNP | 32 Ld 4×4 QFN | L32.4x4C | Reel, 6k | -40 to +85°C |
| RAA489250B2GNP#MA5 | | | | Reel, 1k | |
| RAA489250B2GNP#AA5 | | | | Tray | |
| RTKA489250DE0000BU | Evaluation Board | | | | |
| RTKA489250DK0000BU | Evaluation Kit | | | | |

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 3. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

**Table 33. Key Differences Between Family of Parts[1]**

| Part Number | Cells Supported | | Pack Voltage (V Op) | | Cell Bal. | $I_{PACK}$ Sense | Fuel ga. | Charge/ Discharge FET | | Supply Current (A) | | SA | Int. MCU | Int. ADC | DC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | | | CTRL | FET | Norm. | SP | | | | |
| RAA489250B | 5 | 5 | 5 | 23 | Int. | Low Side | No | High Side | CFET | 100µ | 4µ | No | No | 12-bit | No |
| RAJ240100 | 3 | 10 | 4 | 50 | Int. | Low Side | Yes | High Side | Both | 50µ | 1µ | Yes | Yes RL78 | 18-bit | No |
| RAJ240310 | 3 | 10 | 4 | 50 | Int. | Low Side | Yes | Low Side | Both | 35µ | 1µ | Yes | Yes RL78 | 18-bit | No |
| RAJ240071 | 2 | 5 | 4 | 25 | Int. | Low Side | Yes | High Side | Both | 40µ | 1µ | Yes | Yes RL78 | 18-bit | No |
| RAA489206 | 4 | 16 | 12 | 55 | Int./ Ext. | Low Side | No | Both | Both | 200µ | 10µ | No | No | 16-bit | No |
| RAA489204 | 6 | 14 | 12 | 65 | Int./ Ext. | No | No | No | N/A | 3.3m | 19µ | No | No | 14-bit | Yes |
| ISL94208 | 4 | 6 | 8 | 27 | Int./ Ext. | Low Side | No | Low Side | Both | 850µ | 2µ | No | No | No | No |
| ISL94202 | 3 | 8 | 4 | 36 | Ext. | High Side | No | High Side | Both | 348µ | 13µ | Yes | No | 14-bit | No |

1. Stand Alone = SA, ga. = Gauge, Int. = Internal, DC= Daisy Chain, Bal. = Balance, CTRL = Control, Norm. = Normal, SP = Sleep

# 12. Revision History

| Rev. | Date | Description |
|---|---|---|
| 1.00 | Nov 13, 2024 | Initial release |

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(Disclaimer Rev.1.01 Jan 2024)


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