

2.5V Drive Pch+Pch MOS FET

US6J2

●Structure

Silicon P-channel MOS FET

●Features

- 1) Two Pch MOS FET transistors in a single TUMT6 package.
- 2) Mounting cost and area can be cut in half.
- 3) Low on-resistance.
- 4) Low voltage drive (2.5V) makes this device ideal for portable equipment.
- 5) Drive circuits can be simple.

●Applications

Switching

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6J2		○

●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2>

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DS}	-20	V
Gate-source voltage	V_{GS}	±12	V
Drain current	Continuous	I_D	±1
	Pulsed	I_{DP} *1	±4
Source current (Body diode)	Continuous	I_S	-0.4
	Pulsed	I_{SP} *1	-4
Total power dissipation	P_D *2	1.0	W / TOTAL
		0.7	W / ELEMENT
Channel temperature	T_{ch}	150	°C
Range of Storage temperature	T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 50\%$

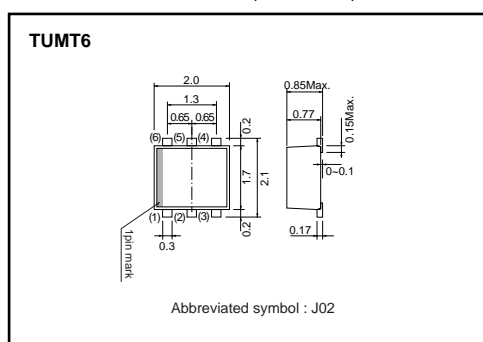
*2 Mounted on a ceramic board

●Thermal resistance

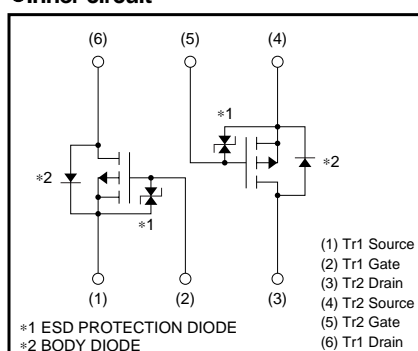
Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	125	°C/W / TOTAL
		179	°C/W / ELEMENT

* Mounted on a ceramic board

●External dimensions (Unit : mm)



●Inner circuit



Transistors

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2 MOS FET>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 12V$, $V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -1mA$, $V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	—	—	-1.0	μA	$V_{DS} = -20V$, $V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	-0.7	—	-2.0	V	$V_{DS} = -10V$, $I_D = -1mA$
Static drain-source on-state resistance	$R_{DS(on)}$	—	280	390	$m\Omega$	$I_D = -1A$, $V_{GS} = -4.5V$
		—	310	430	$m\Omega$	$I_D = -1A$, $V_{GS} = -4V$
		—	570	800	$m\Omega$	$I_D = -0.5A$, $V_{GS} = -2.5V$
Forward transfer admittance	$ Y_{fs} $	* 0.7	—	—	S	$V_{DS} = -10V$, $I_D = -0.5A$
Input capacitance	C_{iss}	—	150	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	20	—	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	—	20	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	* —	9	—	ns	$I_D = -0.5A$
Rise time	t_r	* —	8	—	ns	$V_{DD} = -15V$
Turn-off delay time	$t_{d(off)}$	* —	25	—	ns	$V_{GS} = -4.5V$
Fall time	t_f	* —	10	—	ns	$R_L = 30\Omega$
Total gate charge	Q_g	* —	2.1	—	nC	$V_{DD} = -15V$ $R_L = 15\Omega$
Gate-source charge	Q_{gs}	* —	0.5	—	nC	$V_{GS} = -4.5V$ $R_G = 10\Omega$
Gate-drain charge	Q_{gd}	* —	0.5	—	nC	$I_D = -1A$

* Pulsed

<Body diode (Source-drain)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD}	—	—	-1.2	V	$I_S = -0.4A$, $V_{GS} = 0V$

Transistors

●Electrical characteristic curves

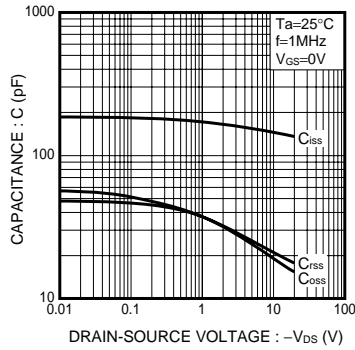


Fig.1 Typical Capacitance vs. Drain-Source Voltage

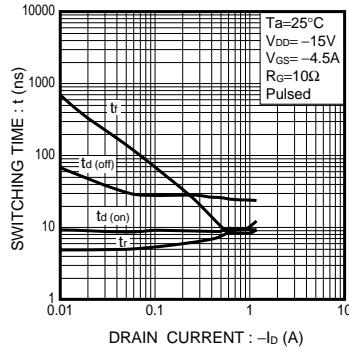


Fig.2 Switching Characteristics

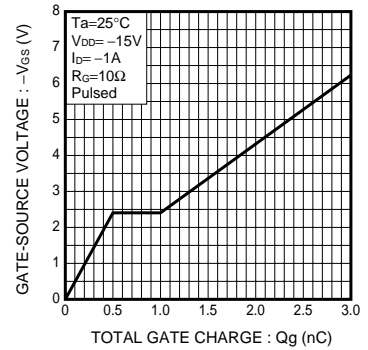


Fig.3 Dynamic Input Characteristics

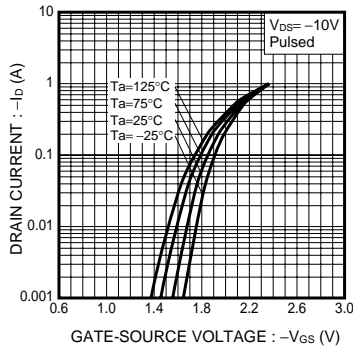


Fig.4 Typical Transfer Characteristics

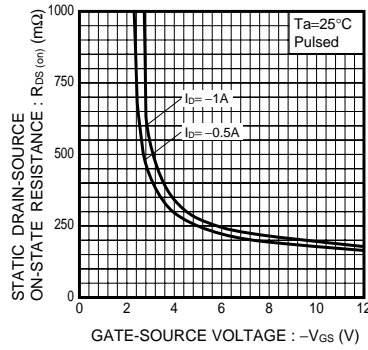


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

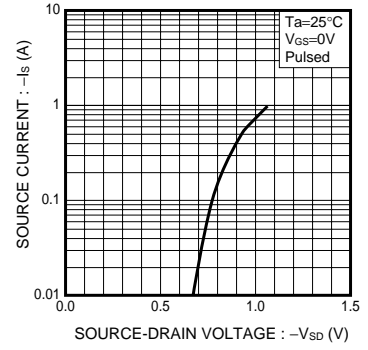


Fig.6 Source Current vs. Source-Drain Voltage

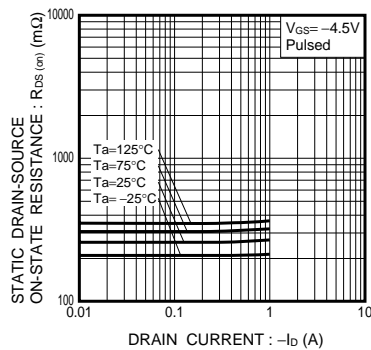


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (II)

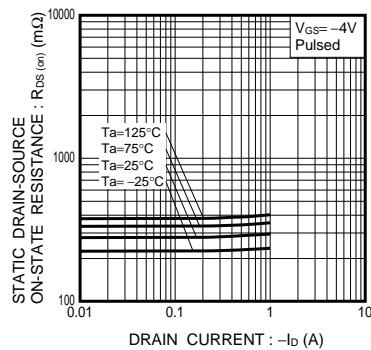


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (III)

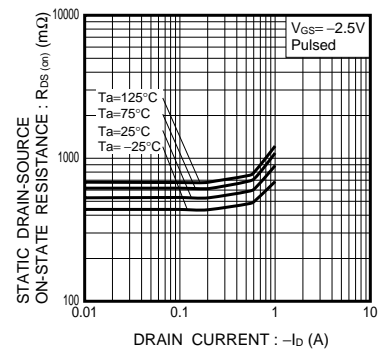


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (I)

Transistors

●Measurement circuits

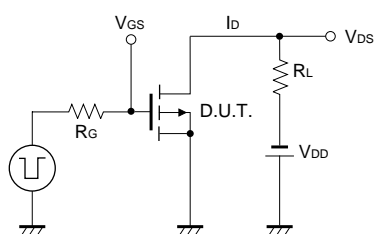


Fig.10 Switching Time Measurement Circuit

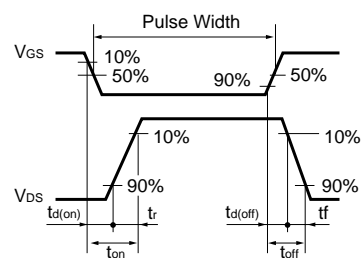


Fig.11 Switching Waveforms

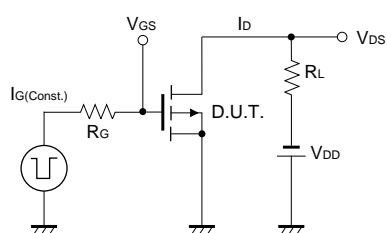


Fig.12 Gate Charge Measurement Circuit

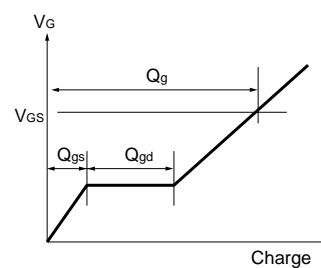


Fig.13 Gate Charge Waveform

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