Peak 3A Bus Termination Regulator

General Description

The RT9173/A regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage which adjusted by two external voltage divider resistors. The regulator is capable of sourcing or sinking up to 3A of peak current while regulating an output voltage to within 2% (DDR 1) and 3% (DDR 2) or less.

The RT9173/A, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses and distributed backplane designs. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM.

Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of the output fault conditions.

Ordering Information

RT9173/A □ □□

- Package Type
  - M5 : TO-263-5
  - L5 : TO-252-5
  - S : SOP-8
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)
- 3A Sink & Source
- 1.5A Sink & Source

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100%matte tin (Sn) plating.

Features

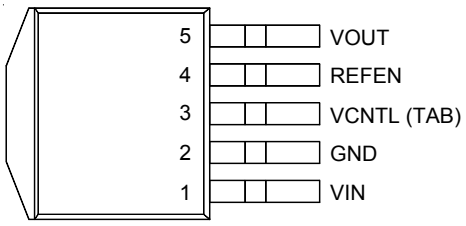
- **Support Both DDR 1 (1.25V_{TT}) and DDR 2 (0.9V_{TT}) Requirements**
- **SOP-8, TO-252-5 and TO-263-5 Packages**
- **Capable of Sourcing and Sinking 3A Peak Current**
- **Current-limiting Protection**
- **Thermal Protection**
- **Integrated Power MOSFETs**
- **Generates Termination Voltages for SSTL-2**
- **High Accuracy Output Voltage at Full-Load**
- **Adjustable V_{OUT} by External Resistors**
- **Minimum External Components**
- **Shutdown for Standby or Suspend Mode Operation with High-impedance Output**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

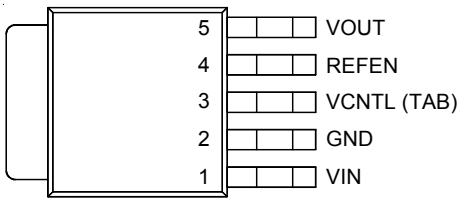
- DDR Memory Termination
- Active Termination Buses
- Supply Splitter

Pin Configurations

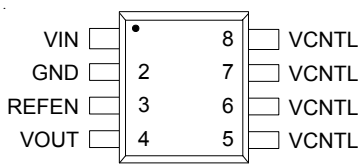
(TOP VIEW)



TO-263-5 (RT9173A)

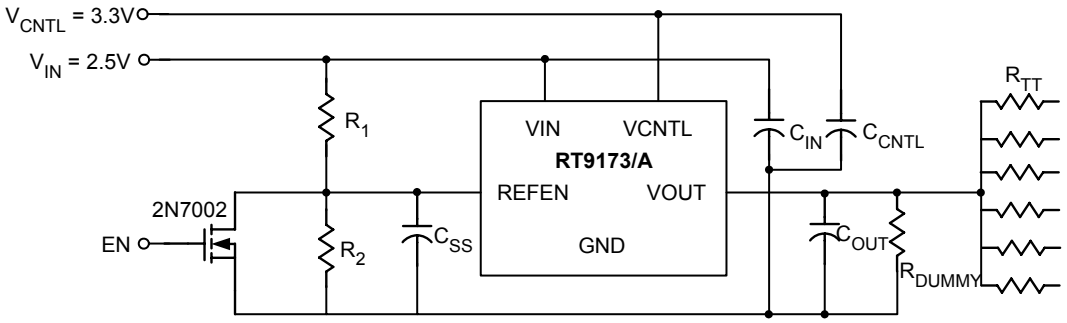


TO-252-5 (RT9173A)



SOP-8 (RT9173)

Typical Application Circuit



$R_1 = R_2 = 100k\Omega$, $R_{TT} = 50\Omega / 33\Omega / 25\Omega$

$C_{OUT(MIN)} = 10\mu F$ (Ceramic) + $1000\mu F$ under the worst case testing condition

$R_{DUMMY} = 1k\Omega$ as for VOUT discharge when VIN is not present but VCNTL is present

$C_{SS} = 1\mu F$, $C_{IN} = 470\mu F$ (Low ESR), $C_{CNTL} = 47\mu F$

Test Circuit

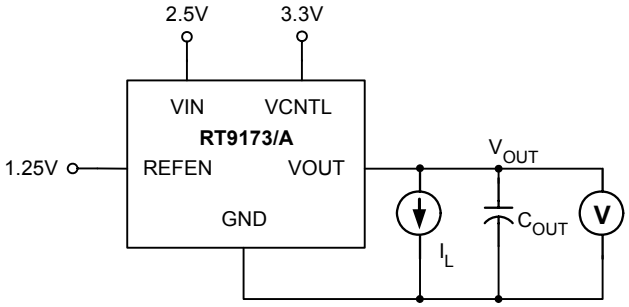


Figure 1. Output Voltage Tolerance, ΔV_{LOAD}

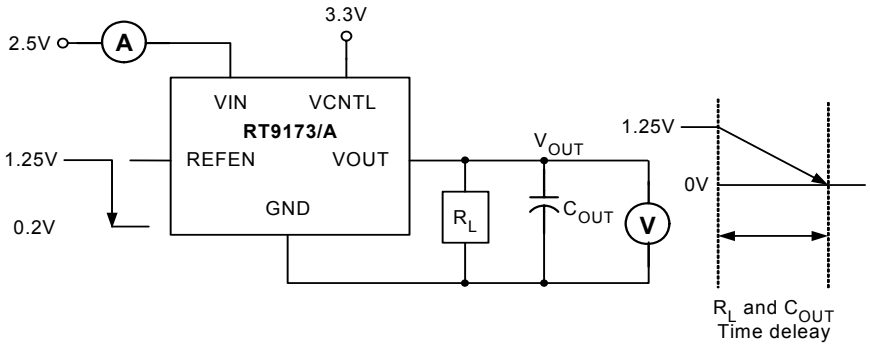


Figure 2. Current in Shutdown Mode, I_{SHDN}

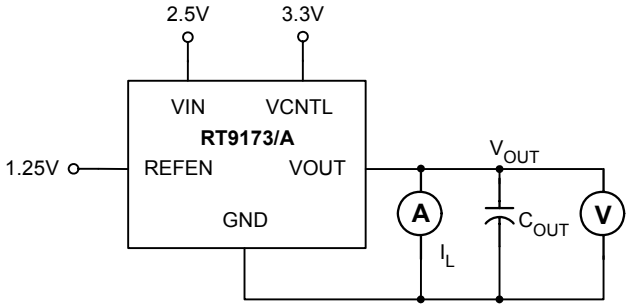


Figure 3. Current Limit for High Side, I_{LIMIT}

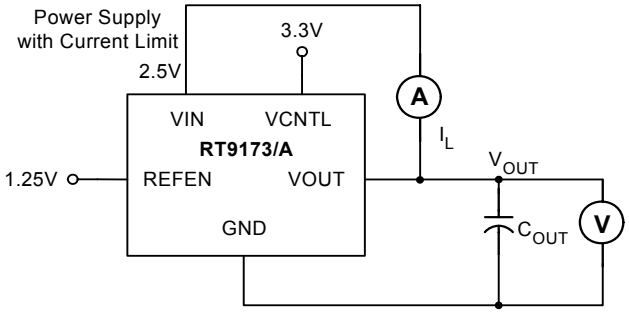


Figure 4. Current Limit for Low Side, I_{LIMIT}

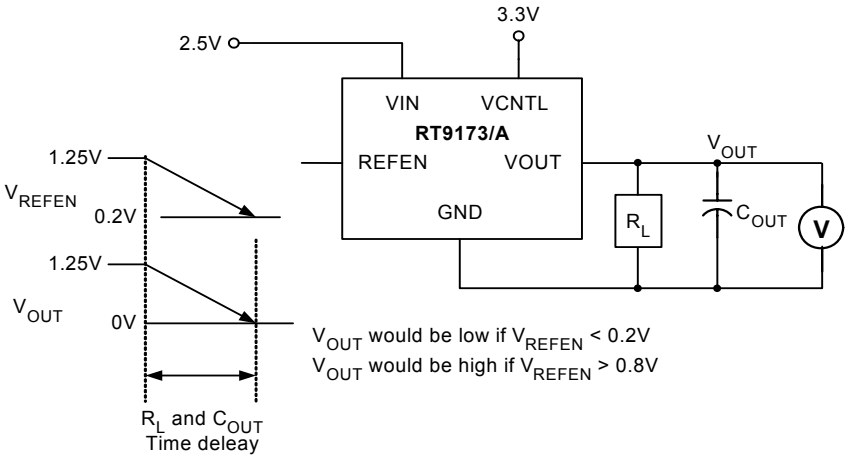
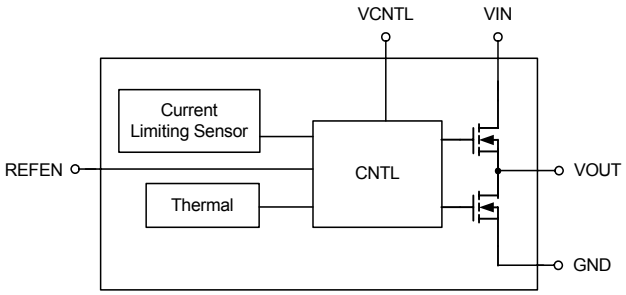


Figure 5. REFEN Pin Shutdown Threshold, $V_{TRIGGER}$

Functional Pin Description

Pin Name	Pin Function
VIN	Power Input Voltage
GND	Ground
VCNTL	Gate Drive Voltage
REFEN	Reference Voltage Input and Chip Enable
VOUT	Output Voltage

Function Block Diagram



Absolute Maximum Ratings

- Input Voltage ---------- 7V
- Power Dissipation ---------- Internally Limited
- ESD Rating ---------- 2kV
- Storage Temperature Range ---------- –65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Power Dissipation, P_D @ T_A = 25°C
  - TO-263-5 ---------- 1.923W
  - TO-252-5 ---------- 1.471W
  - SOP-8 ---------- 0.625W
- Package Thermal Resistance (Note 1)
  - TO-263-5, θ_{JC} ---------- 7.7°C/W
  - TO-252-5, θ_{JC} ---------- 8°C/W
  - SOP-8, θ_{JC} ---------- 23.2°C /W
  - TO-263-5,θ_{JA} ---------- 52°C/W
  - TO-252-5, θ_{JA} ---------- 68°C/W
  - SOP-8, θ_{JA} ---------- 160°C/W

Electrical Characteristics

(V_{IN} = 2.5V, V_{CNTL} = 3.3V, V_{REFEN} = 1.25V, C_{OUT} = 10µF (Ceramic), T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Offset Voltage	V_{OS}	I_{OUT} = 0A, Figure 1 (Note 2)	-20	0	20	mV
Load Regulation (DDR 1/2)	ΔV_{LOAD}	I_L : 0A → 1.5A, Figure 1	--	0.8/1.2	2/3	%
		I_L : 0A → -1.5A	--	0.8/1.2	2/3	
Input Voltage Range (DDR 1/2) (Note 3)	V_{IN}	Keep $V_{CNTL} \geq V_{IN}$ on operation power on and power off sequences	1.6	2.5/1.8	--	V
	V_{CNTL}		--	3.3	6	
Operating Current of VCNTL	I_{CNTL}	No Load	--	6.5	10	mA
Current In Shutdown Mode	I_{SHDN}	$V_{REFEN} < 0.2V$, R_L = 180Ω, Figure 2	--	50	90	µA
Short Circuit Protection						
Current limit	I_{LIMIT}	Figure 3,4	3.0	--	--	A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5V	125	150	--	°C
Thermal Shutdown Hysteresis		Guaranteed by design	--	50	--	°C
Shutdown Function						
Shutdown Threshold Trigger	$V_{TRIGGER}$	Output = High, Figure 5	0.8	--	--	V
	$V_{TRIGGER}$	Output = Low, Figure 5	--	--	0.2	

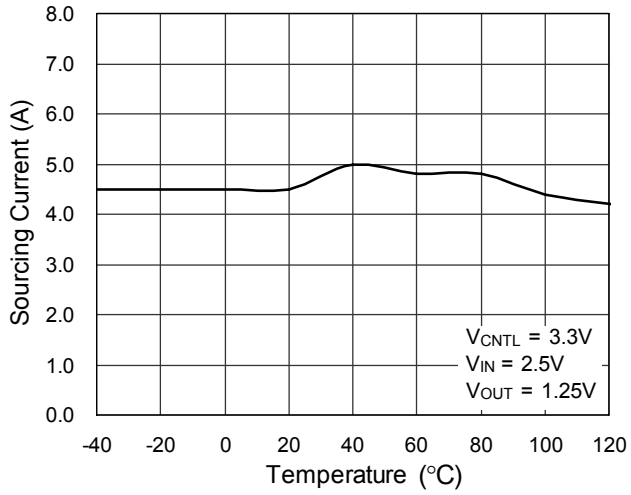
Note 1. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board (single Layers, 1S) of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the on the center of V_{CTRL} pins (Lead 6 & 7) for SOP-8 packages, the center of heat sink (tab) for TO-252-5 and TO-263-5 packages.

Note 2. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REFEN}.

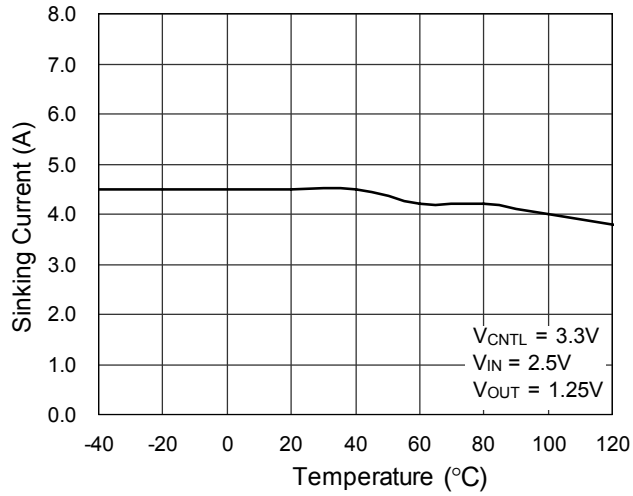
Note 3. For safely operate your system, the 3.3V rail MUST be tied to V_{CNTL} rather than 5V rail, especially for the new part of RT9173ACL5.

Typical Operating Characteristics

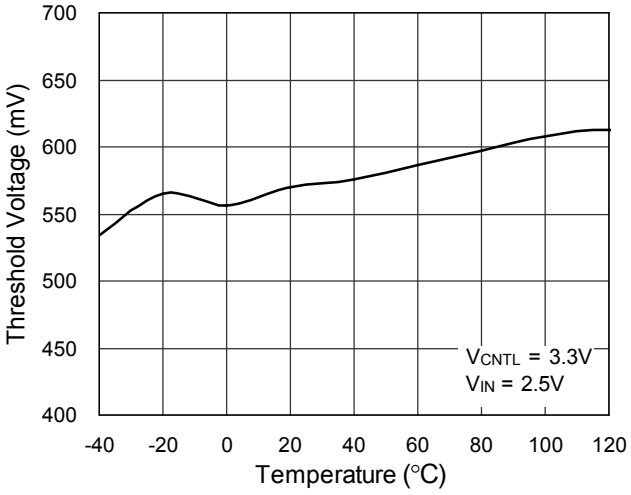
Sourcing Current (Peak) vs. Temperature



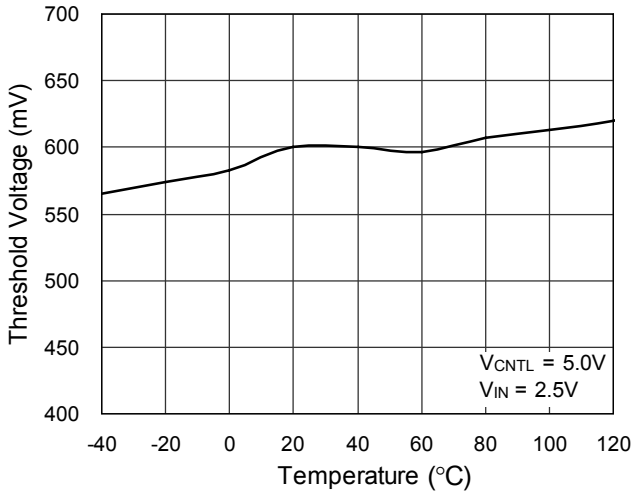
Sinking Current (Peak) vs. Temperature



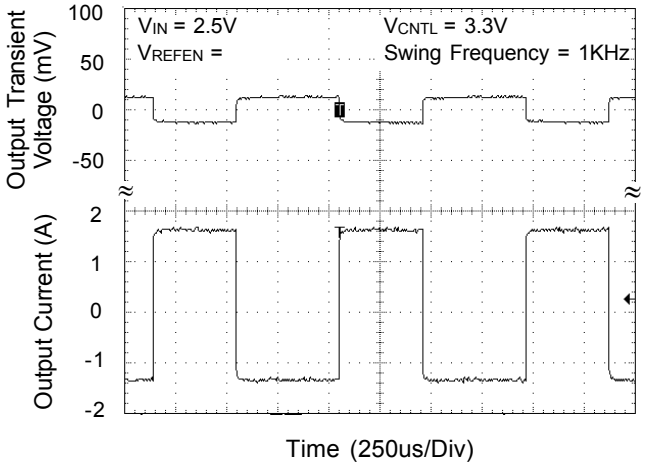
Turn-On Threshold vs. Temperature



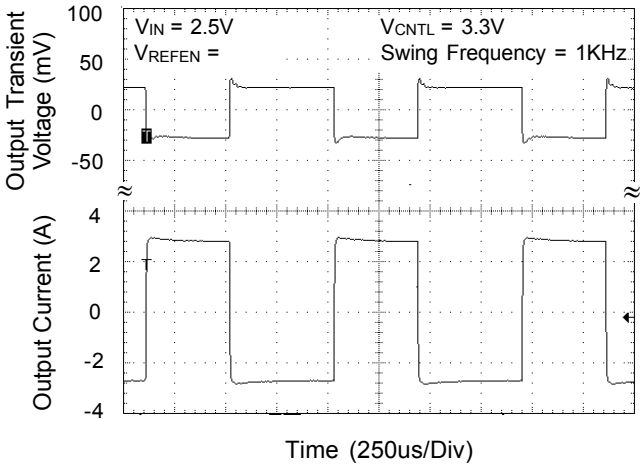
Turn-On Threshold vs. Temperature



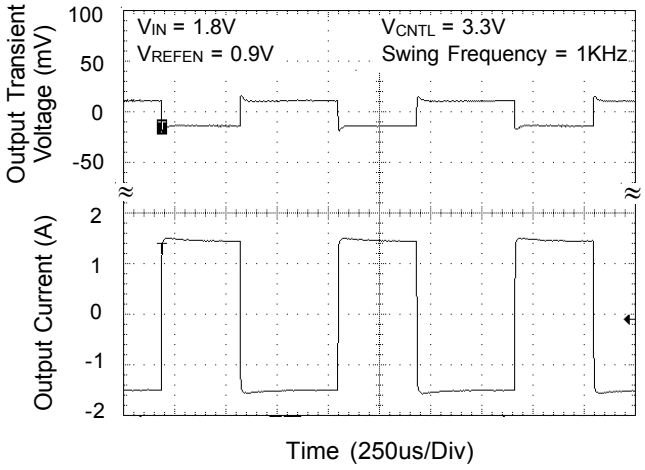
1.25V$_{TT}$ @ 1.5A Transient Response



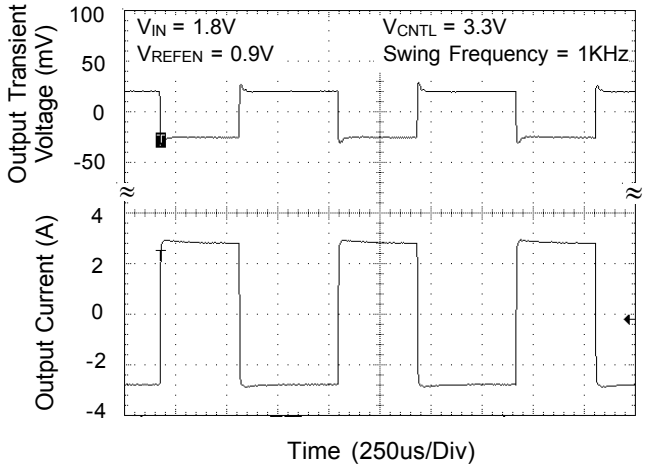
1.25V$_{TT}$ @ 3A Transient Response



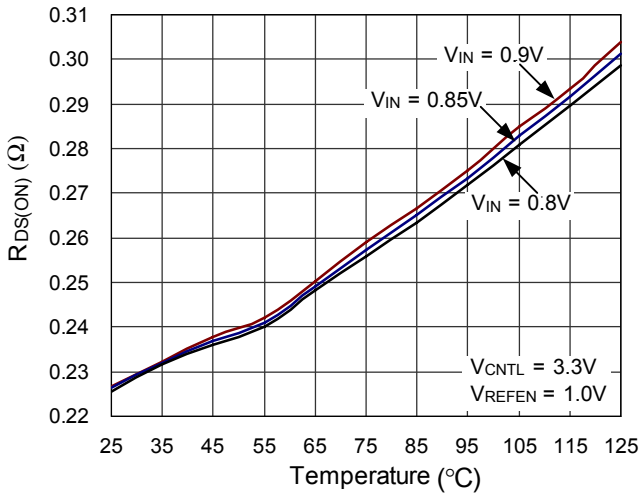
0.9V$_{TT}$ @ 1.5A Transient Response



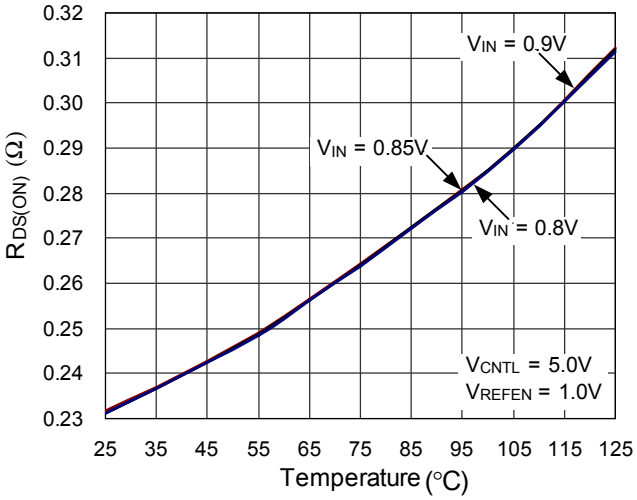
0.9V$_{TT}$ @ 3A Transient Response



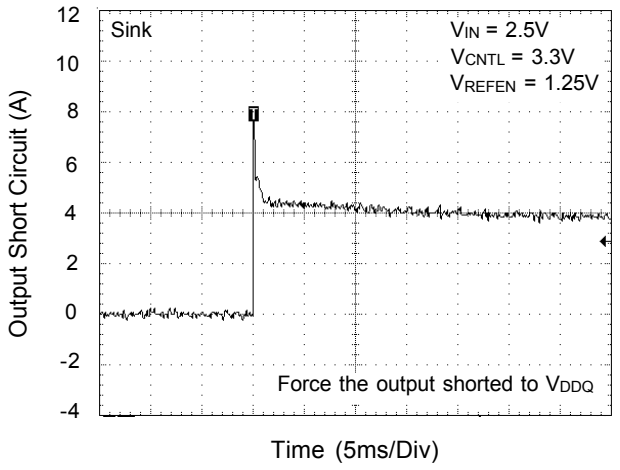
R$_{DS(ON)}$ vs. Temperature



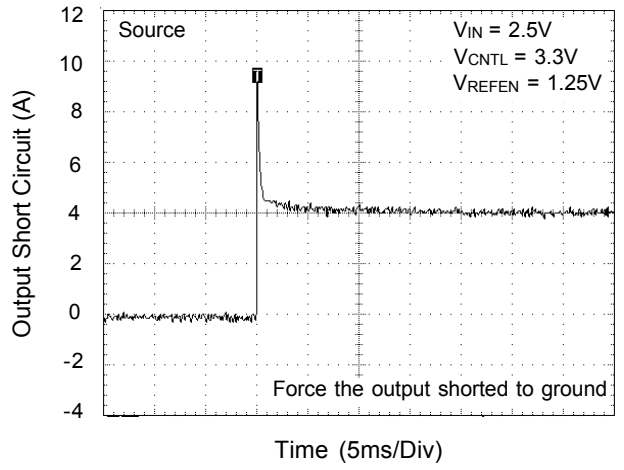
R$_{DS(ON)}$ vs. Temperature



Output Short-Circuit Protection



Output Short-Circuit Protection



Application Information

Internal Parasitic Diode

Avoid forward-bias internal parasitic diode, V_{OUT} to V_{CNTL}, and V_{OUT} to V_{IN}, the V_{OUT} should not be forced some voltage respect to ground on this pin while the V_{CNTL} or V_{IN} is disappeared.

Consideration while Designs the Resistance of Voltage Divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on V_{REFEN} is below 0.2V.

In addition, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.

How to reduce power dissipation on Notebook PC or the dual channel DDR SDRAM application?

In notebook application, using RichTek's Patent "Distributed Bus Terminator Topology" with choosing RichTek's product is encouraged.

Distributed Bus Terminating Topology

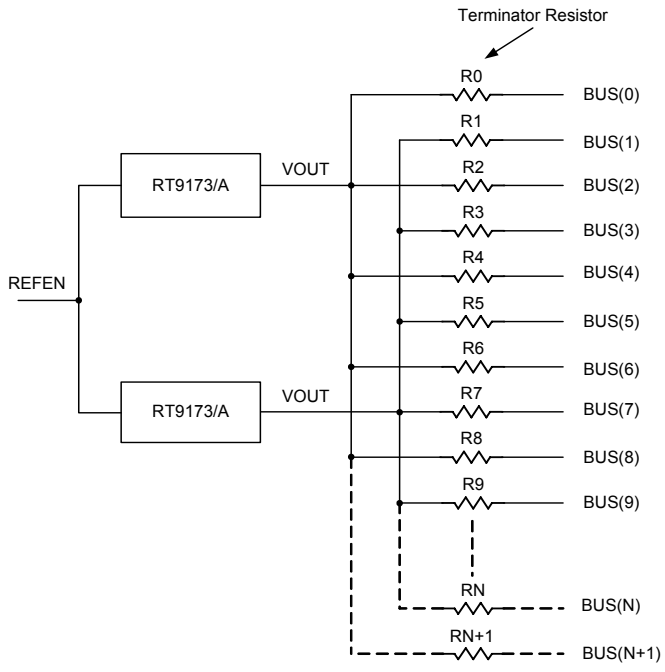


Figure 6

Thermal Consideration

RT9173/A regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continued operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. The junction to ambient thermal resistance θ_{JA} highly depends on IC package, PCB layout, and the rate of surroundings airflow. θ_{JA} for SOP-8 package is 160°C/W and TO-263-5 package is 52°C/W on standard JEDEC 51-3 (**single layer, 1S**) thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following

formula :

$P_{D(MAX)}$ = (125°C - 25°C) / (160 °C/W)= 0.625W (SOP-8 package)

$P_{D(MAX)}$ = (125°C- 25°C) / (52 °C/W)= 1.923W (TO- 263-5 package)

Since the multiple V_{CTRL} pins of the SOP-8 package are internally fused and connected to lead frame, it is efficient to dissipate the heat by adding cooper area on V_{CTRL} footprint. Figure 7 shows the package sectional drawing of SOP-8. Every package has several thermal dissipation paths, as show in Figure 8, the thermal resistance equivalent circuit of SOP-8. The path 2 is the main path of thermal flow due to these materials thermal conductivity. We define the center of multiple V_{CTRL} pins are the case point of the path 2.

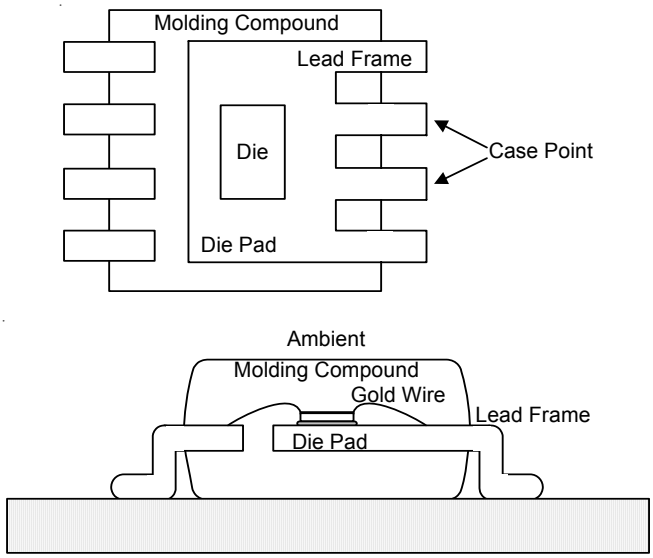


Figure 7. The Package Section Drawing of RT9173/A SOP-8 Package

The thermal resistance θ_{JA} of IC package is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased efficiently by adding copper under the main path of thermal flow on the package.

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9173/A package, the Figure 9 and the Figure 10 show the thermal resistance θ_{JA} vs. copper area of SOP-8 and TO-263-5 packages on single layer (1S) and 4-layer (2S2P) thermal test board at T_A = 25°C, PCB copper thickness = 2oz.

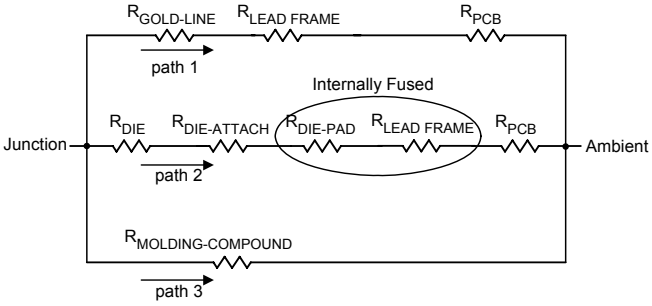


Figure 8. Thermal Resistance Equivalent Circuit of RT9173/A SOP-8 Package

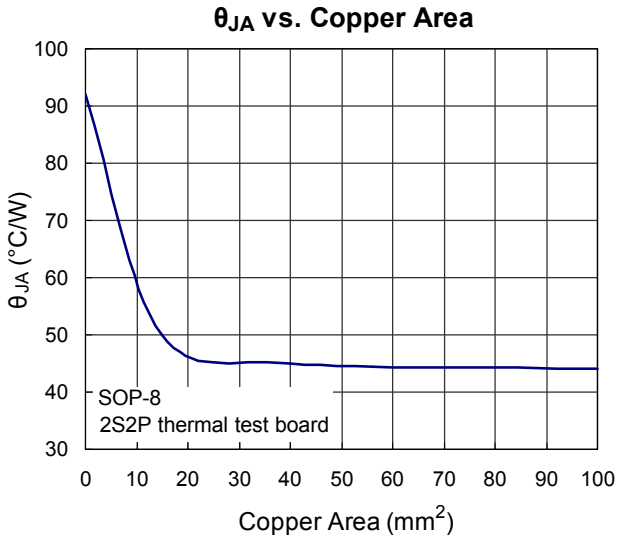


Figure 9. Thermal Resistance θ_{JA} vs. Copper Area of SOP-8 Packages

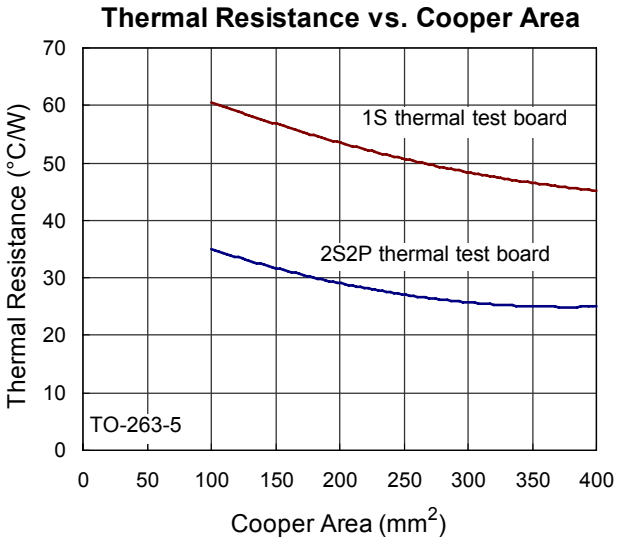


Figure 10. Thermal Resistance θ_{JA} vs. Copper Area of TO-263-5 Packages

For example, as shown in Figure 9, RT9173/A SOP-8 with 10mm x 10mm cooper area on 4-layers (2S2P) thermal test board at T_A = 25°C, we can obtain the lower thermal resistance about 45°C/W. The power maximum dissipation can be calculated as :

$P_{D(MAX)}$ = (125°C - 25°C) / (45 °C/W) = 2.22W (SOP-8)

As shown in Figure 10, RT9173/A TO-263-5 with 15mm x 15mm cooper area on 4-layers (2S2P) thermal test board at T_A = 25°C, we can obtain the lower thermal resistance about 29°C/W. The power maximum dissipation

can be calculated as :

$P_{D(MAX)}$ = (125°C - 25°C) / (29°C/W) = 3.45W (TO-263-5)

Figure 11 and Figure 12 of power dissipation vs. copper area allow the designer to see the effect of rising ambient temperature on the maximum power allowed.

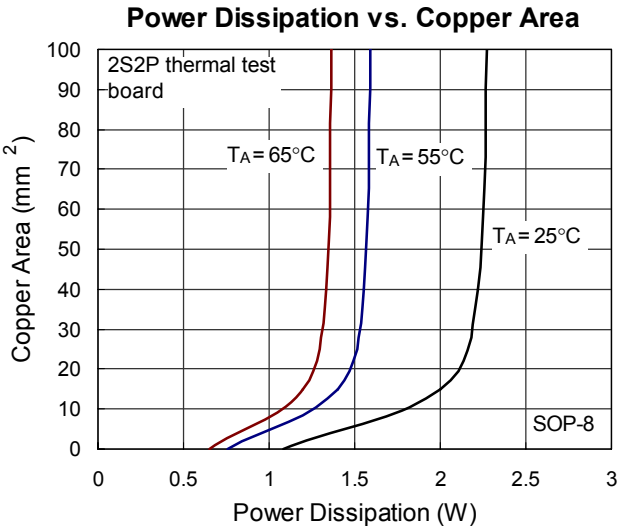


Figure 11. Power Dissipation vs. Copper Area of SOP-8 Package

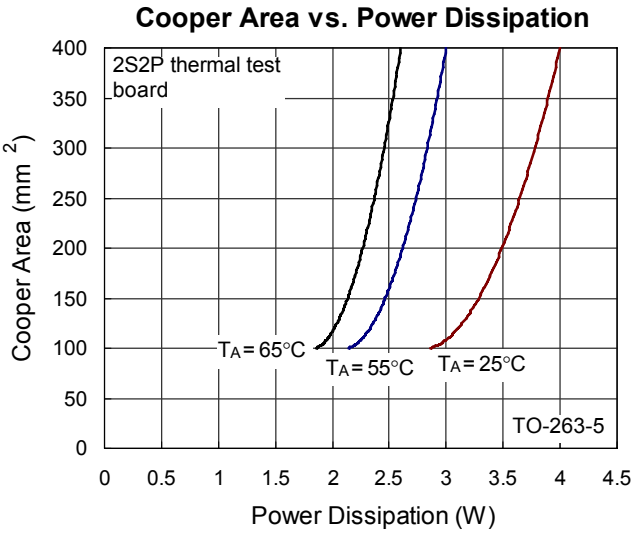
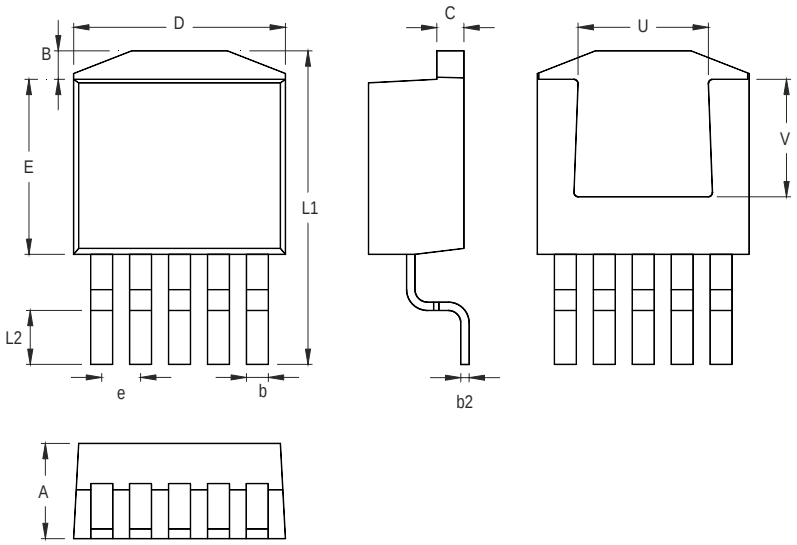


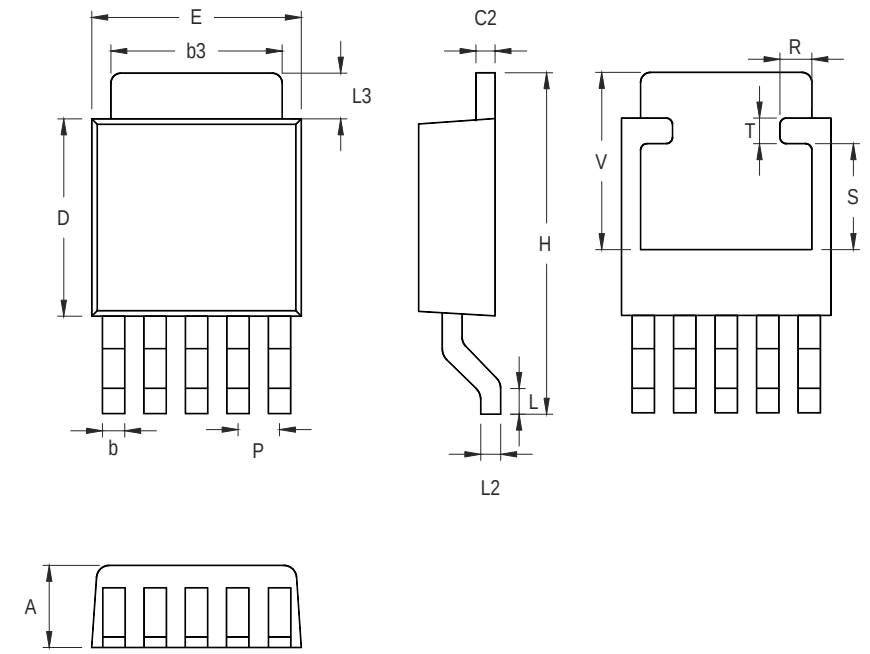
Figure 12. Power Dissipation vs. Copper Area of TO-263-5 Package

Outline Dimension



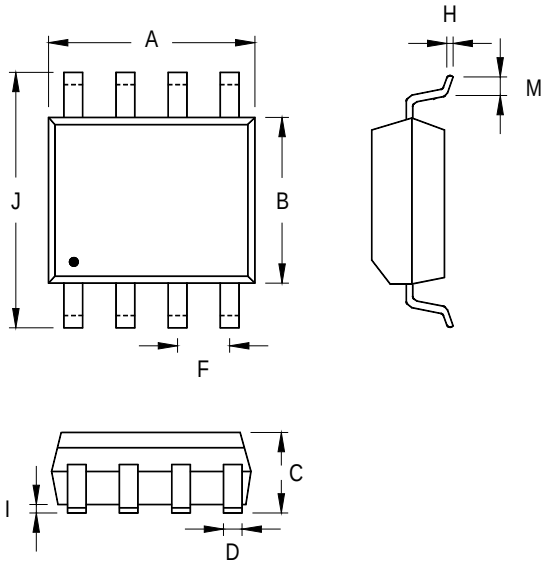
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	9.652	10.668	0.380	0.420
B	1.143	1.676	0.045	0.066
E	8.128	9.652	0.320	0.380
A	4.064	4.826	0.160	0.190
C	1.143	1.397	0.045	0.055
U	6.223 Ref.		0.245 Ref.	
V	7.620 Ref.		0.300 Ref.	
L1	14.605	15.875	0.575	0.625
L2	2.286	2.794	0.090	0.110
b	0.660	0.914	0.026	0.036
b2	0.305	0.584	0.012	0.023
e	1.524	1.829	0.060	0.072

5-Lead TO-263 Plastic Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.184	2.388	0.086	0.094
b	0.381	0.889	0.015	0.035
b3	4.953	5.461	0.195	0.215
C2	0.457	0.889	0.018	0.035
D	5.334	6.223	0.210	0.245
E	6.350	6.731	0.250	0.265
H	9.000	10.414	0.354	0.410
L	0.508	1.780	0.020	0.070
L2	0.508 Ref.		0.020 Ref.	
L3	0.889	2.032	0.035	0.080
P	1.270 Ref.		0.050 Ref.	
V	5.200 Ref.		0.205 Ref.	
R	0.200	1.500	0.008	0.059
S	2.500	3.400	0.098	0.134
T	0.500	0.850	0.020	0.033

5-Lead TO-252 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

8-Lead SOP Plastic Package

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