PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT
μPD70F3778,70F3779,70F3780,70F3781,70F3782, 70F3783,70F3784,70F3785,70F3786

V850ES/JH3-E, V850ES/JJ3-E
32-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD70F3778, 70F3779, 70F3780, 70F3781, 70F3782, 70F3783 (V850ES/JH3-E), and μPD70F3784, 70F3785, 70F3786 (V850ES/JJ3-E) are products of the V850 32-bit single-chip microcontrollers, and include peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, a DMA controller , a CAN controller , a USB function controller , and a Ethernet® controller.

In addition to their high real-time responsiveness and one-clock-pitch execution of instructions, the V850ES/JH3-E, and V850ES/JJ3-E include instructions executed via a hardware multiplier, saturation instructions, and bit manipulation instructions.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850ES/JH3-E, V850ES/JJ3-E Hardware User's Manual: To be prepared
V850ES Architecture User's Manual: U15943E

FEATURES

- Number of instructions: 83
- Minimum instruction execution time:
  20 ns (@ 50 MHz operation with main clock (f_{XX}))
- Clock
  - Main clock oscillation: f_X = 3 to 6.25 MHz
  - Subclock oscillation: f_{XT} = 32.768 kHz
  - Internal oscillation: f_R = 220 kHz (TYP.)
- General-purpose registers: 32 bits × 32 registers
- Instruction set:
  Signed multiplication, saturation operations, 32-bit shift instructions, bit manipulation instructions, load/store instructions
- Memory space:
  64 MB linear address space
- External bus interface:
  Multiplexed bus mode
  Separate bus mode
- Internal memory
  Flash memory: 256/384/512 KB
  RAM: 76/124 KB
  (Including 16/64 KB of data RAM area)
- I/O lines Total: 84/100
- Interrupts and exceptions
  Non-maskable interrupts: 2 sources
  Maskable interrupts: 99/103/109/113 sources
- Timer/counters
  16-bit timer/event counter AA (TAA): 6 channels
  16-bit timer/event counter AB (TAB): 2 channels
  Motor control function supported
  16-bit interval timer M (TMM): 4 channels
  16-bit encoder timer T (TMT): 1 channel
- Real-time counter: 1 channel
- Watchdog timer: 1 channel
- Real-time output function: 6 channels
- A/D converter: 10-bit resolution × 10/12 channels
- Serial interface
  - Ethernet controller: 1 channel
  - USB function controller: 1 channel
  - CAN :1 channel (μPD70F3783, 70F3786 only)
  - Asynchronous serial interface B with FIFO: 2 channels
  - Asynchronous serial interface C(UARTC): 6/8 channels
  - Clocked serial interface E(CSIE) with FIFO: 2 channels
  - Clocked serial interface F(CSIF): 5/6 channels
  - I^2C bus interface: 4/5 channels
- DMA controller: 4 channels
- Power save function:
  HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE mode
- On-chip debug function
- Package: 128-pin LQFP (V850ES/JH3-E)
  144-pin LQFP (V850ES/JJ3-E)
- Operating supply voltage: 2.85 to 3.6 V

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Function list (V850ES/JH3-E)

Generic Name		V850ES/JH3-E					
Product Name		μPD70F3778	μPD70F3779	μPD70F3780	μPD70F3781	μPD70F3782	μPD70F3783
Internal memory	Flash memory	256 KB	384 KB	512 KB	384 KB	512 KB	512 KB
	Internal RAM	60 KB	60 KB	60 KB	60 KB	60 KB	60 KB
	Data RAM	16 KB	16 KB	16 KB	64 KB	64 KB	64 KB
Memory space	Logical space	64 MB					
	External memory area	4 MB					
External bus interface		Address buses: 22, Address/data buses: 16 Separate bus/Multiplexed bus mode supported					
General-purpose register		32 bits × 32 registers					
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)					
	Subclock oscillation	f_{XT} = 32.768 kHz					
	Internal oscillation	f_R = 220 kHz (TYP.)					
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))					
I/O ports		I/O: 84 (5 V tolerant : 48)					
Timer	16-bit TAA	6 channels (among which one channel has the interval function only)					
	16-bit TAB	2 channels					
	16-bit TMM	4 channels					
	16-bit TMT	1 channel					
	Motor control	1 channel (functions when used in combination with TAA and TAB. Hi-Z output control function available)					
	Watch timer	1 channel (RTC)					
	WDT	1 channel					
Real-time output function		6 bits × 1 channel					
10-bit A/D converter		10 channels					
Serial interface	CSIF/UARTC	1 channel					
	CSIF/UARTC/I²C	2 channels					
	CSIE/UARTC	1 channel					
	CSIE Note 1/UARTC/I²C	1 channel					
	CSIF/UARTB	2 channels (one of these channels is allocated to two pins)					
	CSIE Note 1	1 channel					
	UARTC/I²C	1 channel					–
	UARTC/I²C/CAN	–					1 channel
	USB function	1 channel					
	Ethernet	1 channel					
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM, external memory)					
Interrupt source	External Note 2, 3	22 (22)	22 (22)	22 (22)	22 (22)	22 (22)	22 (22)
	Internal	79	79	79	79	79	83
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes					
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)					
On-chip debugging		MINICUBE®, MINICUBE2 supported					
Operating supply voltage		2.85 to 3.6 V					
Operating ambient temperature		–40 to +85°C					
Package		128-pin plastic LQFP (fine pitch) (14 × 20 mm)					

Notes 1. The same channel is allocated to two pins.

2. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

3. Include NMI.

Function list (V850ES/JJ3-E)

Generic Name		V850ES/JJ3-E		
Product Name		μPD70F3784	μPD70F3785	μPD70F3786
Internal memory	Flash memory	512 KB	512 KB	512 KB
	Internal RAM	60 KB	60 KB	60 KB
	Data RAM	16 KB	64KB	64 KB
Memory space	Logical space	64 MB		
	External memory area	16 MB		
External bus interface		Address buses: 24 Address/data buses: 16 Separate bus/multiplexed bus mode supported		
General-purpose register		32 bits × 32 registers		
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)		
	Subclock oscillation	f_{XT} = 32.768 kHz		
	Internal oscillation	f_R = 220 kHz (TYP.)		
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))		
I/O ports		I/O: 100 (5 V tolerant : 59)		
Timer	16-bit TAA	6 channels (among which one channel has the interval function only)		
	16-bit TAB	2 channels		
	16-bit TMM	4 channels		
	16-bit TMT	1 channel		
	Motor control	1 channel (functions when used in combination with TAA and TAB. Hi-Z output control function available)		
	Watch timer	1 channel (RTC)		
	WDT	1 channel		
Real-time output function		6 bits × 1 channel		
10-bit A/D converter		12 channels		
Serial interface	CSIF/UARTC	3 channels		
	CSIF/UARTC/I²C	2 channels		
	CSIE/UARTC	1 channel		
	CSIE Note 1/UARTC/I²C	1 channel		
	CSIF/UARTB	2 channels (one of these channels is allocated to two pins)		
	CSIE Note 1	1 channel		
	I²C	1 channel		
	UARTC/I²C	1 channel		–
	UARTC/I²C/CAN	–		1 channel
	USB function	1 channel		
	Ethernet	1 channel		
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM, external memory)		
Interrupt source	External Note 2, 3	27 (27)	27 (27)	27 (27)
	Internal	84	84	88
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes		
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)		
On-chip debugging		MINICUBE®, MINICUBE2 supported		
Operating supply voltage		2.85 to 3.6 V		
Operating ambient temperature		−40 to +85°C		
Package		144-pin plastic LQFP (fine pitch) (20 × 20 mm)		

Notes 1. The same channel is allocated to two pins.

2. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

3. Include NMI.

APPLICATIONS

○ Applications that require Ethernet controller

Home audio, printers, and scanners.

ORDERING INFORMATION

- V850ES/JH3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3778GF-GAT-AX	128-pin plastic LQFP (fine pitch) (14 × 20)	256 KB
μPD70F3779GF-GAT-AX	128-pin plastic LQFP (fine pitch) (14 × 20)	384 KB
μPD70F3780GF-GAT-AX	128-pin plastic LQFP (fine pitch) (14 × 20)	512 KB
μPD70F3781GF-GAT-AX	128-pin plastic LQFP (fine pitch) (14 × 20)	384 KB
μPD70F3782GF-GAT-AX	128-pin plastic LQFP (fine pitch) (14 × 20)	512 KB
μPD70F3783GF-GAT-AX	128-pin plastic LQFP (fine pitch) (14 × 20)	512 KB

- V850ES/JJ3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3784GJ-GAE-AX	144-pin plastic LQFP (fine pitch) (20 × 20)	512 KB
μPD70F3785GJ-GAE-AX	144-pin plastic LQFP (fine pitch) (20 × 20)	512 KB
μPD70F3786GJ-GAE-AX	144-pin plastic LQFP (fine pitch) (20 × 20)	512 KB

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

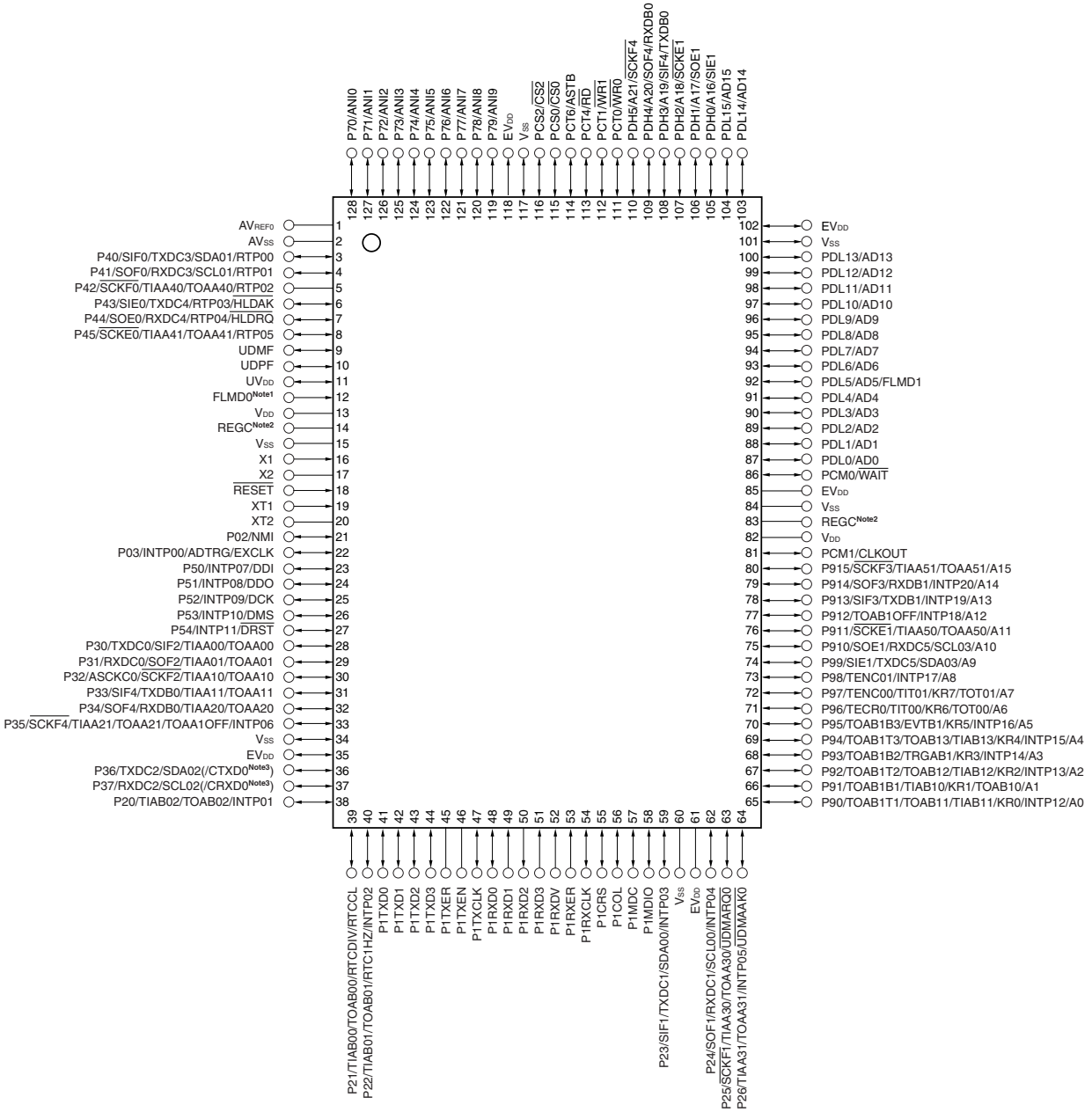
PIN CONFIGURATION

- V850ES/JH3-E

  128-pin plastic LQFP (fine pitch) (14 × 20)

  μPD70F3778GF-GAT-AX　　μPD70F3779GF-GAT-AX　　μPD70F3780GF-GAT-AX

  μPD70F3781GF-GAT-AX　　μPD70F3782GF-GAT-AX　　μPD70F3783GF-GAT-AX



Notes 1. Connect to VSS in normal mode.

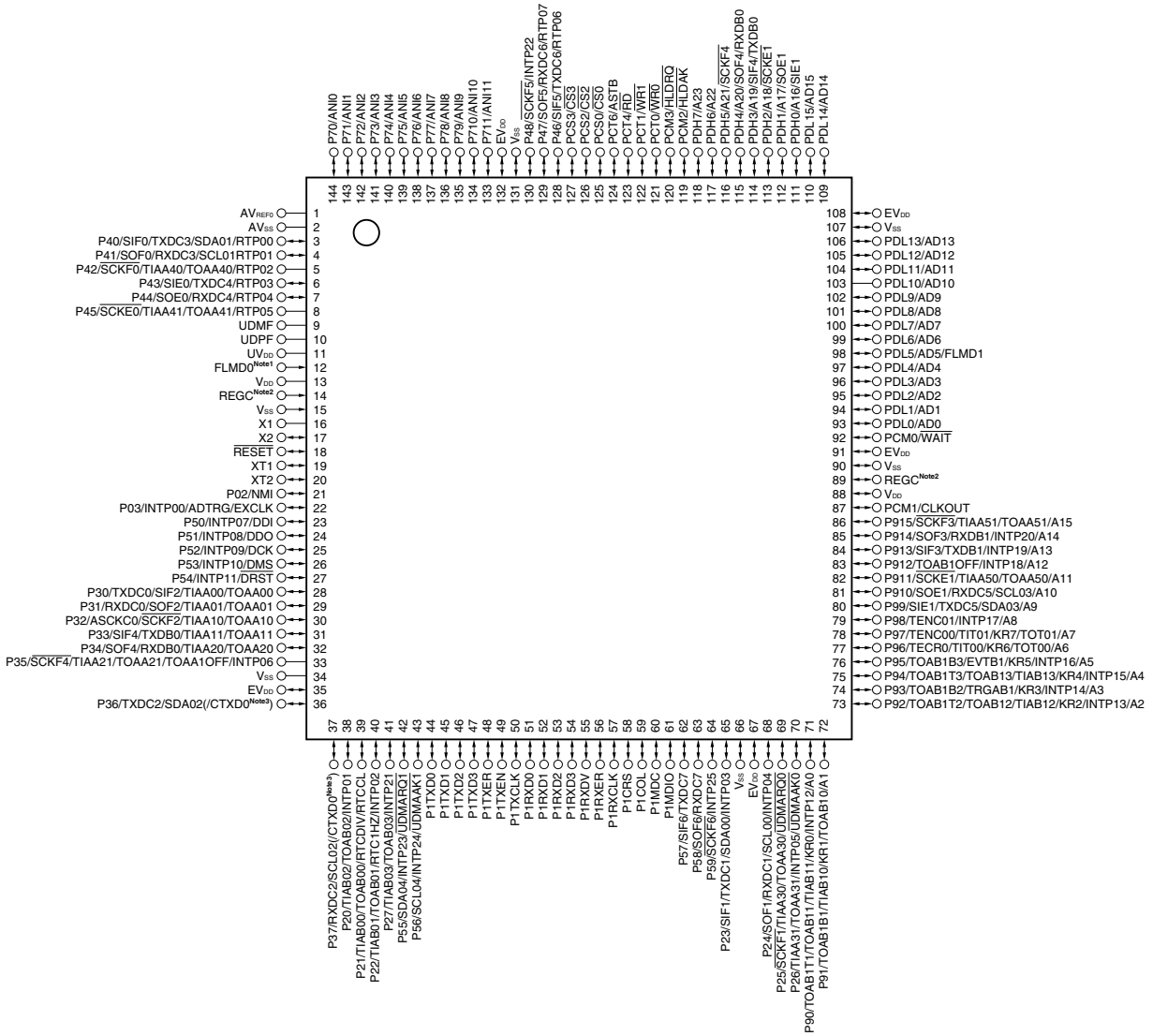
2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

3. μ PD70F3783 only.

- V850ES/JJ3-E

  144-pin plastic LQFP (fine pitch) (20 × 20)

  μPD70F3784GJ-GAE-AX μPD70F3785GJ-GAE-AX μPD70F3786GJ-GAE-AX



Notes 1. Connect to VSS in normal mode.

2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

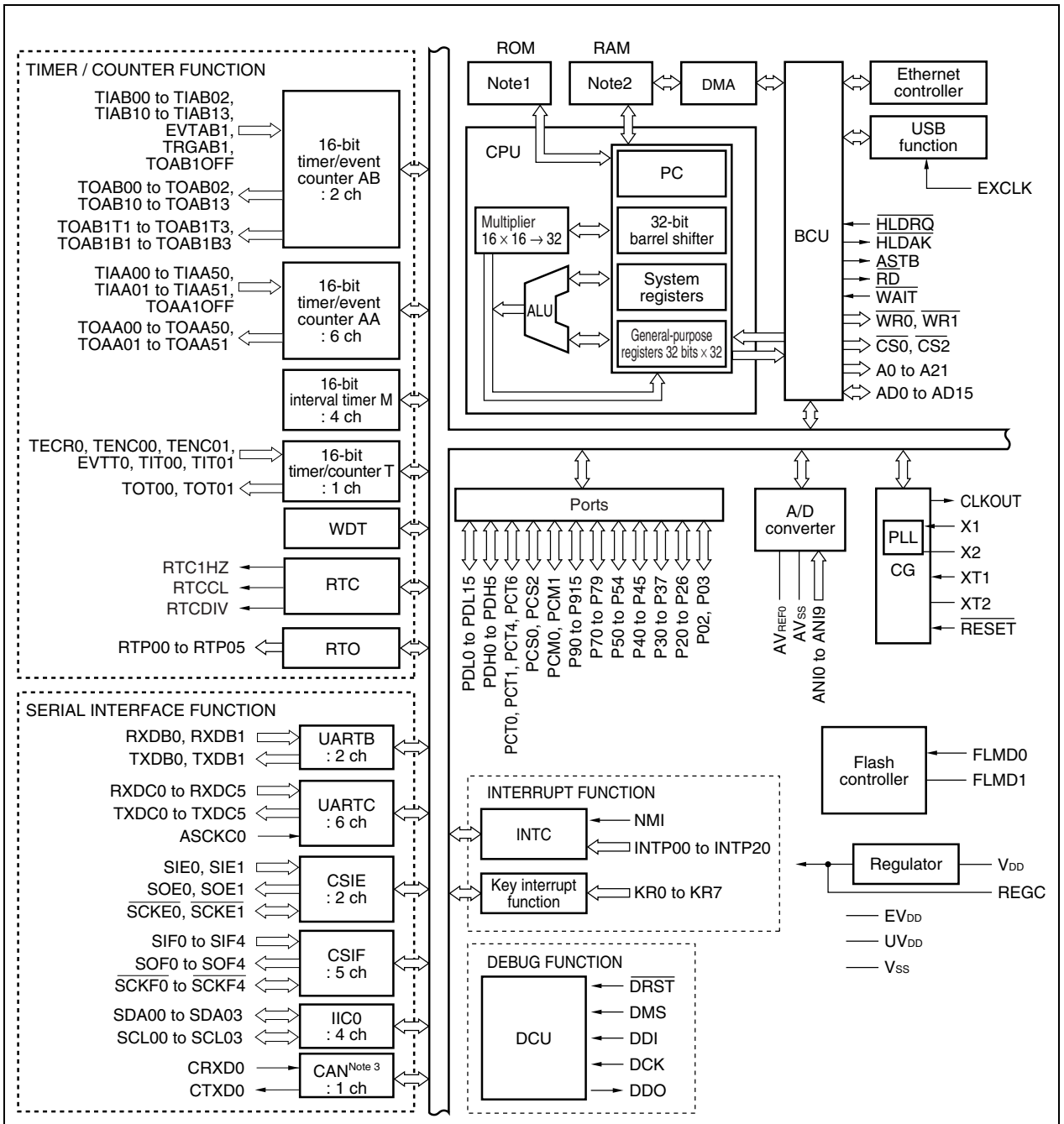
3. μ PD70F3786 only.

PIN IDENTIFICATION

A0 to A23:	Address Bus
AD0 to AD15:	Address/Data Bus
ADTRG:	A/D Trigger Input
ANI0 to ANI11:	Analog Input
ASCKC0:	Asynchronous Serial Clock
ASTB:	Address Strobe
AV_{REF0}:	Analog Reference Voltage
AV_{SS}:	Grand for Analog Pin
CLKOUT:	Clock Output
CRXD0:	CAN Receive Data
$\overline{CS0}$, $\overline{CS2}$, $\overline{CS3}$:	Chip Select
CTXD0:	CAN Transmit Data
DCK:	Debug Clock
DDI:	Debug Data Input
DDO:	Debug Data Output
$\overline{DMS}$:	Debug Mode Select
$\overline{DRST}$:	Debug Reset
EV_{DD}:	Power Supply for External Pin
EVTAB1:	Timer Event Count Input
FLMD0, FLMD1:	Flash Programming Mode
$\overline{HLDAK}$:	Hold Acknowledge
$\overline{HLDRQ}$:	Hold Request
INTP00 to INTP25:	External Interrupt Input
KR0 to KR7:	Key Return
NMI:	Non-maskable Interrupt Request
P02, P03:	Port0
P1COL, P1CRS, P1MDC, P1MDIO, P1RXCLK, P1RXD0 to P1RXD3, P1RXDV, P1RXER P1TXCLK, P1TXD0 to P1TXD3, P1TXEN, P1TXER:	Ethernet PHY Interface
P20 to P27:	Port2
P30 to P37:	Port3
P40 to P48:	Port4
P50 to P59:	Port5
P70 to P711:	Port7
P90 to P915:	Port9
PCM0 to PCM3:	Port CM
PCS0, PCS2, PCS3:	Port CS
PCT0, PCT1, PCT4, PCT6:	Port CT
PDH0 to PDH7:	Port DH
PDL0 to PDL15:	Port DL
$\overline{RD}$:	Read Strobe
REGC:	Regulator Control
$\overline{RESET}$:	Reset
RTC1HZ, RTCCL, RTCDIV:	Real-time Counter Clock Output
RTP00 to RTP07:	Real-time Output Port
RXDB0, RXDB1:	Receive Data
RXDC0 to RXDC7	
$\overline{SCKE0}$, $\overline{SCKE1}$:	Serial Clock
$\overline{SCKF0}$ to $\overline{SCKF6}$:	
SCL00 to SCL04:	Serial Clock
SDA00 to SDA04:	Serial Data
SIE0, SIE1	Serial Input
SIF0 to SIF6:	
SOE0, SOE1:	Serial Output
SOF0 to SOF6:	
TECR0:	Timer Encoder Clear Input
TENC00, TENC01:	Timer Encoder Input
TIAA00, TIAA01, TIAA10, TIAA11, TIAA20, TIAA21, TIAA30, TIAA31, TIAA40, TIAA41, TIAA50, TIAA51, TIAB00 to TIAB03, TIAB10 to TIAB13, TIT00, TIT01:	Timer Input
TOAA00, TOAA01, TOAA10, TOAA11, TOAA20, TOAA21, TOAA30, TOAA31, TOAA40, TOAA41, TOAA50, TOAA51, TOAB00 to TOAB03, TOAB10 to TOAB13, TOAB1B1 to TOAB1B3, TOAB1T1 to TOAB1T3,	Timer Output
TOT00, TOT01: TOAA1OFF, TOAB1OFF	Timer Output Off
TRGAB1:	Timer Trigger Input
TXDB0, TXDB1, TXDC0 to TXDC5:	Serial Output
EXCLK:	USB Clock
$\overline{UDMAAK0}$, $\overline{UDMAAK1}$:	DMA Acknowledge for External USB
$\overline{UDMARQ0}$, $\overline{UDMARQ1}$:	DMA Request for External USB
UDMF:	USB Data I/O (-) Function
UDPF:	USB Data I/O (+) Function
UV_{DD}:	Power Supply for External USB
V_{DD}:	Power Supply
V_{SS}:	Ground
$\overline{WAIT}$:	External Wait Input
$\overline{WR0}$:	Lower Byte Write Strobe
$\overline{WR1}$:	Upper Byte Write Strobe
X1, X2:	Crystal for Main Clock
XT1, XT2:	Crystal for Sub-clock

INTERNAL BLOCK DIAGRAM

- **V850ES/JH3-E**

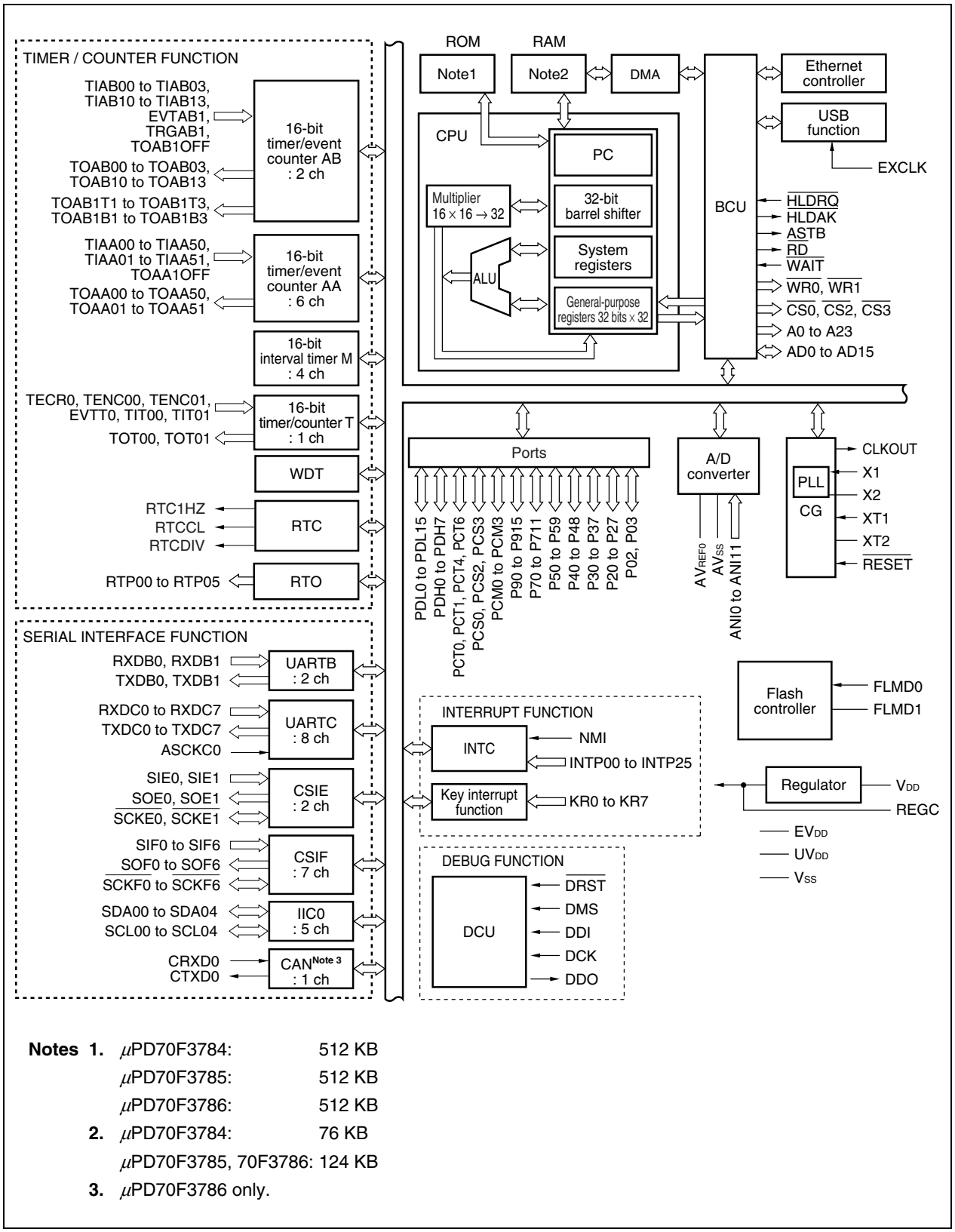


Notes 1. μPD70F3778: 256 KB
μPD70F3779, 70F3781: 384 KB
μPD70F3780, 70F3782, 70F3783: 512 KB

2. μPD70F3778, 70F3779, 70F3780: 76 KB
μPD70F3781, 70F3782, 70F3783: 124 KB

3. μPD70F3783 only.

- **V850ES/JJ3-E**



Notes 1. μPD70F3784: 512 KB
μPD70F3785: 512 KB
μPD70F3786: 512 KB

2. μPD70F3784: 76 KB
μPD70F3785, 70F3786: 124 KB

3. μPD70F3786 only.

CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
P02	I/O	Port 0 2-bit I/O port. Input/output can be specified in 1-bit units.	NMI	21	21
P03			INTP00/ADTRG/EXCLK	22	22
P20	I/O	Port 2 7-bit I/O port(V850ES/JH3-E) 8-bit I/O port(V850ES/JJ3-E) Input/output can be specified in 1-bit units.	TIAB02/TOAB02/INTP01	38	38
P21			TIAB00/TOAB00/RTGDIV/RTCCL	39	39
P22			TIAB01/TOAB01/RTC1HZ/INTP02	40	40
P23			SIF1/TXDC1/SDA00/INTP03	59	65
P24			SOF1/RXDC1/SDL00/INTP04	62	68
P25			$\overline{\text{SCKF1}}$/TIAA30/TOAA30/$\overline{\text{UDMARQ0}}$	63	69
P26			TIAA31/TOAA31/INTP05/$\overline{\text{UDMAAK0}}$	64	70
P27			TIAB03/TOAB03/INTP21	–	41
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TXDC0/SIF2/TIAA00/TOAA00	28	28
P31			RXDC0/SOF2/TIAA01/TOAA01	29	29
P32			ASCKC0/$\overline{\text{SCKF2}}$/TIAA10/TOAA10	30	30
P33			SIF4/TXDB0/TIAA11/TOAA11	31	31
P34			SOF4/RXDB0/TIAA20/TOAA20	32	32
P35			$\overline{\text{SCKF4}}$/TIAA21/TOAA21 /TOAA21OFF/INTP06	33	33
P36			TXDC2/SDA02/CTXD0[Note]	36	36
P37			RXDC2/SCL02/CRXD0[Note]	37	37
P40	I/O	Port 4 6-bit I/O port(V850ES/JH3-E) 9-bit I/O port(V850ES/JJ3-E) Input/output can be specified in 1-bit units.	SIF0/TXDC3/SDA01/RTP00	3	3
P41			SOF0/RXDC3/SCL01/RTP01	4	4
P42			$\overline{\text{SCKF0}}$/TIAA40/TOAA40/RTP02	5	5
P43			SIE0/TXDC4/RTP03	–	6
			SIE0/TXDC4/RTP03/$\overline{\text{HLDAK}}$	6	–
P44			SOE0/RXDC4/RTP04	–	7
			SOE0/RXDC4/RTP04/$\overline{\text{HLDRQ}}$	7	–
P45			$\overline{\text{SCKE0}}$/TIAA41/TOAA41/RTP05	8	8
P46			SIF5/TXDC6/RTP06	–	128
P47			SOF5/RXDC6/RTP07	–	129
P48			$\overline{\text{SCKF5}}$/INTP22	–	130

Note Available only in on-chip CAN controller products

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

(2/3)

Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
P50	I/O	Port 5 5-bit I/O port (V850ES/JH3-E) 10-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units.	INTP07/DDI	23	23
P51			INTP08/DDO	24	24
P52			INTP09/DCK	25	25
P53			INTP10/DMS	26	26
P54			INTP11/$\overline{\text{DRST}}$	27	27
P55			SDA04/INTP23/$\overline{\text{UDMARQ1}}$	–	42
P56			SCL04/INTP24/$\overline{\text{UDMAAK1}}$	–	43
P57			SIF6/TXDC7	–	62
P58			SOF6/RXDC7	–	63
P59			$\overline{\text{SCKF6}}$/INTP25	–	64
P70	I/O	Port 7 10-bit I/O port (V850ES/JH3-E) 12-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units.	ANI0	128	144
P71			ANI1	127	143
P72			ANI2	126	142
P73			ANI3	125	141
P74			ANI4	124	140
P75			ANI5	123	139
P76			ANI6	122	138
P77			ANI7	121	137
P78			ANI8	120	136
P79			ANI9	119	135
P710			ANI10	–	134
P711			ANI11	–	133
P90	I/O	Port 9 16-bit I/O port Input/output can be specified in 1-bit units.	TOAB1T1/TOAB11/TIAB11/KR0 /INTP12/A0	65	71
P91			TOAB1B1/TIAB10/KR1/TOAB10/A1	66	72
P92			TOAB1T2/TOAB12/TIAB12/KR2 /INTP13/A2	67	73
P93			TOAB1B2/TRGAB1/KR3/INTP14/A3	68	74
P94			TOAB1T3/TOAB13/TIAB13/KR4 /INTP15/A4	69	75
P95			TOAB1B3/EVTB1/KR5/INTP16/A5	70	76
P96			TECR0/TIT00/KR6/TOT00/A6	71	77
P97			TENC00/TIT01/KR7/TOT01/A7	72	78
P98			TENC01/INTP17/A8	73	79
P99			SIE1/TXDC5/SDA03/A9	74	80
P910			SOE1/RXDC5/SCL03/A10	75	81
P911			$\overline{\text{SCKE1}}$/TIAA50/TOAA50/A11	76	82
P912			TOAB1OFF/INTP18/A12	77	83
P913			SIF3/TXDB1/INTP19/A13	78	84
P914			SOF3/RXDB1/INTP20/A14	79	85
P915			$\overline{\text{SCKF3}}$/TIAA51/TOAA51/A15	80	86

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

(3/3)

Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
PCM0	I/O	Port CM 2-bit I/O port (V850ES/JH3-E) 4-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$	86	92
PCM1			CLKOUT	81	87
PCM2			$\overline{\text{HLDAK}}$	–	119
PCM3			$\overline{\text{HLDRQ}}$	–	120
PCS0	I/O	Port CS 2-bit I/O port (V850ES/JH3-E) 3-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$	115	125
PCS2			$\overline{\text{CS2}}$	116	126
PCS3			$\overline{\text{CS3}}$	–	127
PCT0	I/O	Port CT 4-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WR0}}$	111	121
PCT1			$\overline{\text{WR1}}$	112	122
PCT4			$\overline{\text{RD}}$	113	123
PCT6			ASTB	114	124
PDH0	I/O	Port DH 6-bit I/O port (V850ES/JH3-E) 8-bit I/O port (V850ES/JJ3-E) Input/output can be specified in 1-bit units.	A16/SIE1	105	111
PDH1			A17/SOE1	106	112
PDH2			A18/$\overline{\text{SCKE1}}$	107	113
PDH3			A19/SIF4/TXDB0	108	114
PDH4			A20/SOF4/RXDB0	109	115
PDH5			A21/$\overline{\text{SCKF4}}$	110	116
PDH6			A22	–	117
PDH7			A23	–	118
PDL0	I/O	Port DL 16-bit I/O port Input/output can be specified in 1-bit units.	AD0	87	93
PDL1			AD1	88	94
PDL2			AD2	89	95
PDL3			AD3	90	96
PDL4			AD4	91	97
PDL5			AD5/FLMD1	92	98
PDL6			AD6	93	99
PDL7			AD7	94	100
PDL8			AD8	95	101
PDL9			AD9	96	102
PDL10			AD10	97	103
PDL11			AD11	98	104
PDL12			AD12	99	105
PDL13			AD13	100	106
PDL14			AD14	103	109
PDL15			AD15	104	110

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

1.2 Non-Port Pins

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
A0	Output	Address bus for external memory (When using separate bus)	P90/TOAB1T1/TOAB11/TIAB11/KR0/INTP12	65	71
A1			P91/TOAB1B1/TIAB10/KR1/TOAB10	66	72
A2			P92/TOAB1T2/TOAB12/TIAB12/KR2/INTP13	67	73
A3			P93/TOAB1B2/TRGAB1/KR3/INTP14	68	74
A4			P94/TOAB1T3/TOAB13/TIAB13/KR4/INTP15	69	75
A5			P95/TOAB1B3/EVTAB1/KR5/INTP16	70	76
A6			P96/TECR0/TIT00/KR6/TOT00	71	77
A7			P97/TENC00/TIT01/KR7/TOT01	72	78
A8			P98/TENC01/INTP17	73	79
A9			P99/SIE1/TXDC5/SDA03	74	80
A10			P910/SOE1/RXDC5/SCL03	75	81
A11			P911/$\overline{\text{SCKE1}}$/TIAA50/TOAA50	76	82
A12			P912/TOAB1OFF/INTP18	77	83
A13			P913/SIF3/TXDB1/INTP19	78	84
A14			P914/SOF3/RXDB1/INTP20	79	85
A15			P915/$\overline{\text{SCKF3}}$/TIAA51/TOAA51	80	86
A16			PDH0/SIE1	105	111
A17			PDH1/SOE1	106	112
A18			PDH2/$\overline{\text{SCKE1}}$	107	113
A19			PDH3/SIF4/TXDB0	108	114
A20			PDH4/SOF4/RXDB0	109	115
A21			PDH5/$\overline{\text{SCKF4}}$	110	116
A22			PDH6	–	117
A23			PDH7	–	118

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
AD0	I/O	Address/data bus for external memory	PDL0	87	93
AD1			PDL1	88	94
AD2			PDL2	89	95
AD3			PDL3	90	96
AD4			PDL4	91	97
AD5			PDL5/FLMD1	92	98
AD6			PDL6	93	99
AD7			PDL7	94	100
AD8			PDL8	95	101
AD9			PDL9	96	102
AD10			PDL10	97	103
AD11			PDL11	98	104
AD12			PDL12	99	105
AD13			PDL13	100	106
AD14			PDL14	103	109
AD15			PDL15	104	110
ADTRG	Input	External trigger input for A/D converter	P03/INTP00/EXCLK	22	22
ANI0	Input	Analog voltage input for A/D converter	P70	128	144
ANI1			P71	127	143
ANI2			P72	126	142
ANI3			P73	125	141
ANI4			P74	124	140
ANI5			P75	123	139
ANI6			P76	122	138
ANI7			P77	121	137
ANI8			P78	120	136
ANI9			P79	119	135
ANI10			P710	–	134
ANI11			P711	–	133
ASCKC0	Input	UARTC0 baud rate clock input	P32/$\overline{\text{SCKF2}}$/TIAA10/TOAA10	30	30
ASTB	Output	Address strobe signal for external memory	PCT6	114	124
AV_{REF0}	–	Reference voltage input for A/D converter, and positive power supply for port 7	–	1	1
AV_{SS}	–	Ground voltage for A/D converter	–	2	2
CLKOUT	Output	Internal system clock output	PCM1	81	87
CRXD0[Note]	Input	CAN receive data input	P37/RXDC2/SCL02	37	37
$\overline{\text{CS0}}$	Output	Chip select output	PCS0	115	125
$\overline{\text{CS2}}$			PCS2	116	126
$\overline{\text{CS3}}$			PCS3	–	127
CTXD0[Note]	Output	CAN transmit data output	P36/TXDC2/SDA02	36	36

Note Available only in on-chip CAN controller products

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
DCK	Input	Clock input for on-chip debugging	P52/INTP09	25	25
DDI	Input	Data input for on-chip debugging	P50/INTP07	23	23
DDO	Output	Data output for on-chip debugging In the on-chip debug mode, high-level output is forcibly set.	P51/INTP08	24	24
DMS	Input	Mode select signal input for on-chip debugging	P53/INTP10	26	26
$\overline{\text{DRST}}$	Input	Reset signal input for on-chip debugging	P54/INTP11	27	27
EV_{DD}	–	Positive power supply for external (same potential as V_{DD})	–	35, 61, 85, 102, 118	35, 67, 91, 108, 132
EVTAB1	Input	External event count input of TAB1	TOAB1B3/KR5/INTP16/A5	70	76
EXCLK	Input	USB clock signal input	P03/INTP00/ADTRG	22	22
FLMD0	Input	Flash programming mode setting pins	–	12	12
FLMD1	Input		PDL5/AD5	92	98
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	PCM2	–	119
			P43/SIE0/TXDC4/RTP03	6	–
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	PCM3	–	120
			P44/SOE0/RXDC4/RTP04	7	–
INTP00	Input	External interrupt request input (maskable, analog noise elimination). Analog noise elimination or digital noise elimination selectable for INTP02 pin.	P03/ADTRG/EXCLK	22	22
INTP01			P20/TIAB02/TOAB02	38	38
INTP02			P22/TIAB01/TOAB01/RTC1HZ	40	40
INTP03			P23/SIF1/TXDC1/SDA00	59	65
INTP04			P24/SOF1/RXDC1/SDL00	62	68
INTP05			P26/TIAA31/TOAA31/$\overline{\text{UDMAAK0}}$	64	70
INTP06			P35/$\overline{\text{SCKF4}}$/TIAA21/TOAA21 /TOAA1OFF	33	33
INTP07			P50/DDI	23	23
INTP08			P51/DDO	24	24
INTP09			P52/DCK	25	25
INTP10			P53/DMS	26	26
INTP11			P54/$\overline{\text{DRST}}$	27	27
INTP12			P90/TOAB1T1/TOAB11/TIAB11 /KR0/A0	65	71
INTP13			P92/TOAB1T2/TOAB12/TIAB12 /KR2/A2	67	73
INTP14			P93/TOAB1B2/TRGAB1/KR3/A3	68	74
INTP15			P94/TOAB1T3/TOAB13/TIAB13 /KR4/A4	69	75
INTP16			P95/TOAB1B3/EVTAB1/KR5/A5	70	76
INTP17			P98/TENC01/A8	73	79
INTP18			P912/TOAB1OFF/A12	77	83
INTP19			P913/SIF3/TXDB1/A13	78	84

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
INTP20	Input	External interrupt request input (maskable, analog noise elimination).	P914/SOF3/RXDB1/A14	79	85
INTP21			P27/TIAB03/TOAB03	–	41
INTP22			P48/$\overline{\text{SCKF5}}$	–	130
INTP23			P55/SDA04/$\overline{\text{UDMARQ1}}$	–	42
INTP24			P56/SCL04/$\overline{\text{UDMAAK1}}$	–	43
INTP25			P59/$\overline{\text{SCKF6}}$	–	64
KR0	Input	Key interrupt input (analog noise elimination)	P90/TOAB1T1/TOAB11/TIAB11 /INTP12/A0	65	71
KR1			P91/TOAB1B1/TIAB10/TOAB10/A1	66	72
KR2			P92/TOAB1T2/TOAB12/TIAB12 /INTP13/A2	67	73
KR3			P93/TOAB1B2/TRGAB1/INTP14/A3	68	74
KR4			P94/TOAB1T3/TOAB13/TIAB13 /INTP15/A4	69	75
KR5			P95/TOAB1B3/EVTAB1/INTP16/A5	70	76
KR6			P96/TECR0/TIT00/TOT00/A6	71	77
KR7			P97/TENC00/TIT01/TOT01/A7	72	78
NMI	Input	External interrupt (non-maskable, ananlog noise elimination)	P02	21	21
P1COL	Input	Collision detection input for Ethernet	–	56	59
P1CRS	Input	Carrier detection input for Ethernet	–	55	58
P1MDC	Output	Seria transmit clock output	–	57	60
P1MDIO	I/O	Serial I/O	–	58	61
P1RXCLK	Input	Receive clock input for Ethernet	–	54	57
P1RXD0	Input	Receive data input for Ethernet	–	48	51
P1RXD1	Input	Receive data input for Ethernet	–	49	52
P1RXD2	Input	Receive data input for Ethernet	–	50	53
P1RXD3	Input	Receive data input for Ethernet	–	51	54
P1RXDV	Input	Receive data VALID input for Ethernet	–	52	55
P1RXER	Input	Receive data error input for Ethernet	–	53	56
P1TXCLK	Output	Transmit clock output for Ethernet	–	47	50
P1TXD0	Output	Transmit data output for Ethernet	–	41	44
P1TXD1	Output	Transmit data output for Ethernet	–	42	45
P1TXD2	Output	Transmit data output for Ethernet	–	43	46
P1TXD3	Output	Transmit data output for Ethernet	–	44	47
P1TXEN	Output	Transmit data enable output for Ethernet	–	46	49
P1TXER	Output	Transmit error output for Ethernet	–	45	48

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
$\overline{RD}$	Output	Read strobe signal output for external memory	PCT4	113	123
REGC	–	Connecting capacitor for regulator output stabilization (4.7 μF (preliminary value))	–	14, 83	14, 89
$\overline{RESET}$	Input	System reset input	–	18	18
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	P22/TIAB01/TOAB01/INTP02	40	40
RTCCL	Output	Real-time counter clock (original 32 kHz clock) output	P21/TIAB00/TOAB00/RTCDIV	39	39
RTCDIV	Output	Real-time counter clock (divided 32 kHz clock) output	P21/TIAB00/TOAB00/RTCCL	39	39
RTP00	Output	Real-time output port RTP00, RTP01, RTP06 and RTP07 are N-ch open-drain output selectable.	P40/SIF0/TXDC3/SDA01	3	3
RTP01			P41/SOF0/RXDC3/SCL01	4	4
RTP02			P42/$\overline{SCKF0}$/TIAA40/TOAA40	5	5
RTP03			P43/SIE0/TXDC4	–	6
			P43/SIE0/TXDC4/$\overline{HLDAK}$	6	–
RTP04			P44/SOE0/RXDC4	–	7
			P44/SOE0/RXDC4/$\overline{HLDRQ}$	7	–
RTP05			P45/$\overline{SCKE0}$/TIAA41/TOAA41	8	8
RTP06			P46/SIF5/TXDC6	–	128
RTP07			P47/SOF5/RXDC6	–	129
RXDB0	Input	Serial receive data input (UARTB0, UARTB1)	P34/SOF4/TIAA20/TOAA20	32	32
			PDH4/A20/SOF4	109	115
RXDB1			P914/SOF3/INTP20/A14	79	85
RXDC0	Input	Serial receive data input (UARTC0 to UARTC7)	P31/SOF2/TIAA01/TOAA01	29	29
RXDC1			P24/SOF1/RXDC1/SDL00/INTP04	62	68
RXDC2			P37/SCL02/CRXD0[Note]	37	37
RXDC3			P41/SOF0/SCL01/RTP01	4	4
RXDC4			P44/SOE0/RTP04	–	7
			P44/SOE0/RTP04/$\overline{HLDRQ}$	7	–
RXDC5			P910/SOE1/SCL03/A10	75	81
RXDC6			P47/SOF5/RTP07	–	129
RXDC7			P58/SOF6	–	63
$\overline{SCKE0}$	I/O	Serial clock I/O (CSIE0, CSIE1)	P45/TIAA41/TOAA41/RTP05	8	8
$\overline{SCKE1}$			P911/TIAA50/TOAA50/A11	76	82
			PDH2/A18	107	113
$\overline{SCKF0}$	I/O	Serial clock I/O (CSIF0 to CSIF6)	P42/TIAA40/TOAA40/RTP02	5	5
$\overline{SCKF1}$			P25/TIAA30/TOAA30/$\overline{UMDARQ0}$	63	69
$\overline{SCKF2}$			P32/ASCKC0/TIAA10/TOAA10	30	30
$\overline{SCKF3}$			P915/TIAA51/TOAA51/A15	80	86
$\overline{SCKF4}$			P35/TIAA21/TOAA21/TOAA1OFF /INTP06	33	33
			PDH5/A21	110	116
$\overline{SCKF5}$			P48/INTP22	–	130
$\overline{SCKF6}$			P59/INTP25	–	64

Note Available only in on-chip CAN controller products

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
SCL00	I/O	Serial clock I/O (I^2C00 to I^2C04)	P24/SOF1/RXDC1/INTP04	62	68
SCL01		N-ch open-drain output selectable.	P41/SOF0/RXDC3/RTP01	4	4
SCL02			P37/RXDC2/CRXD0[Note]	37	37
SCL03			P910/SOE1/RXDC5/A10	75	81
SCL04			P56/INTP24/$\overline{\text{UDMAAK1}}$	–	43
SDA00	I/O	Serial transmit/receive data I/O (I^2C00 to I^2C04)	P23/SIF1/TXDC1/INTP03	59	65
SDA01		N-ch open-drain output selectable.	P40/SIF0/TXDC3/RTP00	3	3
SDA02			P36/TXDC2/CTXD0[Note]	36	36
SDA03			P99/SIE1/TXDC5/A9	74	80
SDA04			P55/INTP23/$\overline{\text{UDMARQ1}}$	–	42
SIE0	Input	Serial receive data input (CSIE0, CSIE1)	P43/TXDC4/RTP03	–	6
			P43/TXDC4/RTP03/$\overline{\text{HLDAK}}$	6	–
SIE1			P99/TXDC5/SDA03/A9	74	80
			PDH0/A16	105	111
SIF0	Input	Serial receive data input (CSIF0 to CSIF6)	P40/TXDC3/SDA01/RTP00	3	3
SIF1			P23/TXDC1/SDA00/INTP03	59	65
SIF2			P30/TXDC0/TIAA00/TOAA00	28	28
SIF3			P913/TXDB1/INTP19/A13	78	84
SIF4			P33/TXDB0/TIAA11/TOAA11	31	31
			PDH3/TXDB0	108	114
SIF5			P46/TXDC6/RTP06	–	128
SIF6			P57/TXDC7	–	62
SOE0	Output	Serial transmit data output (CSIE0, CSIE1)	P44/RXDC4/RTP04	–	7
			P44/RXDC4/RTP04/$\overline{\text{HLDRQ}}$	7	–
SOE1			P910/RXDC5/SCL03/A10	75	81
			PDH1/A17	106	112
SOF0	Output	Serial transmit data output (CSIF0 to CSIF6)	P41/RXDC3/SCL01/RTP01	4	4
SOF1		N-ch open-drain output selectable.	P24/RXDC1/SDL00/INTP04	62	68
SOF2			P31/RXDC0/TIAA01/TOAA01	29	29
SOF3			P914/RXDB1/INTP20/A14	79	85
SOF4			P34/RXDB0/TIAA20/TOAA20	32	32
			PDH4/A20/RXDB0	109	115
SOF5			P47/RXDC6/RTP07	–	129
SOF6			P58/RXDC7	–	63
TECR0	Input	Encoder clear input of TMT0	P96/TIT00/KR6/TOT00/A6	71	77
TENC00		Encoder input/external event input/external trigger input of TMT0	P97/TIT01/KR7/TOT01/A7	72	78
TENC01		Encoder input of TMT0	P98/INTP17/A8	73	79

Note Available only in on-chip CAN controller products

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
TIAA00	Input	Capture trigger input/external event input/external trigger input (TAA0)	P30/TXDC0/SIF2/TOAA00	28	28
TIAA01	Input	Capture trigger input (TAA0)	P31/RXDC0/SOF2/TOAA01	29	29
TIAA10		Capture trigger input/external event input/external trigger input (TAA1)	P32/ASCKC0/$\overline{\text{SCKF2}}$/TOAA10	30	30
TIAA11		Capture trigger input (TAA1)	P33/SIF4/TXDB0/TOAA11	31	31
TIAA20		Capture trigger input/external event input/external trigger input (TAA2)	P34/SOF4/RXDB0/TOAA20	32	32
TIAA21		Capture trigger input (TAA2)	P35/$\overline{\text{SCKF4}}$/TOAA21/TOAA1OFF /INTP06	33	33
TIAA30		Capture trigger input/external event input/external trigger input (TAA3)	P25/$\overline{\text{SCKF1}}$/TOAA30/$\overline{\text{UDMARQ0}}$	63	69
TIAA31		Capture trigger input (TAA3)	P26/TOAA31/INTP05/$\overline{\text{UDMAAK0}}$	64	70
TIAA40		Capture trigger input/external event input/external trigger input (TAA4)	P42/$\overline{\text{SCKF0}}$/TOAA40/RTP02	5	5
TIAA41		Capture trigger input (TAA4)	P45/$\overline{\text{SCKE0}}$/TOAA41/RTP05	8	8
TIAA50		Capture trigger input/external event input/external trigger input (TAA5)	P911/$\overline{\text{SCKE1}}$/TOAA50/A11	76	82
TIAA51		Capture trigger input (TAA5)	P915/$\overline{\text{SCKF3}}$/TOAA51/A15	80	86
TIAB00	Input	Capture trigger input/external event input/external trigger input (TAB0)	P21/TOAB00/RTCDIV/RTCCL	39	39
TIAB01		Capture trigger input (TAB0)	P22/TOAB01/RTC1HZ/INTP02	40	40
TIAB02			P20/TOAB02/INTP01	38	38
TIAB03			P27/TOAB03/INTP21	–	41
TIAB10		Capture trigger input/external event input/external trigger input (TAB1) N-ch open-drain output selectable.	P91/TOAB1B1/KR1/TOAB10/A1	66	72
TIAB11		Capture trigger input (TAB1) N-ch open-drain output selectable.	P90/TOAB1T1/TOAB11/KR0 /INTP12/A0	65	71
TIAB12			P92/TOAB1T2/TOAB12/KR2 /INTP13/A2	67	73
TIAB13			P94/TOAB1T3/TOAB13/KR4 /INTP15/A4	69	75
TIT00	Input	Capture trigger input of TMT0 N-ch open-drain output selectable.	P96/TECR0/KR6/TOT00/A6	71	77
TIT01	Input		P97/TENC00/KR7/TOT01/A7	72	78
TOAA00	Output	Timer output (TAA0) N-ch open-drain output selectable.	P30/TXDC0/SIF2/TIAA00	28	28
TOAA01			P31/RXDC0/SOF2/TIAA01	29	29
TOAA10		Timer output (TAA1) N-ch open-drain output selectable.	P32/ASCKC0/$\overline{\text{SCKF2}}$/TIAA10	30	30
TOAA11			P33/SIF4/TXDB0/TIAA11	31	31
TOAA1OFF	Input	TAA1 High-impedance output control signal input	P35/SCKF4/TIAA21/TOAA21 /INTP06	33	33

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
TOAA20	Output	Timer output (TAA2)	P34/SOF4/RXDB0/TIAA20	32	32
TOAA21		N-ch open-drain output selectable.	P35/$\overline{\text{SCKF4}}$/TIAA21/TOAA1OFF /INTP06	33	33
TOAA30	Output	Timer output (TAA3)	P25/$\overline{\text{SCKF1}}$/TIAA30/$\overline{\text{UDMARQ0}}$	63	69
TOAA31		N-ch open-drain output selectable.	P26/TIAA31/INTP05/$\overline{\text{UDMAAK0}}$	64	70
TOAA40		Timer output (TAA4)	P42/$\overline{\text{SCKF0}}$/TIAA40/RTP02	5	5
TOAA41		N-ch open-drain output selectable.	P45/$\overline{\text{SCKE0}}$/TIAA41/RTP05	8	8
TOAA50		Timer output (TAA5)	P911/$\overline{\text{SCKE1}}$/TIAA50/A11	76	82
TOAA51		N-ch open-drain output selectable.	P915/$\overline{\text{SCKF3}}$/TIAA51/A15	80	86
TOAB00	Output	Timer output (TAB0)	P21/TIAB00/RTCDIV/RTCCL	39	39
TOAB01		N-ch open-drain output selectable.	P22/TIAB01/RTC1HZ/INTP02	40	40
TOAB02			P20/TIAB02/INTP01	38	38
TOAB03			P27/TIAB03/INTP21	–	41
TOAB10	Output	Timer output (TAB1)	P91/TOAB1B1/TIAB10/KR1/A1	66	72
TOAB11		N-ch open-drain output selectable.	P90/TOAB1T1/TIAB11/KR0 /INTP12/A0	65	71
TOAB12			P92/TOAB1T2/TIAB12/KR2 /INTP13/A2	67	73
TOAB13			P94/TOAB1T3/TIAB13/KR4 /INTP15/A4	69	75
TOAB1B1	Output	Pulse signal output for 6-phase PWM low arm of TAB1	P91/TIAB10/KR1/TOAB10/A1	66	72
TOAB1B2			P93/TRGAB1/KR3/INTP14/A3	68	74
TOAB1B3			P95/EVTAB1/KR5/INTP16/A5	70	76
TOAB1OFF	Input	TAB1 High-impedance output control signal input	P912/INTP18/A12	77	83
TOAB1T1	Output	Pulse signal output for 6-phase PWM high arm of TAB1.	P90/TOAB11/TIAB11/KR0 /INTP12/A0	65	71
TOAB1T2		N-ch open-drain output selectable.	P92/TOAB12/TIAB12/KR2 /INTP13/A2	67	73
TOAB1T3			P94/TOAB13/TIAB13/KR4 /INTP15/A4	69	75
TOT00	Output	Timer output of TMT0	P96/TECR0/TIT00/KR6/A6	71	77
TOT01		N-ch open-drain output selectable	P97/TENC00/TIT01/KR7/A7	72	78
TRGAB1	Input	External trigger input of TAB1 N-ch open-drain output selectable	P93/TOAB1B2/KR3/INTP14/A3	68	74
TXDB0	Output	Serial transmit data output (UARTB0, UARTB1)	P33/SIF4/TIAA11/TOAA11	31	31
			PDH3/A19/SIF4	108	114
TXDB1			P913/SIF3/INTP19/A13	78	84

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

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Pin Name	I/O	Function	Alternate Function	Pin number	
				JH3-E	JJ3-E
TXDC0	Output	Serial transmit data output (UARTC0 to UARTC7)	P30/SIF2/TIAA00/TOAA00	28	28
TXDC1		N-ch open-drain output selectable.	P23/SIF1/SDA00/INTP03	59	65
TXDC2			P36/SDA02/CTXD0[Note]	36	36
TXDC3			P40/SIF0/SDA01/RTP00	3	3
TXDC4			P43/SIE0/RTP03	–	6
			P43/SIE0/RTP03/$\overline{\text{HLDAK}}$	6	–
TXDC5			P99/SIE1/SDA03/A9	74	80
TXDC6			P46/SIF5/RTP06	–	128
TXDC7			P57/SIF6	–	62
EXCLK	Input	USB clock signal input	P03/INTP00/ADTRG	22	22
$\overline{\text{UDMAAK0}}$	Output	DMA acknowledge for USB	P26/TIAA31/TOAA31/INTP05	64	70
$\overline{\text{UDMAAK1}}$			P56/SCL04/INTP24	–	43
$\overline{\text{UDMARQ0}}$	Input	DMA request for USB	P25/$\overline{\text{SCKF1}}$/TIAA30/TOAA30	63	69
$\overline{\text{UDMARQ1}}$			P55/SDL04/INTP23	–	42
UDMF	I/O	USB data I/O (–) function	–	9	9
UDPF		USB data I/O (+) function	–	10	10
UV_{DD}	–	3.3 V positive power supply for USB	–	11	11
V_{DD}	–	Positive power supply for internal circuit	–	13, 82	13, 88
V_{SS}	–	Ground potential for internal circuit	–	15, 34, 60, 84, 101, 117	15, 34, 66, 90, 107, 131
$\overline{\text{WAIT}}$	Input	External wait input	PCM0	86	92
$\overline{\text{WR0}}$	Output	Write strobe for external memory (lower 8 bits)	PCT0	111	121
$\overline{\text{WR1}}$		Write strobe for external memory (higher 8 bits)	PCT1	112	122
X1	Input	Connecting resonator for main clock	–	16	16
X2	–		–	17	17
XT1	Input	Connecting resonator for subclock	–	19	19
XT2	–		–	20	20

Note Available only in on-chip CAN controller products.

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the schematic circuit diagram of each type, refer to **Figure 1-1**.

Table 1-1. Types of Pin I/O Circuits (1/4)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JH3-E	JJ3-E
P02	NMI	10-D	nput: Independently connect to EV_{DD} or V_{SS} via a resistor.	√	√
P03	INTP00/ADTRG/EXCLK		Output: Leave open.	√	√
P20	TIAB02/TOAB02/INTP01	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor.	√	√
P21	TIAB00/TOAB00/RTCDIV/RTCCL		Output: Leave open.	√	√
P22	TIAB01/TOAB01/RTC1HZ/INTP02			√	√
P23	SIF1/TXDC1/SDA00/INTP03			√	√
P24	SOF1/RXDC1/SDL00/INTP04			√	√
P25	$\overline{\text{SCKF1}}$/TIAA30/TOAA30/$\overline{\text{UDMARQ0}}$			√	√
P26	TIAA31/TOAA31/INTP05/$\overline{\text{UDMAAK0}}$			√	√
P27	TIAB03/TOAB03/INTP21			–	√
P30	TXDC0/SIF2/TIAA00/TOAA00	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor.	√	√
P31	RXDC0/SOF2/TIAA01/TOAA01		Output: Leave open.	√	√
P32	ASCKC0/$\overline{\text{SCKF2}}$/TIAA10/TOAA10			√	√
P33	SIF4/TXDB0/TIAA11/TOAA11			√	√
P34	SOF4/RXDB0/TIAA20/TOAA20			√	√
P35	$\overline{\text{SCKF4}}$/TIAA21/TOAA21 /TOAA1OFF/INTP06			√	√
P36	TXDC2/SDA02/CTXD0[Note]			√	√
P37	RXDC2/SCL02/CRXD0[Note]			√	√
P40	SIF0/TXDC3/SDA01/RTP00	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor.	√	√
P41	SOF0/RXDC3/SCL01/RTP01		Output: Leave open.	√	√
P42	$\overline{\text{SCKF0}}$/TIAA40/TOAA40/RTP02			√	√
P43	SIE0/TXDC4/RTP03			–	√
	SIE0/TXDC4/RTP03/HLDAK			√	–
P44	SOE0/RXDC4/RTP04			–	√
	SOE0/RXDC4/RTP04/HLDRQ			√	–
P45	$\overline{\text{SCKE0}}$/TIAA41/TOAA41/RTP05			√	√
P46	SIF5/TXDC6/RTP06			–	√
P47	SOF5/RXDC6/RTP07			–	√
P48	$\overline{\text{SCKF5}}$/INTP22			–	√

Note Available only in on-chip CAN controller products.

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JJ3-E

Table 1-1. Types of Pin I/O Circuits (2/4)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JH3-E	JJ3-E
P50	INTP07/DDI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
P51	INTP08/DDO			√	√
P52	INTP09/DCK			√	√
P53	INTP10/DMS			√	√
P54	INTP11/$\overline{\text{DRST}}$	10-N	Input: Independently connect to V_{SS} via a resistor. Fixing to V_{DD} level is prohibited. Output: Leave open. Internally pull-down after reset by $\overline{\text{RESET}}$ pin.	√	√
P55	SDA04/INTP23/$\overline{\text{UDMARQ1}}$	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	√
P56	SCL04/INTP24/$\overline{\text{UDMAAK1}}$			–	√
P57	SIF6/TXDC7			–	√
P58	SOF6/RXDC7			–	√
P59	$\overline{\text{SCKF6}}$/INTP25			–	√
P70 to P79	ANI0 to ANI9	11-G	Input: Independently connect to AV_{REF0} or AV_{SS} via a resistor. Output: Leave open.	√	√
P710, P711	ANI10, ANI11			–	√
P90	TOAB1T1/TOAB11/TIAB11/KR0/INTP12/A0	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
P91	TOAB1B1/TIAB10/KR1/TOAB10/A1			√	√
P92	TOAB1T2/TOAB12/TIAB12/KR2/INTP13/A2			√	√
P93	TOAB1B2/TRGAB1/KR3/INTP14/A3			√	√
P94	TOAB1T3/TOAB13/TIAB13/KR4/INTP15/A4			√	√
P95	TOAB1B3/EVTB1/KR5/INTP16/A5			√	√
P96	TECR0/TIT00/KR6/TOT00/A6			√	√
P97	TENC00/TIT01/KR7/TOT01/A7			√	√
P98	TENC01/INTP17/A8			√	√
P99	SIE1/TXDC5/SDA03/A9			√	√
P910	SOE1/RXDC5/SCL03/A10			√	√
P911	$\overline{\text{SCKE1}}$/TIAA50/TOAA50/A11			√	√
P912	TOAB1OFF/INTP18/A12			√	√
P913	SIF3/TXDB1/INTP19/A13			√	√
P914	SOF3/RXDB1/INTP20/A14			√	√
P915	$\overline{\text{SCKF3}}$/TIAA51/TOAA51/A15			√	√
PCM0	$\overline{\text{WAIT}}$	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
PCM1	CLKOUT			√	√
PCM2	$\overline{\text{HLDAK}}$			–	√
PCM3	$\overline{\text{HLDRQ}}$			–	√

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JE3-E

Table 1-1. Types of Pin I/O Circuits (3/4)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JH3-E	JJ3-E
PCS0	$\overline{CS0}$	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
PCS2	$\overline{CS2}$			√	√
PCS3	$\overline{CS3}$			–	√
PCT0	$\overline{WR0}$	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
PCT1	$\overline{WR1}$			√	√
PCT4	$\overline{RD}$			√	√
PCT6	ASTB			√	√
PDH0	A16/SIE1	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
PDH1	A17/SOE1	5		√	√
PDH2	A18/$\overline{SCKE1}$	10-D		√	√
PDH3	A19/SIF4/TXDB0			√	√
PDH4	A20/SOF4/RXDB0			√	√
PDH5	A21/$\overline{SCKF4}$			√	√
PDH6, PDH7	A22, A23	5		–	√
PDL0 to PDL4	AD0 to AD4	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	√	√
PDL5	AD5/FLMD1			√	√
PDL6 to PDL15	AD6 to AD15			√	√
AV_{REF0}	–	–	Directly connect to V_{DD} and always supply power.	√	√
AV_{SS}	–	–	Directly connect to V_{SS}.	√	√
EV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	√	√
FLMD0	–	–	Connect to V_{SS} in other than flash mode.	√	√
P1COL	–	5	Independently connect to EV_{DD} or V_{SS} via a resistor.	√	√
P1CRS	–	5		√	√
P1MDIO	–	5		√	√
P1RXCLK	–	5		√	√
P1RXD0	–	5		√	√
P1RXD1	–	5		√	√
P1RXD2	–	5		√	√
P1RXD3	–	5		√	√
P1RXDV	–	5		√	√
P1RXER	–	5		√	√
P1TXCLK	–	5		√	√
P1MDC	–	5	Leave open.	√	√
P1TXD0	–	5		√	√
P1TXD1	–	5		√	√
P1TXD2	–	5		√	√
P1TXD3	–	5		√	√
P1TXEN	–	5		√	√
P1TXER	–	5		√	√

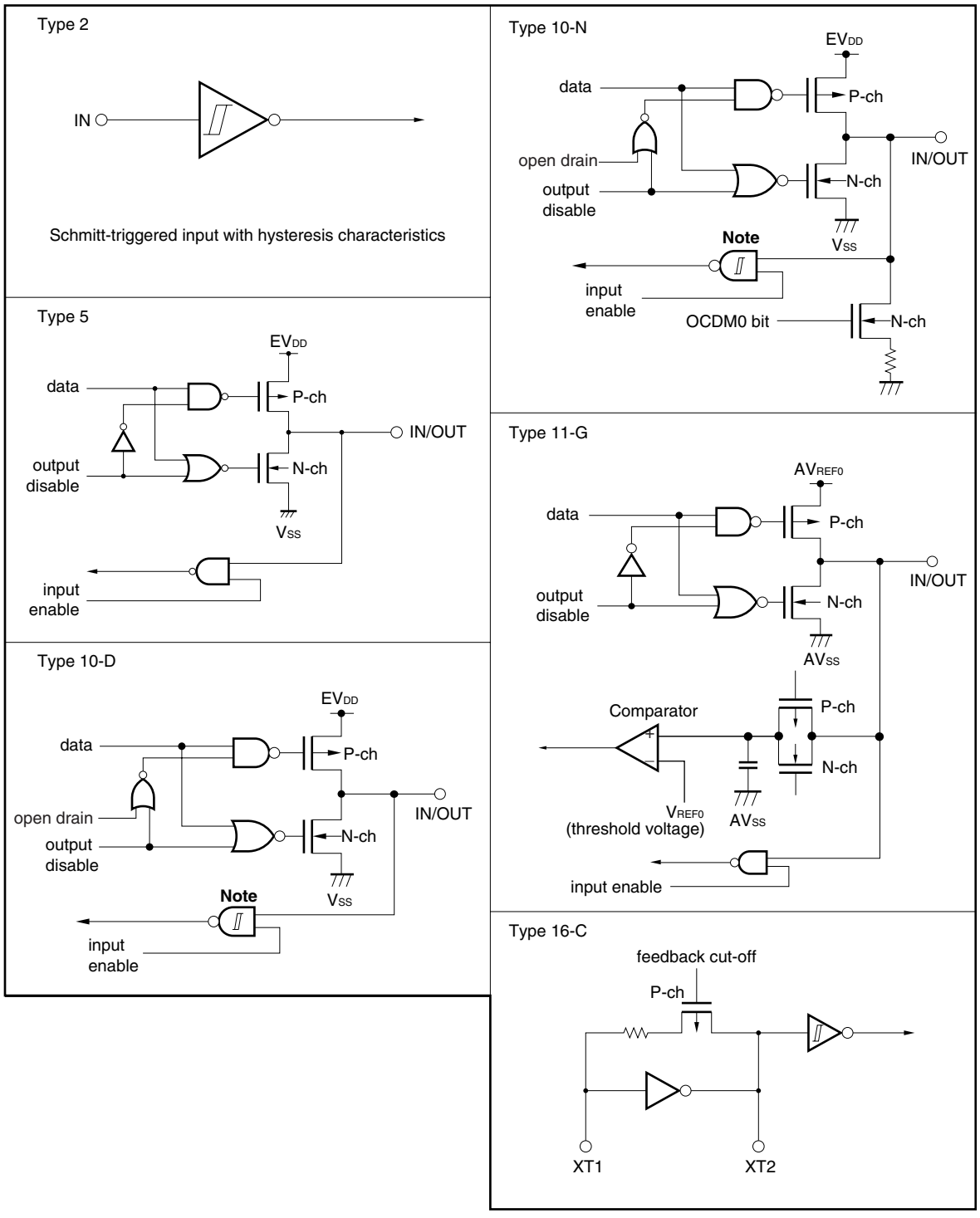
Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JE3-E

Table 1-1. Types of Pin I/O Circuits (4/4)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JH3-E	JJ3-E
REGC	–	–	Connect to regulator output stabilization (4.7 μF (preliminary value)) capacitor.	√	√
$\overline{\text{RESET}}$	–	2	–	√	√
UDMF	–	–	Leave open.	√	√
UDPF	–	–	Leave open.	√	√
UV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	√	√
V_{DD}	–	–	–	√	√
V_{SS}	–	–	–	√	√
X1	–	–	–	√	√
X2	–	–	–	√	√
XT1	–	16-C	Connect to V_{SS} via a resistor.	√	√
XT2	–	16-C	Leave open.	√	√

Remark JH3-E: V850ES/JH3-E, JJ3-E: V850ES/JE3-E

Figure 1-1. Pin I/O Circuits



Note Hysteresis characteristics are not available in port mode.

2. CPU FUNCTIONS

The CPU of the V850ES/JH3-E, V850ES/JJ3-E is based on RISC architecture and executes most instructions in a 1-clock cycle by using a 5-stage pipeline.

The features of the CPU are as follows.

- Minimum instruction execution time: 20 ns (@ 50 MHz operation with main clock (f_{XX}))
  30.5 μs (@ 32.768 kHz operation with sub-clock (f_{XT}))
- Memory space Program space: 64 MB linear
  Data space: 4 GB linear
- General-purpose registers: 32 bits × 32 registers
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiplication/division instructions
- Saturation operation instructions
- 1-clock 32-bit shift instruction
- Load/store instructions with long/short format
- Internal memory

Table 2-1. ROM/RAM

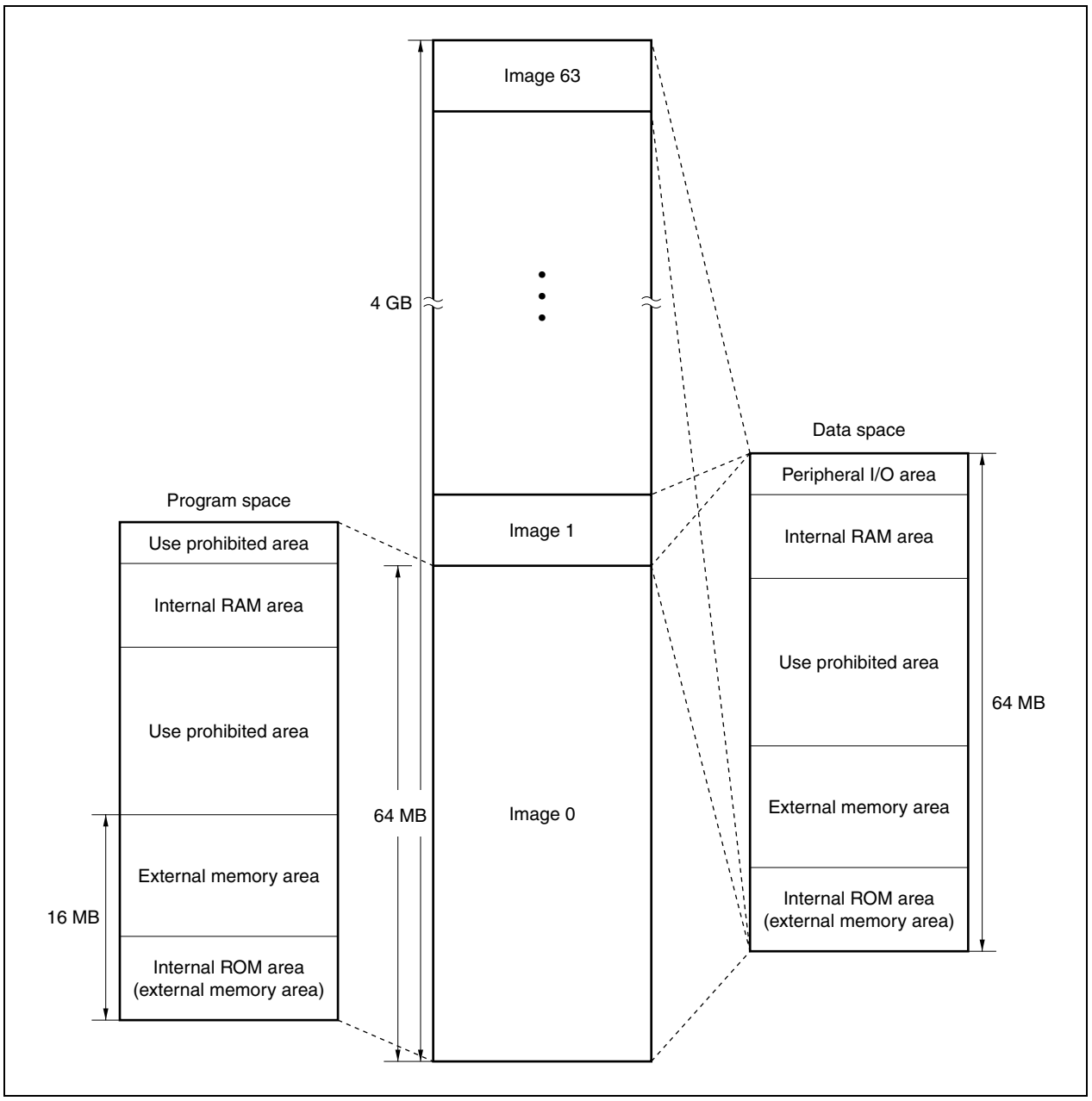
Generic Name	Products	Flash Memory Size	RAM Size	
			Internal RAM	Data RAM
V850ES/JH3-E	μPD70F3778	256 KB	60 KB	16 KB
	μPD70F3779	384 KB	60 KB	16 KB
	μPD70F3780	512 KB	60 KB	16 KB
	μPD70F3781	384 KB	60 KB	64 KB
	μPD70F3782	512 KB	60 KB	64 KB
	μPD70F3783	512 KB	60 KB	64 KB
V850ES/JJ3-E	μPD70F3784	512 KB	60 KB	16 KB
	μPD70F3785	512 KB	60 KB	64 KB
	μPD70F3786	512 KB	60 KB	64 KB

- Four types of bit manipulation instructions
  - SET1
  - CLR1
  - NOT1
  - TST1

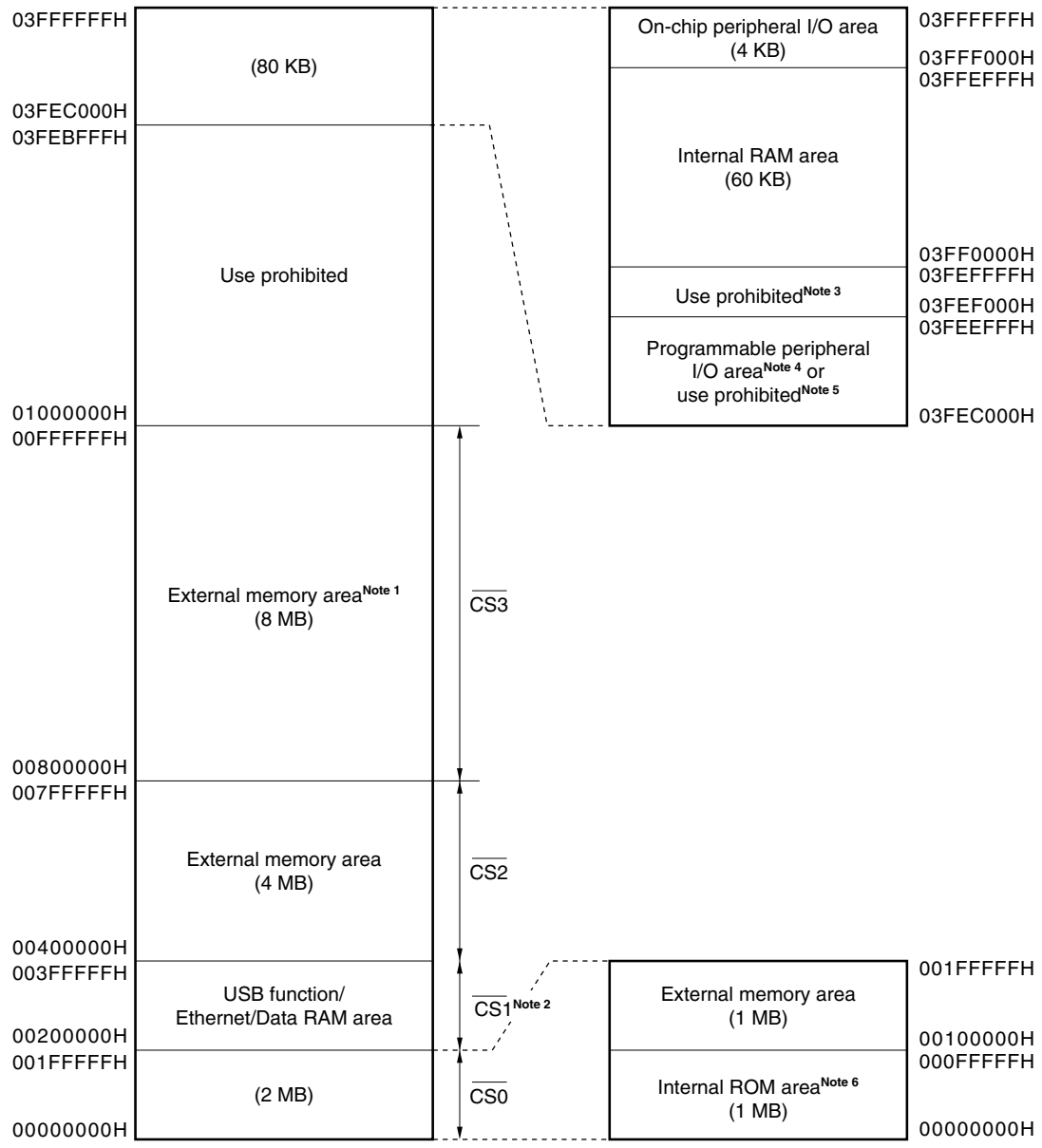
3. MEMORY MAP

The memory maps of the V850ES/JH3-E, V850ES/JJ3-E are shown below.

○ Address Space



○ **Data Memory Map**



Notes 1. In the V850ES/JJ3-E, this can be used as the external memory area.In the V850ES/JH3-E, use of this area is prohibited.

2. $\overline{CS1}$ is not provided as an external signal of the V850ES/Jx3-E. It is used as a chip select signal for the USB, Ethernet in the V850ES/Jx3-E.

3. Use of addresses 03FEF000H to 03FEFFFFH is prohibited because they overlap an on-chip peripheral I/O area.

4. The programmable peripheral I/O area is seen as 256 MB areas in the 4 GB address space.

5. In on-chip CAN controller products, addresses 03FEC000H to 03FEEFFFH are assigned to addresses 03FEC000H to 03FECBFFH as a programmable peripheral I/O area. In other products, use of this area is prohibited.

6. Data write access to these addresses is made to the external memory area.

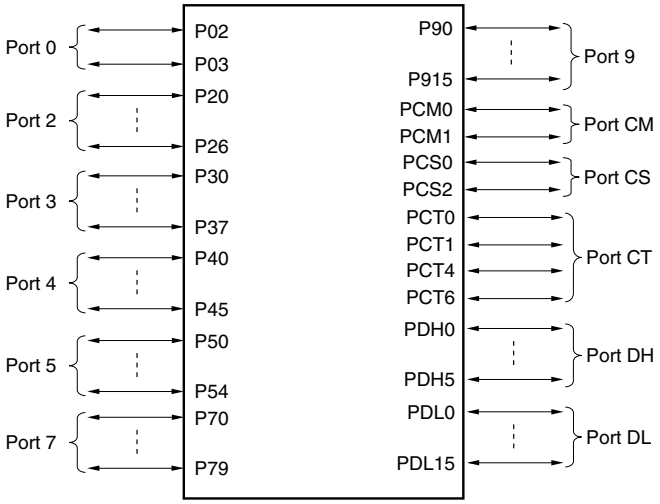
4. PORTS

The number of I/O ports of the V850ES/Jx3-E is shown below.

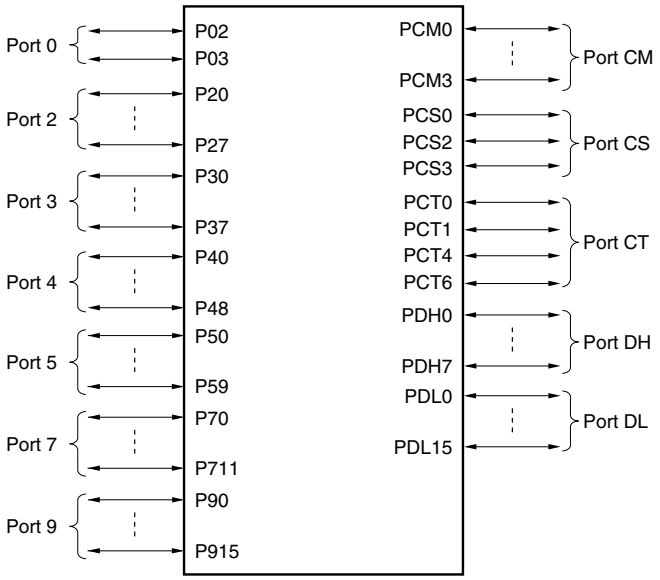
Product Name	V850ES/JH3-E	V850ES/JJ3-E
Number of ports (5 V tolerant)	84 (48)	100 (59)

The following figure shows the basic configurations of ports.

(a) V850ES/JH3-E



(b) V850ES/JJ3-E



5. EXTERNAL BUS INTERFACE FUNCTION

The V850ES/JH3-E, V850ES/JJ3-E incorporate an external bus interface function that can be used to connect memories, such as ROM or RAM, and peripheral I/O externally.

The external bus interface function has the following features.

- Separate bus/ Multiplexed bus output selectable.
- 8-bit/16-bit data bus sizing function
- Wait function
  - Programmable wait function
  - External wait function
- Idle state function
- Bus hold function

The following pins are used for the external bus interface.

Table 5-1. List of bus Control Pins (Multiplexed Bus Selected)

Bus Control Pin	Alternate Function		I/O	Function
AD0 to AD15	PDL0 to PDL15		I/O	Address/data bus
A16 to A23[Note 1]	PDH0 to PDH7		Output	Address bus
$\overline{\text{WAIT}}$	PCM0		Input	External wait control
CLKOUT	PCM1		Output	Internal system clock
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1		Output	Write strobe signal
$\overline{\text{RD}}$	PCT4		Output	Read strobe signal
ASTB	PCT6		Output	Address strobe signal
$\overline{\text{HLDRQ}}$	P44[Note 2]	PCM3[Note 3]	Input	Bus hold control
$\overline{\text{HLDAK}}$	P43[Note 2]	PCM2[Note 3]	Output	
$\overline{\text{CS0}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$[Note 3]	PCS0, PCS2, PSC3		Output	Chip select

Notes 1. V850ES/JJ3-E supports A16 to A23, and V850ES/JH3-E supports A16 to A21.

2. V850ES/JH3-E only.

3. V850ES/JJ3-E only.

Table 5-2. List of bus Control Pins (Separate Bus Selected)

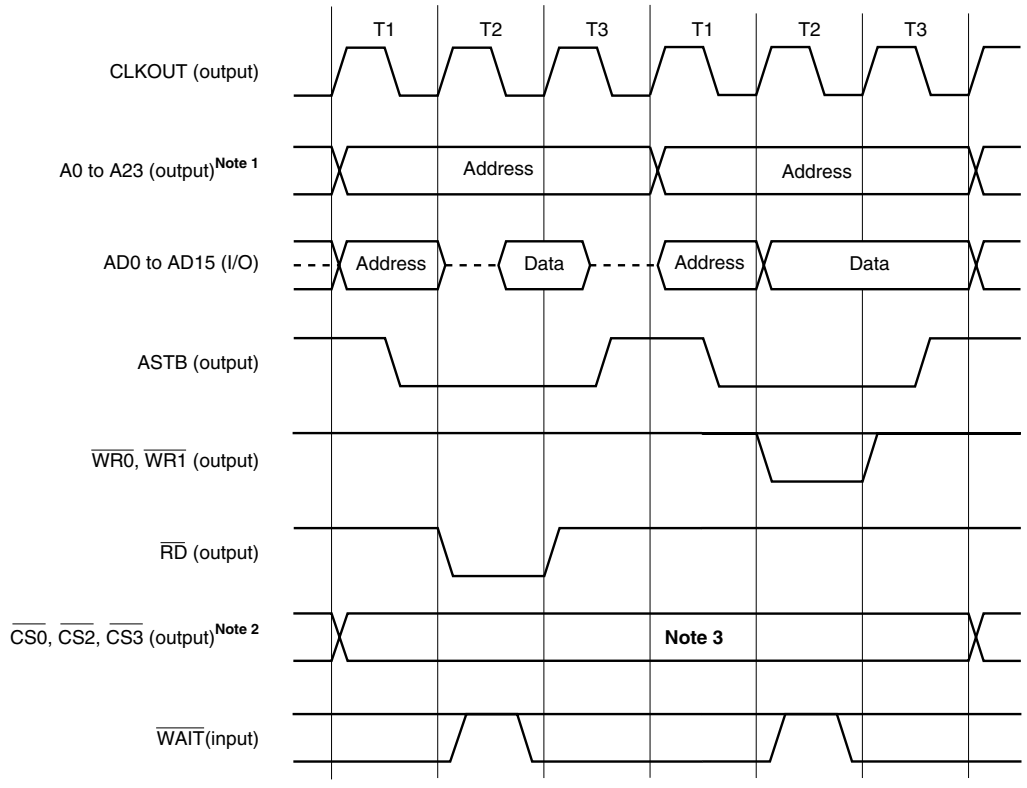
Bus Control Pin	Alternate Function		I/O	Function
AD0 to AD15	PDL0 to PDL15		I/O	Data bus
A0 to A15	P90 to P915		Output	Address bus
A16 to A23[Note 1]	PDH0 to PDH7		Output	Address bus
$\overline{WAIT}$	PCM0		Input	External wait control
CLKOUT	PCM1		Output	Internal system clock
$\overline{WR0}$, $\overline{WR1}$	PCT0, PCT1		Output	Write strobe signal
$\overline{RD}$	PCT4		Output	Read strobe signal
ASTB	PCT6		Output	Address strobe signal
$\overline{HLDRQ}$	P44[Note 2]	PCM3[Note 3]	Input	Bus hold control
$\overline{HLDAK}$	P43[Note 2]	PCM2[Note 3]	Output	
$\overline{CS0}$, $\overline{CS2}$, $\overline{CS3}$[Note 3]	PCS0, PCS2, PSC3		Output	Chip select

Notes 1. V850ES/JJ3-E supports A16 to A23, and V850ES/JH3-E supports A16 to A21.

2. V850ES/JH3-E only.

3. V850ES/JJ3-E only.

Figure 5-1. Timing Example in Separate Bus Mode (Read → Write)



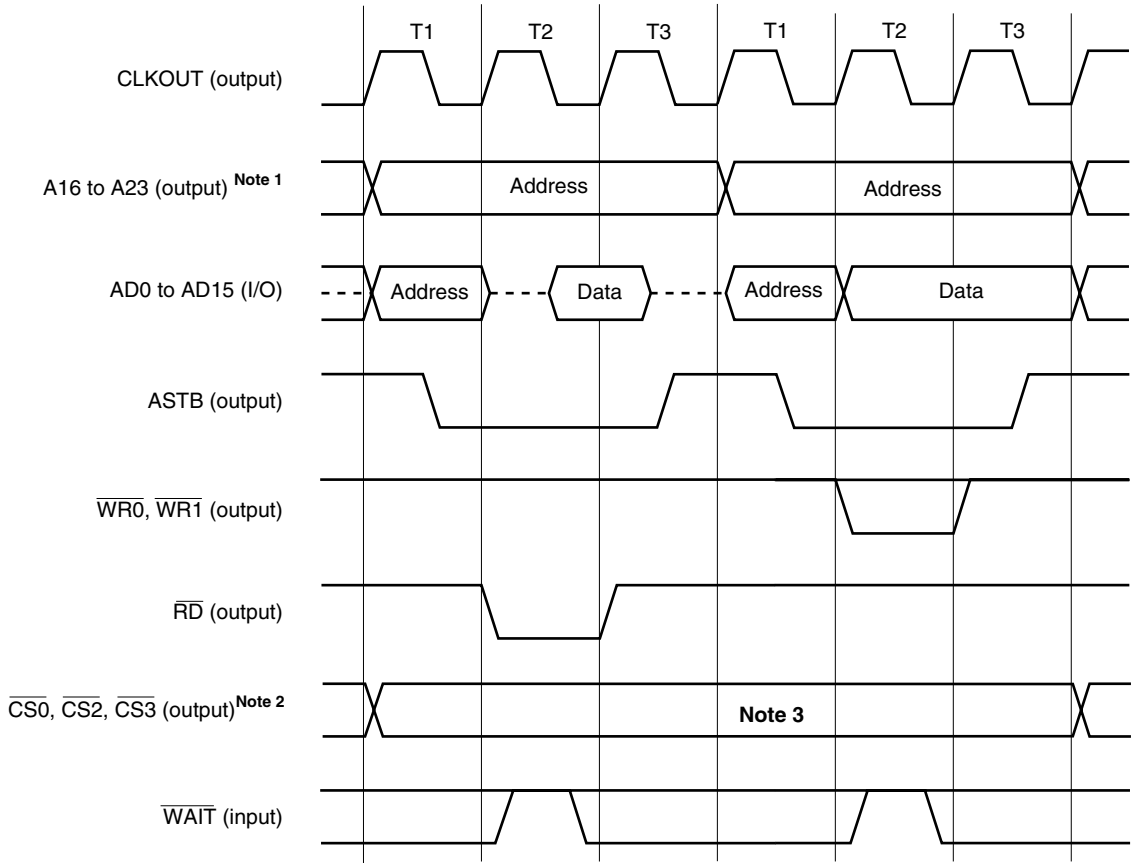
Notes1. V850ES/JH3-E supports A0 to A21, and V850ES/JJ3-E supports A0 to A23.

2. V850ES/JH3-E supports $\overline{CS0}$, $\overline{CS2}$ and V850ES/JJ3-E supports $\overline{CS0}$, $\overline{CS2}$, and $\overline{CS3}$.

3. Only the $\overline{CS}$ space to be accessed becomes active.

Remark The broken lines indicate high-impedance state.

Figure 5-2. Timing Example in Multiplexed Bus Mode (Read → Write)



Notes1. V850ES/JH3-E supports A16 to A21, and V850ES/JJ3-E supports A16 to A23.

2. V850ES/JH3-E supports $\overline{CS0}$, $\overline{CS2}$ and V850ES/JJ3-E supports $\overline{CS0}$, $\overline{CS2}$, and $\overline{CS3}$.

3. Only the $\overline{CS}$ space to be accessed becomes active.

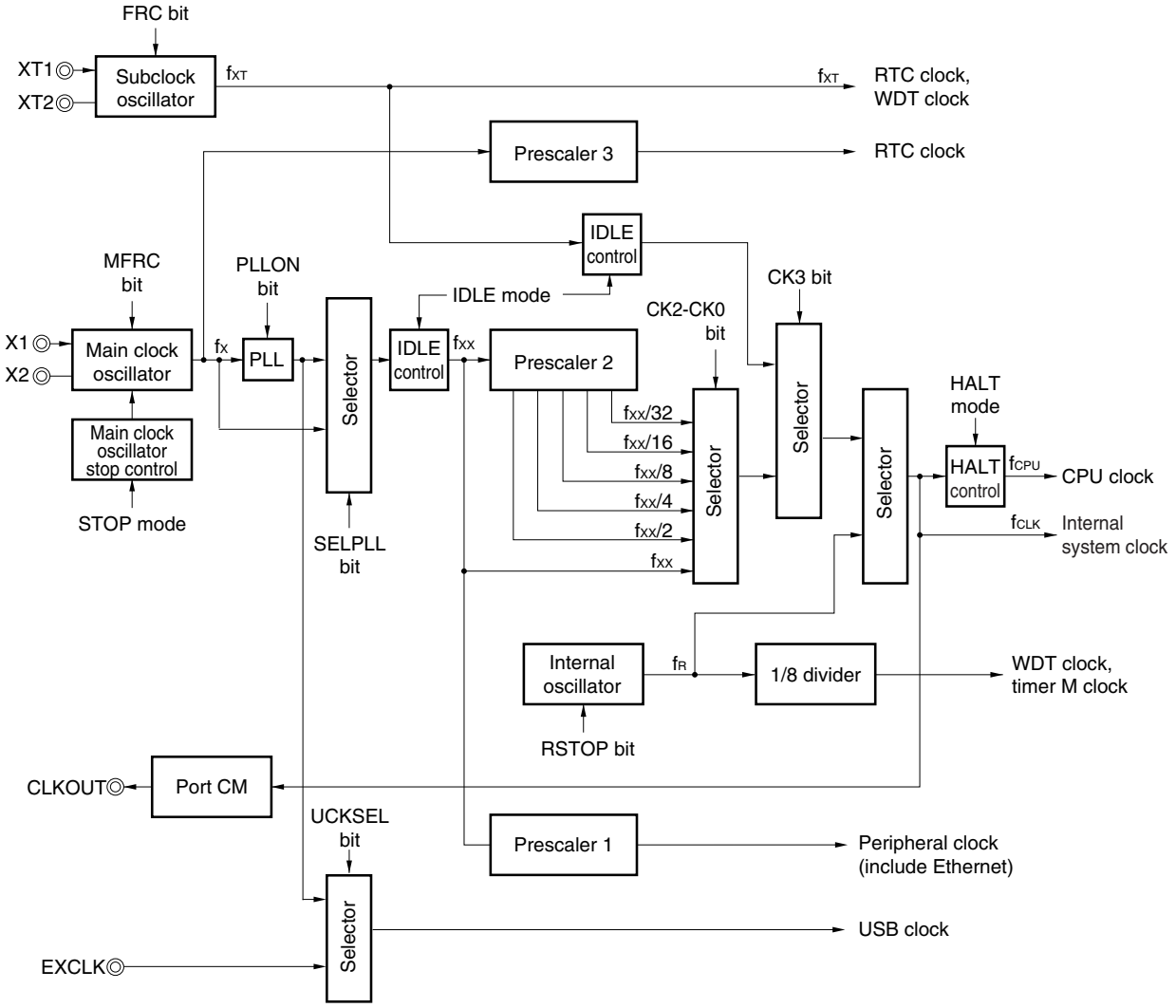
Remark The broken lines indicate high-impedance state.

6. CLOCK GENERATION FUNCTION

The clock generation function has the following features.

- ○ Main clock oscillator
  - PLL mode (×8): f_X = 3 to 6.25 MHz (f_{XX} = 24 to 50 MHz)
  - Clock through mode: f_X = 3 to 6.25 MHz (f_{XX} = 3 to 6.25 MHz)
- ○ Subclock oscillator
  - f_{XT} = 32.768 kHz
- ○ Internal oscillator (f_R = 220 kHz)
  - Default clock of watchdog timer
  - Sampling clock for clock monitor function of the main clock oscillator
  - Can be used as the internal system clock after the main clock is stopped
- ○ Internal system clock generation
  - 7 levels (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, f_{XT})
- ○ Peripheral clock generation
- ○ Clock output function

The following figure shows the configuration of the clock generation function.



Remark f_X: Main clock oscillation frequency
f_R: Internal oscillation frequency
f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_{CLK}: Internal system clock frequency

7. 16-BIT TIMER/EVENT COUNTER AA (TAA)

In the V850ES/Jx3-E, six channels of TAA are provided.

The timer/counter function has the following features.

- 16 bit timer/counter (TAAn)
- Clock selection: 8 ways
- Capture/trigger input pins (TIAAn0, TIAAn1): 2
- External event count input pin[Note]: 1
- External trigger input pin[Note]: 1
- Timer/counter: 1
- Capture/compare registers: 2
  (32-bit capture function available by using a cascade connection with timer AA.)
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOAAn0, TOAAn1): 2

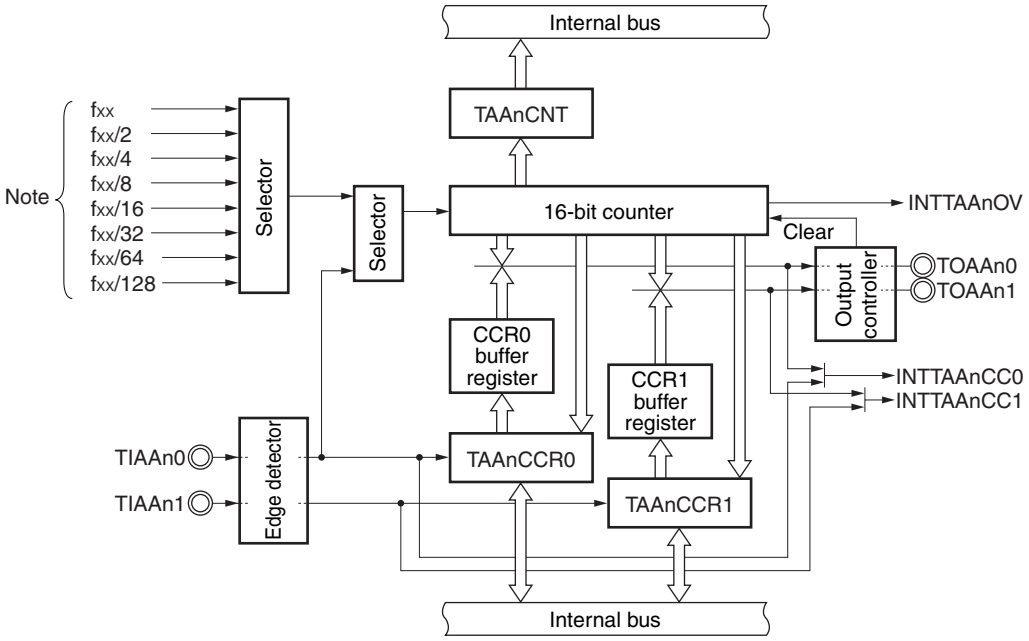
The TAAn function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Timer tuning function
- Simultaneous start function

Note The external event count input pin and external trigger input pin also function as the capture trigger input pin (TIAAn0).

Remark n = 0 to 5

The following figure shows the configuration of TAA.



Note fxx/2, fxx/4, fxx/8, fxx/16, fxx/64, fxx/256, fxx/512, fxx/1024 for TAA2, TAA3 or TAA5

Remark fxx = Main clock frequency

n = 0 to 5

8. 16-BIT TIMER/EVENT COUNTER AB (TAB)

In the V850ES/Jx3-E, two channels of TAB are provided.

The TAB function has the following features.

- 16-bit timer/counter (TABn)
- Clock selection: 8 ways
- Capture/trigger input pins (TIABn0 to TIABn3[Note 1, 2]): 4
- External event count input pin (EVTAB1): 1
- External trigger input pin (TRGAB1): 1
- Timer/counter: 1
- Capture/compare registers: 4
- Capture/compare match interrupt request signals: 4
- Timer output pins (TOABn0 to TOABn3[Note 2]): 4

The TABn function has the following features.

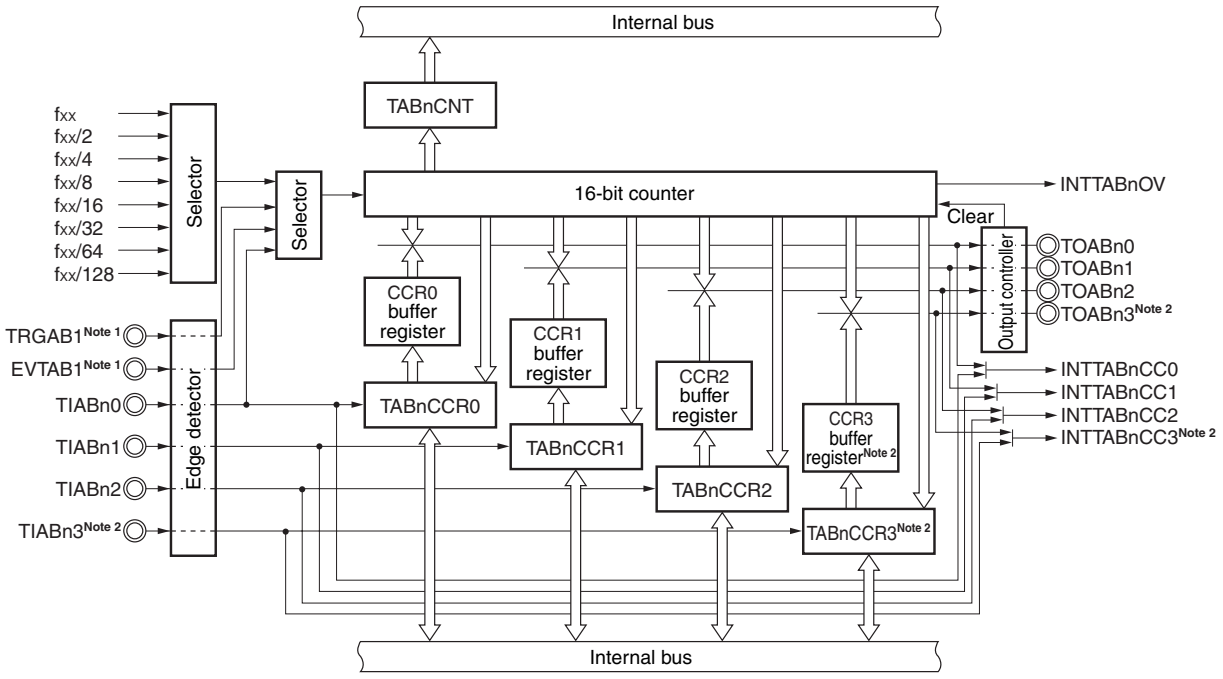
- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Timer tuning function

Notes 1. The external event count input pin and external trigger input pin of TAB0 also function as the capture trigger input pin (TIAB00). These pins do not function alternatively for TAB1 (individually provided as EVTAB1, TRGAB1 and TIAB10).

2. The I/O pins of the V850ES/JH3-E are TIAB00 to TIAB02 and TOAB00 to TOAB02 pins.

Remark n = 0, 1

The following figure shows the configuration of TAB.



Notes 1. Provided only for TAB1. In case of TAB0, the same functions as TRGAB0 and EVTAB0 are allocated to the TIAB00 pin as alternate functions.

2. V850ES/JJ3-E only.

Remark fxx: Main clock frequency

n = 0, 1

9. 16-BIT TIMER/EVENT COUNTER T (TMT)

In the V850ES/Jx3-E, one channel of TMT is provided.

The TMT function has the following features.

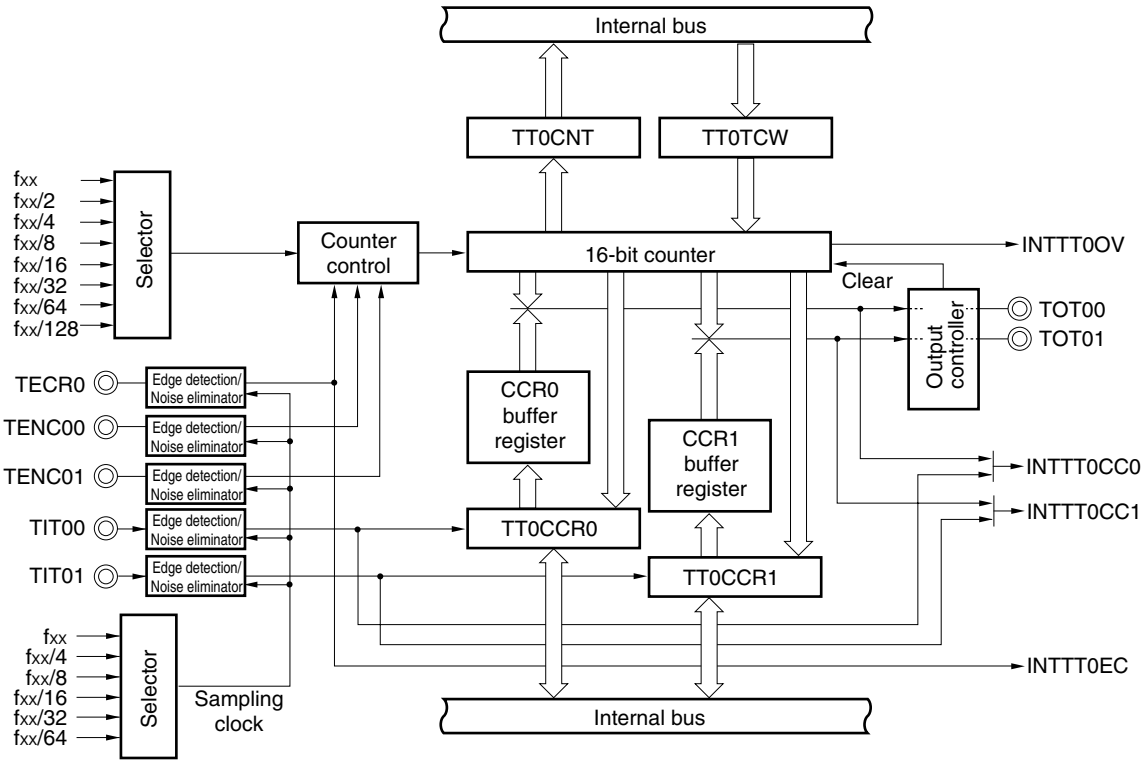
- 16 bit timer/counter (TMT)
- Clock selection: 8 ways
- Capture/trigger input pins (TIT00, TIT01) : 2
- External event count input pin[Note] : 1
- Encoder input pin (TENC00, TENC01) : 2
- Encoder clear input pin (TECR0) : 1
- External trigger input pin[Note]: 1
- Timer/counter: 1
- Capture/compare registers: 2
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOT00, TOT01) : 2

The TMT function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Encoder count function

Note The external trigger input pin and the external event count input pin also function as the encoder input pin (TENC00)

The following figure shows the configuration of TMT.



Remark fxx: Main clock frequency

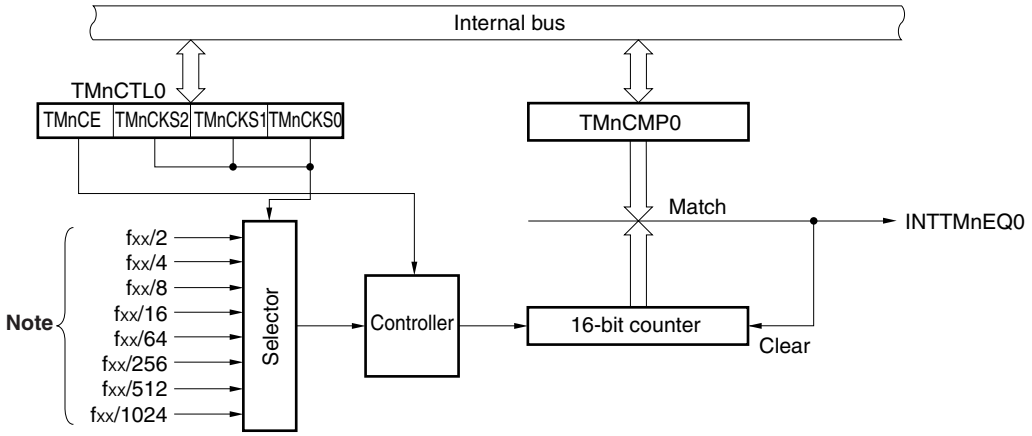
10. 16-BIT INTERVAL TIMER M (TMM)

In the V850ES/Jx3-E, four channels of TMM are provided.

The TMM function has the following features.

- Interval function
- Clock selection: 8 ways
- 16 bit counter × 1 (Not available to counter lead in timer count operation)
- Compare register × 1 (Not available to write compare register in timer count operation)
- Compare match interrupt × 1

The following figure shows the configuration of TMM.



Note In case of TMM0, f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/64$, $f_{XX}/512$, $f_{XX}/1048$, f_R, f_{XT}.

Remark f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
f_R: Internal oscillation frequency

11. MOTOR CONTROL FUNCTION

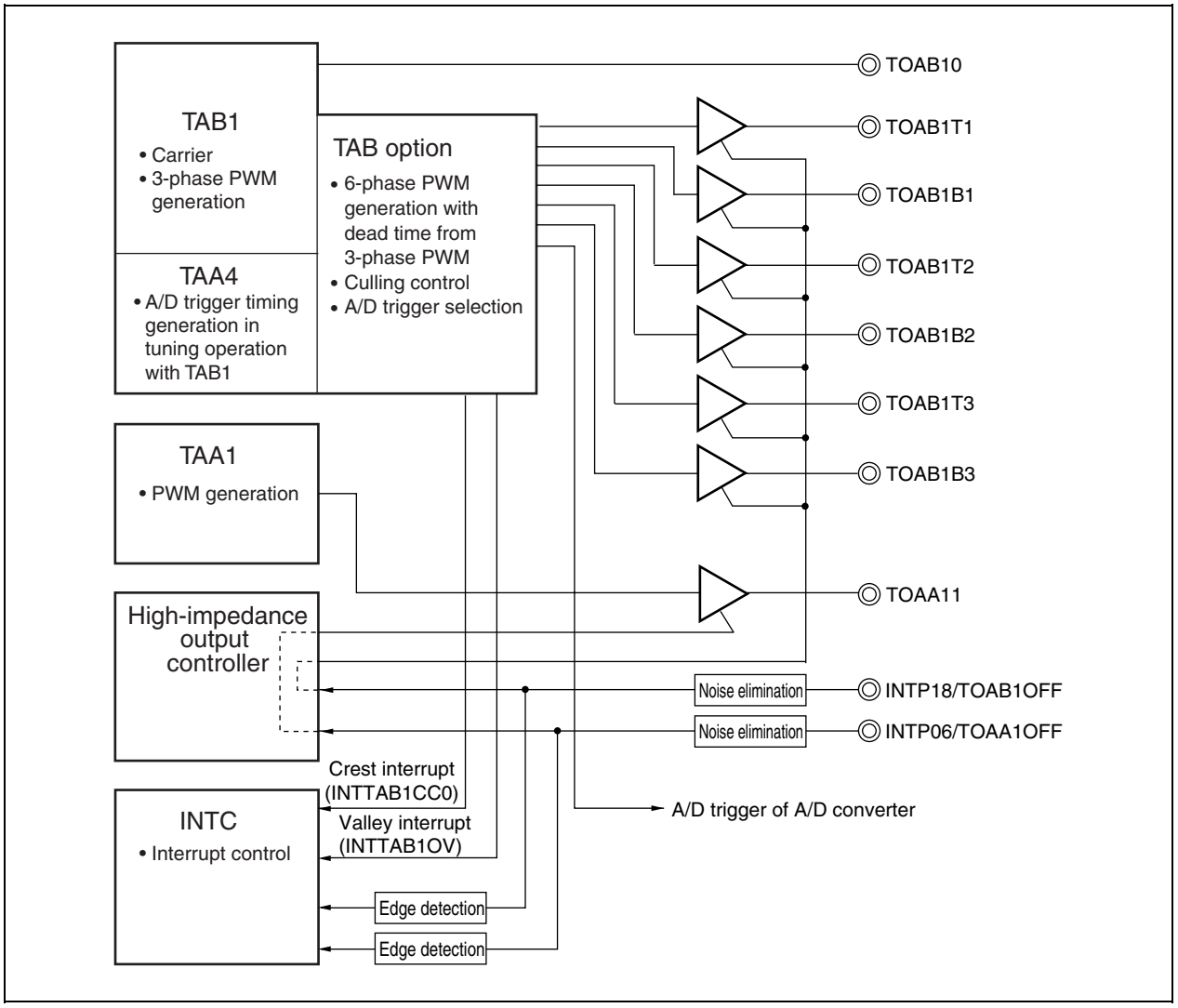
In the V850ES/Jx3-E, one channel of motor control function is provided.

Timer AB1 (TAB) and the TAB option (TABOP) can be used as an inverter function that controls a motor.

It performs a tuning operation with timer AA4 (TAA4) and A/D conversion of the A/D converter can be started when the value of TAB matches the value of TAA4. The following operations can be performed as motor control functions.

- 6-phase PWM output function with 16-bit resolution (with dead-timer, for upper and lower arms)
- Timer tuning operation function (tunable with TAA4)
- Cycle setting function (cycle can be changed during operation of crest or valley interrupt)
- Compare register rewriting: Anytime rewrite, batch rewrite, or intermittent rewrite (selectable during TAB operation)
- Interrupt and transfer culling functions
- Dead-time setting function
- A/D trigger timing function of the A/D converter (four types of timing can be generated)
- 0% output and 100% output available
- 0% output and 100% output selectable by crest interrupt and valley interrupt
- Forced output stop function
  - At valid edge detection by external pin input (INTP06/TOAA1OFF, INTP18/TOAB1OFF)
  - When stoppage of the main clock oscillation is detected by clock monitor function

The following figure shows the configuration of motor control function.



12. REAL-TIME COUNTER

In the V850ES/Jx3-E, one channel of real-time counter is provided.

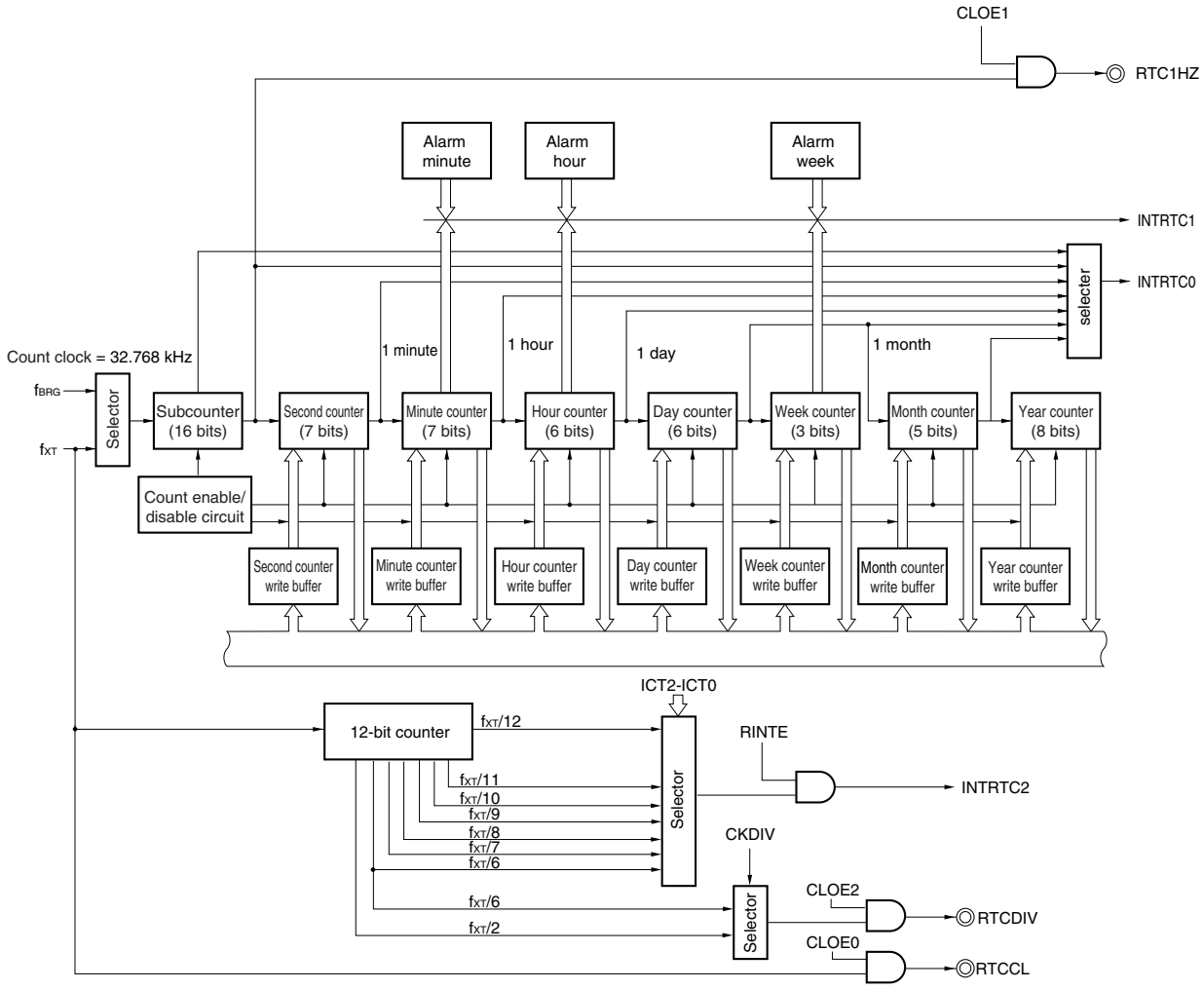
The real-time counter has the following features.

- It has counters for year, month, week, day, hours, minutes and seconds, and it can count up to 99 years.
- The year, month, week, day, hour, minute and second counters show the count in BCD code[Note 1].
- Alarm interrupt function
- Fixed-cycle interrupt function (cycle: 1 month to 0.5 seconds)
- Interval interrupt function (cycle: 1.95 to 125 ms)
- 1 Hz pin output
- 32.768 kHz pin output
- 512 Hz or 16.384 kHz pin output
- Watch error correction function
- Subclock operation or main clock operation[Note 2] selectable

Notes 1. BCD (binary-coded decimal) code is the code that represents each digit of a decimal number in 4-bit binary numerals.

2. The main clock can be divided into 32.768 kHz f_{BRG} with the baud rate generator dedicated to the real-time counter.

The following figure shows the configuration of real-time timer.



Remark f_{BRG}: Real-time counter count clock frequency
f_{XT}: Subclock frequency
INTRTC0: Real-time counter fixed-cycle signal
INTRTC1: Real-time counter alarm match signal
INTRTC2: Real-time counter interval signal

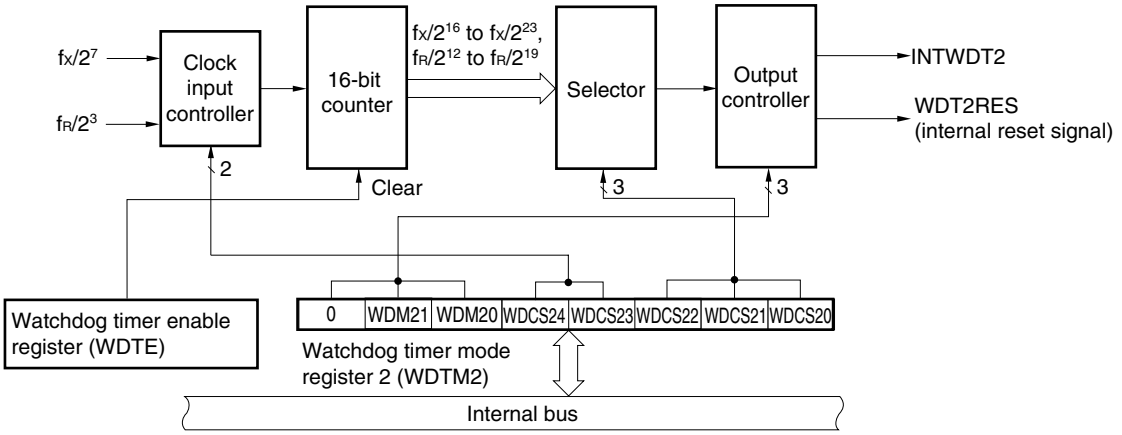
13. WATCHDOG TIMER 2 FUNCTIONS

In the V850ES/Jx3-E, one channel of watchdog timer 2 is provided.

The watchdog timer has the following functions.

- Reset mode: Reset operation upon overflow of watchdog timer (generates the WDT2RES signal)
- Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer (generates the INTWDT2 signal)

The following figure shows the configuration of the watchdog timer functions.



Remark fX: Main clock oscillation frequency
fR: Internal oscillation clock frequency
INTWDT2: Non-maskable interrupt request signal from watchdog timer 2
WDT2RES: Watchdog timer 2 reset signal

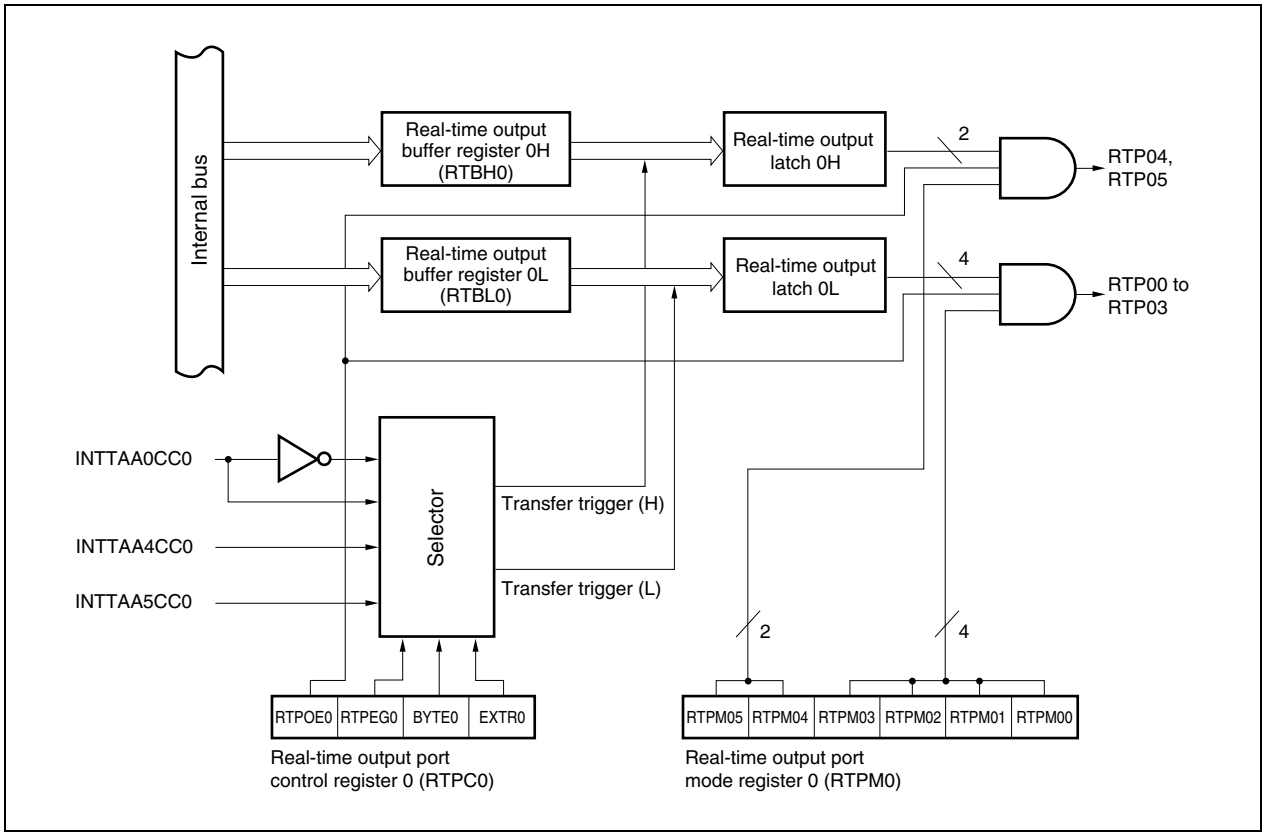
14. REAL-TIME OUTPUT FUNCTION (RTO)

In the V850ES/Jx3-E, one channel of real-time output is provided.

The RTO has the following features.

- 6-bit real-time output port: 1 channel
- The real-time output port can be set to the port mode or real-time output port mode in 1-bit units.

The RTO has the following configurations.



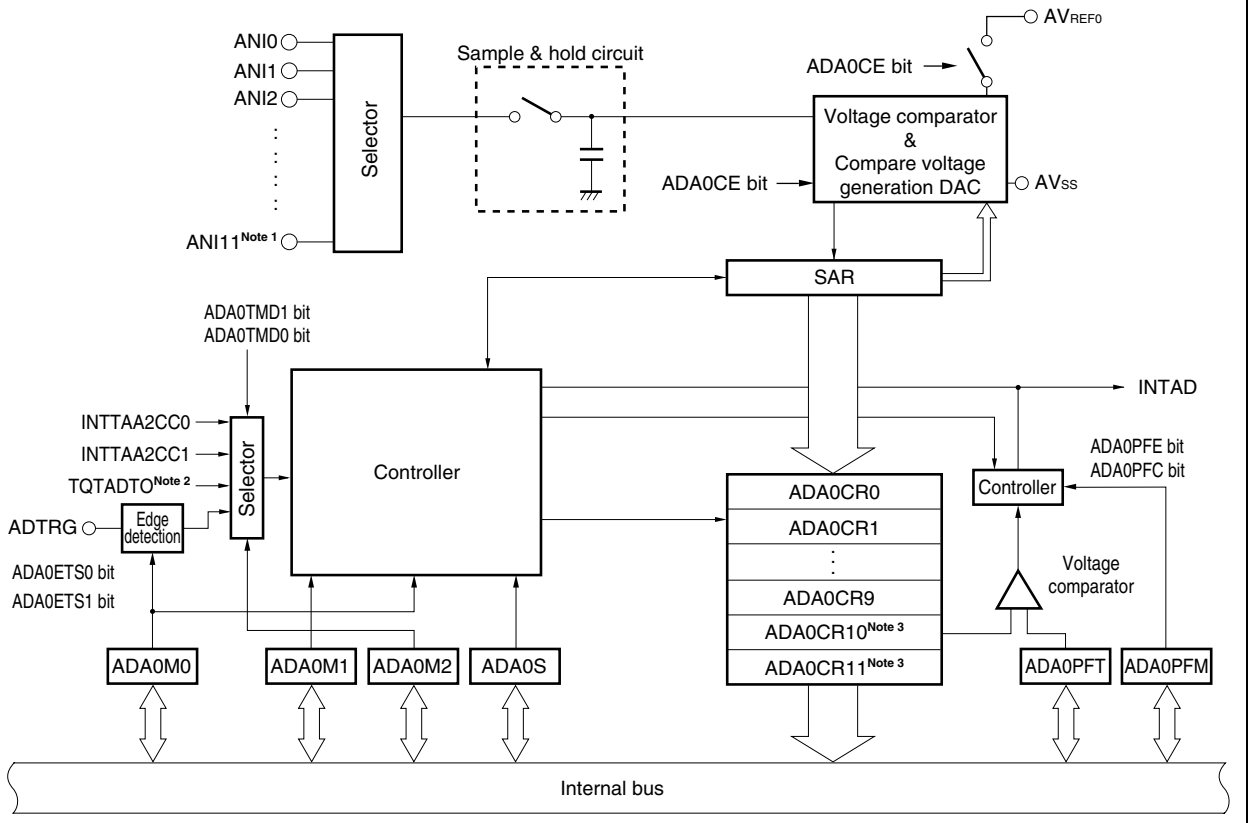
15. A/D CONVERTER

An A/D converter unit with ten channels is provided in the V850ES/JH3-E, and an A/D converter unit with twelve channels is provided in the V850ES/JJ3-E.

The A/D converter has the following features.

- 10-bit resolution
- 10 channels (V850ES/JH3-E)
  12 channels (V850ES/JJ3-E)
- Successive approximation method
- Operating voltage: AV_{REF0} = 3.0 to 3.6 V
- Analog input voltage: 0 V to AV_{REF0}
- The following functions are provided as operation modes.
  - Continuous select mode
  - Continuous scan mode
  - One-shot select mode
  - One-shot scan mode
- The following functions are provided as trigger modes.
  - Software trigger mode
  - External trigger mode (external, 1)
  - Timer trigger mode
- Power-fail monitor function (conversion result compare function)

The following figure shows the configuration of the A/D converter.



Notes 1. V850ES/JH3-E supports ANI00 to ANI09.

2. Timer trigger signal from 6-phase PWM output circuit (TABOP)

3. V850ES/JH3-E supports ADA0CR00 to ADA0CR09.

16. ASYNCHRONOUS SERIAL INTERFACE B WITH FIFO (UARTB)

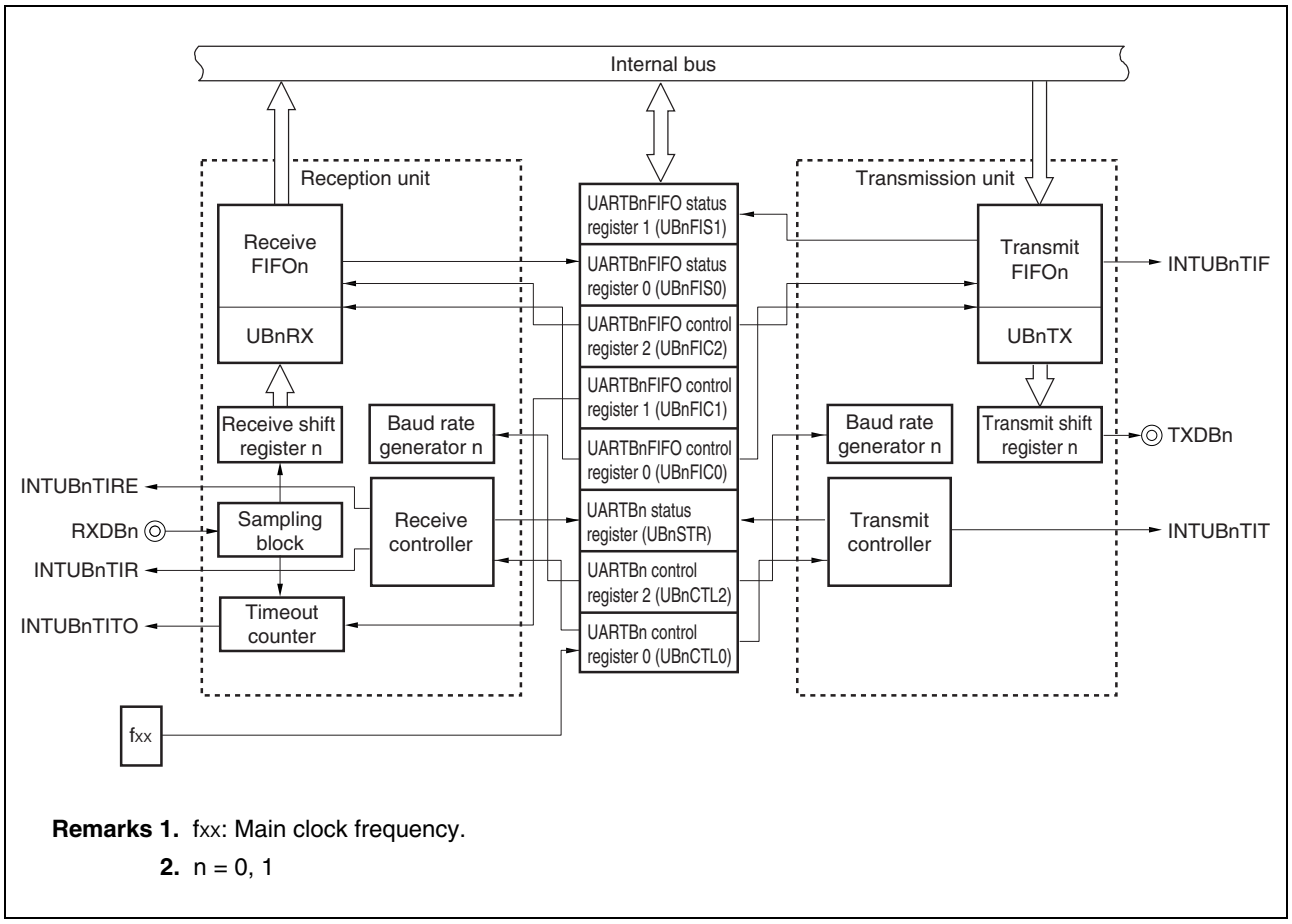
In the V850ES/Jx3-E, two channels of UARTB are provided.

The UARTB has the following features.

- Transfer rate: Maximum 625 kbps (using a dedicated baud rate generator)
- Full-duplex communications
- Single mode and FIFO mode selectable
  - Single mode: 8-bit × 1-stage data register (UBnTX register or UBnRX register) is used for each oftransmission and reception.
  - FIFO mode
    Transmit FIFOn: UBnTX register (8 bits × 16 stages).
    Receive FIFOn: UBnRXAP register (16 bits × 16 stages)
    The error information of a received data is stored in the higher 8 bits of the UBnRXAP register.
- Two-pin configuration
  TXDBn: Transmit data output pin
  RXDBn: Receive data input pin
- Reception error detection function
  - Overflow error (FIFO mode only)
  - Parity error
  - Framing error
  - Overrun error (single mode only)
- Interrupt sources: 5 types
  - Reception error interrupt request signal (INTUBnTIRE)
  - Reception completion interrupt request signal (INTUBnTIR)
  - Transmission enable interrupt request signal (INTUBnTIT)
  - FIFO transmission completion interrupt request signal (INTUBnTIF) (FIFO mode only)
  - Reception timeout interrupt request signal (INTUBnTITO) (FIFO mode only)
- The character length of transmit/receive data is specified according to the UBnCTL0 register
- Character length: 7 or 8 bits
- Parity functions: Odd, even, 0, or none
- Transmission stop bits: 1 or 2 bits
- MSB first/LSB first selectable for transfer data
- On-chip dedicated baud rate generator

Remark n = 0, 1

The following figure shows the configuration of UARTB.



Remarks 1. fXX: Main clock frequency.

2. n = 0, 1

17. ASYNCHRONOUS SERIAL INTERFACE C (UARTC)

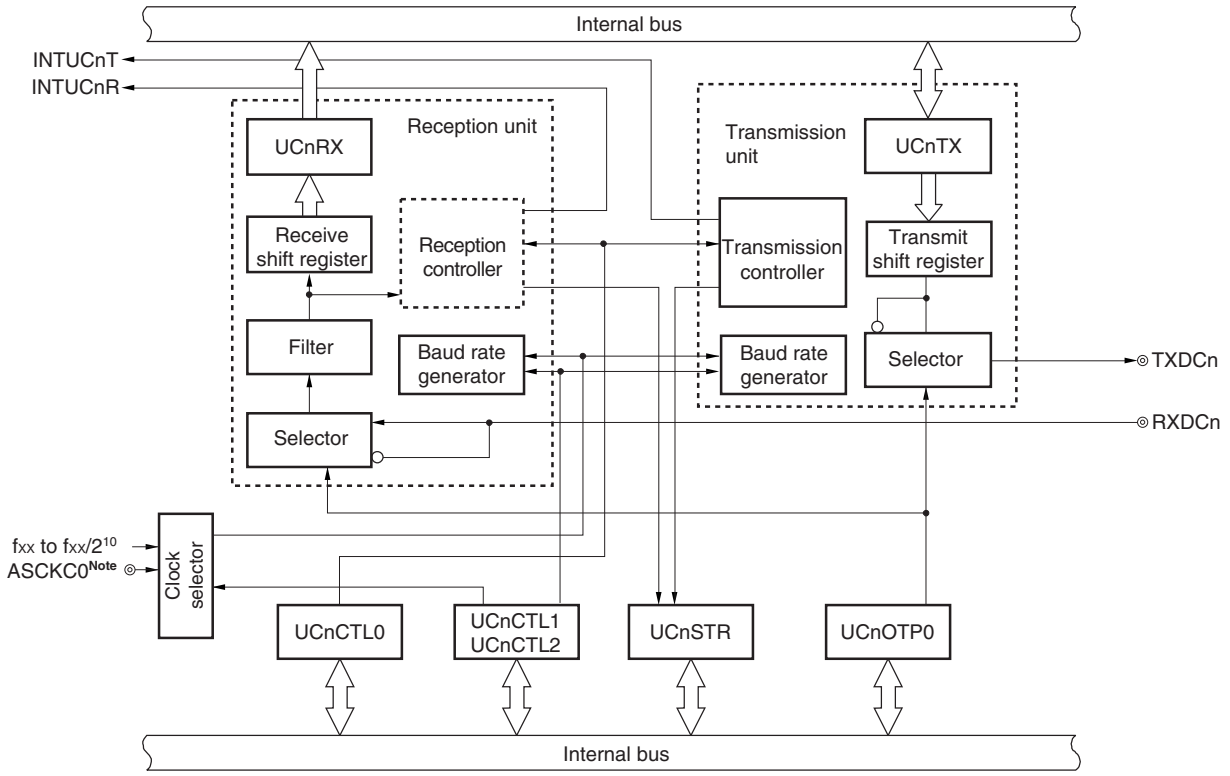
In the V850ES/JH3-E, six channels and V850ES/JJ3-E, eight channels of UARTC are provided.

The UARTC has the following features.

- Transfer rate: 300 bps to 1.25 Mbps (using internal system clock of 24 MHz and dedicated baud rate generator)
- Full-duplex communication: On-chip UARTCn receive data register (UCnRX)
  On-chip UARTCn transmit data register (UCnTX)
- 2-pin configuration: TXDCn: Transmit data output pin
  RXDCn: Receive data input pin
- Reception error detect function
  - Parity error
  - Framing error
  - Overrun error
  - LIN communication data consistency error detect function
  - SBF reception success detect function
- Interrupt sources: 2 types
  - Reception completion interrupt (INTUCnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status.
  - Transmission enable interrupt (INTUCnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status.
- Character length: 7, 8, 9 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output possible
- SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format possible
  - 13 to 20 bits are selectable for SBF transmission
  - Recognition of 11 bits or more possible for SBF reception in LIN format
  - SBF reception flag provided

Remark n = 0 to 5 (V850ES/JH3-E)
n = 0 to 7 (V850ES/JJ3-E)

The following figure shows the configuration of UARTC.



Note UARTC0 only

Remarks 1. fxx: Main clock frequency

2. n = 0 to 5 (V850ES/JH3-E)

n = 0 to 7 (V850ES/JJ3-E)

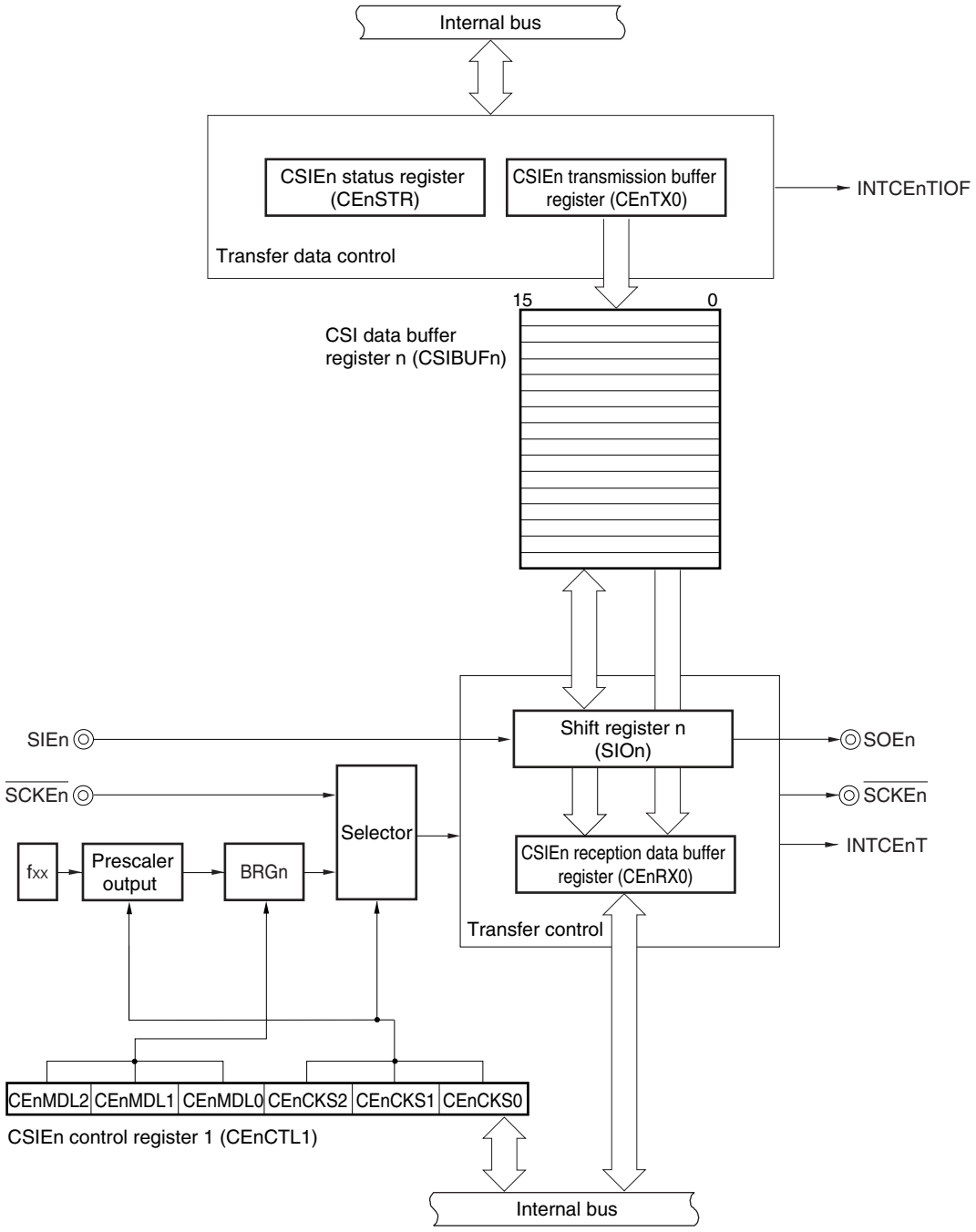
18. CLOCKED SERIAL INTERFACE E WITH FIFO (CSIE)

In the V850ES/Jx3-E, two channels of CSIE are provided.

- ○ Transfer rate: Maximum 5 Mbps
- ○ Master mode and slave mode selectable
- ○ Transfer data length selectable in 1-bit units between 8 and 16 bits
- ○ Transfer data MSB-first/LSB-first switchable
- ○ Serial clock and data phase switchable
- ○ Sixteen on-chip 16-bit transmission/reception buffers (CSIBUFn) available
- ○ Transmission mode, reception mode, and transmission/reception mode specifiable
  - Transmission mode : Transmission is started by writing transmit data to the CSIEn transmit buffer register (CEnTX0) while transmission is enabled.
  - Reception mode : Reception is started by writing dummy data to the CSIEn transmit buffer register (CEnTX0) while reception is enabled.
  - Transmission/reception mode: Transmission/reception is started by writing transmit data to the CSIEn transmit buffer register (CEnTX0) while transmission/reception is enabled.
- ○ Interrupt request signals
  - Transmit/receive completion interrupt (INTCEnT)
  - CSIBUFn overflow interrupt (INTCEnTIOF)
- ○ 3-wire SOEn : Serial data output
  SIEn : Serial data input
  $\overline{\text{SCKEn}}$: Serial clock I/O

Remark n = 0, 1

The following figure shows the configuration of CSIE.



Remarks 1. n = 0, 1

2. fxx: Main clock frequency.

19. CLOCKED SERIAL INTERFACE F (CSIF)

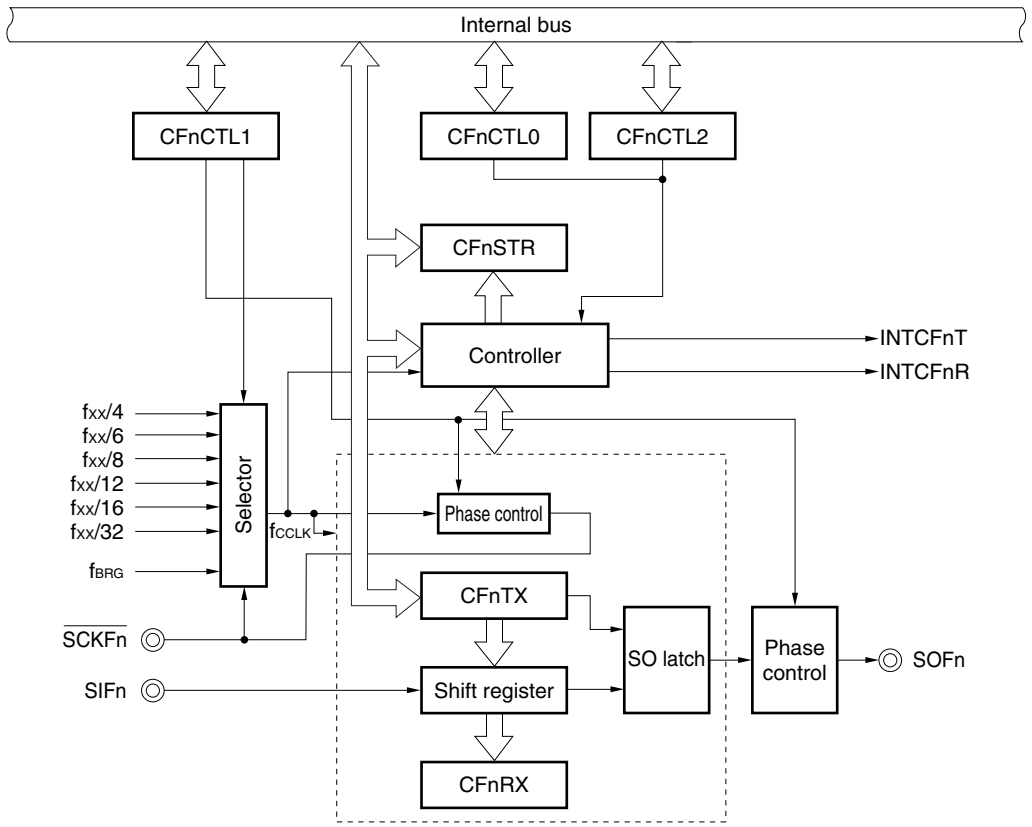
In the V850ES/JH3-E, five channels and V850ES/JJ3-E, seven channels of CSIF are provided.

- Transfer rate: 8 Mbps max. (f_{XX} = 50 MHz, using internal clock) (CSIF0, CSIF4, CSIF5)
  5 Mbps max. (f_{XX} = 50 MHz, using internal clock) (CSIF1 to CSIF3, CSIF6)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCFnT, INTCFnR)
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire
  SOFn: Serial data output
  $\overline{\text{SIFn}}$: Serial data input
  $\overline{\text{SCKFn}}$: Serial clock I/O

  Transmission mode, reception mode, and transmission/reception mode specifiable

Remark n = 0 to 5 (V850ES/JH3-E)
n = 0 to 7 (V850ES/JJ3-E)

The following figure shows the configuration of CSIF.



Remarks 1. n = 0 to 5 (V850ES/JH3-E)
n = 0 to 7 (V850ES/JJ3-E)

2. f_{XX}: Main clock frequency
f_{BRG}: Baud rate generator count clock
f_{CCLK}: Communication clock

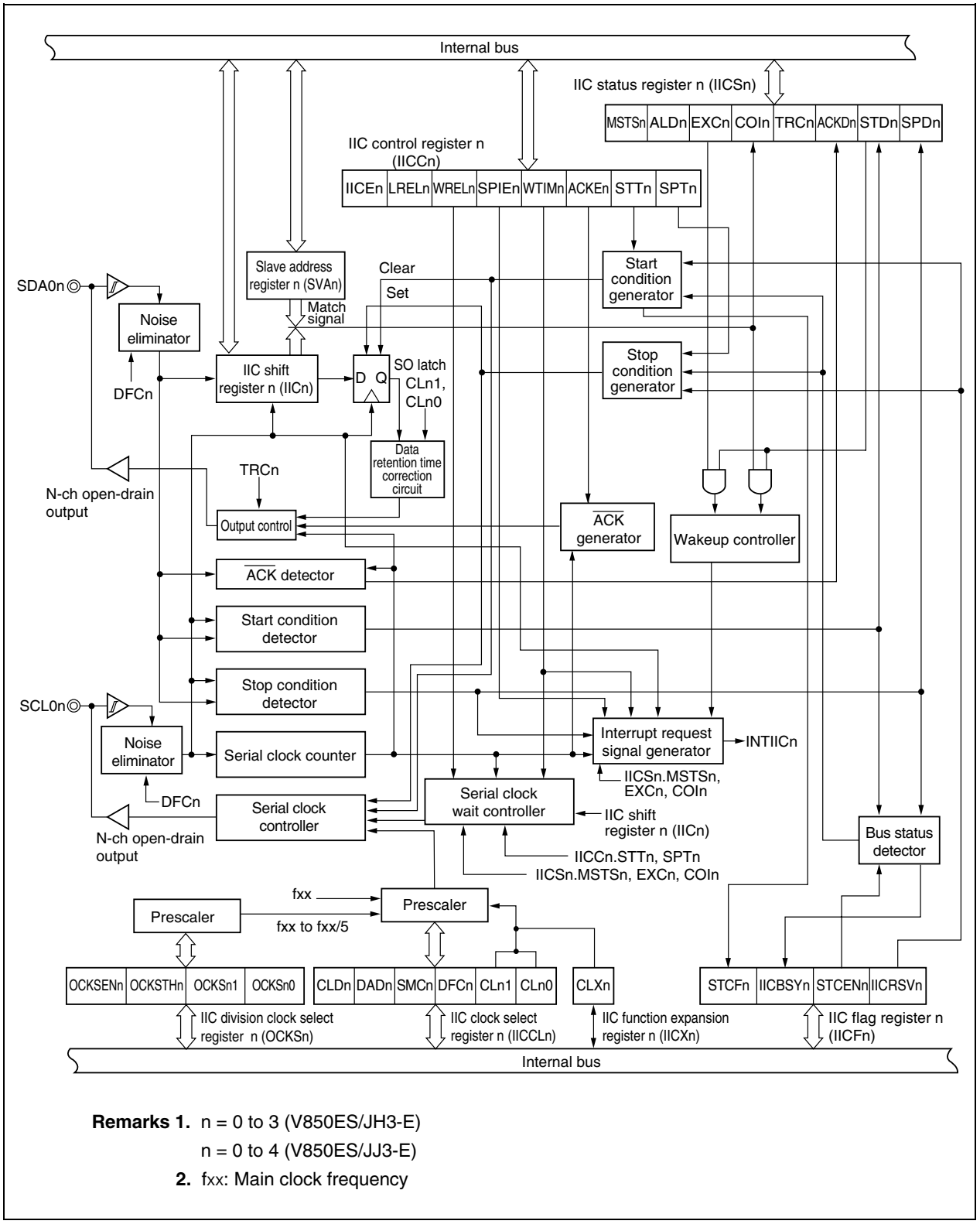
20. I²C BUS

In the V850ES/JH3-E, four channels and V850ES/JJ3-E, five channels of I²C are provided.

- Transfer rate: Standard mode (100 kbps max.)/high-speed mode (400 kbps max.)
- Conforms to I²C bus format (multimaster supported)
- 2-wire SCL0n: Serial clock pin
  SDA0n: Serial data bus pin

Remark n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

The following figure shows the configuration of I²C.



Remarks 1. n = 0 to 3 (V850ES/JH3-E)
n = 0 to 4 (V850ES/JJ3-E)

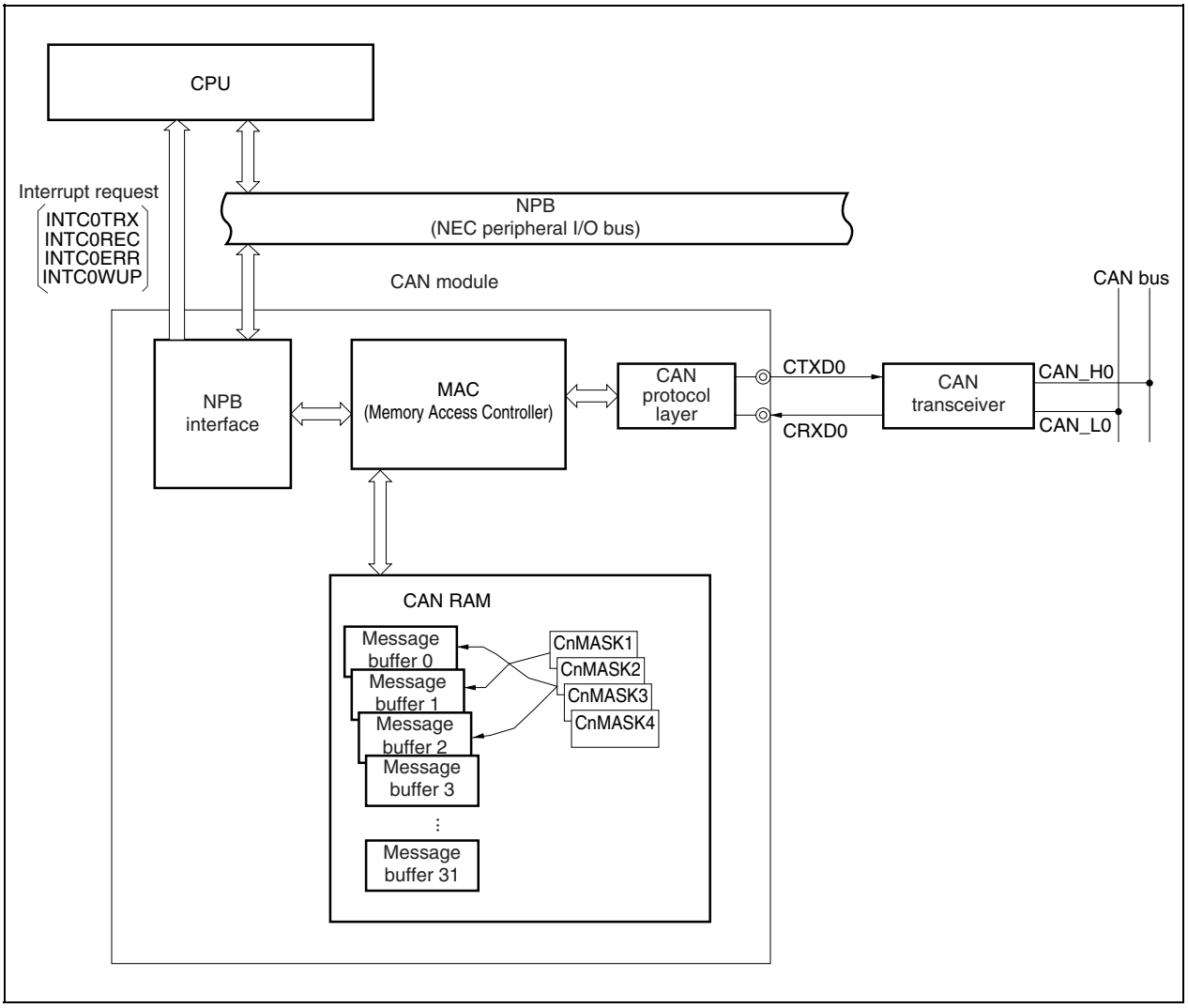
2. fxx: Main clock frequency

21. CAN CONTROLLER

In the μPD70F3783, 70F3786, one channel of CAN controller is provided.

- Compliant with ISO 11898 and tested according to ISO/DIS 16845 (CAN conformance test)
- Standard frame and extended frame transmission/reception enabled
- Transfer rate: 1 Mbps max. (CAN clock input ≥ 8 MHz)
- 32 message buffers/channels
- Receive/transmit history list function
- Automatic block transmission function
- Multi-buffer receive block function
- Mask setting of four patterns is possible for each channel

The following figure shows the configuration of CAN controller.



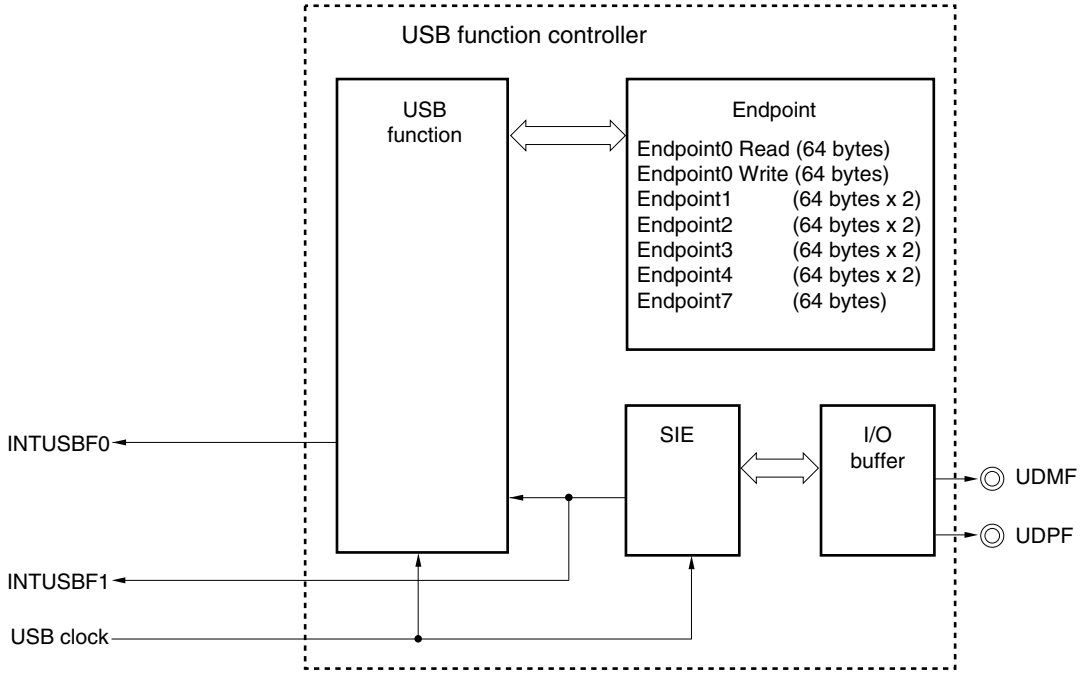
22. USB FUNCTION CONTROLLER (USBF)

In the V850ES/Jx3-E, one channel of USBF is provided.

- Conforms to the Universal Serial Bus (USB) Specification.
- USB 2.0-compatible full-speed transfer (12 Mbps) supported
- Endpoint for transfer incorporated

Endpoint Name	FIFO Size (Bytes)	Transfer Type	Remark
Endpoint0 Read	64	Control transfer	−
Endpoint0 Write	64	Control transfer	−
Endpoint1	64 × 2	Bulk 1 transfer (IN)	2-buffer configuration
Endpoint2	64 × 2	Bulk 1 transfer (OUT)	2-buffer configuration
Endpoint3	64 × 2	Bulk 2 transfer (IN)	2-buffer configuration
Endpoint4	64 × 2	Bulk 2 transfer (OUT)	2-buffer configuration
Endpoint7	8	Interrupt transfer (IN)	−

The following figure shows the configuration of USB function controller.



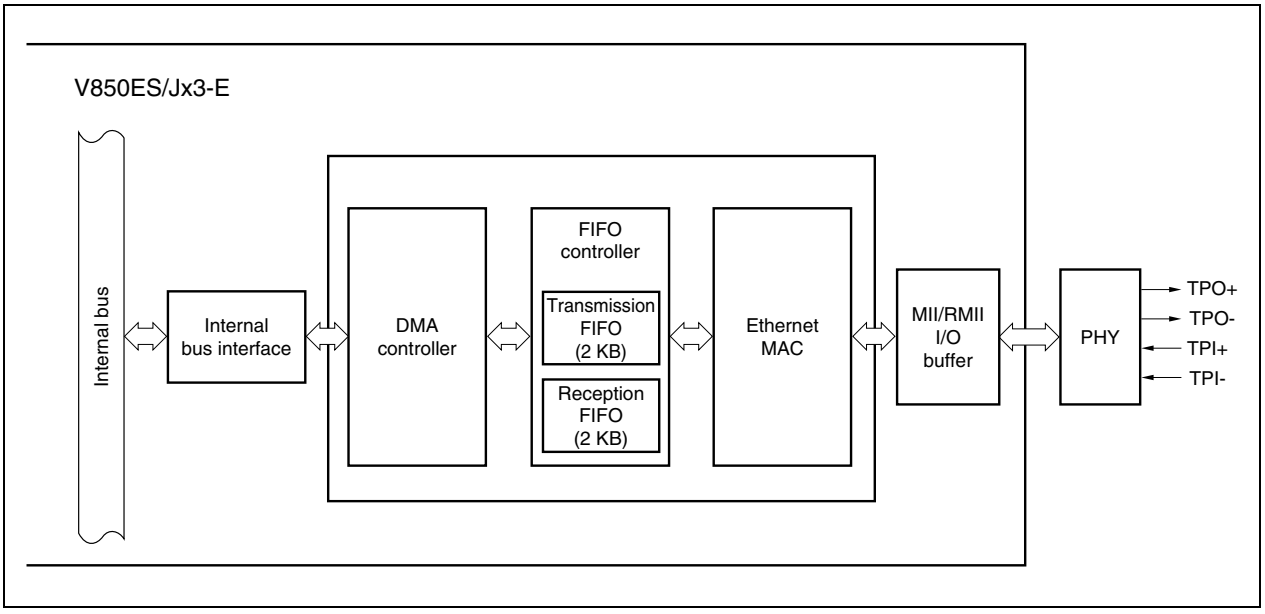
Remark Area enclosed with dashed line: Functions included in USB function controller

23. ETHERNET CONTROLLER

In the V850ES/Jx3-E, one channel of Ethernet controller is provided.

- 10 Mbps/100 Mbps MAC function conforming to the IEEE802.3 standard
  - Full-duplex and half-duplex communications and a flow control function are supported
  - On-chip packet filtering function based on address type
  - On-chip VLAN detection function
- Ethernet-dedicated DMA controller
  - Reception status DMA transfer possible
  - Reading (in pointer-chain format), analysis, and writing back of buffer descriptors possible
  - Interrupt control functions for packet transfers
- FIFO controller
  - Transmission/reception FIFO size: Transmission FIFO (2 KB), reception FIFO (2 KB)
  - On-chip FIFO status register
  - Interrupts occur in accordance with the transmission/reception status and FIFO status.
- MII is supported as the interface with physical-layer devices (PHY)
- On-chip reception checksum calculation function conforming to RFC1071

The following figure shows the configuration of USB function controller.

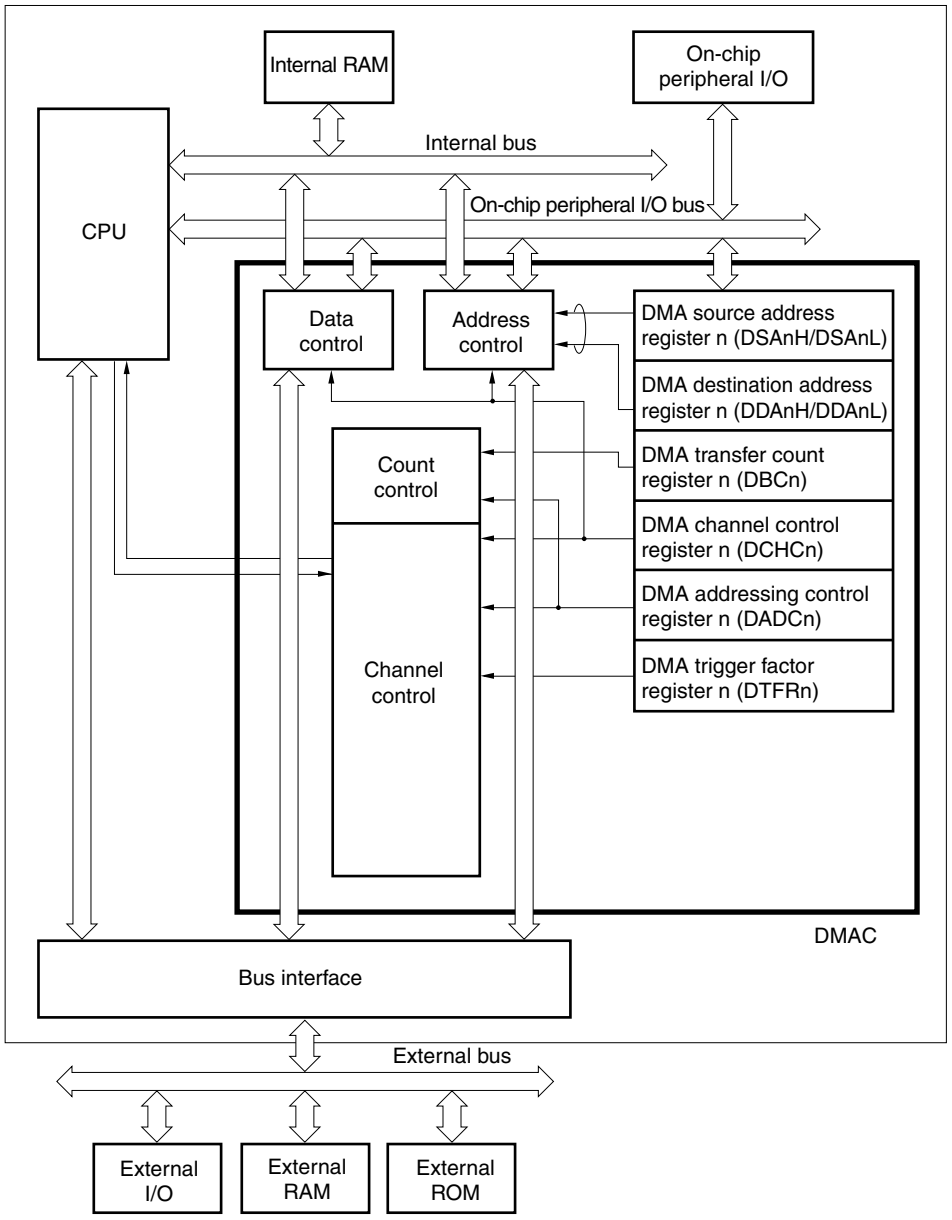


24. DMA CONTROLLER

In the V850ES/Jx3-E, four channels of DMA controller are provided.

- 4 independent DMA channels
- Transfer unit: 8/16 bits
- Maximum transfer count: 65,536 (2^{16})
- Transfer type: Two-cycle transfer
- Transfer mode: Single transfer mode
- Transfer requests
  - Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, real-time counter, A/D converter) or interrupts from external input pin
  - Requests by software trigger
- Transfer targets
  - Internal RAM ⇔ Peripheral I/O
  - Peripheral I/O ⇔ Peripheral I/O
  - Internal RAM ⇔ External memory
  - External memory ⇔ Peripheral I/O
  - External memory ⇔ External memory

The following figure shows the configuration of DMA controller.



Remark n = 0 to 3

25. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The features of interrupt/exception processing function is shown below.

○ Interrupts

		Internal			External		
		Non maskable	Maskable	Total	Non maskable	Maskable	Total
V850ES/JH3-E	μPD70F3778	1	78	79	1	21	22
	μPD70F3779	1	78	79	1	21	22
	μPD70F3780	1	78	79	1	21	22
	μPD70F3781	1	78	79	1	21	22
	μPD70F3782	1	78	79	1	21	22
	μPD70F3783	1	82	83	1	21	22
V850ES/JJ3-E	μPD70F3784	1	83	84	1	26	27
	μPD70F3785	1	83	84	1	26	27
	μPD70F3786	1	87	88	1	26	27

- 8 levels of programmable priorities
- Masks interrupt requests according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions

- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 25-1.

Table 25-1. Interrupt Source List (1/4)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Interrupt Control Register	V850ES/JH3-E	V850ES/JJ3-E
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input/reset input from internal source	RESET	–	√	√
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	Pin	–	√	√
		–	INTWDT2	WDT2 overflow	WDT2	–	√	√
Software exception	Exception	–	TRAP0n (n = 0-FH)	TRAP instruction	–	–	√	√
		–	TRAP1n (n = 0-FH)	TRAP instruction	–	–	√	√
Exception trap	Exception	–	ILGOP/DBG0	Illegal instruction code/DBTRAP instruction	–	–	√	√
Maskable	Interrupt	0	INTLVI	Detection of low voltage	POCLVI	LVIIC	√	√
		1	INTP00	Detection of external interrupt pin input edge (INTP00)	Pin	PIC0	√	√
		2	INTP01	Detection of external interrupt pin input edge (INTP01)	Pin	PIC1	√	√
		3	INTP02	Detection of external interrupt pin input edge (INTP02)	Pin	PIC2	√	√
		4	INTP03	Detection of external interrupt pin input edge (INTP03)	Pin	PIC3	√	√
		5	INTP04	Detection of external interrupt pin input edge (INTP04)	Pin	PIC4	√	√
		6	INTP05	Detection of external interrupt pin input edge (INTP05)	Pin	PIC5	√	√
		7	INTP06	Detection of external interrupt pin input edge (INTP06)	Pin	PIC6	√	√
		8	INTP07	Detection of external interrupt pin input edge (INTP07)	Pin	PIC7	√	√
		9	INTP08	Detection of external interrupt pin input edge (INTP08)	Pin	PIC8	√	√
		10	INTP09	Detection of external interrupt pin input edge (INTP09)	Pin	PIC9	√	√
		11	INTP10	Detection of external interrupt pin input edge (INTP10)	Pin	PIC10	√	√
		12	INTP11	Detection of external interrupt pin input edge (INTP11)	Pin	PIC11	√	√
		13	INTP12	Detection of external interrupt pin input edge (INTP12)	Pin	PIC12	√	√
		14	INTP13	Detection of external interrupt pin input edge (INTP13)	Pin	PIC13	√	√
		15	INTP14	Detection of external interrupt pin input edge (INTP14)	Pin	PIC14	√	√
		16	INTP15	Detection of external interrupt pin input edge (INTP15)	Pin	PIC15	√	√
		17	INTP16	Detection of external interrupt pin input edge (INTP16)	Pin	PIC16	√	√
		18	INTP17	Detection of external interrupt pin input edge (INTP17)	Pin	PIC17	√	√
		19	INTP18	Detection of external interrupt pin input edge (INTP18)	Pin	PIC18	√	√
		20	INTP19	Detection of external interrupt pin input edge (INTP19)	Pin	PIC19	√	√
		21	INTP20	Detection of external interrupt pin input edge (INTP20)	Pin	PIC20	√	√
		22	INTP21	Detection of external interrupt pin input edge (INTP21)	Pin	PIC21	–	√
		23	INTP22	Detection of external interrupt pin input edge (INTP22)	Pin	PIC22	–	√
		24	INTP23	Detection of external interrupt pin input edge (INTP23)	Pin	PIC23	–	√
		25	INTP24	Detection of external interrupt pin input edge (INTP24)	Pin	PIC24	–	√
		26	INTP25	Detection of external interrupt pin input edge (INTP25)	Pin	PIC25	–	√
		27	INTTAB0OV	TAB0 overflow	TAB0	TAB0OVIC	√	√
		28	INTTAB0CC0	TAB0 capture 0/compare 0 match	TAB0	TAB0CCIC0	√	√
		29	INTTAB0CC1	TAB0 capture 1/compare 1 match	TAB0	TAB0CCIC1	√	√
		30	INTTAB0CC2	TAB0 capture 2/compare 2 match	TAB0	TAB0CCIC2	√	√
		31	INTTAB0CC3	TAB0 capture 3/compare 3 match	TAB0	TAB0CCIC3	–	√

Table 25-1. Interrupt Source List (2/4)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Interrupt Control Register	V850ES/JH3-E	V850ES/JJ3-E
Maskable	Interrupt	32	INTTAB1OV	TAB1 overflow	TAB1	TAB1OVIC	√	√
		33	INTTAB1CC0	TAB1 capture 0/compare 0 match	TAB1	TAB1CCIC0	√	√
		34	INTTAB1CC1	TAB1 capture 1/compare 1 match	TAB1	TAB1CCIC1	√	√
		35	INTTAB1CC2	TAB1 capture 2/compare 2 match	TAB1	TAB1CCIC2	√	√
		36	INTTAB1CC3	TAB1 capture 3/compare 3 match	TAB1	TAB1CCIC3	√	√
		37	INTTT0OV	TMT0 overflow	TMT0	TT0OVIC	–	√
		38	INTTT0CC0	TMT0 capture 0/compare 0 match	TMT0	TT0CCIC0	√	√
		39	INTTT0CC1	TMT0 capture 1/compare 1 match	TMT0	TT0CCIC1	√	√
		40	INTTT0EC	TMT0 encoder input	TMT0	TT0ECIC	√	√
		41	INTTAA0OV	TAA0 overflow	TAA0	TAA0OVIC	√	√
		42	INTTAA0CC0	TAA0 capture 0/compare 0 match	TAA0	TAA0CCIC0	√	√
		43	INTTAA0CC1	TAA0 capture 1/compare 1 match	TAA0	TAA0CCIC1	√	√
		44	INTTAA1OV	TAA1 overflow	TAA1	TAA1OVIC	√	√
		45	INTTAA1CC0	TAA1 capture 0/compare 0 match	TAA1	TAA1CCIC0	√	√
		46	INTTAA1CC1	TAA1 capture 1/compare 1 match	TAA1	TAA1CCIC1	√	√
		47	INTTAA2OV	TAA2 overflow	TAA2	TAA2OVIC	√	√
		48	INTTAA2CC0	TAA2 capture 0/compare 0 match	TAA2	TAA2CCIC0	√	√
		49	INTTAA2CC1	TAA2 capture 1/compare 1 match	TAA2	TAA2CCIC1	√	√
		50	INTTAA3OV	TAA3 overflow	TAA3	TAA3OVIC	–	√
		51	INTTAA3CC0	TAA3 capture 0/compare 0 match	TAA3	TAA3CCIC0	–	√
		52	INTTAA3CC1	TAA3 capture 1/compare 1 match	TAA3	TAA3CCIC1	–	√
		53	INTTAA4OV	TAA4 overflow	TAA4	TAA4OVIC	–	√
		54	INTTAA4CC0	TAA4 capture 0/compare 0 match	TAA4	TAA4CCIC0	–	√
		55	INTTAA4CC1	TAA4 capture 1/compare 1 match	TAA4	TAA4CCIC1	–	√
		56	INTTAA5OV	TAA5 overflow	TAA5	TAA5OVIC	√	√
		57	INTTAA5CC0	TAA5 capture 0/compare 0 match	TAA5	TAA5CCIC0	√	√
		58	INTTAA5CC1	TAA5 capture 1/compare 1 match	TAA5	TAA5CCIC1	√	√
		59	INTTM0EQ0	TMM0 compare match	TMM0	TM0EQIC0	√	√
		60	INTTM1EQ0	TMM1 compare match	TMM1	TM1EQIC0	√	√
		61	INTTM2EQ0	TMM2 compare match	TMM2	TM2EQIC0	√	√
		62	INTTM3EQ0	TMM3 compare match	TMM3	TM3EQIC0	√	√
		63	INTCE0T/INTUC4R	CSIE0 transfer completion/UARTC4 reception error	CSIE0 /UARTC4	CE0TIC /UC4RIC	√	√
		64	INTCE0TIOF/INTUC4T	CSIE0 buffer overflow/ UARTC4 continuous transfer write enable	CSIE0 /UARTC4	CE0TIOFIC /UC4TIC	√	√
		65	INTCE1T /INTUC5R /INTIIC3	CSIE1 transfer completion/UARTC5 reception error /IIC2 transfer completion	CSIE1 /UARTC5 /IIC3	CE1TIC /UC5RIC /IICIC3	√	√
		66	INTCE1TIOF /NTUC5T	CSIE1 buffer overflow/UARTC5 continuous transfer write enable	CSIE1 /UARTC5	CE1TIOFIC /UC5TIC	√	√

Table 25-1. Interrupt Source List (3/4)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Interrupt Control Register	V850ES/JH3-E	V850ES/JJ3-E
Maskable	Interrupt	67	INTCF0R /INTUC3R /INTIIC1	CSIF0 transfer completion/UARTC3 reception completion/UARTC3 reception error/IIC1 transfer completion	CSIF0 /UARTC3 /IIC1	CE0RIC /UC3RIC /IICIC1	√	√
		68	INTCF0T /INTUC3T	CSIF0 continuous transfer write enable/ UARTC3 continuous transfer write enable	CSIF0 /UARTC3	CF0TIC /UC3TIC	√	√
		69	INTCF1R /INTUC1R /INTIIC0	CSIF1 reception completion/ CSIF1 reception error /UARTC1 reception completion/UARTC1 reception error/IIC0 transfer completion	CSIF1 /UARTC1 /IIC0	CF1RIC /UC1RIC /IICIC0	√	√
		70	INTCF1T /INTUC1T	CSIF1 continuous transfer write enable/ UARTC1 continuous transfer write enable	CSIF1 /UARTC1	CF1TIC /UC1TIC	√	√
		71	INTCF2R /INTUC0R	CSIF2 reception completion/CSIF2 reception error/UARTC0 reception completion/UARTC0 reception error	CSIF2 /UARTC0	CF2RIC /UC0RIC	√	√
		72	INTCF2T /INTUC0T	CSIF2 continuous transfer write enable/UARTC0 continuous transfer write enable	CSIF2 /UARTC0	CF2TIC /UC0TIC	√	√
		73	INTCF3R /INTUB1TIR	CSIF3 reception completion/CSIF3 reception error/UARTB1 reception completion	CSIF3 /UARTB1	CF3RIC /UB1TIRIC	√	√
		74	INTCF3T /INTUB1TIT	CSIF3 continuous transfer write enable/UARTB1 transfer completion	CSIF3 /UARTB1	CF3TIC /UB1TITIC	√	√
		75	INTUB1TIF	UARTB1 FIFO transfer completion	UARTB1	UB1TIFIC	√	√
		76	INTUB1TIRE	UARTB1 reception error	UARTB1	UB1TIREIC	√	√
		77	INTUB1TITO	UARTB1 reception timeout	UARTB1	UB1TITOIC	√	√
		78	INTCF4R /INTUB0TIR	CSIF4 reception completion/CSIF4 reception error/UARTB0 reception completion	CSIF4 /UARTB0	CF4RIC /UB0TIRIC	√	√
		79	INTCF4T /INTUB0TIT	CSIF4 continuous transfer write enable/UARTB0 transfer completion	CSIF4 /UARTB0	CF4TIC /UB0TITIC	√	√
		80	INTUB0TIF	UARTB0 FIFO transfer completion	UARTB0	UB0TIFIC	√	√
		81	INTUB0TIRE	UARTB0 reception error	UARTB0	UB0TIREIC	√	√
		82	INTUB0TITO	UARTB0 reception timeout	UARTB0	UB0TITOIC	√	√
		83	INTCF5R /INTUC6R	CSIF5 reception completion/CSIF5 reception error/UARTC6 reception completion/UARTC6 reception error	CSIF5 /UARTC6	CF5RIC /UC6RIC	–	√
		84	INTCF5T /INTUC6T	CSIF5 continuous transfer write enable/UARTC6 continuous transfer write enable	CSIF5 /UARTC6	CF5TIC /UC6TIC	–	√
		85	INTCF6R /INTUC7R	CSIF6 reception completion/CSIF6 reception error/UARTC7 reception completion/UARTC7 reception error	CSIF6 /UARTC7	CF6RIC /UC7RIC	–	√
		86	INTCF6T /INTUC7T	CSIF6 continuous transfer write enable/UARTC7 continuous transfer write enable	CSIF6 /UARTC7	CF6TIC /UC7TIC	–	√
		87	INTUC2R /INTIIC2	UARTC2 reception completion/UARTC2 reception error/IIC2 transfer completion	UARTC2 /IIC2	UC2RIC /IICIC2	√	√
		88	INTUC2T	UARTC2 continuous transfer write enable	UARTC2	UC2TIC	√	√
		89	INTIIC4	IIC4 transfer completion	IIC4	IICIC4	–	√
		90	INTAD	A/D converter completion	A/D	ADIC	√	√

Table 25-1. Interrupt/Exception Source List (4/4)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Interrupt Control Register	V850ES/JH3-E	V850ES/JJ3-E
Maskable	Interrupt	91	INTDMA0	DMA0 transfer completion	DMA	DMAIC0	√	√
		92	INTDMA1	DMA1 transfer completion	DMA	DMAIC1	√	√
		93	INTDMA2	DMA2 transfer completion	DMA	DMAIC2	√	√
		94	INTDMA3	DMA3 transfer completion	DMA	DMAIC3	√	√
		95	INTKR	Key return interrupt	KR	KRIC	√	√
		96	INTRTC0	RTC fixed-cycle signal	RTC	RTC0IC	√	√
		97	INTRTC1	RTC alarm match	RTC	RTC1IC	√	√
		98	INTRTC2	RTC interval signal	RTC	RTC2IC	√	√
		99	INTUSBF0	USBF interrupt	USBF	UFIC0	√	√
		100	INTUSBF1	USBF resume interrupt	USBF	UFIC1	√	√
		101	INTETMRX	Packet reception	Ethernet	ETMRXIC	√	√
		102	INTETMTX	Packet transmission	Ethernet	ETMTXIC	√	√
		103	INTETMRQ	Received packet read request	Ethernet	ETMRQIC	√	√
		104	INTETMFS	FIFO status	Ethernet	ETMFSIC	√	√
		105	INTETMTS	Transmission status	Ethernet	ETMTSIC	√	√
		106	INTETMRS	Reception status	Ethernet	ETMRSIC	√	√
		107	INTETMOV	Statistic counter overflow	Ethernet	ETMOVIC	√	√
		108	INTETBER	Error interrupt	Ethernet	ETBERIC	√	√
		110	INTC0ERR	CAN0 error	CAN0	ERRIC0	√Note 1	√Note 2
		111	INTC0WUP1	CAN0 wakeup	CAN0	WUPIC0	√Note 1	√Note 2
		112	INTC0REC	CAN0 reception	CAN0	RECIC0	√Note 1	√Note 2
		113	INTC0TRX	CAN0 transmission	CAN0	TRXIC0	√Note 1	√Note 2

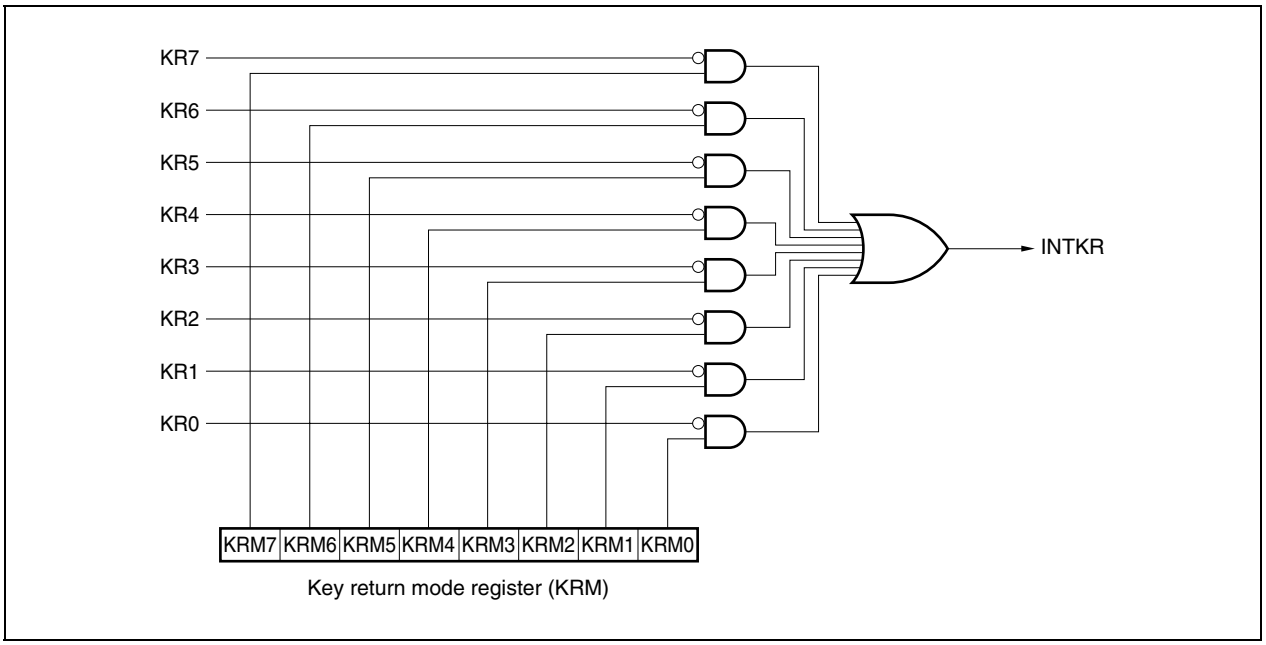
Notes 1. μPD70F3783 only

2. μPD70F3786 only

26. KEY INTERRUPT FUNCTION

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7).

The following figure shows the configuration of key interrupt.



27. STANDBY FUNCTION

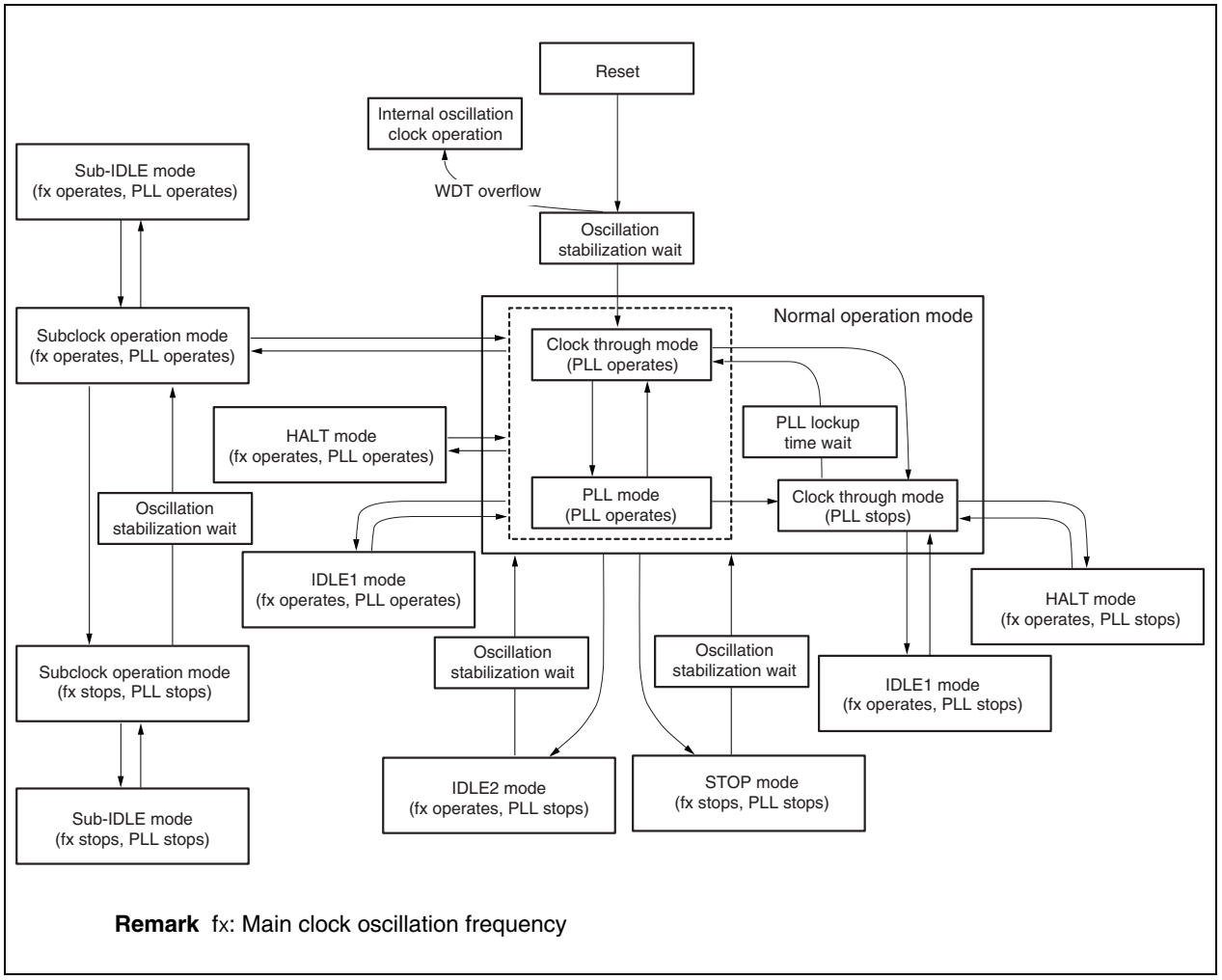
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 27-1.

Table 27-1. Standby Modes

Mode	Function Overview
HALT mode	Mode to stop only the operating clock of the CPU
IDLE1 mode	Mode to stop all the operations of the internal circuit except the oscillator, PLL operation[Note], and flash memory
IDLE2 mode	Mode to stop all the operations of the internal circuit except the oscillator
STOP mode	Mode to stop all the operations of the internal circuit except the subclock oscillator
Subclock operation mode	Mode to operate internal system clock by subclock
Sub-IDLE mode	Mode to stop all the operations of the internal circuit except the oscillator in subclock operation mode

Note PLL retains the previous operation status.

The following figure shows the status transitions of the standby function.



Remark fx: Main clock oscillation frequency

28. RESET FUNCTIONS

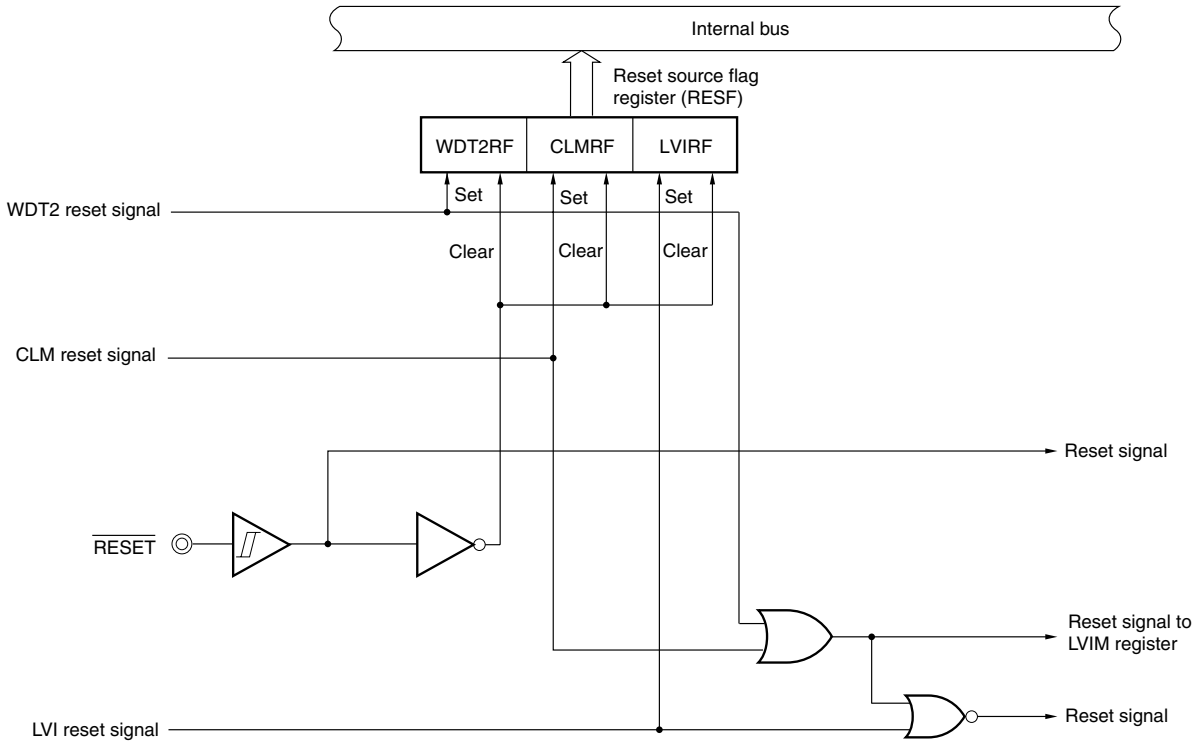
The following reset functions are available.

(1) Four types of reset sources
- External reset input via the $\overline{\text{RESET}}$ pin
- Reset via the watchdog timer 2 (WDT2) overflow (WDT2RES)
- System reset by comparing the supply voltage and detection voltage by using the low-voltage detector (LVI)
- System reset by the clock monitor (CLM) upon detection of oscillation stop

After a reset is released, the source of the reset can be confirmed with the reset source flag register (RESF).

(2) Emergency operation mode
If the WDT2 overflows during the main clock oscillation stabilization time inserted after reset, a main clock oscillation anomaly is judged and the CPU starts operating on the internal oscillation clock.

The outline of the reset functions is shown below.



Remark LVIM: Low-voltage detection register

29. CLOCK MONITOR, LOW-VOLTAGE DETECTOR

(1) Clock monitor

The clock monitor samples the main clock by using the internal oscillation clock (f_R) and generates a reset request signal when oscillation of the main clock is stopped.

(2) Low-voltage detector

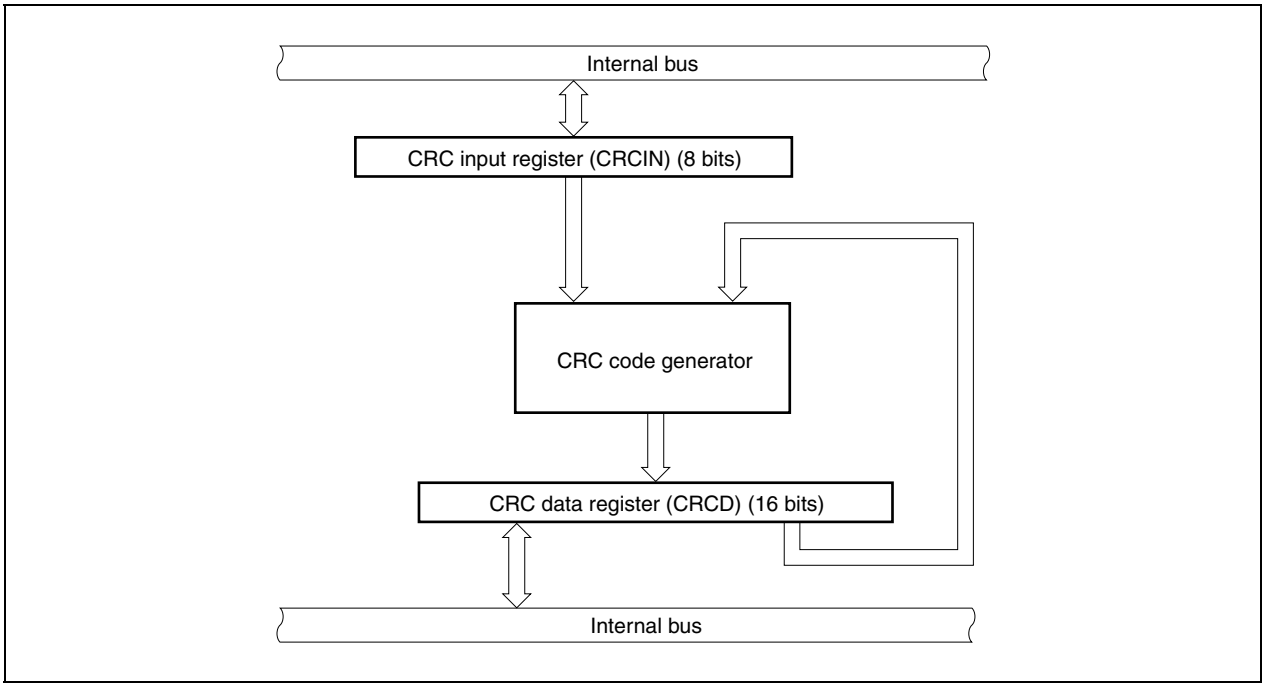
The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in STOP mode.
- Operation can be stopped by software.

30. CRC FUNCTIONS

The outline of the CRC function is shown below.

- CRC operation circuit for detection of data block errors
- Generation of 16-bit CRC code using a CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) generation polynomial for blocks of data of any length in 8-bit units
- CRC code is set to the CRCD data register each time 1-byte data is transferred to the CRCIN register, after the initial value is set to the CRCD register.

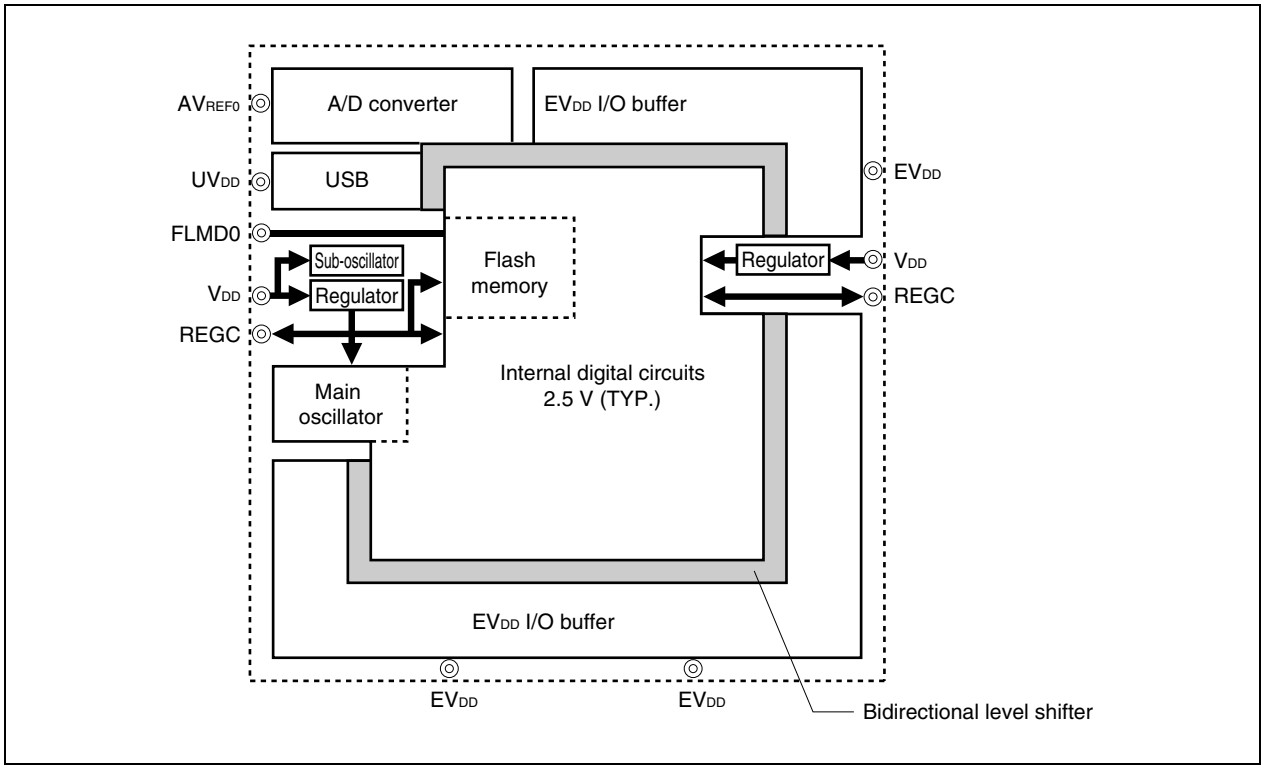


31. REGULATOR FUNCTION

The V850ES/Jx3-E includes a regulator to reduce power consumption and noise.

This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits except the A/D converter and output buffers). The regulator output voltage is set to 2.5 V (TYP.).

The outline of the regulator functions is shown below.



32. FLASH MEMORY

Flash memory versions offer the following advantages for development environments and mass production applications.

- For altering software after the V850ES/Jx3-E is soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

The flash memory in the V850ES/Jx3-E has the following features.

- 4-byte/1-clock access (when instruction is fetched)
- Capacity: 256/384/512 KB
- Rewrite voltage: Erase/write with a single power supply
- Rewriting method
  - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Flash memory write prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

33. ON-CHIP DEBUG FUNCTION

Debugging can be implemented with the V850ES/Jx3-E mounted on the target system.

The NEC Electronics on-chip debug emulators MINICUBE and MINICUBE2 are planned to support the V850ES/Jx3-E.

○ MINICUBE

An on-chip debug function is implemented by using the DCU (debug control unit) in the V850ES/Jx3-E, using the $\overline{\text{DRST}}$, DCK, DMS, DDI, and DDO pins as the debug interface pins.

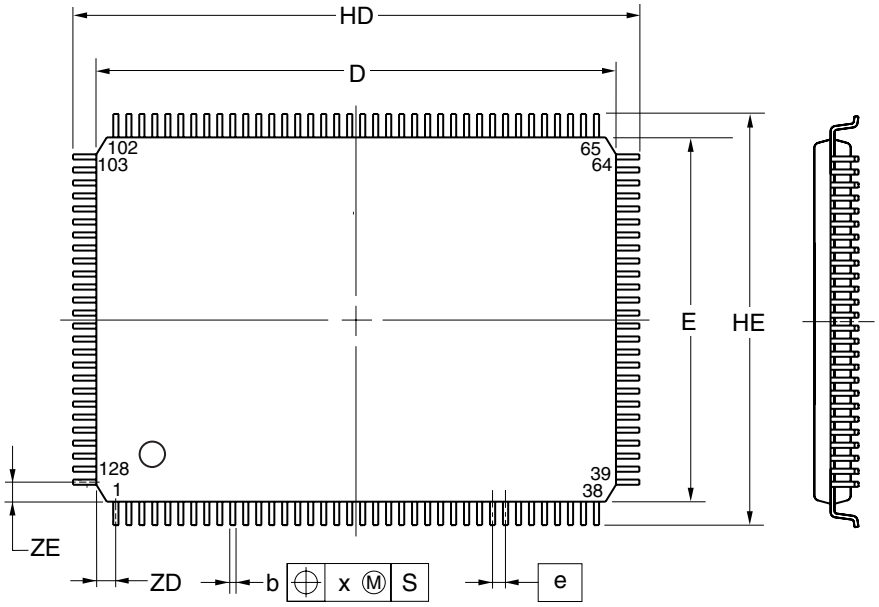
○ MINICUBE2

An on-chip debug function is implemented by using the user resources (on-chip flash memory, internal RAM, etc.) instead of the DCU, and using the SIF0, SOF0, and $\overline{\text{SCKF0}}$ pins or the SIF3, SOF3, and $\overline{\text{SCKF3}}$ pins or the RXDC0 and TXDC0 pins as the interface pins.

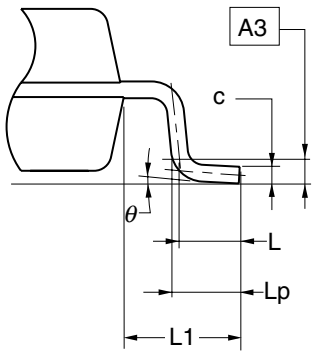
34. PACKAGE DRAWINGS

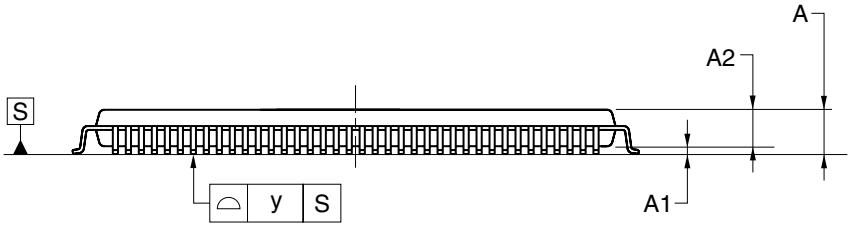
- V850ES/JH3-E

128-PIN PLASTIC LQFP (FINE PITCH) (14x20)



detail of lead end





NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

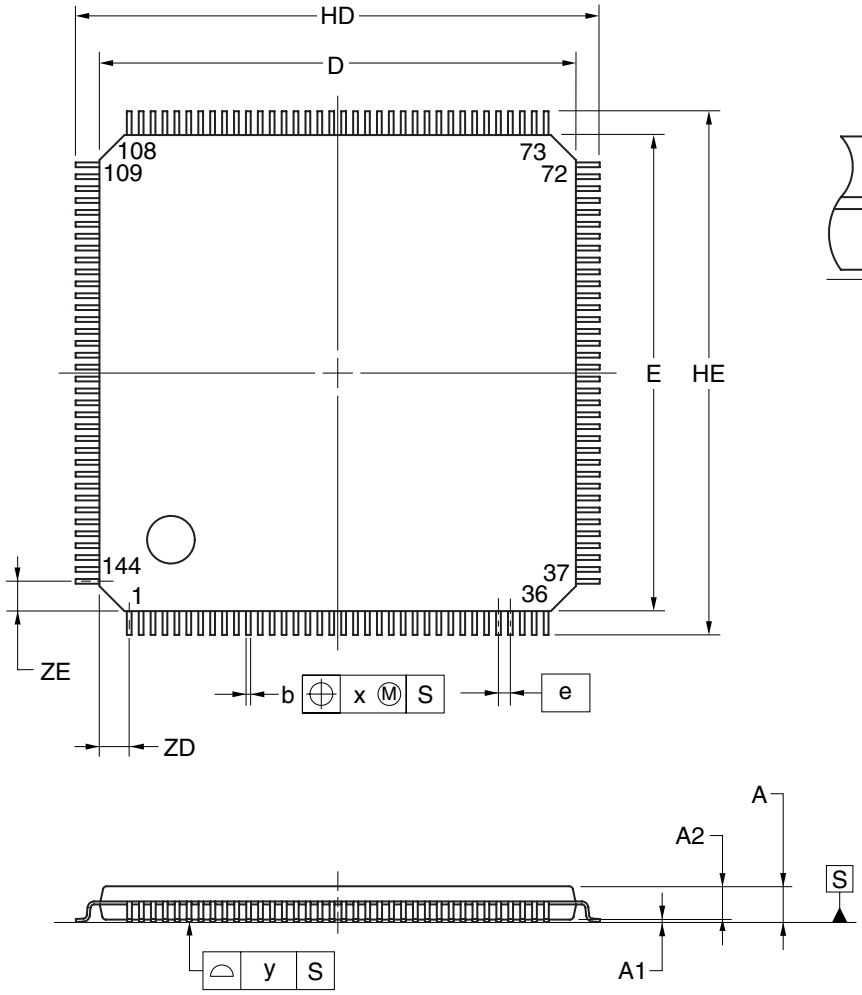
(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

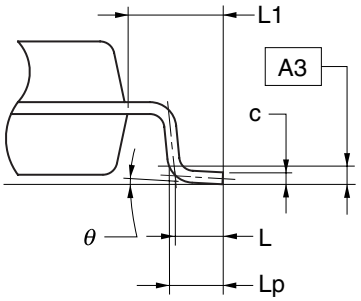
P128GF-50-GAT

- V850ES/JJ3-E

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	20.00±0.20
HD	22.00±0.20
HE	22.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P144GJ-50-GAE-2

APPENDIX A. DEVELOPMENT TOOLS

(1) Hardware

Product Name		Description
Full-function in-circuit emulator (IECUBE®)	QB-V850ESJX3E[Note 1, 2]	In-circuit emulator for V850ES/Jx3-E
On-chip debug emulator (MINICUBE)	QB-V850MINI[Note 1]	Emulator for on-chip debugging
On-chip emulator with programming function (MINICUBE2)	QB-MINI2[Note 1]	Emulator for on-chip debugging. Also used as a programmer.
Flash programmer (Flash Pro V)	PG-FP5[Note 1]	Flash programmer for writing programs to products with a single-power supply flash memory

Notes 1. Under development

2. Tentative name

(2) Software

Product Name		Description
Compiler	CA850[Note]	C compiler conforming to ANSI-C standards
Debugger	ID850QB[Note]	Used in combination with in-circuit emulator
Real-time OS	RX850[Note], RX850 Pro[Note]	Real-time OS conforming to μITRON specifications
Project Manager	PM+[Note]	Integrated development environment platform
Device file	DF703786[Note]	Definition file for V850ES/Jx3-E

Note Under development

APPENDIX B. COMPARISON BETWEEN V850ES/Jx3-E AND V850ES/Jx3-H

Table B-1. Major Differences Between V850ES/Jx3-E and V850ES/Jx3-H

Major Difference	V850ES/Jx3-E	V850ES/Jx3-H
Minimum instruction execution time	20 ns (50 MHz operation)	20.8 ns (48 MHz operation)
Max RAM size	60 KB + 64 KB[Note]	48 KB + 8 KB[Note]
D/A controller	None	Available
USB interface	Function only	Function/host
Ethernet controller	Available	None
Asynchronous serial interface	UARTC: 6/8 channels	UARTC: 5 channels
	UARTB (UART with FIFO function): 2 channels	None
Clock serial interface	CSIE (CSI with FIFO function): 2 channels	None
I^2C	4/5 channels	3 channels

Note Data RAM.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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