Panasonic

NN30295A

VIN = 4.5 V to 5.6 V, 6 A Synchronous DC-DC Step down Regulator comprising of Controller IC and Power MOSFET with I²C Interface

FEATURES

- High-Speed Response DC-DC Step Down Regulator Circuit that employs Hysteretic Control System
- Two 25 mΩ (Typ.) MOSFETs for High Efficiency at 6 A
- Mode Selection Option via I²C:
  (1) Pulse Skip Mode (PSM) with coast mode function for high light load efficiency
  (2) Forced Continuous Conduction Mode (FCCM) for quick load transient response
- Up to 6 A Output Current
- Input VoltageRange : AVIN : 4.5 V to 5.6 V, PVIN : 3.1 V to 5.6 V, VDD : 1.7 V to 3.6 V
  Output Voltage Range : 0.6 V to 3.5 V
  Selectable Switching Frequency 500 kHz to 2 MHz (7 steps) using I²C : Default 1MHz
- Adjustable Soft Start
- Low Operating and Standby Quiescent Current
- Open Drain Power Good Indication for Output Over , Under Voltage
- Built-in Under Voltage Lockout (UVLO), Thermal Shut Down (TSD), Over Voltage Detection (OVD), Under Voltage Detection (UVD), Over Current Protection (OCP), Short Circuit Protection (SCP)
- HQFN024-A3-0404A (Size : 4 mm X 4 mm, 0.5 mm pitch), 24pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)

DESCRIPTION

NN30295A is a synchronous DC-DC Step down Regulator (1-ch) comprising of a Controller IC and two power MOSFETs and employs the hysteretic control system.

By this system, when load current changes suddenly, it responds at high speed and minimizes the changes of output voltage.

Since it is possible to use capacitors with small capacitance and it is unnecessary to add external parts for system phase compensation, this IC realizes downsizing of set and reducing in the number of external parts. Output voltage is adjustable by user.

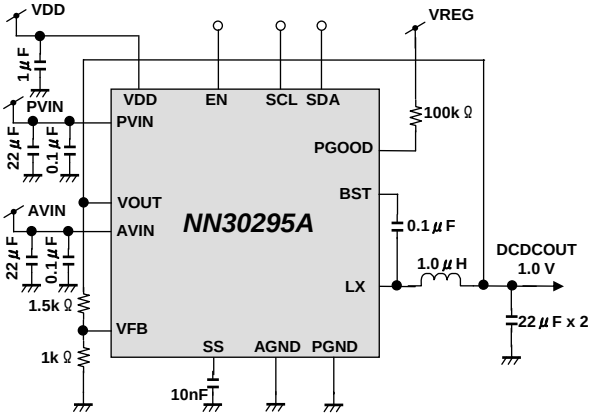
Maximum current is 6 A.

APPLICATIONS

High Current Distributed Power Systems such as

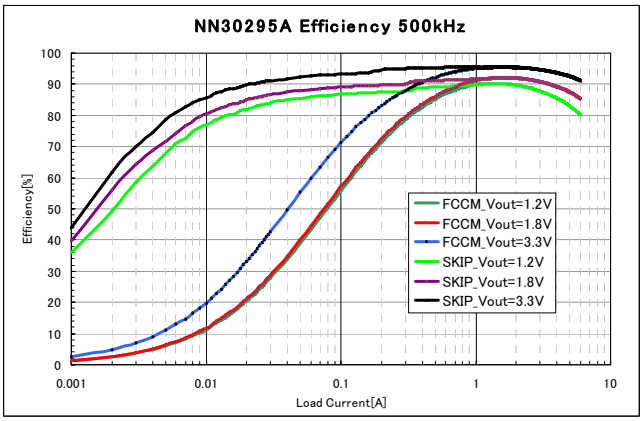
- HDDs (Hard Disk Drives)
- SSDs (Solid State Drives)
- PCs
- Game consoles
- Servers
- Security Cameras
- Network TVs
- Home Appliances
- OA Equipment etc.

SIMPLIFIED APPLICATION



Notes) This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

EFFICIENCY CURVE



Condition)

V_{IN} = 5.0 V, Vout = 1.2 V , 1.8 V , 3.3 V,
Lo = 1 µH, Co = 44 µF (22 µF x 2), Frequency = 500 kHz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{IN}	6.0	V	*1
	VDD	3.6	V	*1
Operating free-air temperature	T_{opr}	– 40 to + 85	°C	*2
Operating junction temperature	T_j	– 40 to + 150	°C	*2
Storage temperature	T_{stg}	– 55 to + 150	°C	*2
Input Voltage Range	EN,VFB,VOUT	-0.3 to (V_{IN} + 0.3)	V	*1, *3
	SCL,SDA	-0.3 to (VDD + 0.3)	V	*1, *3
Output Voltage Range	LX,PGOOD	-0.3 to (V_{IN} + 0.3)	V	*1, *3
ESD	HBM (Human Body Model)	2	kV	—

Notes) Do not apply external currents and voltages to any pin not specifically mentioned.

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1:The values under the condition not exceeding the above absolute maximum ratings and the power dissipation. V_{IN} is voltage for AVIN, PVIN. VDD is voltage for VDD.

*2:Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C.

*3:(V_{IN} + 0.3) V must not exceed 6 V. (VDD + 0.3) V must not be exceeded 3.6 V.

■ POWER DISSIPATION RATING

PACKAGE	θ_{JA}	PD (Ta = 25 °C)	PD (Ta = 85 °C)	Notes
24 pin Plastic Quad Flat Non-leaded Package Heat Slug Down (QFN Type)	61.6 °C / W	2.03 W	1.06 W	*1

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1:Glass Epoxy Substrate (4 Layers) [Glass-Epoxy: 50 X 50 X 0.8 t (mm)], Die Pad Exposed , Soldered.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it.
Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	AVIN	4.5	5.0	5.6	V	—
	PVIN	3.1	5.0	5.6	V	—
	VDD	1.7	1.85	3.3	V	—
Input Voltage Range	EN	– 0.3	—	V_{IN} + 0.3	V	*1
	SDA	– 0.3	—	VDD + 0.3	V	*1
	SCL	– 0.3	—	VDD + 0.3	V	*1
Output Voltage Range	LX	– 0.3	—	V_{IN} + 0.3	V	*1
	PGOOD	– 0.3	—	V_{IN} + 0.3	V	*1

Note) Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND. AGND = PGND
Vin is voltage for AVIN, PVIN. AVIN = PVIN.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*1 : (V_{IN} + 0.3) V must not be exceeded 6 V. (VDD + 0.3) V must not be exceeded 3.6 V.

ELECRTRICAL CHARACTERISTICS

Co = 22 µF X 2, Lo= 1 µH, VOUT Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = Low (Skip), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Consumption current at active	I_{VDDACT}	CTL1 = 5 V, I_{OUT} = 0 A RFB1 = 1.0 kΩ RFB2 = 1.5 kΩ	—	400	700	µA	—
Consumption current at standby	I_{VDDSTB}	EN = 0 V, I_{OUT} = 0 A	—	—	2	µA	—
Enable Pin Characteristics							
EN pin Low-level input voltage	V_{EN1L}	—	– 0.3	—	0.3	V	—
EN pin High-level input voltage	V_{EN1H}	—	1.5	—	V_{IN} + 0.3	V	—
EN pin leak current	$I_{LEAKEN1}$	EN = 5 V	—	3.5	10.0	µA	—
Internal Reference Characteristics							
VFB comparator threshold	V_{FBTS}	—	0.595	0.603	0.611	V	—
Under Voltage Lock Out							
PVIN UVLO start voltage 1	$V_{UVLODET1}$	PV_{IN} = 5 V to 0 V	2.45	2.60	2.75	V	—
PVIN UVLO recover voltage 1	$V_{UVLOHYS1}$	PV_{IN} = 0 V to 5 V	50	200	350	mV	—
AVIN UVLO start voltage 2	$V_{UVLODET2}$	AV_{IN} = 5 V to 0 V	3.25	3.40	3.55	V	—
AVIN UVLO recover voltage 2	$V_{UVLOHYS2}$	AV_{IN} = 0 V to 5 V	10	100	250	mV	—
VDD UVLO start voltage 2	$V_{UVLODET3}$	VDD = 3 V to 0 V	1.00	1.25	1.50	V	—
VDD UVLO recover voltage 2	$V_{UVLOHYS3}$	VDD = 0 V to 3 V	10	50	90	mV	—
PGOOD Pin Characteristics							
PGOOD Threshold 1 (VFB ratio for UVD detect)	V_{THPG1}	PGOOD : High to Low	78	85	92	%	—
PGOOD Hysteresis 1 (UVD Hysteresis)	V_{HYSPG1}	PGOOD : Low to High	2	5	8	%	—
PGOOD Threshold 2 (VFB ratio for OVD detect)	V_{THPG2}	PGOOD : High to Low	108	115	122	%	—
PGOOD Hysteresis 2 (OVD Hysteresis)	V_{HYSPG2}	PGOOD : Low to High	2	5	8	%	—
PGOOD ON resistance	RPG	EN = 0 V	—	10	15	Ω	—

ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 2, Lo= 1 µH, VOUT Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = Low (Skip), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
DC-DC Characteristics							
DC-DC line regulation	DDREGIN	PVIN = 4.5 V to 5.6 V I_{OUT} = – 1.5 A	—	0.5	1.5	%/V	—
DC-DC load regulation	DDREGLD	I_{OUT} = – 10 mA to – 6 A	—	3	—	%	*1
DC-DC output current limit	DDILMT	—	—	9.0	—	A	*1
DC-DC efficiency 1	DDEFF1	I_{OUT} = – 10 mA	—	70	—	%	*1
DC-DC efficiency 2	DDEFF2	I_{OUT} = – 4 A	—	81	—	%	*1
DC-DC output ripple voltage 1	DDVRPL1	I_{OUT} = – 10 mA	—	25	—	mV [p-p]	*1
DC-DC output ripple voltage 2	DDVRPL2	I_{OUT} = – 4 A	—	10	—	mV [p-p]	*1
DC-DC load transient response	DDDVAC	I_{OUT} = – 100 mA ↔ – 4 A Δt = 0.5 A / µs	—	20	—	mV	*1
DC-DC High Side MOS ON resistance	DDRONH	VGS = 5 V	—	25	50	mΩ	—
DC-DC Low Side MOS ON resistance	DDRONL	VGS = 5 V	—	25	50	mΩ	—
PROTECTION							
DC-DC Output GND Short Protection Threshold	DDSHPTH	FB = 0.6 V to 0.0 V	55	70	85	%	—

*1 : Typical Value checked by design.

ELECRTRICAL CHARACTERISTICS (Continued)

Co = 22 µF X 2, Lo= 1 µH, VOUT Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = Low (Skip), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Soft-Start Timing							
SS Charge Current	ISSCHG	V_{SS} = 0.3 V	– 4	– 2	—	µA	—
SS Discharge Resistance (Shut-down)	RSSDIS	EN = 0 V, I_{OUT} = 0 A	—	2	4	kΩ	—
Switching Frequency Adjustment							
DC-DC Switching Frequency 1	DDFSW1	I_{OUT} = – 6 A I2C Setting: 10h:10h	—	500	—	kHz	*1
DC-DC Switching Frequency 2	DDFSW2	I_{OUT} = – 6 A I2C Setting: 10h:30h	—	1000	—	kHz	*1
DC-DC Switching Frequency 3	DDFSW3	I_{OUT} = – 6 A I2C Setting: 10h:70h	—	2000	—	kHz	*1
Soft-Start Timing							
VFB pin leak current 1	ILEAKFB1	VFB = 0 V	– 1	—	1	µA	—
VFB pin leak current 2	ILEAKFB2	VFB = 3.6 V	– 1	—	1	µA	—
DC-DC							
MIN Input and output voltage difference	DV	DV = PVIN – VOUT	—	2	—	V	*1

*1 : Typical Value checked by design.

APPLICATION INFORMATION

REFERENCE VALUES FOR DESIGN

Co = 22 µF X 2, Lo= 1 µH, VOUT Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = Low (Skip), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Reference Values			Unit	Note
			Min	Typ	Max		
I²C Bus (Internal I/O Stage Characteristics)							
Low-level input voltage	VIL1	Voltage which recognized that SDA and SCL are Low-level	–0.5	—	0.3× VDD	V	*1
High-level input voltage	VIH1	Voltage which recognized that SDA and SCL are High-level	0.7× VDD	—	VDD_{max} +0.5	V	*1
Low-level output voltage 1	VOL1	VDD > 2 V SDA (sink current=3 mA)	0	—	0.4	V	—
Low-level output voltage 2	VOL2	VDD < 2 V SDA (sink current=3 mA)	0	—	0.2× VDD	V	—
Input current each I/O pin	IL	SDA, SCL = 0.1 × VDD_{max} to 0.9 × VDD_{max}	–10	—	10	µA	—
SCL clock frequency	FOSC	—	0	—	400	kHz	—
Hysteresis of Schmitt trigger input 1	Vhys1	V_{IO} > 2 V, Hysteresis 1 of SDA, SCL	0.05× VDD	—	—	V	*2
Hysteresis of Schmitt trigger input 2	Vhys2	V_{IO} < 2 V, Hysteresis 2 of SDA, SCL	0.1× VDD	—	—	V	*2
Output fall time from V_{IHmin} to V_{ILmax}	Tof	Bus capacitance : 10pF to 400pF I_P ≤ 6 mA, (V_{OLmax} = 0.6 V) I_P : Max. sink current	20+ 0.1×C_b	—	250	ns	*2
Pulse width of spikes which must be suppressed by the input filter	Tsp	—	0	—	50	ns	*2
Capacitance for each I/O pin	Ci	—	—	—	10	pF	*2

Note) Checked by design, not production tested.

*1 : The input threshold voltage of I²C bus (Vth) is linked to VDD.

In case the pull-up voltage is not VDD, the threshold voltage (Vth) is fixed to ((VDD / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.

In this case, pay attention to Low-level (max.) value (V_{ILmax}).

It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

*2 : The timing of Fast-mode devices in I2C-bus is specified as the following. All values referred to VIHmin and VILmax level.

APPLICATION INFORMATION (Continued)

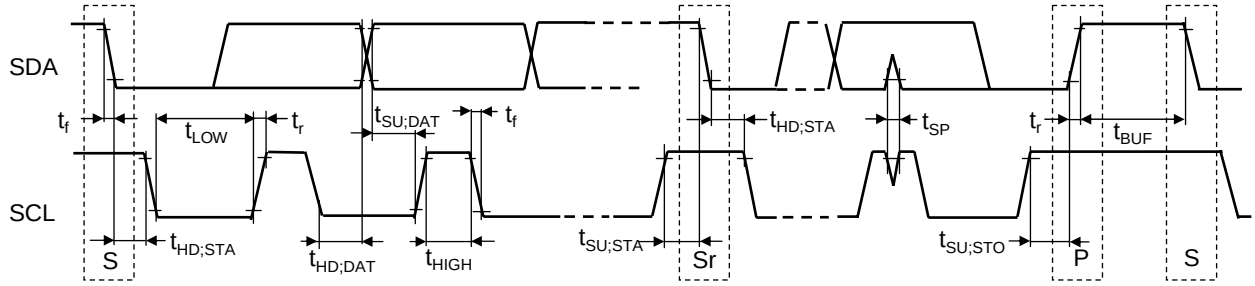
REFERENCE VALUES FOR DESIGN

Co = 22 µF X 2, Lo= 1 µH, VOUT Setting = 1.0 V, V_{IN} = AV_{IN} = PV_{IN} = 5 V, Switching Frequency = 1 MHz, MODE = Low (Skip), T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Reference Values			Unit	Note
			Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA}$.	0.6	—	—	µs	*3
Low period of the SCL clock	t_{LOW}	—	1.3	—	—	µs	*3
High period of the SCL clock	t_{HIGH}	—	0.6	—	—	µs	*3
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.6	—	—	µs	*3
Data hold time	$t_{HD:DAT}$	—	0	—	0.9	µs	*3
Data set-up time	$t_{SU:DAT}$	—	100	—	—	ns	*3
Rise time of both SDA and SCL signals	t_r	—	20+ 0.1×C_b	—	300	ns	*3
Fall time of both SDA and SCL signals	t_f	—	20+ 0.1×C_b	—	300	ns	*3
Set-up time of STOP condition	$t_{SU:STO}$	—	0.6	—	—	µs	*3
Bus free time between STOP and START condition	t_{BUF}	—	1.3	—	—	µs	*3
Capacitive load for each bus line	C_b	—	—	—	400	pF	*3
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1× VDD	—	—	V	*3
Noise margin at the High-level for each connected device	V_{nH}	—	0.2× VDD	—	—	V	*3

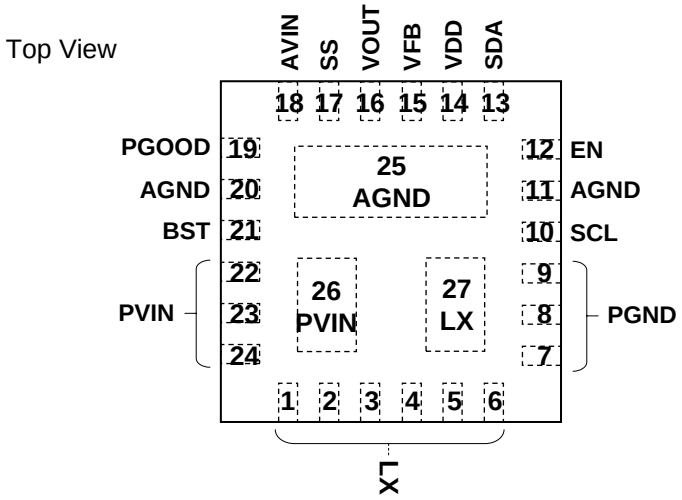
Note) Checked by design, not production tested.

*3 : The timing of Fast-mode devices in I²C-bus is specified as the following.
All values referred to V_{IHmin} and V_{ILmax} level.



S : START condition
Sr : Repeat START condition
P : STOP condition

PIN CONFIGURATION

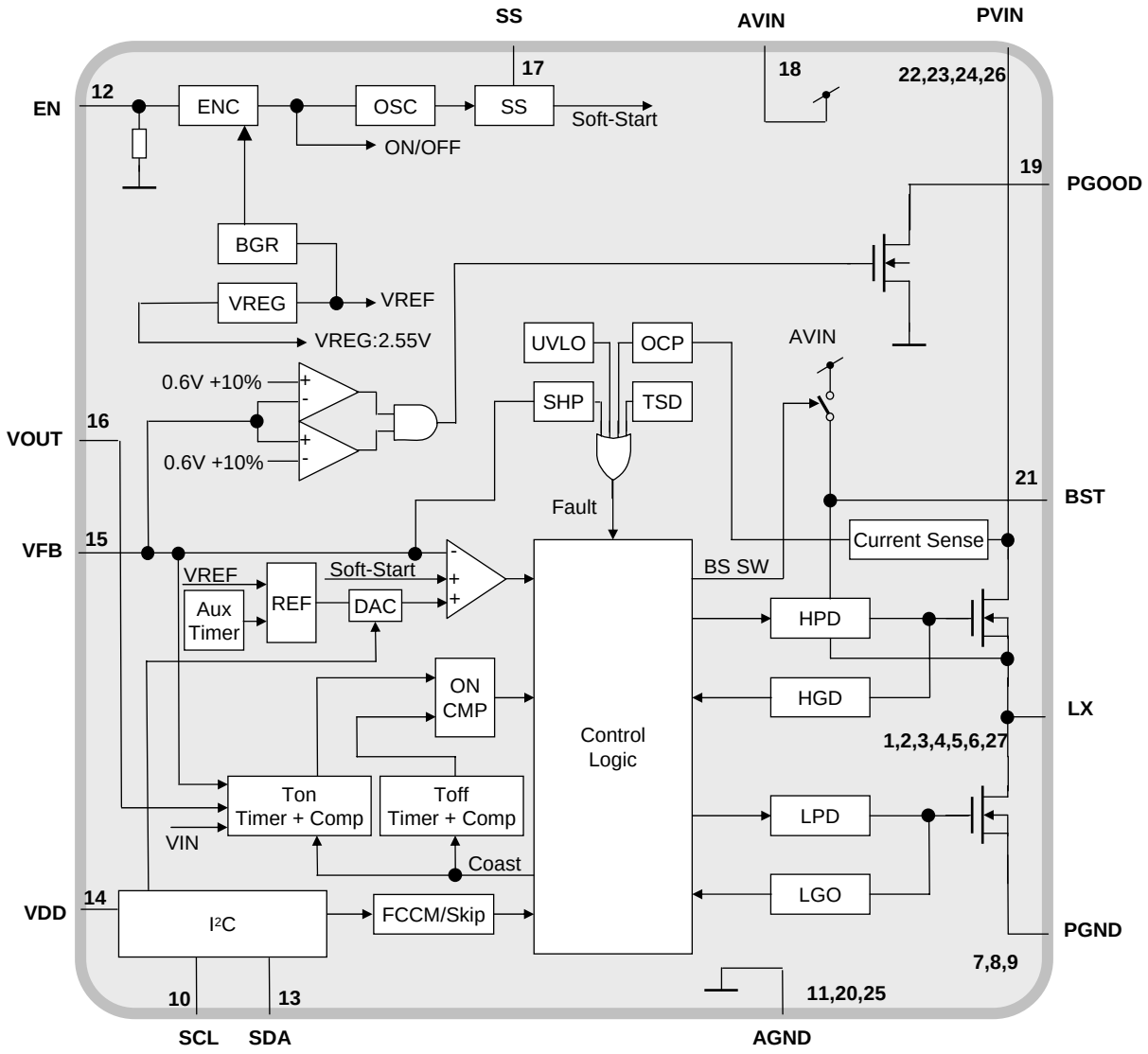


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	LX	Output	Power MOSFET output pin
2			
3			
4			
5			
6			
7	PGND	Ground	Ground pin for Power MOSFET
8			
9			
10	SCL	Input	I^2C Interface Clock Input pin
11	AGND	Ground	Ground pin
12	EN	Input	ON/OFF control pin
13	SDA	Input/Output	I^2C Interface Data I/O pin
14	VDD	Power Supply	Power supply pin for Digital Circuit
15	VFB	Input	Comparator negative input pin
16	VOUT	Input	Output voltage sense pin
17	SS	Output	Soft start capacitor connect pin
18	AVIN	Power supply	Power supply pin
19	PGOOD	Output	Power good open drain pin
20	AGND	Ground	Ground pin
21	BST	Output	Supply input pin for high side FET gate driver
22	PVIN	Power supply	Power supply pin for Power MOSFET
23			
24			
25	AGND	Ground	Ground pin for radiation of heat
26	PVIN	Power supply	Power supply pin for radiation of heat
27	LX	Output	Power MOSFET output pin for radiation of heat

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Notes) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

1. Protection

(1).Output Over-Current Protection (OCP) function And Short-Circuit Protection (SCP) function

1) The Over Current Protection is activated at about 9 A (Typ.) During the OCP, the output voltage continues to drop at the specified current.
2) The Short-Circuit Protection function is implemented when the output voltage decreases and the VFB pin reaches to about 70 % of the set voltage of 0.6 V.
3) The SCP operates intermittently at 2 ms-ON, 16 ms OFF intervals.

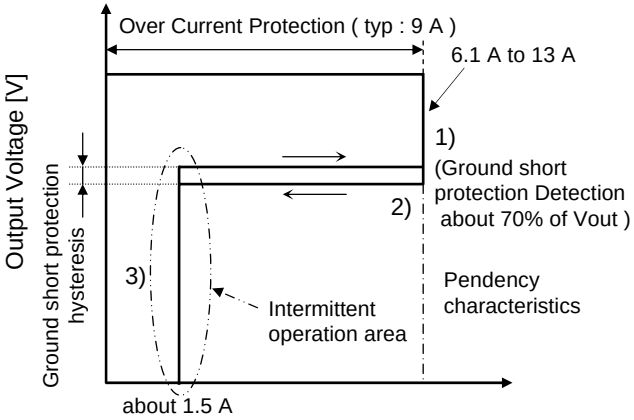


Figure : OCP and SCP Operation

(2).Over Voltage Detection (OVD) and Under Voltage Detection (UVD)

1).The NMOS connected to the PGOOD pin turns ON when the output voltage rises and the VFB pin voltage reaches 115 % of its set voltage (0.6 V).
2).After (1) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 110 % of its set voltage (0.6 V).
3).The NMOS connected to the PGOOD pin turns ON when the output voltage drops and the VFB pin voltage reaches 85 % of its set voltage (0.6 V).
4).After (3) above, the NMOS connected to the PGOOD pin is turned OFF after 1 ms when the output voltage drops and the VFB pin voltage reaches 90 % of its set voltage (0.6 V).

(3).Thermal Shut Down (TSD)

When the IC internal temperature becomes more than about 140 °C, TSD operates and DCDC turns off.

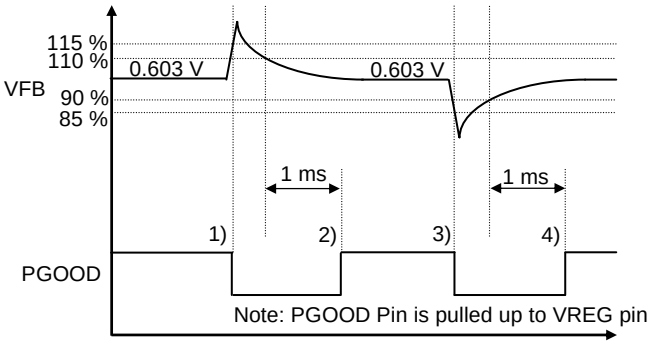
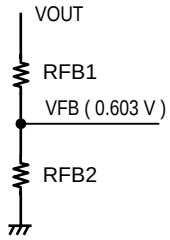


Figure : OVD and UVD Operation

2. Output Voltage Setting

The Output Voltage is set by adjusting the value of the external resistors RFB1 and RFB2. The equation below represents the relation between the external resistors and VOUT.

(VIN = 5V, IOUT = – 1 A, FCCM, Fsw = 1 MHz)



$$VOUT = -0.0119\left(\frac{RFB1}{RFB2}\right)^2 + 0.616\left(\frac{RFB1}{RFB2}\right) + 0.593$$

The following table represents the Feedback Resistor setting (RFB) Below resistors are recommended for following popular output voltage.

VOUT [V]	RFB1 [Ω]	RFB2 [Ω]
1.8	3.0 k	1.5 k
1.2	1.0 k	1.0 k
1.0	1.0 k	1.5 k

Note: RFB2 can be set to a maximum value of 10 kΩ. A larger FBR2 value will be more susceptible to noise.

VFB comparator threshold is adjusted to ± 1.33 %, but the actual output voltage accuracy becomes more than ± 1.33 % due to the influence from the circuits other than VFB comparator.

In the case of VOUT setting = 1.0 V, the actual output voltage accuracy becomes ± 2 %.

(VIN = 5.0 V, IOUT = – 1 A, Skip Mode, Fsw = 1 MHz).

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

3. Soft Start Setting

Soft Start function maintains the smooth control of the output voltage during start up by adjusting soft start time. When the CTL1 or CTL2 (or both) pin becomes High, the current (2 µA) begin to charge toward the external capacitor (Css) of SS pin, and the voltage of SS pin increases straightly.

Because the voltage of FB pin is controlled by the voltage of SS pin during start up, the voltage of FB increase straightly to the regulation voltage (0.6 V) together with the voltage of SS pin and keep the regulation voltage after that. On the other hand, the voltage of SS pin increase to about 2.8 V and keep the voltage. The calculation of Soft Start Time is as follows.

$$Soft\ Start\ Time(\sec) = \frac{0.6}{2\mu} \times Css$$

When Css is set at 10 nF, soft-start time is approximately 3 ms.

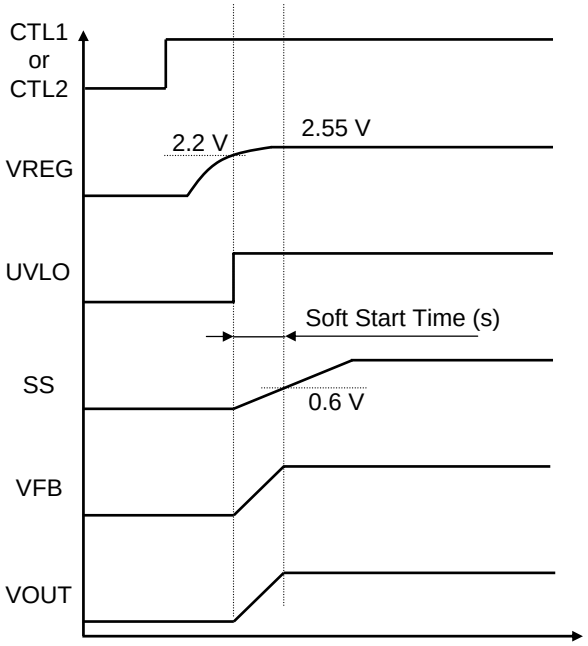


Figure : Soft Start Operation

4. Power ON / OFF sequence

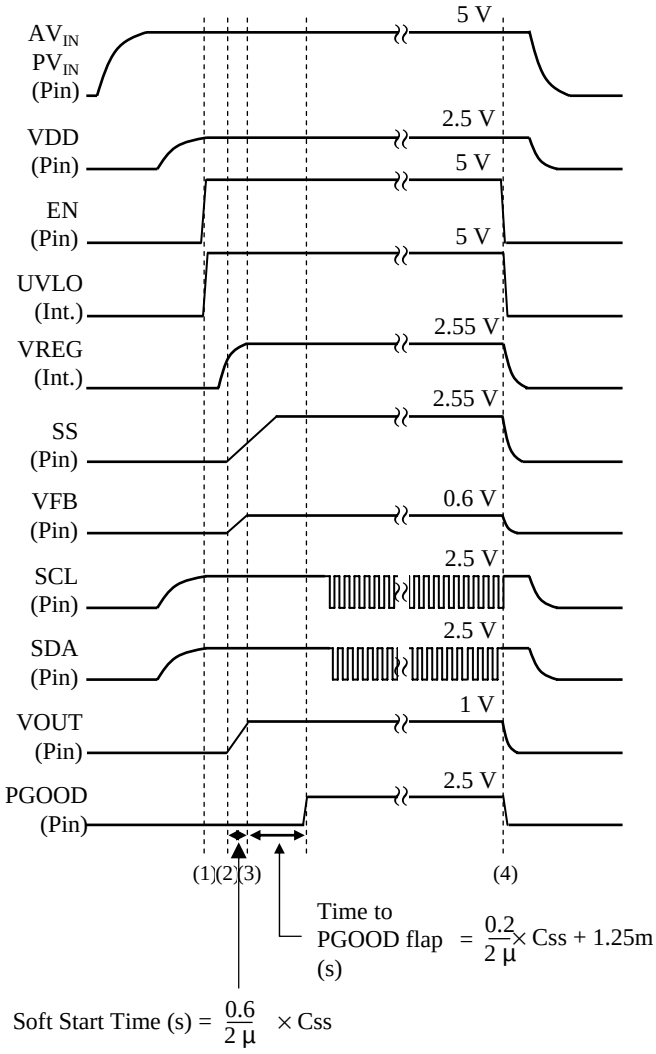
(1) When the EN pin is set to “High” after the VIN settles, UVLO is released if VIN exceeds its threshold, then the VREG starts up.

(2) When VREG voltage exceeds its threshold, the SOFT START sequence is enabled. The capacitor connected to the SS pin begins to charge and the SS pin voltage increases linearly.

(3) The VOUT pin (DCDC Output) voltage increases at the same rate as the SS pin. Normal operation begins after the VOUT pin reaches the set voltage.

(4) When the EN pin is set to “Low”, VREG and UVLO stop operation. The VOUT pin / SS pin voltage drops to 0 V.

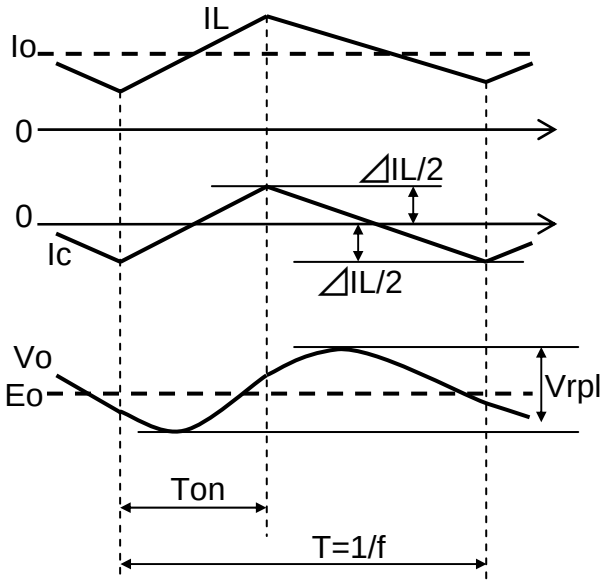
Note: The SS pin capacitor should be discharged completely before restarting the startup sequence. An incomplete discharge process might result in an overshoot of the output voltage.

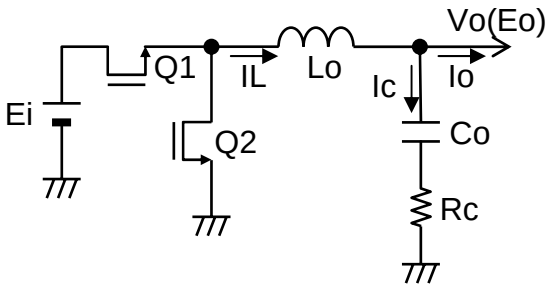


OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

5. Inductor and Output Capacitor Setting





Given the desired input and output voltages, the inductor value and operating frequency determine the ripple Current.

$$\Delta IL = \frac{Eo \cdot (Ei - Eo)}{Ei \cdot Lo \cdot f}$$

$$Iox = \frac{\Delta IL}{2}$$

Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off among component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40 % of IOUT(MAX). The largest ripple current occurs at the highest VIN. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$Lo \geq \frac{Eo \cdot (Ei - Eo)}{2Ei \cdot Iox \cdot f} \quad @\ \mathrm{Ei} = \mathrm{Ei\_max}$$

And its maximum current rating is

$$IL\_\max = \mathrm{Io\_max} + \frac{\Delta IL}{2} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

The selection of COUT is primarily determined by the ESR (Rc) required to minimize voltage ripple and load transients. The output ripple Vrpl is approximately bounded by:

$$Vrpl = Vop - Vob = Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{\Delta IL}{8Co \cdot f}$$

$$= Ei \cdot \frac{Co \cdot Rc^2}{2Lo} + \frac{Eo \cdot (Ei - Eo)}{8Ei \cdot Lo \cdot Co \cdot f^2}$$

From the above equation, to achieve desired output ripple, low ESR ceramic capacitors are recommended, and its required RMS current rating is:

$$Ic(\mathrm{rms})\_\max = \frac{\Delta IL}{2\sqrt{3}} \quad (@\ \mathrm{Ei} = \mathrm{Ei\_max})$$

OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

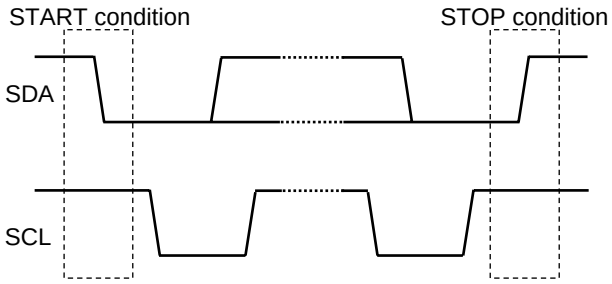
6. I²C-bus Interface

a.) Basic Rules

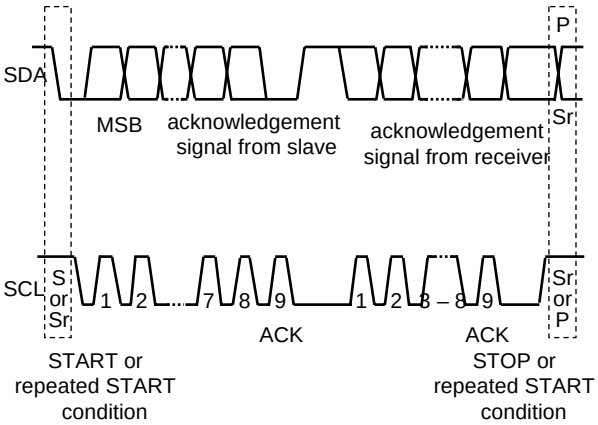
This IC, I2C-bus, is designed to correspond to the Standard-mode (100 kbps) and Fast-mode(400 kbps) devices in the version 2.1 of NXP's specification. However, it does not correspond to the HS-mode (to 3.4 Mbps). This IC will operate as a slave device in the I²C-bus system. This IC will not operate as a master device. The program operation check of this IC has not been conducted on the multi-master bus system and the mix-speed bus system, yet. The connected confirmation of this IC to the CBUS receiver also has not been checked. Please confirm with our company if the IC will be used in these mode systems. The I²C is the brand of NXP.

b.) START and STOP conditions

A High to Low transition on the SDA line while SCL is High is one such unique case. This situation indicates START condition. A Low to High transition on the SDA line while SCL is High defines STOP condition. START and STOP conditions are always generated by the master. After START condition occur, the bus will be busy. The bus is considered to be free again a certain time after the STOP condition.



Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

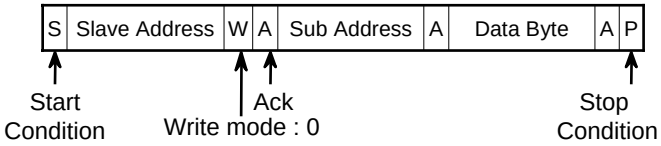


d.) Data format

Slave Address

A6	A5	A4	A3	A2	A1	A0	R/W	Hex
1	1	1	0	0	1	0	x	72h

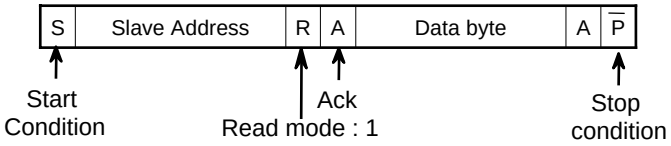
Write mode



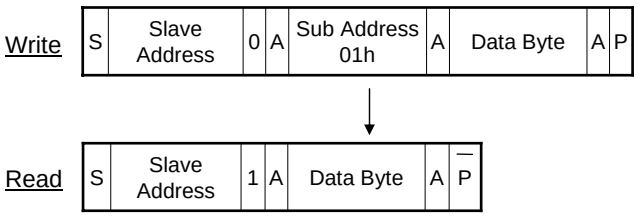
Read mode

d1.) When Sub address is not specified

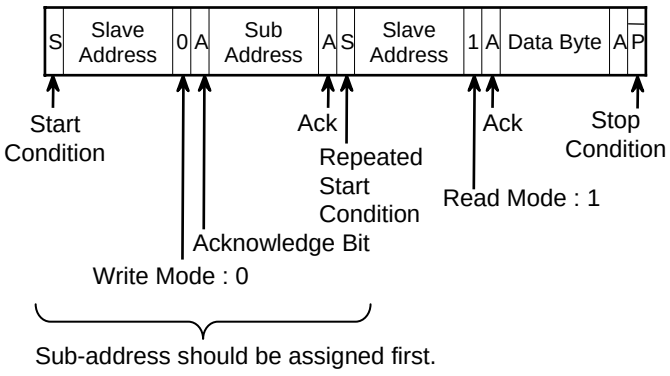
When data is read without assigning sub-address, it is possible to read the value of sub-address specified in Write mode immediately before.



Ex) When writing data into address and reading data from "01 h".



d2.) When Sub address is specified



OPERATION (Continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

6. I²C-bus Interface

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	CNT	Name	—	FSEL[2:0]			—	—	FCCM	DCDCOFF
			Default	—	0	0	0	—	—	0	0
11h	R/W	DAC	Name	—	—	—	—	VDC[3:0]			
			Default	—	—	—	—	0	0	0	0

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	R/W	CNT	Name	—	FSEL[2:0]			—	—	FCCM	DCDCOFF
			Default	—	0	0	0	—	—	0	0

Sub Address	R/W	Register Name	Bit	Data							
				D7	D6	D5	D4	D3	D2	D1	D0
11h	R/W	DAC	Name	—	—	—	—	VDC[3:0]			
			Default	—	—	—	—	0	0	0	0

D6-D4 (FSEL Setting)

FSEL[6:4]			FREQUENCY (MHz)
D6	D5	D4	
0	0	0	1.00 (Default)
0	0	1	0.50
0	1	0	0.75
0	1	1	1.00
1	0	0	1.25
1	0	1	1.50
1	1	0	1.75
1	1	1	2.00

D1: FCCM:

0 : Default (Skip Mode)

1 : Force CCM Mode

D0: DCDCOFF

0 : Default (DCDC On)

1 : DCDC Off

D3-0 : DCDC Output Voltage Setting Register

VDC1[3:0]				Output Voltage [V]
D3	D2	D1	D0	
0	0	0	0	1.000 (Default)
0	0	0	1	0.880
0	0	1	0	0.895
0	0	1	1	0.910
0	1	0	0	0.925
0	1	0	1	0.940
0	1	1	0	0.955
0	1	1	1	0.970
1	0	0	0	0.985
1	0	0	1	1.000
1	0	1	0	1.015
1	0	1	1	1.030
1	1	0	0	1.045
1	1	0	1	1.060
1	1	1	0	1.075
1	1	1	1	1.090

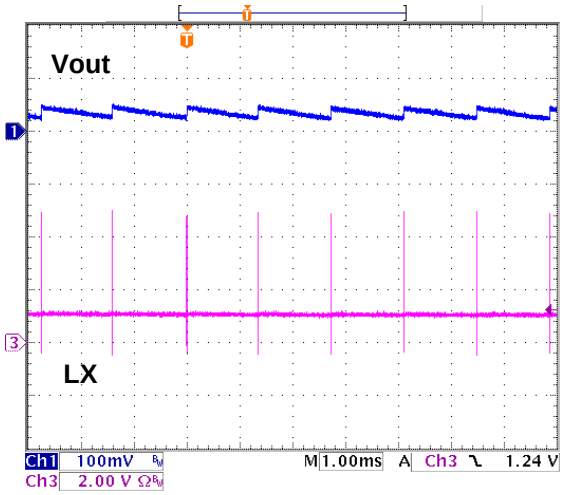
Note) The required output voltage is set by changing the DAC step by 1 bit at a time. An interval of more than 50 µs is required at every bit step while changing the DAC.

TYPICAL CHARACTERISTICS CURVES

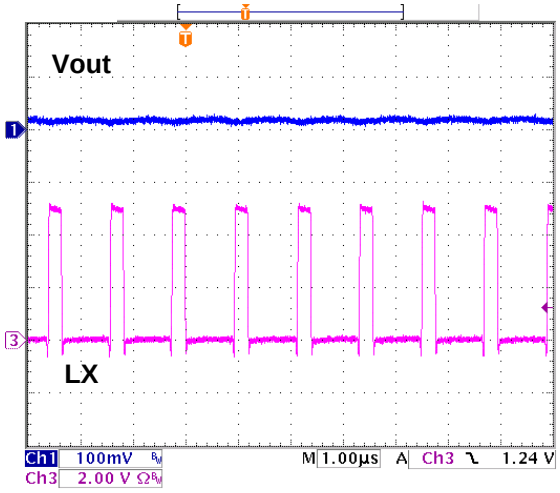
(1) Output Ripple Voltage

Condition : VIN=5V,Vout = 1.0V,Frequency = 1000kHz,Skip Mode

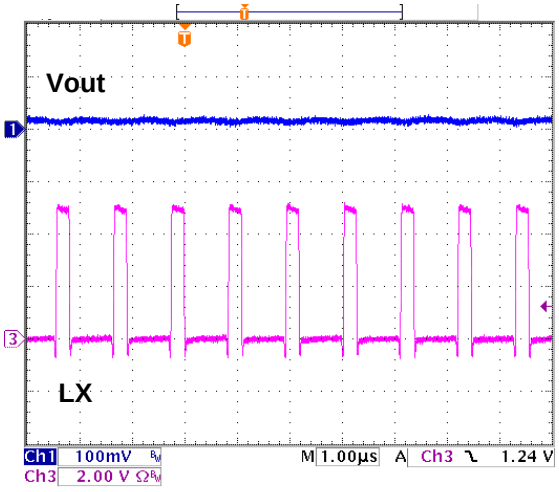
I Load = 0A



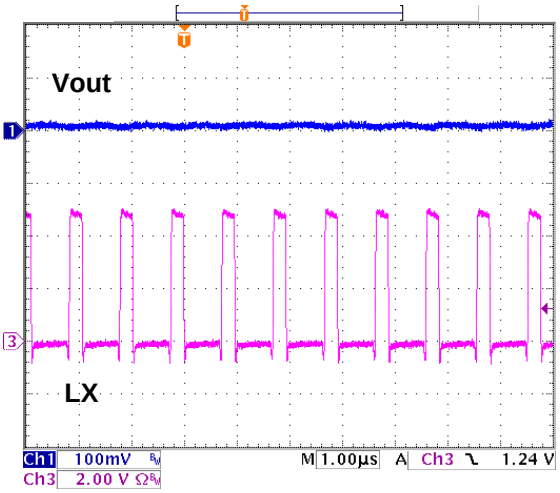
I Load = 1A



I Load = 3A



I Load = 6A

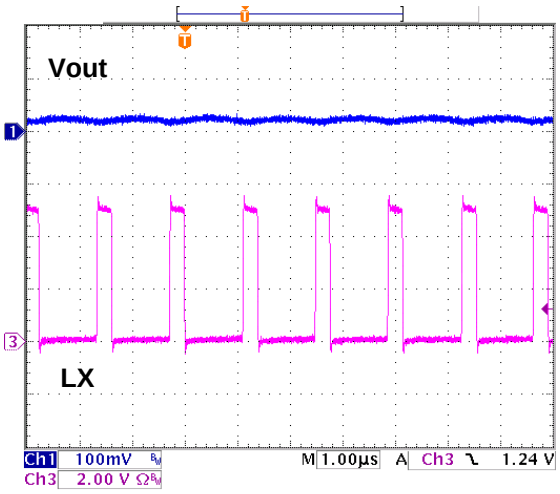


TYPICAL CHARACTERISTICS CURVES (Continued)

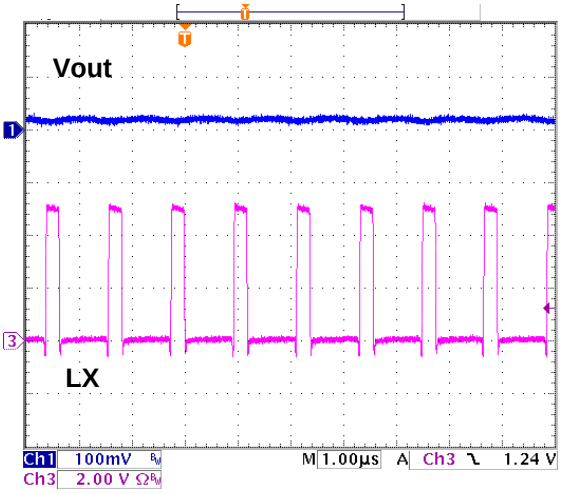
(1) Output Ripple Voltage

Condition : VIN=5V,Vout = 1.0V,Frequency = 1000kHz,FCCM Mode

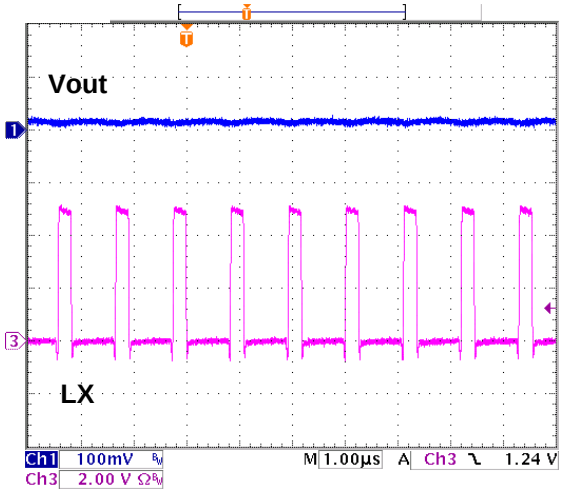
I Load = 0A



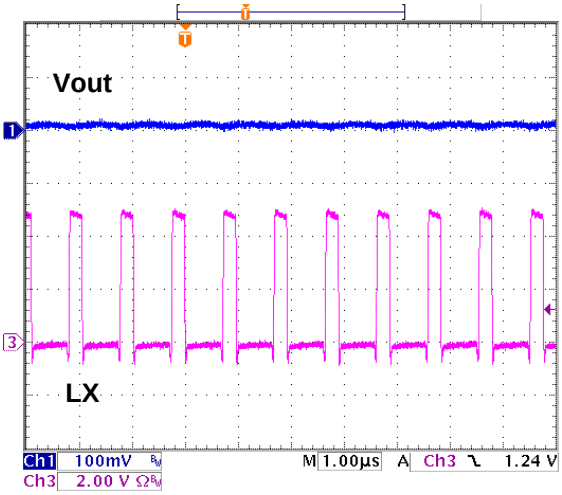
I Load = 1A



I Load = 3A



I Load = 6A

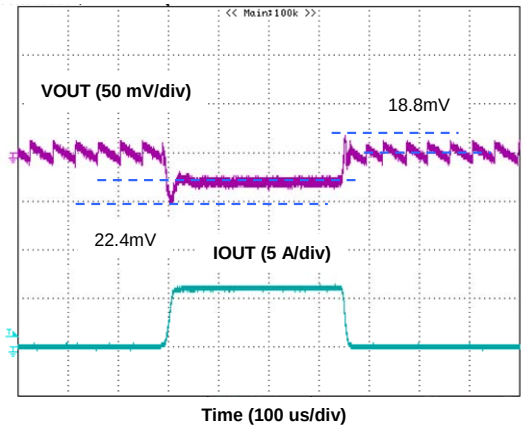


TYPICAL CHARACTERISTICS CURVES (Continued)

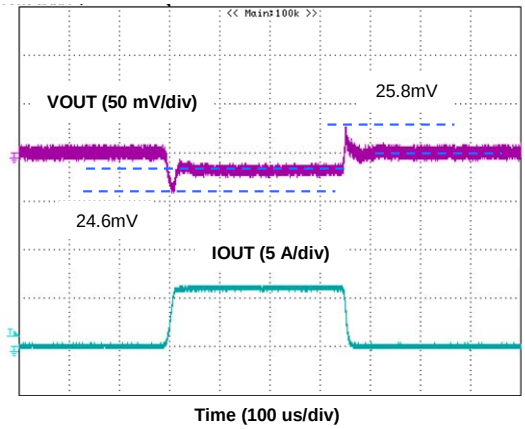
(2) Load transient

Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz, Iout = 10 mA ←→ 6 A (0.5 A / µs)

Skip Mode

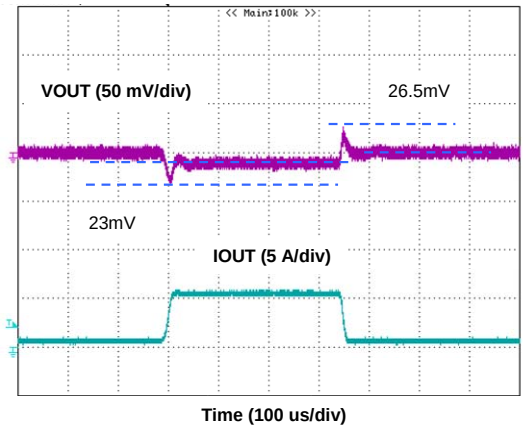


FCCM Mode

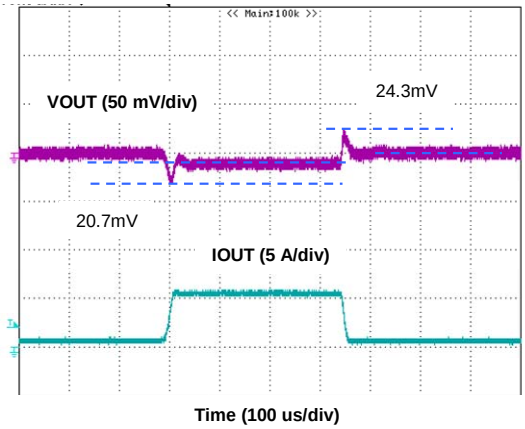


Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz, Iout = 0.6 A ←→ 5.4 A (0.5 A / µs)

Skip Mode

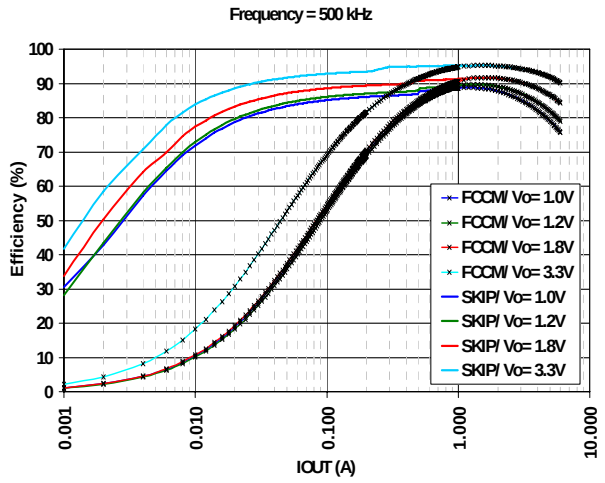


FCCM Mode

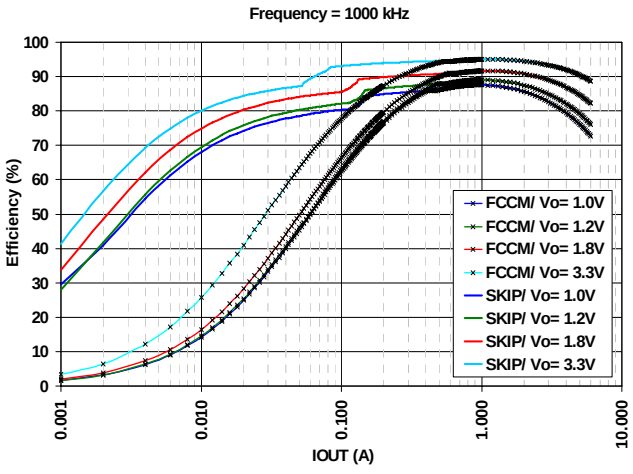


(3) Efficiency

Condition : Vin = 5.0 V, Vout = 1.0 V / 1.2 V / 1.8V / 3.3V,
L = 1 µH, Cout = 44 µF (22 µF x 2), Frequency = 500 kHz



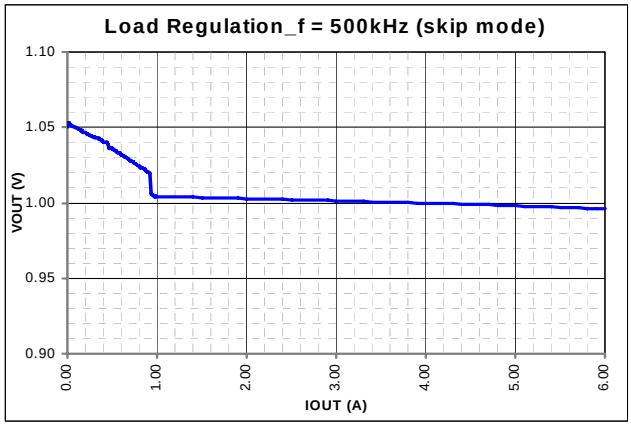
Condition : Vin = 5.0 V, Vout = 1.0 V / 1.2 V / 1.8V / 3.3V,
L = 1 µH, Cout = 44 µF (22 µF x 2), Frequency = 1 MHz

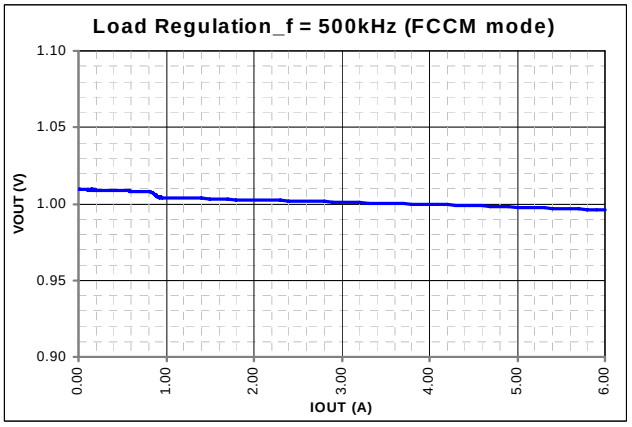


TYPICAL CHARACTERISTICS CURVES (Continued)

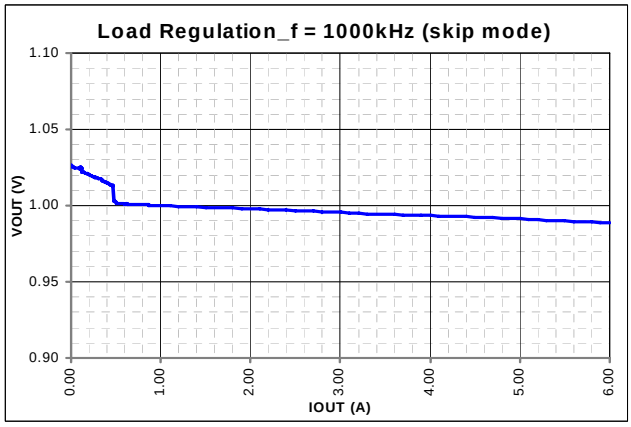
(4) Load regulation

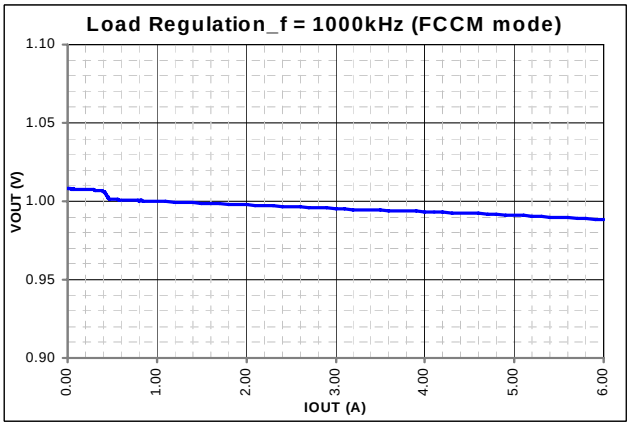
Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 500 kHz





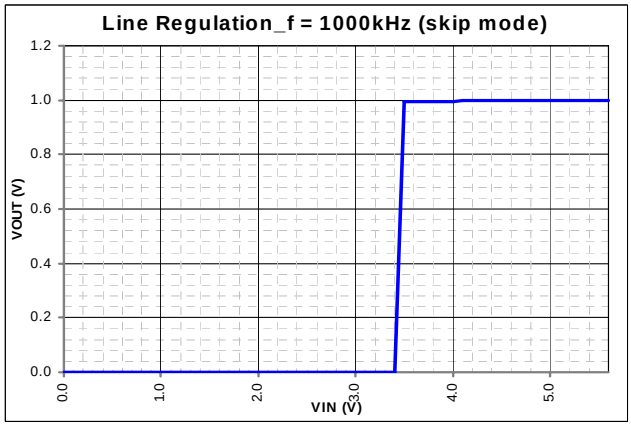
Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz

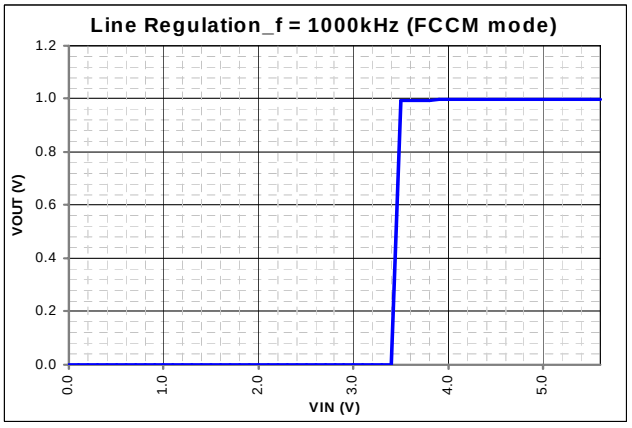




(5) Line regulation

Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz, Iout = 1.5 A

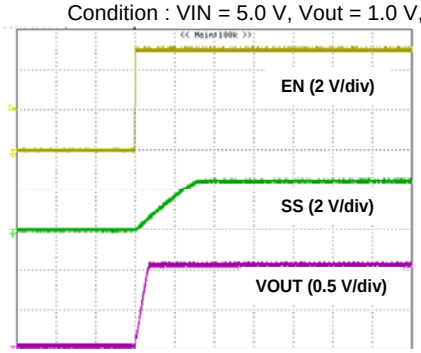


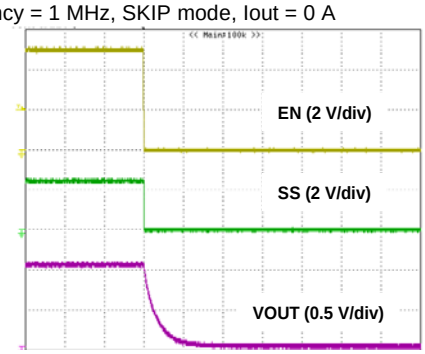


TYPICAL CHARACTERISTICS CURVES (Continued)

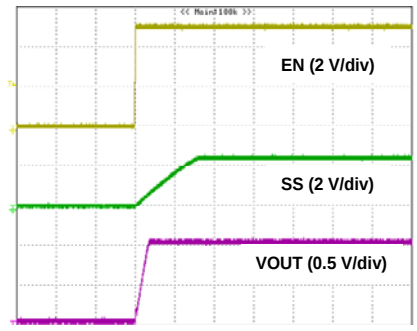
(6) start/shut down

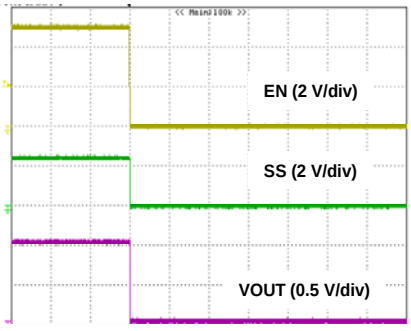
Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz, SKIP mode, Iout = 0 A





Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz, SKIP mode, Rload = 0.5 Ω

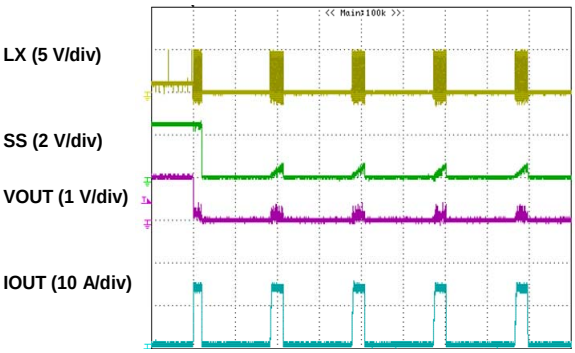




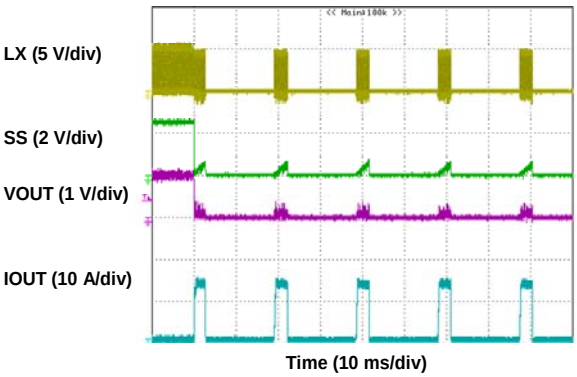
(7) Short Current Protection

Condition : VIN = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz

Skip Mode



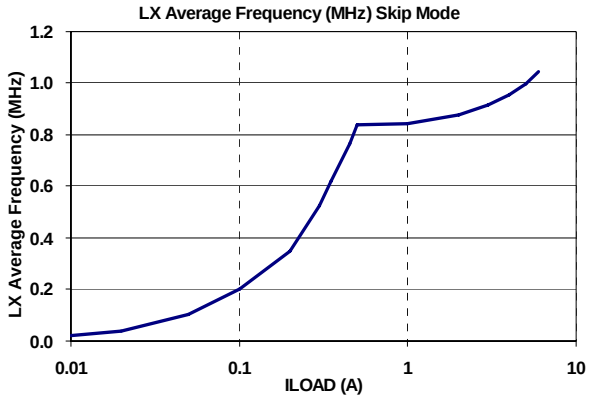
FCCM Mode

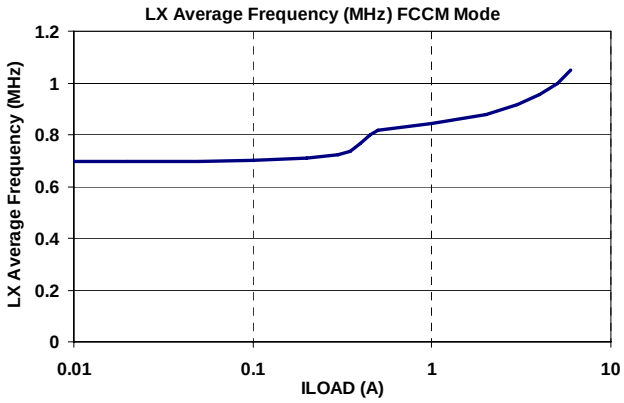


TYPICAL CHARACTERISTICS CURVES (Continued)

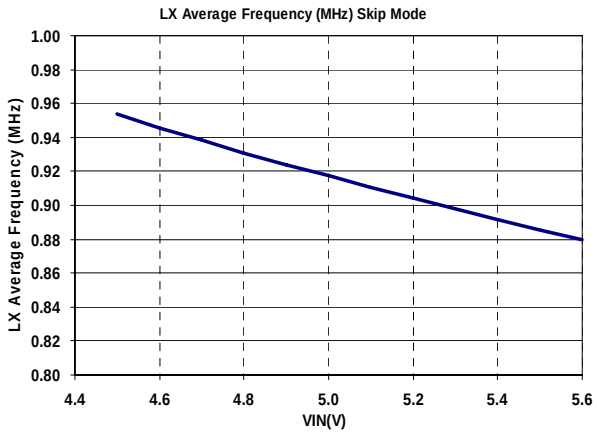
(8) Switching Frequency

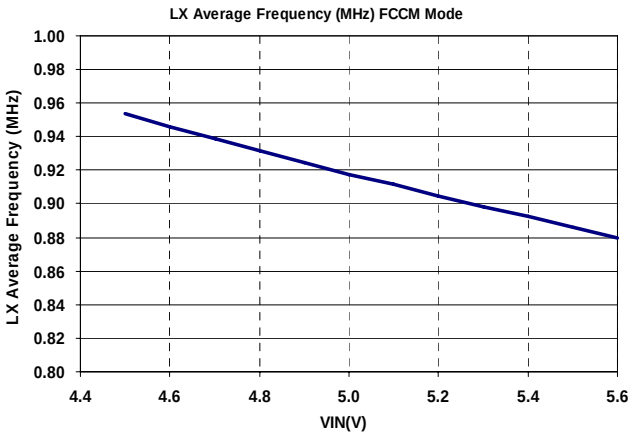
Condition : Vin = 5.0 V, Vout = 1.0 V, Frequency = 1 MHz, Iout = 10 mA ~ 6 A





Condition : Vout = 1.0 V, Frequency = 1 MHz, Iout = 3 A

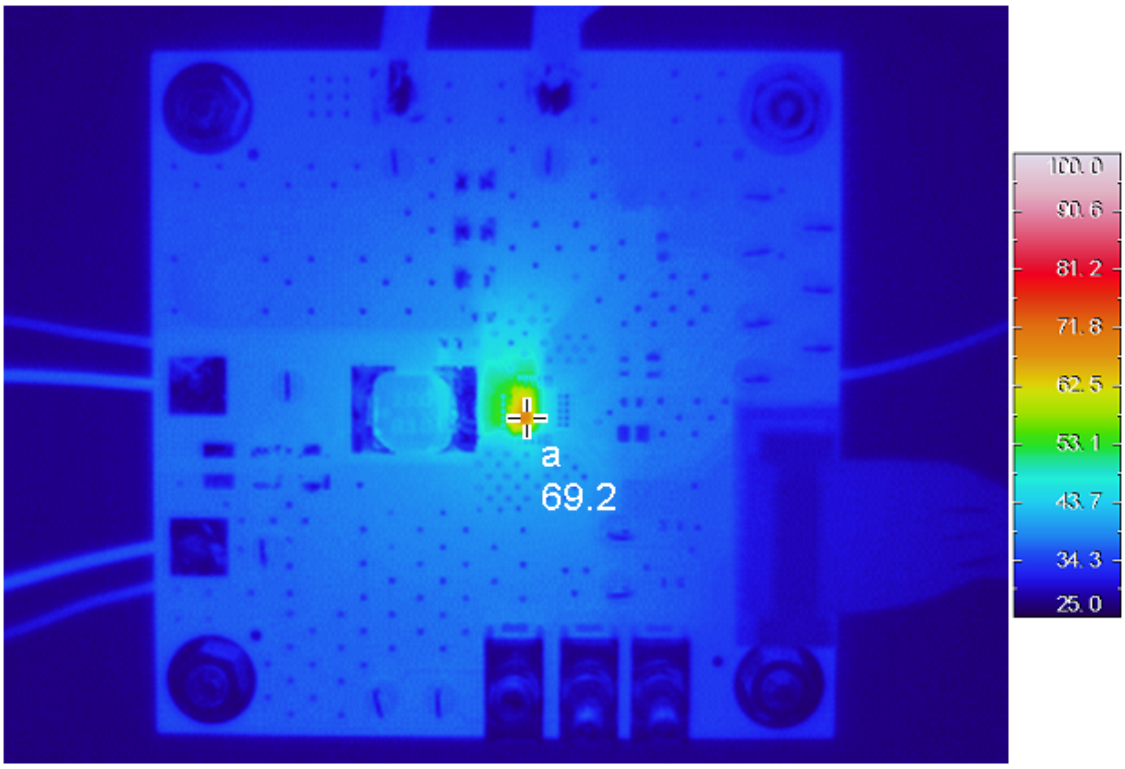




TYPICAL CHARACTERISTICS CURVES (Continued)

(9) Thermal Performance

Condition : VIN=5V , Vout = 1.0V , Frequency = 1000kHz , ILoad = 5A , FCCM Mode

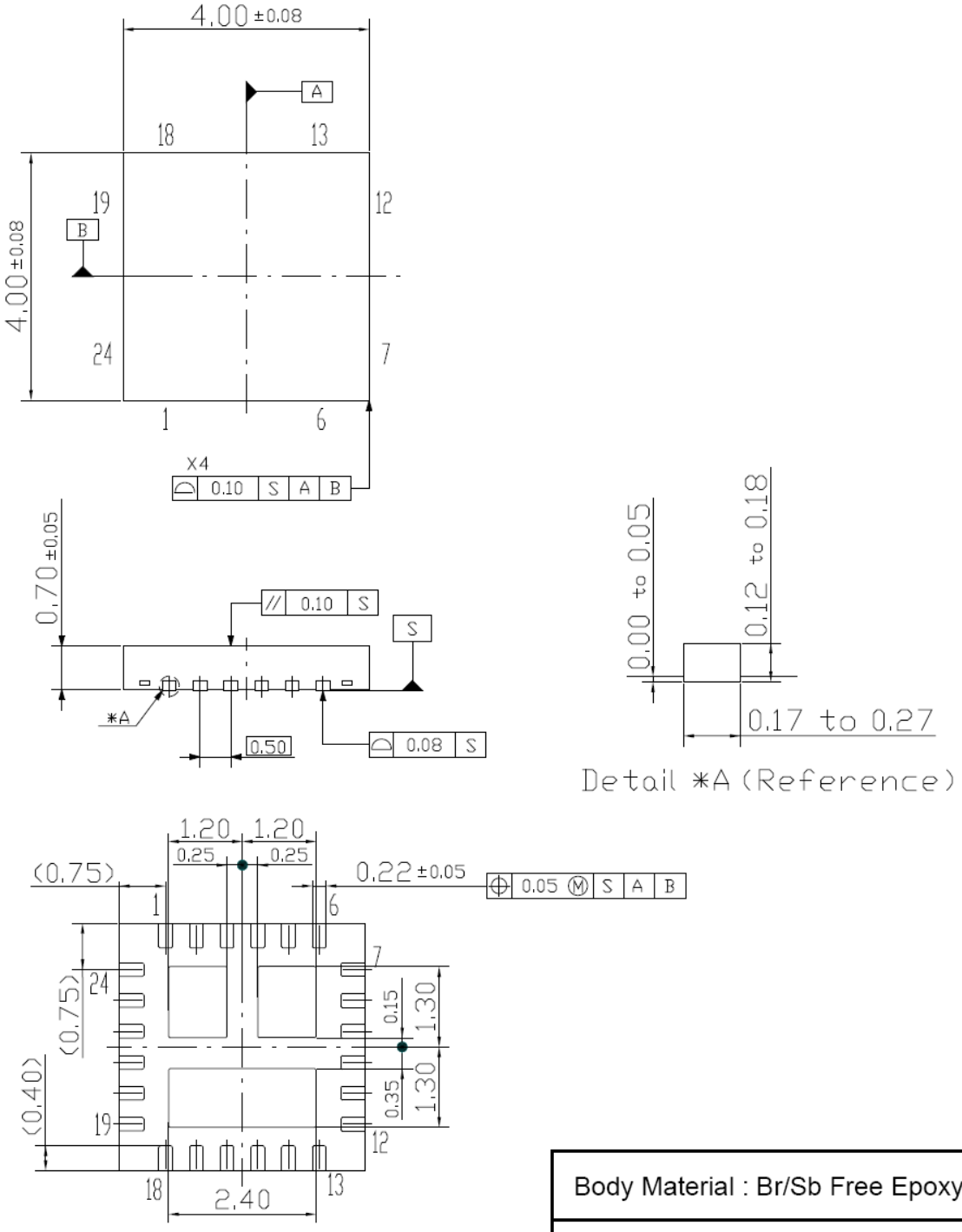


PACKAGE INFORMATION (Reference Data)

Outline Drawing

Package Code : HQFN024-A3-0404A

Unit : mm



Body Material : Br/Sb Free Epoxy Resin
Lead Material : Cu Alloy
Lead Finish Method : Pd Plating

PACKAGE INFORMATION (Reference Data)

Power dissipation (Supplementary explanation)

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity.　　（Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta　：Ambient air temperature

※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc　：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj　：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

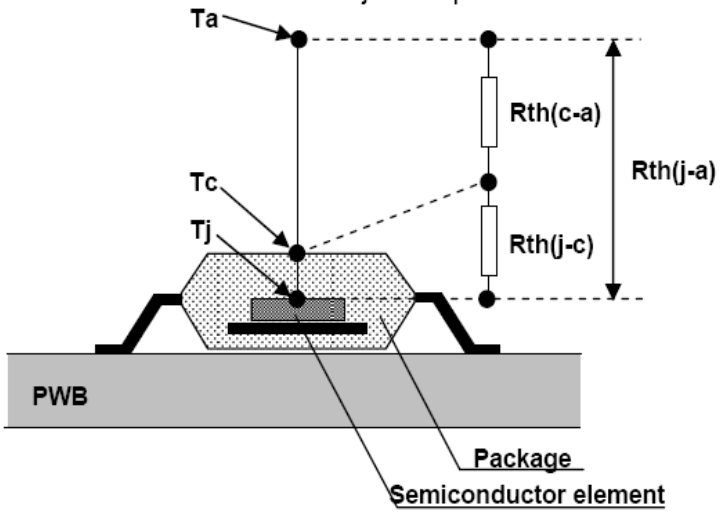


Fig1. Definition image

[Definition formula]

$$Tj=\{Rth(j\text{-}c)+Rth(c\text{-}a)\}\times P+Ta$$
$$=Rth(j\text{-}a)\times P+Ta$$

$$Rth(j\text{-}c)=\frac{Tj-Tc}{P}\quad(℃/W)$$

$$Rth(c\text{-}a)=\frac{Tc-Ta}{P}\quad(℃/W)$$

$$Rth(j\text{-}a)=\frac{Tj-Ta}{P}\quad(℃/W)$$

$$=Rth(j\text{-}c)+Rth(c\text{-}a)$$

P:power(W)

IMPORTANT NOTICE

1.The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

2.When using the LSI for new models, verify the safety including the long-term reliability for each product.

3.When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.

4.The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.

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6.This LSI is intended to be used for general electronic equipment.
Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
Any applications other than the standard applications intended.
(1) Space appliance (such as artificial satellite, and rocket)
(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
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9. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive.
Our company shall not be held responsible for any damage incurred as a result of your using the LSI not complying with the applicable laws and regulations.

USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO

10. Verify the risks which might be caused by the malfunctions of external components.

11. Connect the metallic plates on the back side of the LSI with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.