power-one®
Changing the Shape of Power

PFE1100-12-054NA Data Sheet

1100 Watts, 12 VDC Output

Features

- Best-in-class, 80 PLUS certified “Platinum” efficiency
- Wide input voltage range: 90-264 VAC
- AC input with power factor correction
- Always-On 16.5W programmable standby output (3.3/5 V)
- Hot-plug capable
- Parallel operation with active digital current sharing
- Full digital controls for improved performance
- High density design: 25.6 W/in^3
- Small form factor: 54.5 x 40.0 x 321.5 mm
- I^2C communication interface for control, programming and monitoring with PSMI and PMBus™ protocol
- Overtemperature, output overvoltage and overcurrent protection
- 256 Bytes of EEPROM for user information
- 2 Status LEDs: AC OK and DC OK with fault signaling

Applications

- High performance servers, routers, and switches.

Description

The PFE1100-12-054NA is an 1100 watt AC to DC power-factor-corrected (PFC) power supply that converts standard AC mains power into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches. The PFE1100-12-054NA meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

Content

1 ORDERING INFORMATION

PFE	1100	-	12	-	054	N	A	
Product Family PFE Front-Ends	**Power Level** 1100W	**Dash**	**V1 Output** 12V	**Dash**	**Width** 54mm	**Airflow** N: normal R: reversed	**Input** A: AC D: DC	

2 OVERVIEW

The PFE1100-12-054NA AC-DC power supply is a fully DSP controlled, highly efficient front-end. It incorporates resonance-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range and minimal linear derating of output power with input voltage and temperature, the PFE1100-12-054NA maximizes power availability in demanding server, switch, and router applications. The front-end is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous front-ends. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems.

The always On standby output with selectable voltage level (3.3/5V) provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LEDs. In addition, the power supply can be controlled and fan speed set via the I²C bus. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I²C bus.

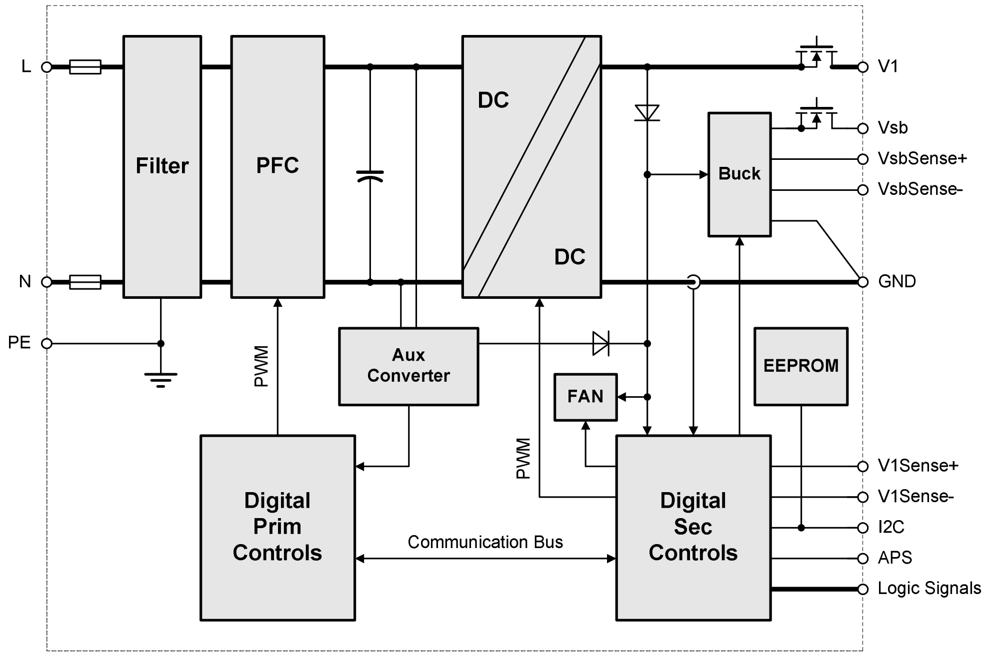


Figure 1: PFE1100-12-054NA Block Diagram

3 ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

Parameter		Conditions / Description	Min	Nom	Max	Unit
$V_{i\,maxc}$	Max continuous input	Continuous			264	VAC

4 ENVIRONMENTAL AND MECHANICAL

Parameter		Conditions / Description	Min	Nom	Max	Unit
T_A	Ambient temperature	$V_{i\,min}$ to $V_{i\,max}$, $I_{1\,nom}$, $I_{SB\,nom}$	0		+45	°C
T_{Aext}	Extended temp range	Derated output (see Figure 20 and Figure 38)	+45		+65	°C
T_S	Storage temperature	Non-operational	-20		+70	°C
N_a	Audible noise	$V_{i\,nom}$, 50% $I_{o\,nom}$, T_A = 25°C		42		dBA
	Dimensions	Width		54.5		mm
		Height		40.0		mm
		Depth		321.5		mm
M	Weight			1.05		kg

5 INPUT SPECIFICATIONS

General Condition: T_A = 0… 45 °C unless otherwise noted.

Parameter		Conditions / Description	Min	Nom	Max	Unit
$V_{i\,nom}$	Nominal input voltage		100	230	230	VAC
V_i	Input voltage ranges	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	90		264	VAC
$V_{i\,red}$	Derated input voltage range	See Figure 20 and Figure 38.	90		115	VAC
$I_{i\,max}$	Max input current				13	A_{rms}
$I_{i\,p}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, 90°, T_{NTC} = 25°C (see Figure 5)			40	A_p
F_i	Input frequency		47	50/60	64	Hz
PF	Power Factor	$V_{i\,nom}$, 50Hz, > 0.3 $I_{1\,nom}$	0.96			W/VA
$V_{i\,on}$	Turn-on input voltage[1)]	Ramping up	80		87	VAC
$V_{i\,off}$	Turn-off input voltage[1)]	Ramping down	75		85	VAC
η	Efficiency without fan	$V_{i\,nom}$, $0.1 \cdot I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		90.3		%
		$V_{i\,nom}$, $0.2 \cdot I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		93.4		
		$V_{i\,nom}$, $0.5 \cdot I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		94.5		
		$V_{i\,nom}$, $I_{x\,nom}$, $V_{x\,nom}$, T_A = 25 °C		93.8		
T_{hold}	Hold-up Time	After last AC zero point, V_1 > 10.8 V, V_{SB} within regulation, V_i = 230 VAC, $P_{x\,nom}$	12			ms

[1)] The Front-End is provided with a minimum hysteresis of 3 V during turn-on and turn-off within the ranges.

5.1 INPUT FUSE

16A input fuses (5 × 20 mm) in series with both the L- and N-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

5.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 3.2 µF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through an NTC which will limit the inrush current.

Note: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (NTC) may not sufficiently cool down and excessive inrush current or component failure(s) may result.

5.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input undervoltage lockout threshold $V_{i\ on}$, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

5.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

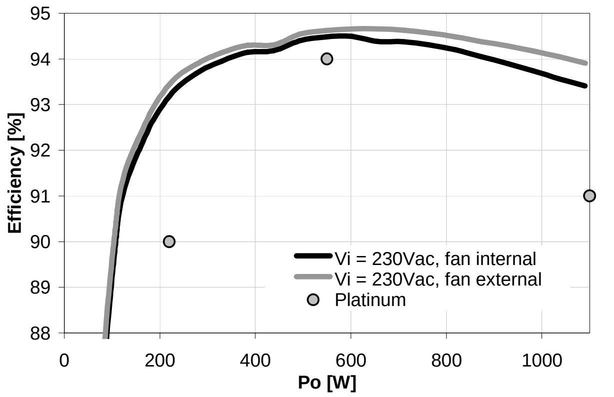


Figure 2: Efficiency vs. load current (ratio metric loading)

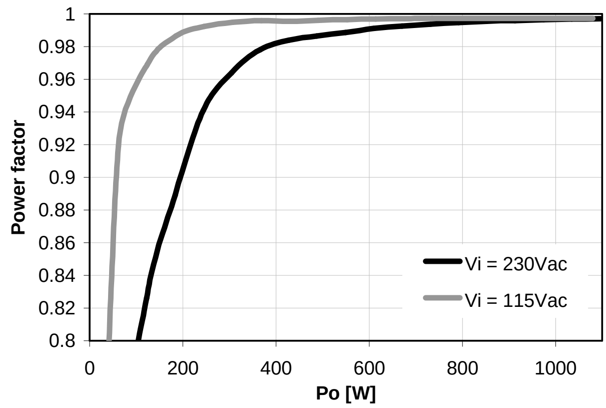


Figure 3: Power factor vs. load current

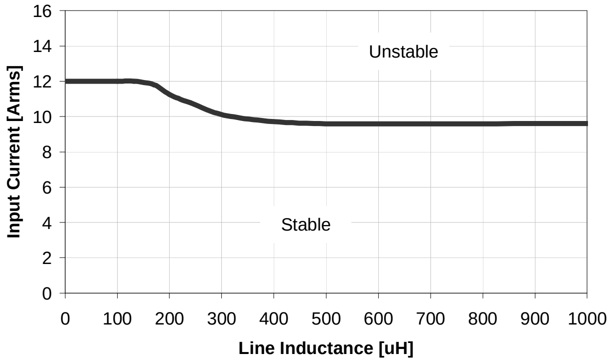


Figure 4: PFC stability region

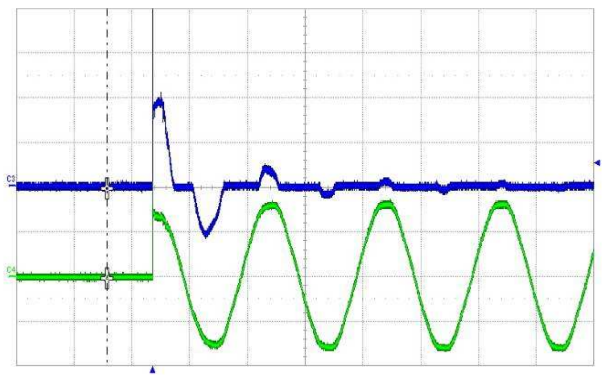


Figure 5: Inrush current, V_{in} = 230Vac, 90°
CH4: V_{in} (200V/div), CH3: I_{in} (20A/div)

In addition, the PFC circuit has a stability region to be observed when operating the power supply at high input current amplitudes. At a low source inductance (<150 µH) the power supply will work stable up to its full maximum input current (13 Arms). If the source inductance is higher, the region with stable PFC operation is slightly reduced (as shown in Figure 4). The power supply will also work in the unstable region, but it may exhibit a slight current oscillation during the sinusoidal peak.

5.5 EFFICIENCY

The high efficiency (see Figure 2) is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components with an optimal operating temperature regardless of the ambient temperature and load conditions.

6 OUTPUT SPECIFICATIONS

General Condition: T_a = 0 … +45 °C unless otherwise noted.

Parameter		Conditions / Description	Min	Nom	Max	Unit
***Main Output* V₁**						
$V_{1\ nom}$	Nominal output voltage	$0.5 \cdot I_{1\ nom}$, T_{amb} = 25 °C		12.0		VDC
$V_{1\ set}$	Output setpoint accuracy	$0.5 \cdot I_{1\ nom}$, T_{amb} = 25 °C	-0.5		+0.5	% $V_{1\ nom}$
$dV_{1\ tot}$	Total regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-1		+1	% $V_{1\ nom}$
$P_{1\ nom}$	Nominal output power	V_1 = 12 VDC		1080		W
$I_{1\ nom}$	Nominal output current	V_1 = 12 VDC		90.0		ADC
$v_{1\ pp}$	Output ripple voltage	$V_{1\ nom}$, $I_{1\ nom}$, 20 MHz BW (See chapter 6.1)			150	mVpp
$dV_{1\ Load}$	Load regulation	$V_i = V_{i\ nom}$, 0 - 100 % $I_{1\ nom}$		60		mV
$dV_{1\ Line}$	Line regulation	$V_i = V_{i\ min} ... V_{i\ max}$		0		mV
$I_{1\ max}$	Current limitation	V_i > 115 VAC, T_a < 45 °C V_i > 90 VAC, T_a < 45 °C	95 74		100 78	ADC
dI_{share}	Current sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 10%	-3		+3	A
dV_{dyn}	Dynamic load regulation	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1 A/µs, recovery within 1% of $V_{1\ nom}$	-0.6		0.6	V
T_{rec}	Recovery time	ΔI_1 = 50% $I_{1\ nom}$, I_1 = 5 … 100% $I_{1\ nom}$, dI_1/dt = 1 A/µs, recovery within 1% of $V_{1\ nom}$			1	ms
$t_{AC\ V1}$	Start-up time from AC	V_1 = 10.8 VDC (see Figure 7)			2	sec
$t_{V1\ rise}$	Rise time	V_1 = 10…90% $V_{1\ nom}$ (see Figure 8)		1	10	ms
C_{Load}	Capacitive loading	T_a = 25 °C			30000	µF
***Standby Output* V_SB**						
$V_{SB\ nom}$	Nominal output voltage	$0.5 \cdot I_{SB\ nom}$, T_{amb} = 25 °C; VSB_SEL = 1		3.3		VDC
$V_{SB\ nom}$	Nominal output voltage	$0.5 \cdot I_{SB\ nom}$, T_{amb} = 25 °C; VSB_SEL = 0		5.0		VDC
$V_{SB\ set}$	Output setpoint accuracy	$0.5 \cdot I_{SB\ nom}$, T_{amb} = 25 °C; VSB_SEL = 0 / 1	-0.5		+0.5	% $V_{1\ nom}$
$dV_{SB\ tot}$	Total regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, $T_{a\ min}$ to $T_{a\ max}$	-1		+1	% V_{SBnom}
$P_{SB\ nom}$	Nominal output power	VSB_SEL = 0 / 1		16.5		W
$I_{SB\ nom}$	Nominal output current	V_{SB} = 3.3 VDC		5		ADC
$I_{SB\ nom}$	Nominal output current	V_{SB} = 5.0 VDC		3.3		ADC

Parameter		Conditions / Description	Min	Nom	Max	Unit
Standby Output V_{SB} (Cont.)						
$V_{SB\,pp}$	Output ripple voltage	$V_{SB\,nom}$, $I_{SB\,nom}$, 20 MHz BW (See chapter 6.1)			100	mVpp
dV_{SB}	Droop	0 - 100 % $I_{SB\,nom}$, VSB_SEL = 1		67		mV
		0 - 100 % $I_{SB\,nom}$, VSB_SEL = 0		44		mV
$I_{SB\,max}$	Current limitation	VSB_SEL = 1	5.25		6	ADC
		VSB_SEL = 0	3.45		4.3	ADC
dV_{SBdyn}	Dynamic load regulation	ΔI_{SB} = 50% $I_{SB\,nom}$, I_{SB} = 5 … 100% $I_{SB\,nom}$, dI_o/dt = 0.5 A/µs, recovery within 1% of $V_{1\,nom}$	-3		3	% V_{SBnom}
T_{rec}	Recovery time				250	µs
$t_{AC\,VSB}$	Start-up time from AC	V_{SB} = 90% $V_{SB\,nom}$ (see Figure 24)			2	sec
$t_{VSB\,rise}$	Rise time	V_{SB} = 10…90% $V_{SB\,nom}$ (see Figure 24)		4	20	ms
C_{Load}	Capacitive loading	T_{amb} = 25 °C			10000	µF

6.1 OUTPUT RIPPLE VOLTAGE

The internal output capacitance at the power supply output (behind oring element) is minimized to prevent disturbances during hot plug. In order to provide low output ripple voltage in the application, external capacitors should be added close to the power supply output.

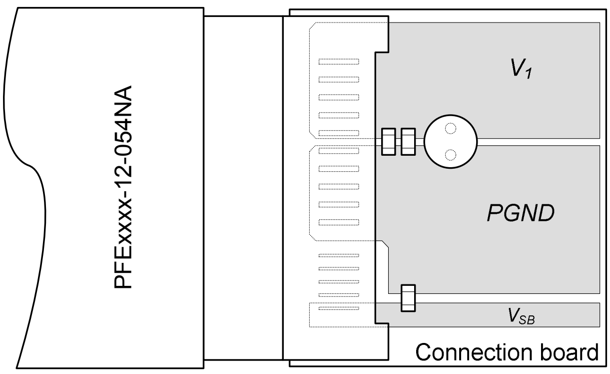


Figure 6: Output ripple test setup

The setup of Figure 6 has been used to evaluate suitable capacitor types. The capacitor combinations of Table 1 and Table 2 should be used to reduce the output ripple voltage. The ripple voltage is measured with 20MHz BWL, close to the external capacitors.

Note: Care must be taken when using ceramic capacitors with a total capacitance of 1µF to 50µF on output V1, due to their high quality factor the output ripple voltage may be increased in certain frequency ranges due to resonance effects.

Table 1: Suitable capacitors for V_1

External capacitor V1	dV1max	Unit
2Pcs 47µF/16V/X5R/1210	150	mVpp
1Pcs 1000µF/16V/Low ESR Aluminum/ø10x20	150	mVpp
1Pcs 270µF/16V/Conductive Polymer/ø8x12	120	mVpp
2Pcs 47µF/16V/X5R/1210 plus 1Pcs 270µF Conductive Polymer OR 1Pcs 1000µF Low ESR AlCap	60	mVpp

The output ripple voltage on VSB is influenced by the main output V1. Evaluating VSB output ripple must be done when maximum load is applied to V1.

Table 2: Suitable capacitors for V_{SB}

External capacitor VSB	dV1max	Unit
1Pcs 10µ/16V/X5R/1206	100	mVpp
2Pcs 10µ/16V/X5R/1206	60	mVpp
1Pcs 47µF/16V/X5R/1210	50	mVpp
2Pcs 100µ/6.3V/X5R/1206	35	mVpp

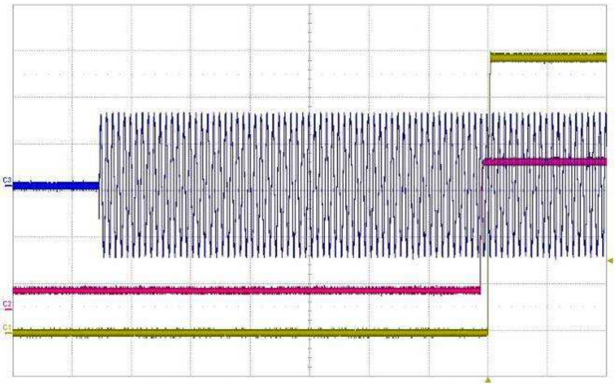


Figure 7: Turn-On AC Line 230 VAC, full load (200 ms/div)
CH1: V_1 (2 V/div) CH2: V_{SB} (2 V/div)
CH3: Vin (200 V/div)

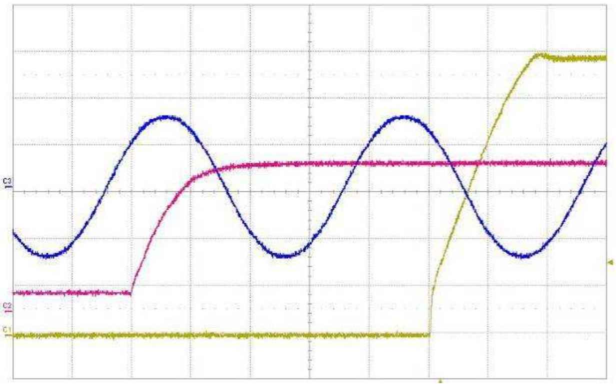


Figure 8: Turn-On AC Line 230 VAC, full load (5 ms/div)
CH1: V_1 (2 V/div) CH2: V_{SB} (2 V/div)
CH3: Vin (200 V/div)

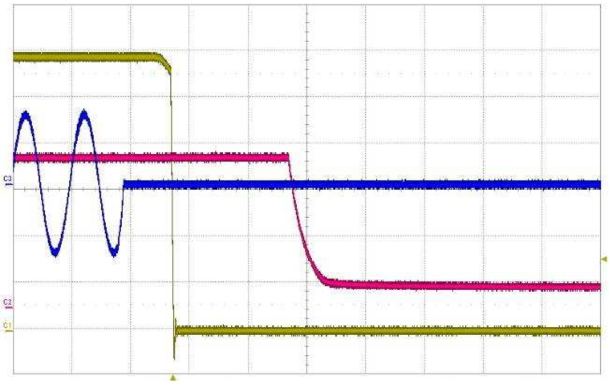


Figure 9: Turn-Off AC Line 230 VAC, full load (20 ms/div)
CH1: V_1 (2 V/div) CH2: V_{SB} (2 V/div)
CH3: Vin (200 V/div)

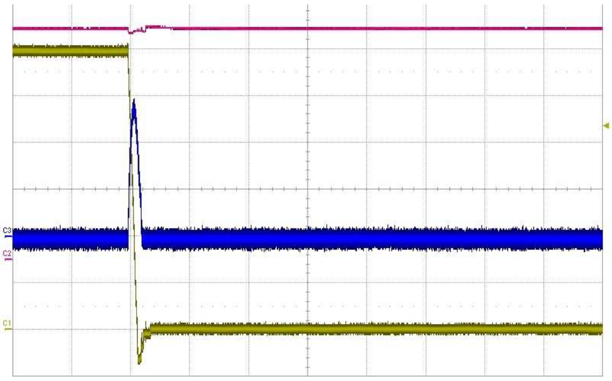


Figure 10: Short circuit on V1 (500 µs/Div)
CH1: V_1 (2 V/div) CH2: V_{SB} (1 V/div)
CH3: I_1 (200 A/div)

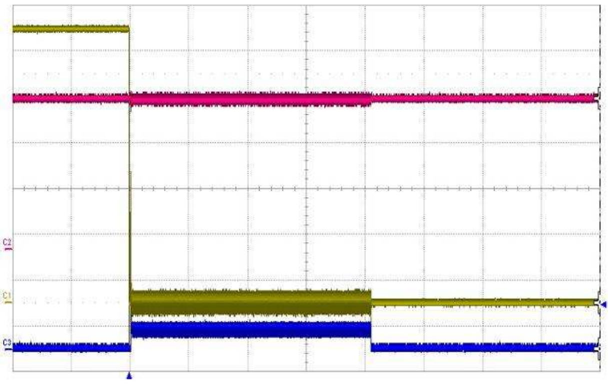


Figure 11: Short circuit on V1 (50 ms/div)
CH1: V_1 (2 V/div) CH2: V_{SB} (1 V/div)
CH3: I_1 (200 A/div)

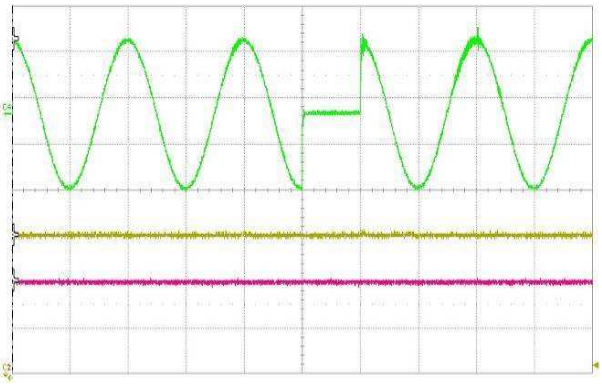


Figure 12: AC drop out 10ms (10 ms/div)
CH1: V_1 (2 V/div) CH2: V_{SB} (1 V/div)
CH4: V_{in} (200 V/div)

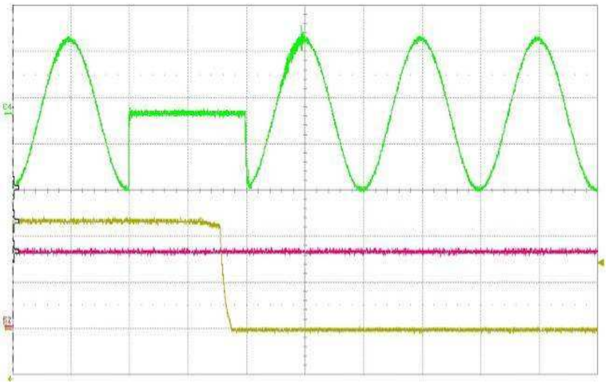


Figure 13: AC drop out 20 ms (10 ms/div)
CH1: V_1 (5 V/div) CH2: V_{SB} (2 V/div)
CH4: V_{in} (200 V/div)

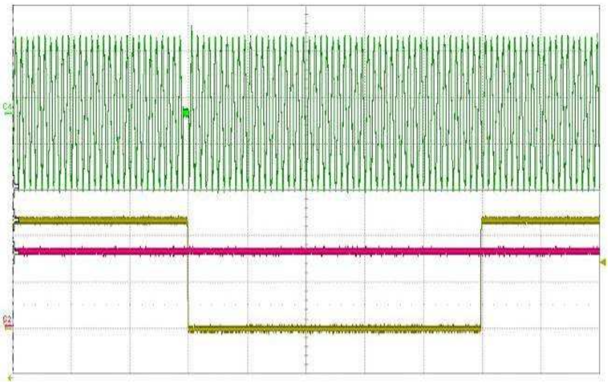


Figure 14: AC drop out 20 ms (200 ms/div), V_1 restart after 1 sec
CH1: V_1 (5 V/div) CH2: V_{SB} (2 V/div)
CH4: I_1 (200 V/div)

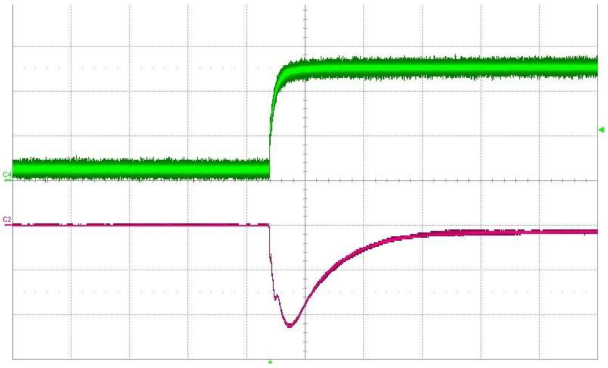


Figure 15: Load transient V_1, 5 to 50 A (500 µs/div)
CH2: V_1 (200 mV/div)
CH4: I_1 (20 A/div)

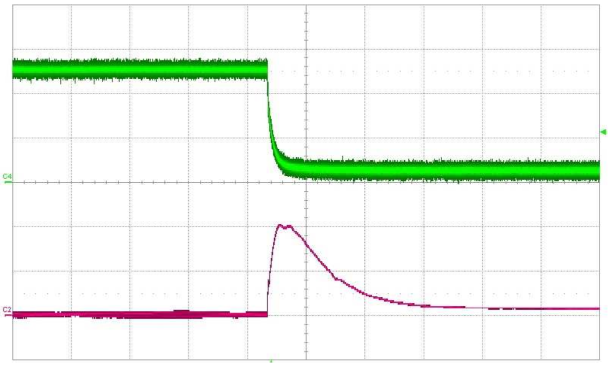


Figure 16: Load transient V_1, 50 to 5 A (500 µs/div)
CH2: V_1 (200 mV/div)
CH4: I_1 (20 A/div)

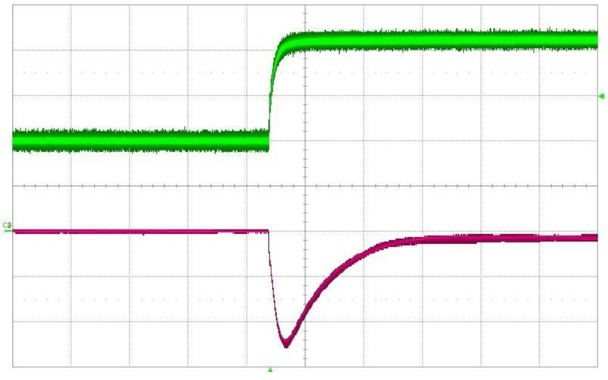


Figure 17: Load transient V_1, 40 to 85 (500 µs/div)
CH2: V_1 (200 mV/div)
CH4: I_1 (20 A/div)

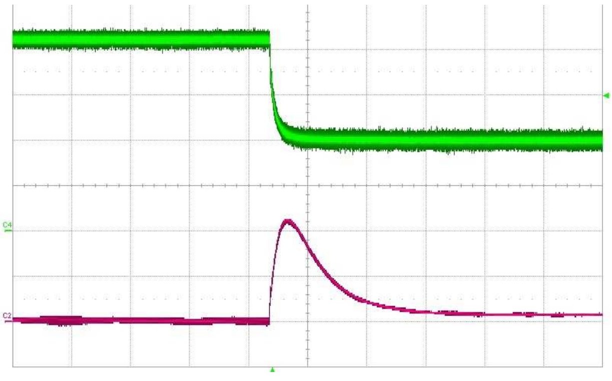


Figure 18: Load transient V_1, 85 to 40 A (500 µs/div)
CH2: V_1 (200 mV/div)
CH4: I_1 (20 A/div)

7 PROTECTION

Parameter		Conditions / Description	Min	Nom	Max	Unit
F	Input fuses (L+N)	Not user accessible, time lag characteristic		16		A
$V_{1\,OV}$	OV threshold V_1		13.3		14.5	VDC
$t_{OV\,V1}$	OV latch off time V_1				1	ms
$V_{SB\,OV}$	OV threshold V_{SB}		115		125	% V_{SB}
$t_{OV\,VSB}$	OV latch off time V_{SB}				1	ms
$I_{V1\,lim}$	Current limit V_1	V_i > 115 VAC, T_a < 45 °C V_i > 90 VAC, T_a < 45 °C	95 74		100 78	A
$I_{V1\,SC}$	Max short circuit current V_1	V_1 < 3 V			110	A
$t_{V1\,SC}$	Short circuit regulation time	V_1 < 3 V, time until I_{V1} is limited to < $I_{V1\,sc}$			2	ms
$t_{V1\,SC\,off}$	Short circuit latch off time	Time to latch off when in short circuit			200	ms
T_{SD}	Over temperature on heat sinks	Automatic shut-down		115		°C

7.1 OVERVOLTAGE PROTECTION

The PFE front-ends provide a fixed threshold overvoltage (OV) protection implemented with a HW comparator. Once an OV condition has been triggered, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON input.

7.2 VSB UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK pin signal if output voltage exceeds ±5% of its nominal voltage.

Output undervoltage protection is provided on the standby output only. When V_{SB} falls below 75% of its nominal voltage, the main output V_1 is inhibited.

7.3 CURRENT LIMITATION

Main Output: The main output exhibits a substantially rectangular output characteristic. If it runs in current limitation and its voltage drops below ~10.0 VDC for more than 200 ms, the output will latch off (standby remains on, software current limit triggers).

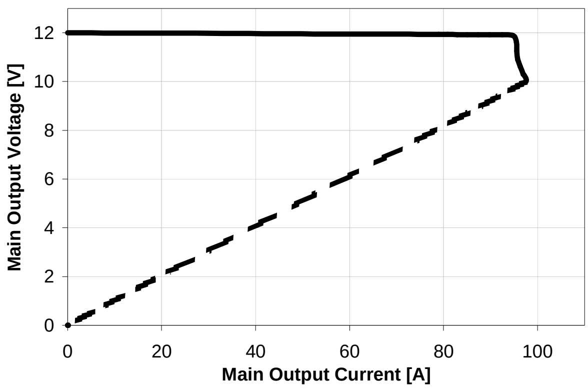


Figure 19: Current limitation on V_1 (V_i = 230 VAC)

A second current limitation circuit on V1 will immediately switch off the main output if the output current increases beyond the peak current trip point. The supply will re-start 4 ms later with a soft start, if the short circuit persists (V_1 < 10.0V for >200 ms) the output will latch off; otherwise it continuous to operate (hardware current limit triggers).

The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON input.

The main output current limitation will decrease if the ambient (inlet) temperature increases beyond 45 °C or if the AC input voltage is too low (see Figure 20). Note that the actual current limitation on V1 will kick in at a current level approximately 6A higher than what is shown in Figure 20 (see also TEMPERATURE AND FAN CONTROL on page 19 for additional information).

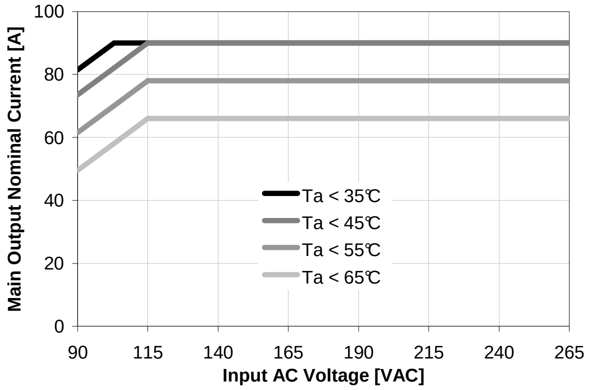


Figure 20: Derating on V_1 vs. V_i and T_a

Standby Output: The standby output exhibits a substantially rectangular output characteristic down to 0V (no hiccup mode / latch off) If it runs in current limitation and its output voltage drops below the UV threshold, then the main output will be inhibited (standby remains on). The current limitation of the standby output is independent of the AC input voltage and temperature (no derating).

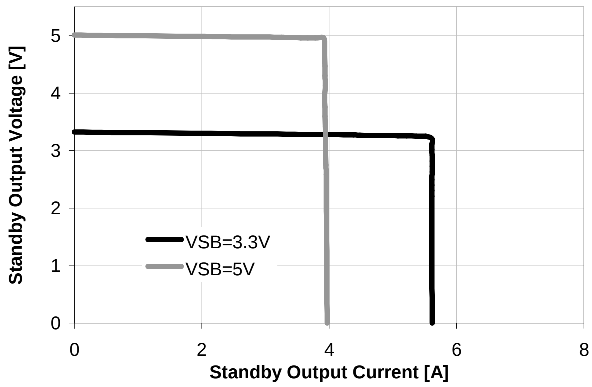


Figure 21: Current limitation on V_{SB}

8 MONITORING

Parameter		Conditions / Description	Min	Nom	Max	Unit
$V_{i\,mon}$	Input RMS voltage	$V_{i\,min} \leq V_i \leq V_{i\,max}$	-2		+2	%
$I_{i\,mon}$	Input RMS current	$I_i > 4\ A_{rms}$	-5		+5	%
		$I_i \leq 4\ A_{rms}$	-0.2		+0.2	A_{rms}
$P_{i\,mon}$	True input power	$P_i > 100$ W	-5		+5	%
		$P_i \leq 100$ W	-5		+5	W
$V_{1\,mon}$	V1 voltage		-2		+2	%
$I_{1\,mon}$	V1 current	I1 > 10 A	-2		+2	%
		I1 ≤ 10 A	-0.2		+0.2	A
$P_{o\,nom}$	Total output power	Po > 120 W	-4		+4	%
		Po ≤ 120 W	-4.5		+4.5	W
$V_{SB\,mon}$	Standby voltage		-0.1		+0.1	V
$I_{SB\,mon}$	Standby current	$I_{SB} \leq I_{SB\,nom}$	-0.2		+0.2	A

See chapter 9.12 to 9.17 and PFE Programming Manual BCA.00006 for further information on communication interface.

9 SIGNALING AND CONTROL

9.1 ELECTRICAL CHARACTERISTICS

Parameter		Conditions / Description	Min	Nom	Max	Unit
PSKILL / PSON / VSB_SEL / HOTSTANDBYEN inputs						
V_{IL}	Input low level voltage		-0.2		0.8	V
V_{IH}	Input high level voltage		2.4		3.5	V
$I_{IL, H}$	Maximum input sink or source current		0		1	mA
$R_{puPSKILL}$	Internal pull up resistor on PSKILL			100		kΩ
R_{puPSON}	Internal pull up resistor on PSON			10		kΩ
R_{puVSB_SEL}	Internal pull up resistor on VSB_SEL			10		kΩ
$R_{puHOTSTANDBYEN}$	Internal pull up resistor on HOTSTANDBYEN			10		kΩ
R_{LOW}	Resistance pin to SGND for low level		0		1	kΩ
R_{HIGH}	Resistance pin to SGND for high level		50			kΩ
PWOK output						
V_{OL}	Output low level voltage	Isink < 4mA	0		0.4	V
V_{OH}	Output high level voltage	Isource < 0.5mA	2.6		3.5	V
R_{puPWOK}	Internal pull up resistor on PWOK			1		kΩ
ACOK output						
V_{OL}	Output low level voltage	Isink < 2mA	0		0.4	V
V_{OH}	Output high level voltage	Isource < 50µA	2.6		3.5	V
R_{puACOK}	Internal pull up resistor on ACOK			10		kΩ
SMB_ALERT output						
V_{ext}	Maximum external pull up voltage				12	V
V_{OL}	Output low level voltage	Isource < 4mA	0		0.4	V
I_{OH}	Maximum high level leakage current				10	µA
R_{puSMB_ALERT}	Internal pull up resistor on SMB_ALERT			None		kΩ

9.2 INTERFACING WITH SIGNALS

All signal pins have protection diodes implemented to protect internal circuits. When the power supply is not powered, the protection devices start clamping at signal pin voltages exceeding ±0.5V. Therefore all input signals should be driven only by an open collector/drain to prevent back feeding inputs when the power supply is switched off.

If interconnecting of signal pins of several power supplies is required, then this should be done by decoupling with small signal schottky diodes as shown in examples in Figure 22 (except for SMB_ALERT, ISHARE and I²C pins). This will ensure the pin voltage is not affected by an unpowered power supply.

SMB_ALERT pins can be interconnected without decoupling diodes, since these pins have no internal pull up resistor and use a 15V zener diode as protection device against positive voltage on pins.

ISHARE pins must be interconnected without any additional components. This in-/output also has a 15V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

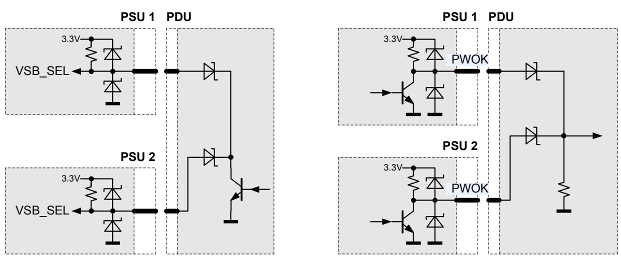


Figure 22: Interconnection of signal pins

9.3 FRONT LED

Table 3: LED Status

Operating Condition	LED Signaling
AC LED	
AC Line within range	Solid Green
AC Line UV condition	Off
DC LED [1]	
PSON High	Blinking Yellow (1:1)
Hot-Standby Mode	Blinking Yellow/Green (1:2)
V_1 or V_{SB} out of regulation	Solid Yellow
Over temperature shutdown	
Output over voltage shutdown (V_1 or V_{SB})	
Output over current shutdown (V_1 or V_{SB})	
Fan error (>15%)	
Over temperature warning	Blinking Yellow/Green (2:1)
Minor fan regulation error (>5%, <15%)	Blinking Yellow/Green (1:1)

[1] The order of the criteria in the table corresponds to the testing precedence in the controller.

The front-end has 2 front LEDs showing the status of the supply. LED number one is green and indicates AC power is on or off, while LED number two is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the position of the LEDs see Figure 42.

9.4 PRESENT_L

This signaling pin is recessed within the connector and will contact only once all other connector contacts are closed. This pin is used to indicate to a power distribution unit controller that a supply is plugged in. The maximum current on PRESENT_L pin should not exceed 10mA.

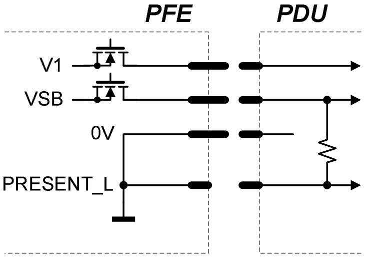


Figure 23: PRESENT_L signal pin

9.5 PSKILL INPUT

The PSKILL input is located on a recessed pin on the connector, and is used to enable the main output only when power supply is fully seated on the power distribution unit. This pin should be connected to SGND in the power distribution unit. The standby output will remain on regardless of the PSKILL input state.

9.6 AC TURN-ON / DROP-OUTS / ACOK

The power supply will automatically turn-on when connected to the AC line under the condition that the PSON signal is pulled low and the AC line is within range. The timing diagram is shown in Figure 24 and referenced in Table 4.

Table 4: AC Turn-on / Dip Timing

Operating Condition		Min	Max	Unit
$t_{AC\ VSB}$	AC Line to 90% V_{VSB}		2	sec
$t_{AC\ V1}$	AC Line to 90% V_1		2	sec
$t_{ACOK\ on1}$	ACOK signal on delay (start-up)		2000	ms
$t_{ACOK\ on2}$	ACOK signal on delay (dips)		100	ms
$t_{ACOK\ off}$	ACOK signal off delay		5	ms
$t_{VSB\ V1\ del}$	V_{SB} to V_1 delay	10	500	ms
$t_{V1\ holdup}$	Effective V_1 holdup time	12		ms
$t_{VSB\ holdup}$	Effective V_{SB} holdup time	20		ms
$t_{ACOK\ V1}$	ACOK to V_1 holdup	7		ms
$t_{ACOK\ VSB}$	ACOK to V_{SB} holdup	15		ms
$t_{V1\ off}$	Minimum V_1 off time	1000	1200	ms
$t_{VSB\ off}$	Minimum V_{SB} off time	1000	1200	ms

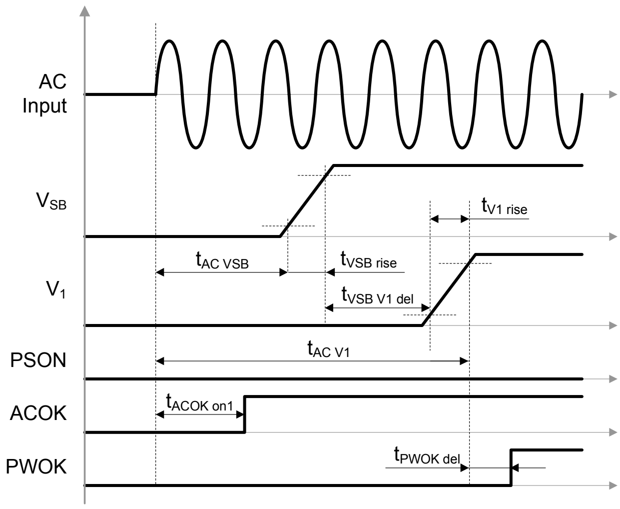


Figure 24: AC turn-on timing

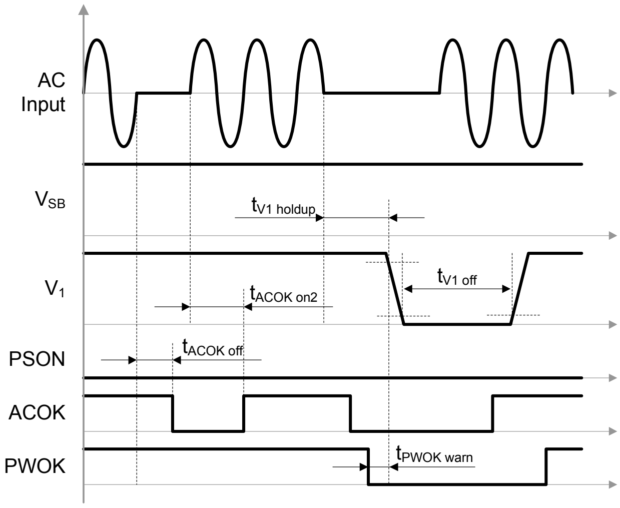


Figure 25: AC short dips

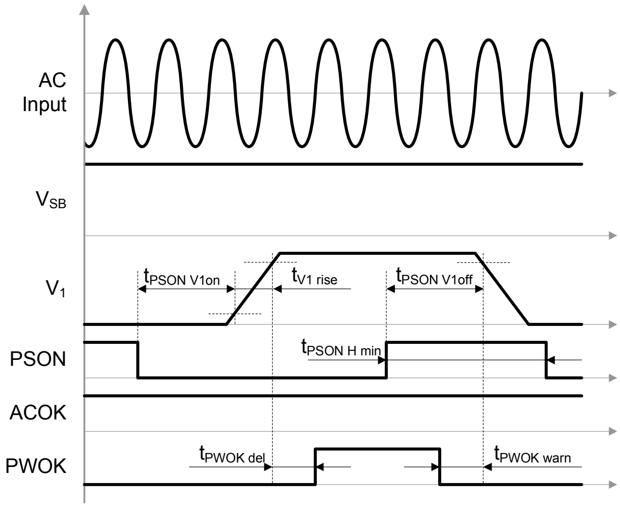


Figure 27: PSON turn-on/off timing

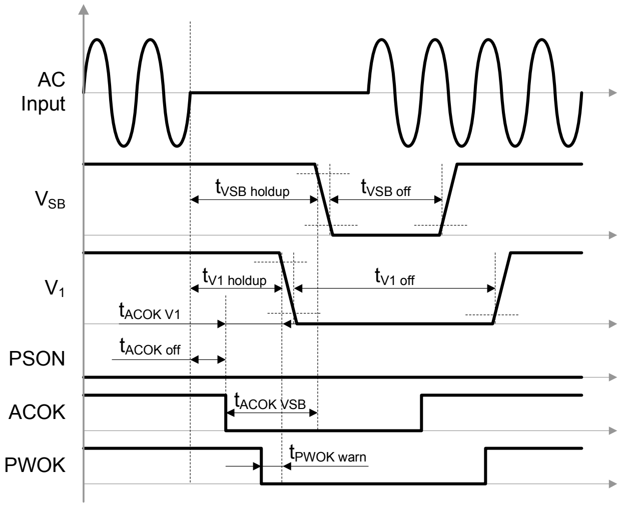


Figure 26: AC long dips

9.7 PSON INPUT

The PSON is an internally pulled-up (3.3V) input signal to enable / disable the main output V_1 of the front-end. The pin is also used to clear any latched fault condition. The timing diagram is given in Figure 27 and the table below.

Table 5: PSON timing

Operating Condition		Min	Max	Unit
$t_{PSON\ V1on}$	PSON to V_1 delay (on)	2	20	ms
$t_{PSON\ V1off}$	PSON to V_1 delay (off)	2	20	ms
$t_{PSON\ H\ min}$	PSON minimum High time	10		ms

9.8 PWOK SIGNAL

The PWOK is an open drain output with an internal pull-up to 3.3V indicating whether both V_{SB} and V_1 outputs are within regulation. The timing diagram is shown in Figure 24/Figure 27 and referenced in the following table .

Table 6: PWOK timing

Operating Condition		Min	Max	Unit
$t_{PWOK\ del}$	PWOK to V_1 delay (on)	100	500	ms
$t_{PWOK\ warn}$ *)	PWOK to V_1 delay (off) caused by:			
	PSKILL	0	1	ms
	PSON, ACOK, OT, Fan Failure	1	2.5	ms
	UV and OV on VSB	1	30	ms
	OC on V1 (Software trigger)	-11	0	ms
	OC on V1 (Hardware trigger)	-1	0	ms
	OV on V1	-3	0	ms

*) A positive value means a warning time, a negative value a delay (after fact).

9.9 CURRENT SHARE

The PFE front-ends have an active current share scheme implemented for V_1. All the CS current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its CS pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses a digital bi-directional data exchange on a recessive bus configuration to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV.

The standby output uses a passive current share method (droop output voltage characteristic).

9.10 SENSE INPUTS

Both main and standby outputs have sense lines implemented to compensate for voltage drop on load wires. The maximum allowed voltage drop is 200mV on the positive rail and 100mV on the PGND rail.

With open sense inputs the main output voltage will rise by 270mV and the standby output by 50mV. Therefore if not used, these inputs should be connected to the power output and PGND close to the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

9.11 HOT-STANDBY OPERATION

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable its DC/DC stage. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency. In order to enable the hot standby operation, the HOTSTANDBYEN and the CS pins need to be inter-connected. A power supply will only be allowed to enter the hot-standby mode, when the HOTSTANDBYEN pin is high, the load current is low (see Figure 28) and the supply was allowed to enter the hot-standby mode by the system controller via the appropriate I²C command (by default disabled). The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode.

If a power supply is in a fault condition, it will pull low its HOTSTANDBYEN pin which indicates to the other power supply that it is not allowed to enter the hot-standby mode or that it needs to return to normal operation should it already have been in the hot-standby mode.

Note: The system controller needs to ensure that only one of the power supplies is allowed to enter the hot-standby mode!

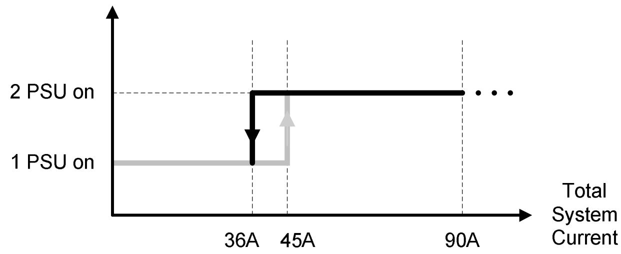


Figure 28: Hot-standby enable/disable current thresholds

Figure 29 shows the achievable power loss savings when using the hot-standby mode operation. A total power loss reduction of 45% is achievable.

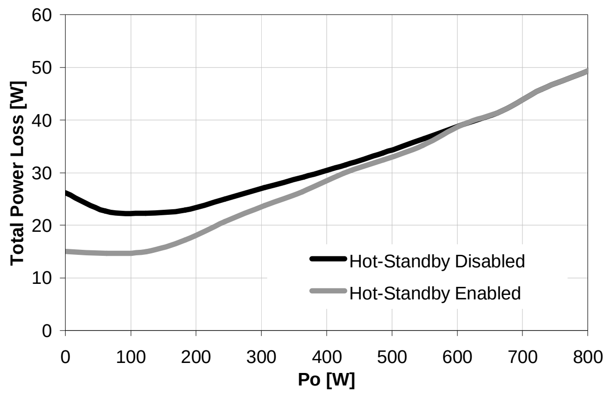


Figure 29: PSU power losses with/without hot-standby mode

In order to prevent voltage dips when the active power supply is unplugged while the other is in hot-standby mode, it is strongly recommended to add the external circuit as shown in Figure 30. If the PRESENT_L pin status needs also to be read by the system controller, it is recommended to exchange the bipolar transistors with small signal MOS transistors or with digital transistors.

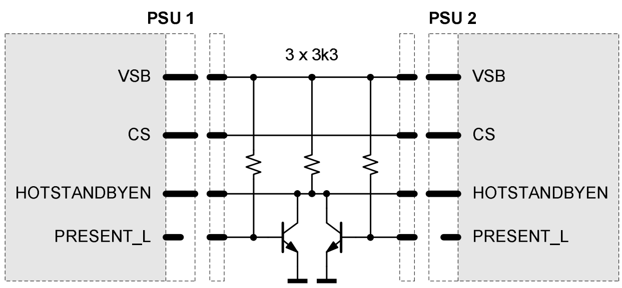


Figure 30: Recommended hot-standby configuration

9.12 I2C / SMBUS COMMUNICATION

The interface driver in the PFE supply is referenced to the V1 Return. The PFE supply is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in Table 7 further characterized through:

- There are no internal pull-up resistors
- The SDA/SCL IOs are 3.3/5V tolerant
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

The SMB_ALERT signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. The power supply responds to a read command on the general SMB_ALERT call address 25(0x19) by sending its status register.

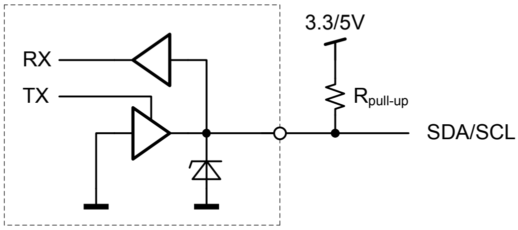


Figure 31: Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V1 output (provided e.g. by the redundant unit). If only VSB is provided, communication is not possible.

Table 7: I²C / SMBus Specification

Par	Description	Condition	Min	Max	Unit
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	5.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	Ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	Ns
I_i	Input current SCL/SDA	0.1VDD < Vi < 0.9VDD	-10	10	μA
C_i	Capacitance for each SCL/SDA			10	pF
f_{SCL}	SCL clock frequency		0	100	kHz
R_{pu}	External pull-up resistor	$f_{SCL} \le 100$ kHz		1000ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	4.0		μs
t_{LOW}	Low period of the SCL clock	$f_{SCL} \le 100$ kHz	4.7		μs
t_{HIGH}	High period of the SCL clock	$f_{SCL} \le 100$ kHz	4.0		μs
t_{SUSTA}	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	4.7		μs
t_{HDDAT}	Data hold time	$f_{SCL} \le 100$ kHz	0	3.45	μs
t_{SUDAT}	Data setup time	$f_{SCL} \le 100$ kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	$f_{SCL} \le 100$ kHz	4.0		μs
t_{BUF}	Bus free time between STOP and START	$f_{SCL} \le 100$ kHz	4.7		μs

[1] C_b = capacitance of one bus line in pF, typically in the range 10 pF … 400 pF

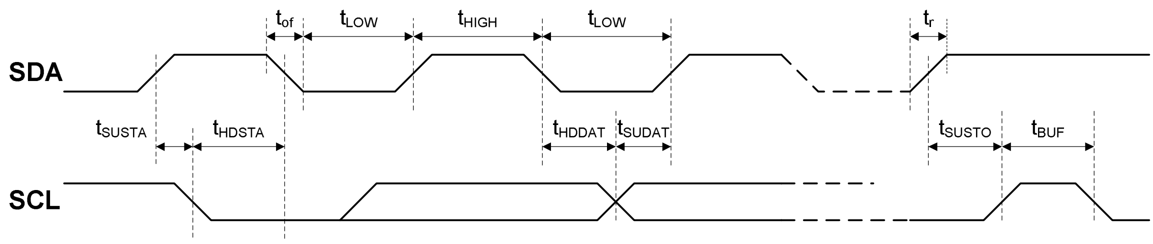


Figure 32: I2C / SMBus Timing

9.13 ADDRESS/PROTOCOL SELECTION (APS)

The APS pin provides the possibility to select the communication protocol and address by connecting a resistor to V1 return (0V). A fixed addressing offset exists between the Controller and the EEPROM.

Note

- If the APS pin is left open, the supply will operate with the PSMI protocol at controller / EEPROM addresses 0xB6 / 0xA6.
- The ASP pin is only read at start-up of the power supply. Therefore it is not possible to change the communication protocol and address dynamically.

Table 8: Address and protocol encoding

R_{APS} (Ω) 1)	Protocol	I2C Address 2)	
		Controller	EEPROM
820	PMBus™	0xB0	0xA0
2700		0xB2	0xA2
5600		0xB4	0xA4
8200		0xB6	0xA6
15000	PSMI	0xB0	0xA0
27000		0xB2	0xA2
56000		0xB4	0xA4
180000		0xB6	0xA6

1) E12 resistor values, use max 5% resistors, see also Figure 33.
2) The LSB of the address byte is the R/W bit.

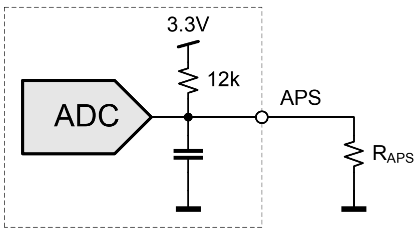


Figure 33: I2C address and protocol setting

9.14 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 34). An I2C driver device assures logic level shifting (3.3 / 5V) and a glitch-free clock stretching. The driver also pulls the SDA/SCL line to nearly 0V when driven low by the DSP or the EEPROM providing maximum flexibility when additional external bus repeaters are needed. Such repeaters usually encode the low state with different voltage levels depending on the transmission direction.

The DSP will automatically set the I2C address of the EEPROM with the necessary offset when its own address is changed / set. In order to write to the EEPROM, first the write protection needs to be disabled by sending the appropriate command to the DSP. By default the write protection is on.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

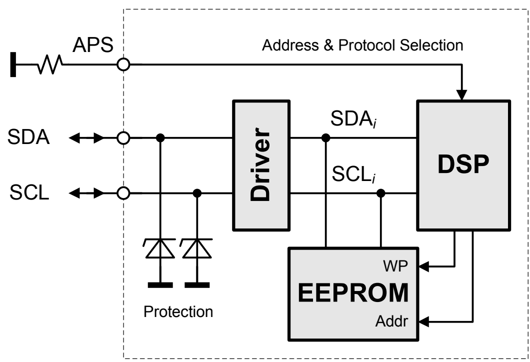


Figure 34: I2C Bus to DSP and EEPROM

9.15 EEPROM PROTOCOL

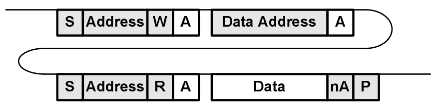
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



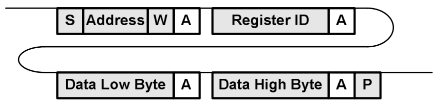
9.16 PSMI PROTOCOL

New power management features in computer systems require the system to communicate with the power supply to access current, voltage, fan speed, and temperature information. Current measurements provide data to the system for determining potential system configuration limitations and provide actual system power consumption for facility planning. Temperature and fan monitoring allow the system to better manage fan speeds and temperatures for optimizing system acoustics. Voltage monitoring allows the system to calculate input wattage and warning of system voltage regulation problems. The Power Supply Management Interface (PSMI) supports diagnostic capabilities and allows managing of redundant power supplies. The communication method is SMBus. The current design guideline is version 2.12.

The communication protocol is register based and defines a read and write communication protocol to read / write to a single register address. All registers are accessed via the same basic command given below. No PEC (Packet Error Code) is used.

WRITE

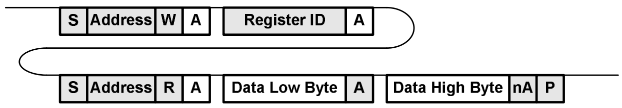
The write protocol used is the SMBus 2.0 Write Word protocol. All writes are 16-bit words; byte reads are not supported nor allowed. The shaded areas in the figure indicate bits and bytes written by the PSMI master device.



See PFE Programming Manual for further information.

READ

The read protocol used is the SMBus 2.0 Read Word protocol. All reads are 16-bit words; byte reads are not supported nor allowed. The shaded areas in the figure indicate bits and bytes written by the PSMI master device.



See PFE Programming Manual for further information.

9.17 PMBus™ PROTOCOL

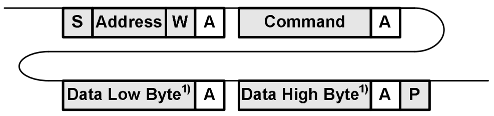
The Power Management Bus (PMBus™) is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at www.powerSIG.org.

PMBus™ command codes are not register addresses. They describe a specific command to be executed. The PFE1100-12-054NA supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

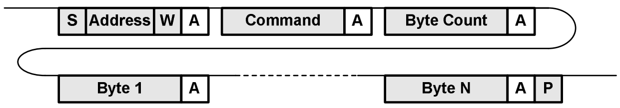
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



1) Optional

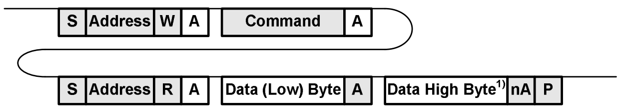
In addition, Block write commands are supported with a total maximum length of 255 bytes.



See PFE Programming Manual for further information.

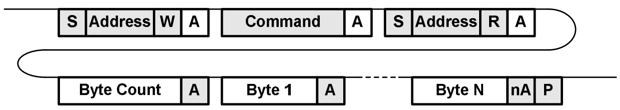
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.



See PFE Programming Manual BCA.00006 for further information.

9.18 GRAPHICAL USER INTERFACE

Power-One provides with its "Power-One I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE1100-12-054NA Front-End. The utility can be downloaded on www.power-one.com and supports both the PSMI and PMBus™ protocols.

The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.

If the GUI is used in conjunction with the PFE1100-12-054NA Evaluation Kit it is also possible to control the PSON pin(s) of the power supply.

Further there is a button to disable the internal fan for approximately 10 seconds. This allows the user to take input power measurements without fan consumptions to check efficiency compliance to the Climate Saver Computing Platinum specification.

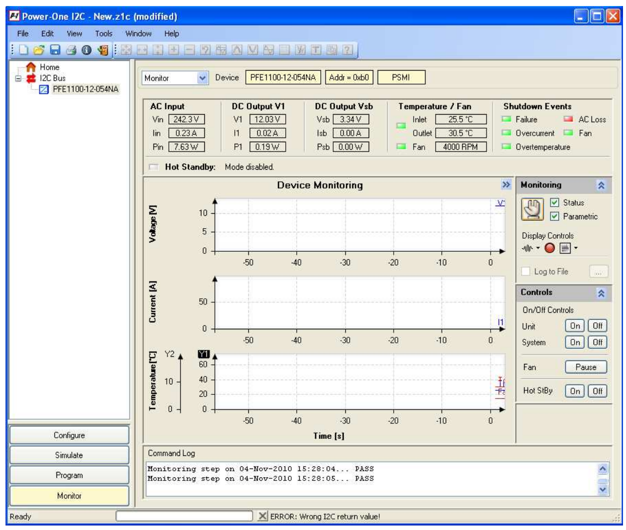


Figure 35: I²C Bus to DSP and EEPROM

The monitoring screen also allows to enable the hot-standby mode on the power supply. The mode status is monitored and by changing the load current it can be monitored when the power supply is being disabled for further energy savings. This obviously requires 2 power supplies being operated as a redundant system (like the evaluation kit).

Note: The user of the GUI needs to ensure that only one of the power supplies have the hot-standby mode enabled.

10 TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the airflow at the rear of the supply by placing large objects directly at the output connector. The PFE1100-12-054NA is provided with a normal airflow, which means the air enters through the rear of the supply and leaves at the front. PFE supplies have been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The hot air is exiting the power supply unit on the front. The temperature on the handle and the front are remaining below 85 °C (at an inlet temperature of 45 °C) as defined as maximum temperature in IEC 60950 for touchable plastic knobs / handles. The IEC connector on the unit is rated 105 °C, but the mating connector used might only be rated to 70 °C. In such cases the input power at low line needs to be further derated to meet a maximum temperature at the front of 70 °C (see Figure 38).

Note: It is the responsibility of the user to check the front temperature in such cases. The unit is not limiting its power automatically to meet such a temperature limitation.

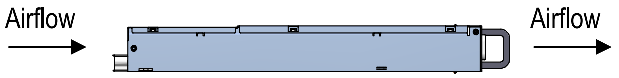


Figure 36: Airflow direction

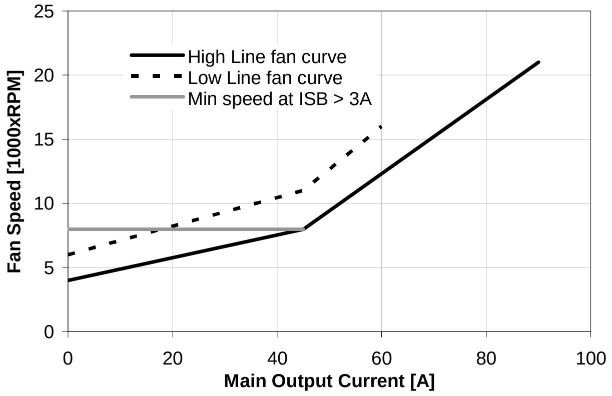


Figure 37: Fan speed vs. main output load

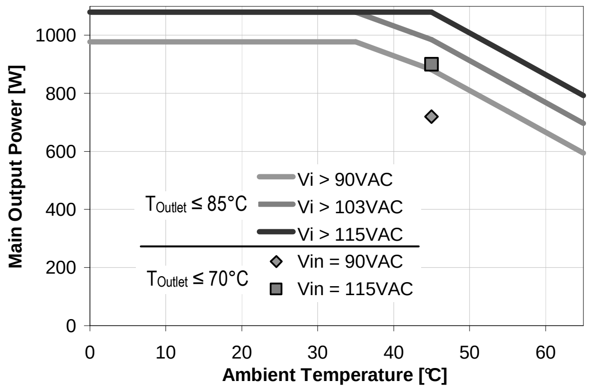


Figure 38: Thermal derating

11 ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

Note: Most of the immunity requirements are derived from EN 55024:1998/A2:2003.

Test	Standard / Description	Criteria
ESD Contact Discharge	IEC / EN 61000-4-2, ±8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body)	B
ESD Air Discharge	IEC / EN 61000-4-2, ±15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces)	B
Radiated Electromagnetic Field	IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 µs Pulse Modulation, 10 kHz…2 GHz	A
Burst	IEC / EN 61000-4-4, level 3 AC port ±2 kV, 1 minute DC port ±1 kV, 1 minute	B
Surge	IEC / EN 61000-4-5 Line to earth: level 3, ±2 kV Line to line: level 2, ±1 kV	 VSB: A, V1: B[2] A
RF Conducted Immunity	IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A
Voltage Dips and Interruptions	IEC/EN 61000-4-11 1: Vi 230V, 100% Load, Phase 0°, Dip 100%, Duration 10 ms 2: Vi 230V, 100% Load, Phase 0°, Dip 100%, Duration 20 ms 3: Vi 230V, 100% Load, Phase 0°, Dip 100%, Duration >20ms	 A VSB: A, V1: B VSB, V1: B

11.2 EMISSION

Test	Standard / Description	Criteria
Conducted Emission	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single unit	Class A 6 dB margin
	EN55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 units in rack system	Class A 6 dB margin
Radiated Emission	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, single unit	Class A 6 dB margin
	EN55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 units in rack system	Class A 6 dB margin
Harmonic Emissions	IEC61000-3-2, Vin = 100 VAC/ 60 Hz, 100% Load	Class A
	IEC61000-3-2, Vin = 120 VAC/ 60 Hz, 100% Load	Class A
	IEC61000-3-2, Vin = 200 VAC/ 60 Hz, 100% Load	Class A
	IEC61000-3-2, Vin = 230 VAC/ 50 Hz, 100% Load	Class A
	IEC61000-3-2, Vin = 240 VAC/ 50 Hz, 100% Load	Class A
Acoustical Noise	Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load	42 dBA
AC Flicker	IEC / EN 61000-3-3, d_{max} < 3.3%	PASS

[2] V_1 drops to 90 … 97% $V_{1\ nom}$ for 3ms

12 SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Power-One will not honor any warranty claims resulting from electric strength field tests.

Parameter		Description / Conditions	Min	Nom	Max	Unit
	Agency Approvals	UL 60950-1 Second Edition CAN/CSA-C22.2 No. 60950-1-07 Second Edition IEC 60950-1:2005 EN 60950-1:2006		Approved by independent body (see CE Declaration)		
	Isolation strength	Input (L/N) to case (PE)		Basic		
		Input (L/N) to output		Reinforced		
		Output to case (PE)		Functional		
d_C	Creepage / clearance	Primary (L/N) to protective earth (PE)		According to safety standard		mm
		Primary to secondary				mm
	Electrical strength test	Input to case				kVAC
		Input to output				kVAC
		Output and Signals to case				kVAC

13 MECHANICAL

13.1 DIMENSIONS

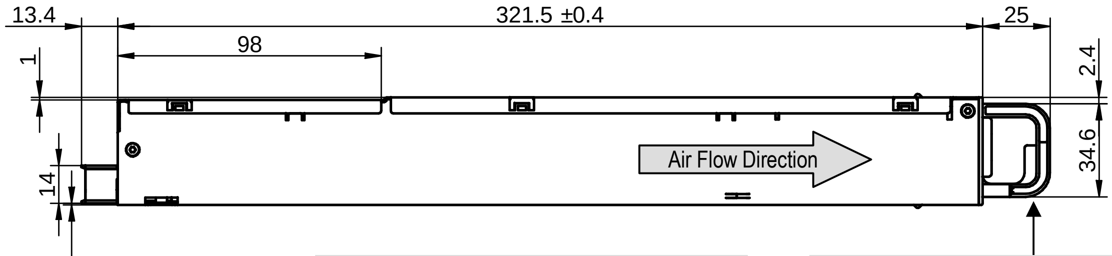


Figure 39: Side view 1

Note: A 3D step file of the power supply casing is available on request.

Note: Unlatching the supply is performed by pulling the green trigger in the handle.

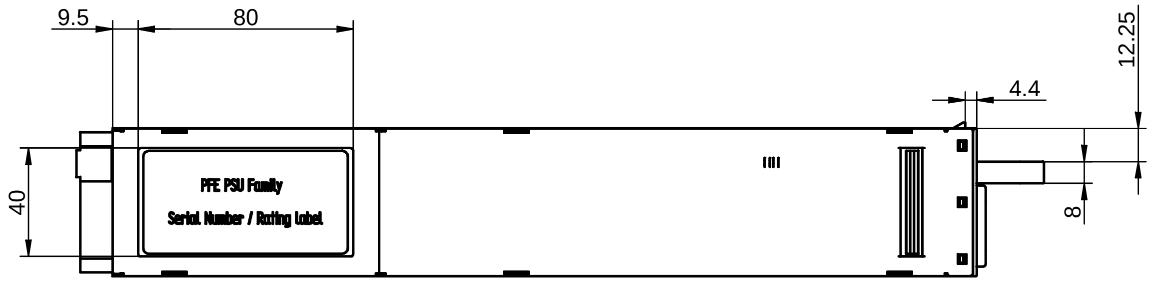


Figure 40: Top view

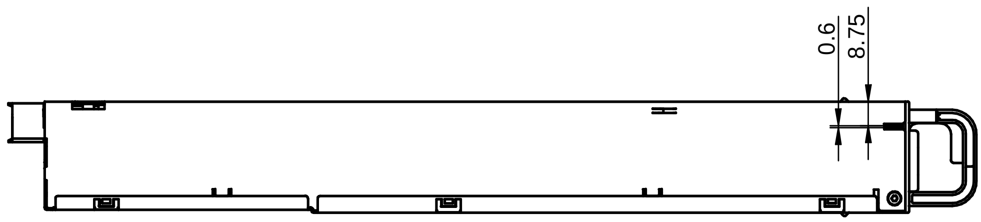


Figure 41: Side view 2

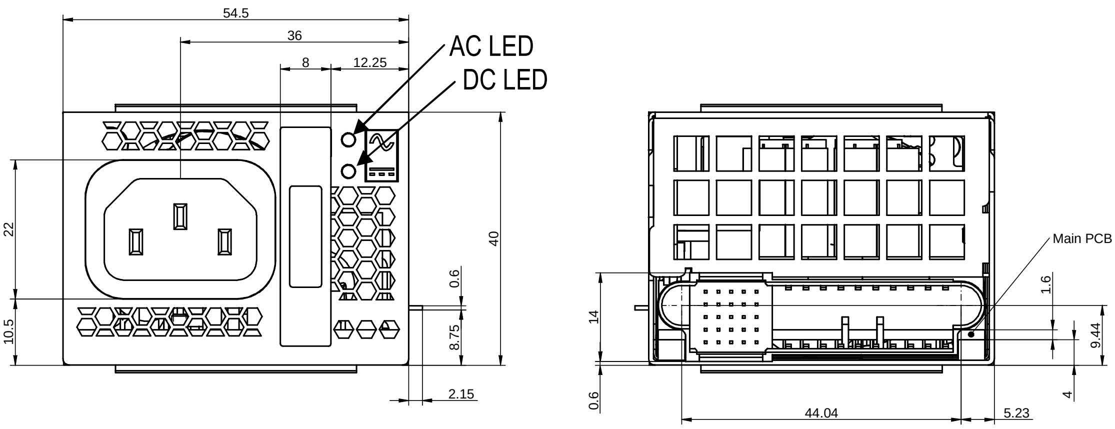
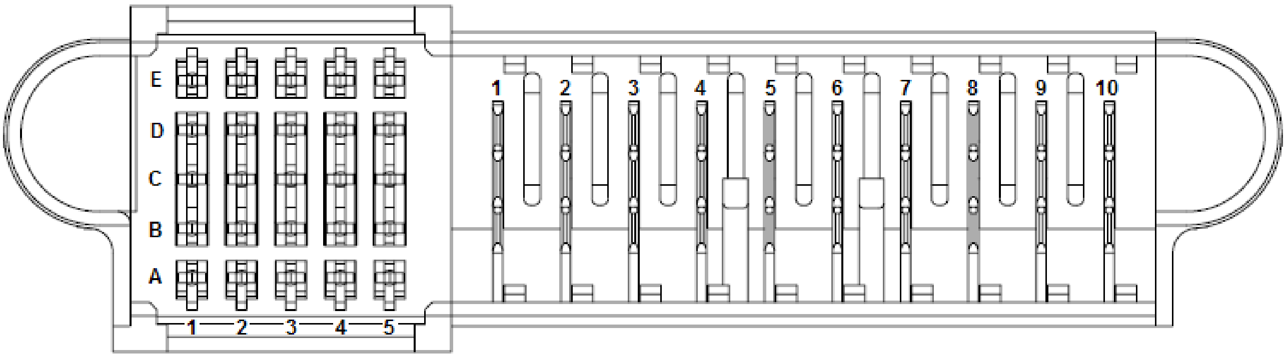


Figure 42: Front view

13.2 CONNECTIONS



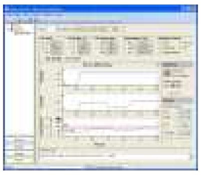
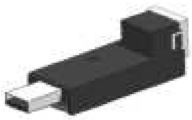
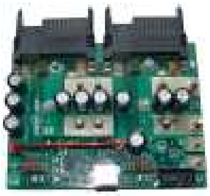
Unit: Tyco Electronics P/N 2-1926736-3

Counter part: Tyco Electronics P/N 2-1926733-5

Note: Column 5 is lagging (short pins)

Pin	Name	Description
Output		
6, 7, 8, 9, 10	V1	+12 VDC main output
1, 2, 3, 4, 5	PGND	Power ground (return)
Control Pins		
A1	VSB	Standby positive output (+3.3/5 V)
B1	VSB	Standby positive output (+3.3/5 V)
C1	VSB	Standby positive output (+3.3/5 V)
D1	VSB	Standby positive output (+3.3/5 V)
E1	VSB	Standby positive output (+3.3/5 V)
A2	SGND	Signal ground (return)
B2	SGND	Signal ground (return)
C2	HOTSTANDBYEN	Hot standby enable signal
D2	VSB_SENSE_R	Standby output negative sense
E2	VSB_SENSE	Standby output positive sense
A3	APS	I^2C address and protocol selection (select by a pull down resistor)
B3	nc	Reserved
C3	SDA	I^2C data signal line
D3	V1_SENSE_R	Main output negative sense
E3	V1_SENSE	Main output positive sense
A4	SCL	I^2C clock signal line
B4	PSON	Power supply on input (connect to A2/B2 to turn unit on)
C4	SMB_ALERT	SMB Alert signal output
D4	nc	Reserved
E4	ACOK	AC input OK signal
A5	PSKILL	Power supply kill (lagging pin)
B5	ISHARE	Current share bus (lagging pin)
C5	PWOK	Power OK signal output (lagging pin)
D5	VSB_SEL	Standby voltage selection (lagging pin)
E5	PRESENT_L	Power supply present (lagging pin)

14 ACCESSORIES

Item	Description	Ordering Part Number	Source
	**Power-One I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor PFE Front-Ends (and other I²C units)	N/A	www.power-one.com
	**USB to I²C Converter** Master I²C device to program, control and monitor I²C units in conjunction with the *Power-One I²C Utility*	ZM-00056	Power-One
	**Dual Connector Board** Connector board to operate 2 PFE units in parallel. Includes an on-board USB to I²C converter (use *Power-One I²C Utility* as desktop software).	SNP-OP-BOARD-01	Power-One