

# NUP4105MU

## Low Capacitance ESD Protection Array for High Speed Data Lines Protection

The NUP4105MU transient voltage suppressor is designed to protect high speed data lines from ESD, EFT, and lightning.

### Features

- Low Capacitance (5 pF Maximum Between I/O Lines and GND)
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (ESD) Level 4 – 18 kV (Contact)
- This is a Pb-Free Device

### Typical Applications

- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI)
- Monitors and Flat Panel Displays
- T1/E1 and T3/E3

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation	P <sub>pk</sub>	450	W
Maximum Peak Pulse Current 8 x 20 μS @ T <sub>A</sub> = 25°C (Note 1)	I <sub>pp</sub>	26	A
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact (ESD)	ESD	16000 400 18000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Non-repetitive current pulse per Figure 1 (Pin 5 to GND Pad)

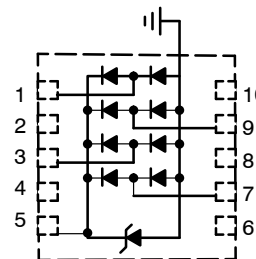


ON Semiconductor®

<http://onsemi.com>

## LOW CAPACITANCE DIODE TVS ARRAY

### PIN CONFIGURATION AND SCHEMATIC



UDFN10  
CASE 517AN

### MARKING DIAGRAM



- 4105 = Specific Device Code
- AA = Assembly Location
- Y = Year
- W = Work Week
- = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NUP4105MUTAG	UDFN10 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NUP4105MU

## ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	(Note 2)			3.3	V
Breakdown Voltage	$V_{BR}$	$I_T=1\text{ mA}$ , (Note 3)	5.0	5.3		V
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3\text{ V}$			5.0	$\mu\text{A}$
Clamping Voltage	$V_C$	$I_{PP} = 1\text{ A}$ (Note 4)			6.2	V
Clamping Voltage	$V_C$	$I_{PP} = 10\text{ A}$ (Note 4)			10	V
Clamping Voltage	$V_C$	$I_{PP} = 25\text{ A}$ (Note 4)			14	V
Maximum Peak Pulse Current	$I_{PP}$	$8 \times 20\ \mu\text{s}$ Waveform			26	A
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f=1\text{ MHz}$ between I/O Pins and GND		3.0	5.0	pF
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f=1\text{ MHz}$ between I/O Pins		1.5	3.0	pF

- TVS devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
- $V_{BR}$  is measured at pulse test current  $I_T$ .
- Non-repetitive current pulse per Figure 1 (Pin 5 to GND Pad)

## TYPICAL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

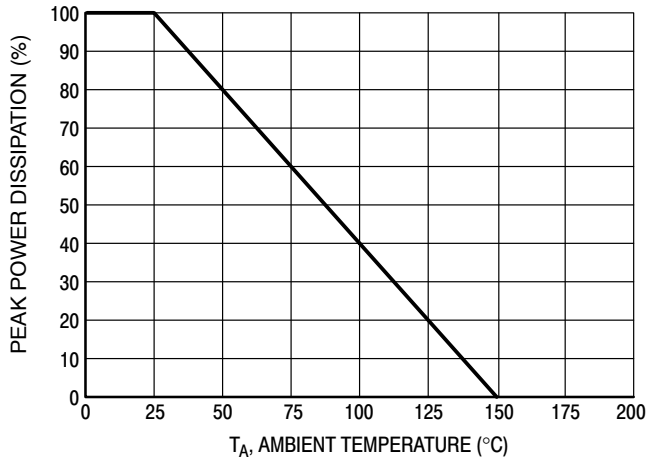


Figure 1. Pulse Derating Curve

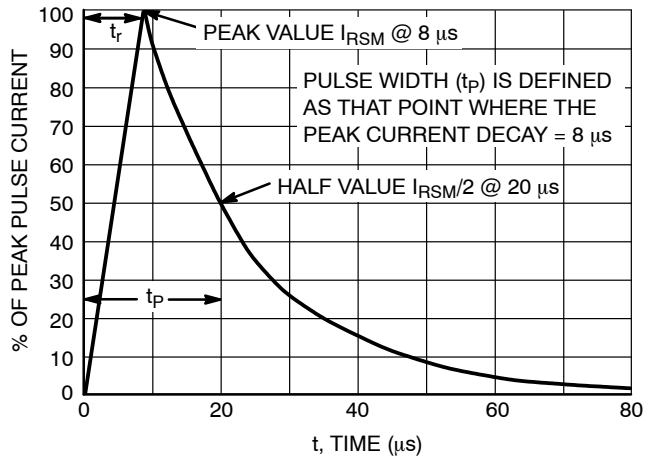
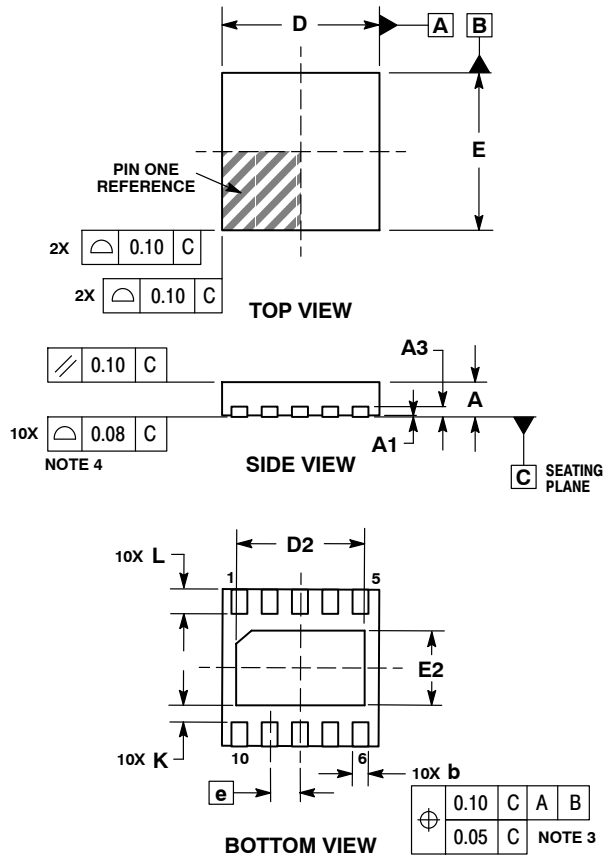


Figure 2.  $8 \times 20\ \mu\text{s}$  Pulse Waveform

# NUP4105MU

## PACKAGE DIMENSIONS

UDFN10 2.6x2.6, 0.5P  
CASE 517AN-01  
ISSUE O

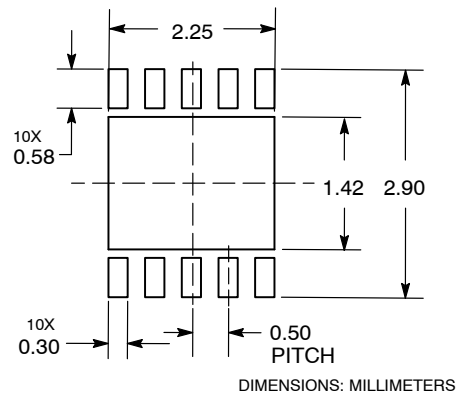


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	2.60 BSC	
D2	2.00	2.25
E	2.60 BSC	
E2	1.11	1.36
e	0.50 BSC	
K	0.20	---
L	0.30	0.40

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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