TEA2096T

GreenChip dual synchronous rectifier controller

Rev. 1 — 9 September 2022 Product data sheet

1 General description

The TEA2096T is a new synchronous rectifier (SR) controller IC for switched-mode power supplies. It incorporates an adaptive gate drive method for maximum efficiency at any load.

The TEA2096T is a dedicated controller IC for synchronous rectification on the secondary side of resonant converters. It has two driver stages for driving the SR MOSFETs, which rectify the outputs of the central tap secondary transformer windings. The two gate driver stages have their own sensing inputs and operate independently.

The TEA2096T is optimized for efficient operation with very low-ohmic MOSFETs and switching at high frequencies.

The TEA2096T is fabricated in a silicon-on-insulator (SOI) process.

2 Features and benefits

2.1 Efficiency features

- Adaptive gate drive for maximum efficiency at any load
- Supply current in energy save operation of 80 µA
- Regulation level of −29 mV for driving low-ohmic MOSFETs

2.2 Application features

- Drain sense voltage to 200 V
- Wide supply voltage range from 4.5 V to 38 V
- Dual synchronous rectification for LLC resonant
- Supports 5 V operation with logic level SR MOSFETs
- Differential inputs for sensing the drain and source voltages of each SR MOSFET
- SO8 package

2.3 Control features

- SR control without minimum on-time
- Adaptive gate drive for fast turn-off at the end of conduction
- Undervoltage lockout (UVLO) protection with active gate pull-down
- Interlock function to prevent simultaneous conduction of the external MOSFETs
- Supports 1 MHz switching frequency

3 Applications

The TEA2096T is intended for resonant power supplies. In such applications, it can drive two external synchronous rectifier MOSFETs for the rectification of the voltages on the two secondary windings of the transformer. These MOSFETs replace diodes. It can be used in all power supplies requiring high efficiency:

- Adapters
- Power supplies for desktop PC and all-in-one PC
- Power supplies for television
- Power supplies for servers
- Power supplies for industrial applications

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA2096T/1	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 Marking

Table 2. Marking

Type number	Marking code
TEA2096T/1	TEA2096

6 Block diagram

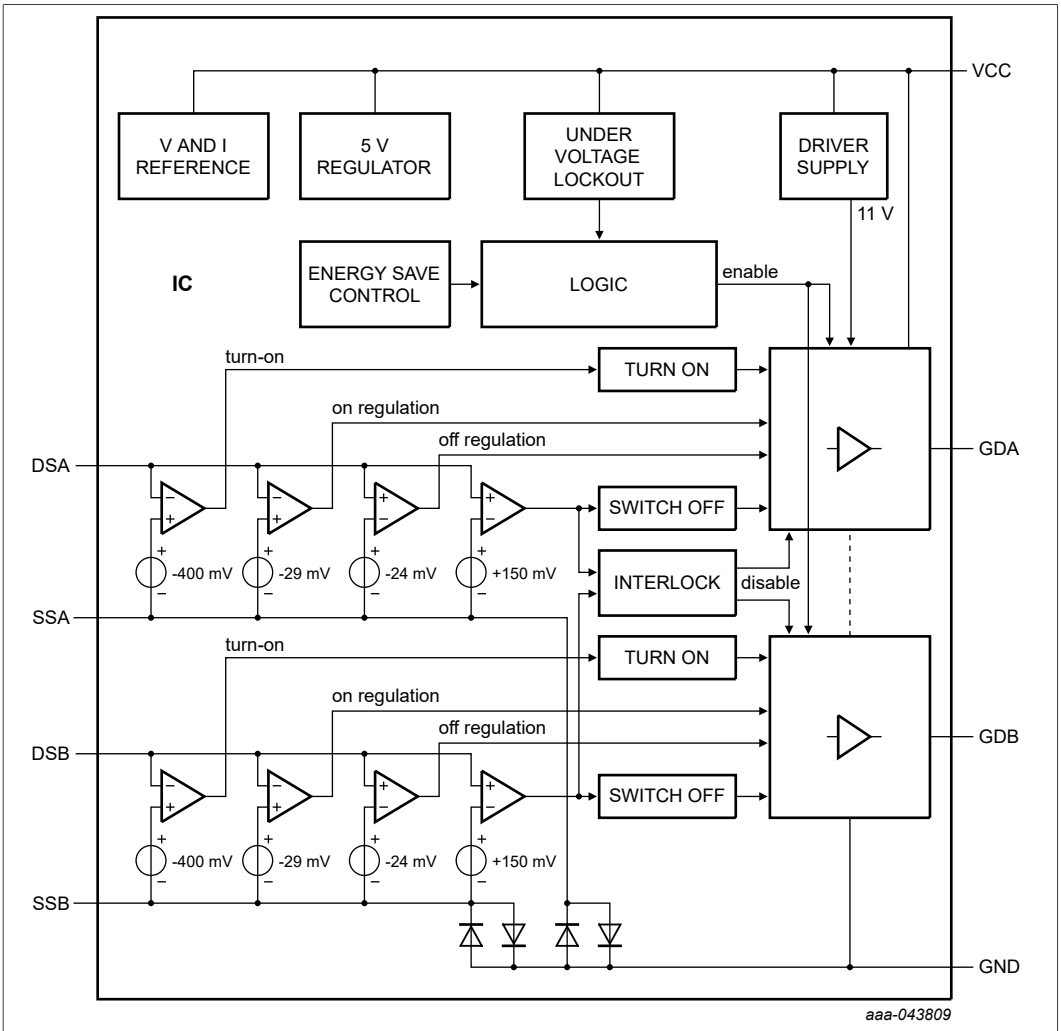


Figure 1. TEA2096T block diagram

7 Pinning information

7.1 Pinning

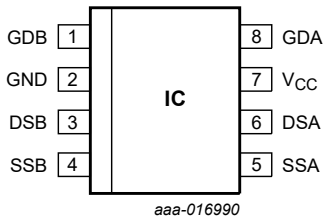


Figure 2. TEA2096T pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GDB	1	gate drive output MOSFET B
GND	2	ground
DSB	3	drain sense input for synchronous timing MOSFET B
SSB	4	source sense input MOSFET B
SSA	5	source sense input MOSFET A
DSA	6	drain sense input for synchronous timing MOSFET A
V_{CC}	7	supply voltage
GDA	8	gate drive output MOSFET A

8 Functional description

8.1 Introduction

The TEA2096T is a controller IC for synchronous rectification. It is perfectly suited to be used in resonant applications. It can drive two synchronous rectifier MOSFETs on the secondary side of the central tap transformer winding. Figure 3 shows a typical configuration.

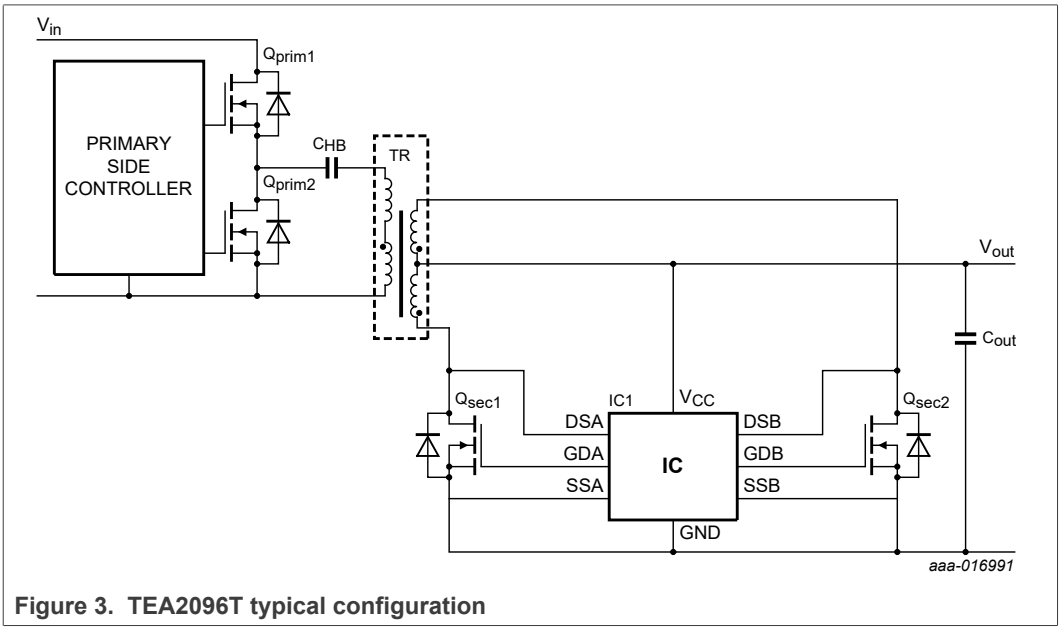


Figure 3. TEA2096T typical configuration

8.2 Start-up and undervoltage lockout (V_{CC} pin)

When the voltage on the V_{CC} pin exceeds V_{start}, the IC leaves the UVLO state and activates the SR circuitry. When the voltage drops to below V_{stop}, the IC reenters the UVLO state. The SR MOSFET gate driver outputs are actively kept low. For proper operation, the V_{CC} pin must be decoupled with an extra capacitor (not only with C_{out}) between the V_{CC} pin and the GND pin. To reduce inductance effects because of high gate driver currents, the extra capacitor must be connected as close as possible to the IC.

8.3 Drain sense (DSA and DSB pins)

The drain sense pins are input pins capable of handling input voltages up to 200 V. At positive drain sense voltages, the gate driver is in off-mode with pulled-down gate driver pins (pins GDA or GDB). At negative drain sense voltages, the IC enables the SR through sensing the drain source differential voltage.

8.4 Synchronous rectification (SR; DSA, SSA, DSB, and SSB pins)

The IC senses the voltage difference between the drain sense (pins DSA and DSB) and the source sense (pins SSA and SSB) connections. The drain source differential voltage of the SR MOSFET is used to drive the gate of the SR MOSFET.

When this absolute voltage difference is higher than $V_{act(drv)}$, the corresponding gate driver output turns on the external SR MOSFET. When the external SR MOSFET is switched on, the absolute voltage difference between the drain and the source sense connections drops to below $V_{act(drv)}$. The regulation phase follows the turn-on phase.

In the regulation phase, the IC regulates the difference between the drain and the source sense inputs to an absolute level ($V_{reg(drv)}$). When the absolute difference is higher than $V_{reg(drv)}$, the gate driver output increases the gate voltage of the external SR MOSFET until the $V_{reg(drv)}$ level is reached. The SR MOSFET does not switch off at low currents. The IC operates without minimum on-time.

When the absolute difference is lower than $V_{deact(drv)}$, the gate driver output decreases the gate voltage of the external SR MOSFET. The voltage waveform on the gate of the SR MOSFET follows the waveform of the current through the SR MOSFET. When the current through the external SR MOSFET reaches zero, the SR MOSFET is quickly switched off.

After the SR MOSFET switch-off, the drain voltage increases. For a drain voltage above V_{swoff}, a low ohmic gate pull-down of $R_{pd(G)}$ keeps the gate of the SR MOSFET switched off.

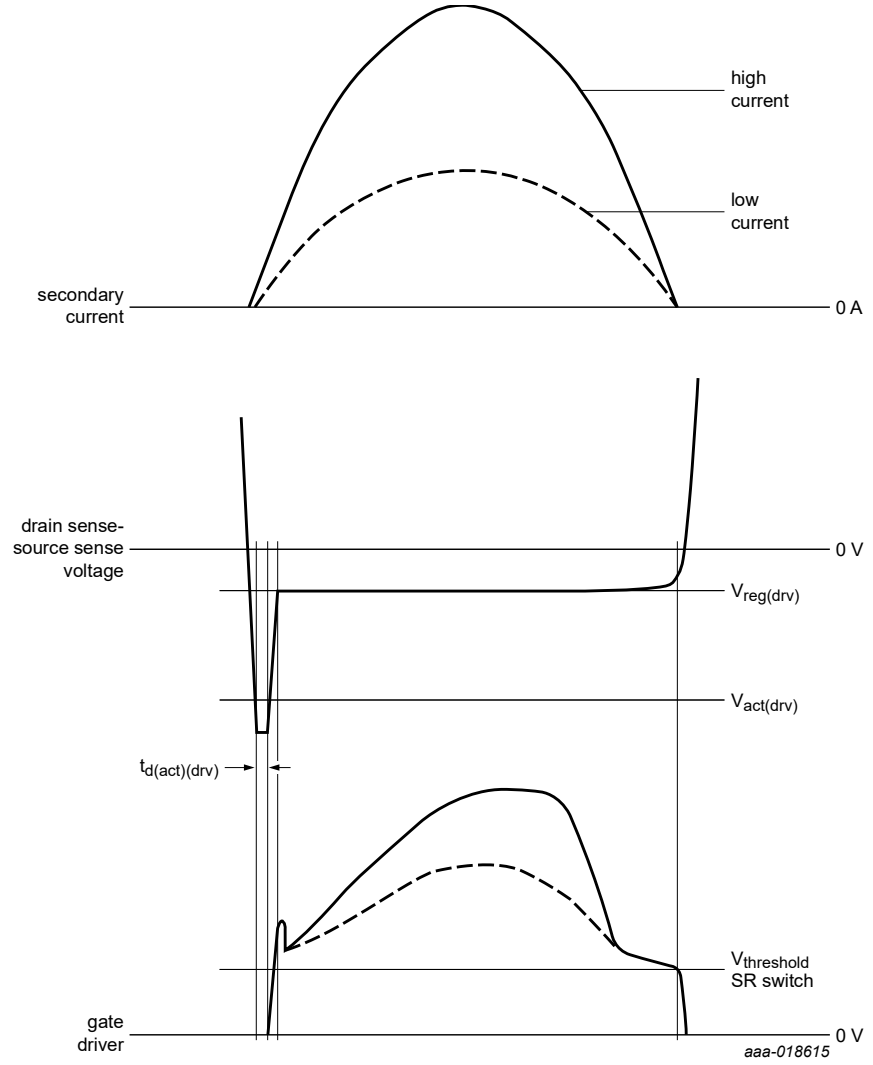


Figure 4. Synchronous rectification signals

8.5 Gate driver (GDA and GDB pins)

The gate driver circuit charges the gate of the external SR MOSFET during the rising part of the current. The driver circuit discharges the gate during the falling part of the current. The gate driver has a source capability of typically I_{source} and a sink capability of typically I_{sink}. The source and sink capability allow a fast turn-on and a fast turn-off of the external SR MOSFET.

The maximum driver output voltage is limited to $V_{G(max)}$. This high output voltage drives all MOSFET brands to the minimum on-state resistance.

In applications where the IC is supplied with 5 V, the maximum output voltage of the driver is limited to 5 V. Logic level SR MOSFETs can be used.

During start-up conditions ($V_{CC} < V_{start}$) and UVLO, the driver output voltage is actively pulled low.

8.6 Source sense connection (SSA and SSB pins)

The IC is equipped with additional source sense pins (SSA and SSB). These pins are used for the measurement of the SR MOSFET drain-to-source voltage. The source sense input must be connected as close as possible to the source pin of the external SR MOSFET. It minimizes errors caused by voltage difference on PCB tracks because of parasitic inductance in combination with large dI/dt values.

8.7 Interlock function

The TEA2096T incorporates an interlock function. The interlock function avoids the turn-on of both gate driver outputs at the same time.

After turn-off of one gate driver output, the IC waits typically 200 ns ($t_{d(interlock)}$) before turning on the other gate driver output.

9 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage			−0.4	+38	V
$V_{sense(D)A}$	drain sense voltage A	DC		−0.8	+200	V
$V_{sense(D)B}$	drain sense voltage B	DC		−0.8	+200	V
$V_{sense(S)A}$	source sense voltage A	DC		−0.4	+0.4	V
$V_{sense(S)B}$	source sense voltage B	DC		−0.4	+0.4	V
V_{GDA}	voltage on pin GDA	DC	[1]	−0.4	+12.0	V
V_{GDB}	voltage on pin GDB	DC	[1]	−0.4	+12.0	V
General						
f_{max}	maximum frequency	if not limited by T_j		-	1	MHz
T_{stg}	storage temperature			−55	+150	°C
T_j	junction temperature			−40	+150	°C
Electrostatic discharge (ESD)						
V_{ESD}	electrostatic discharge voltage	human body model (HBM)	[2]	-	2000	V
		charged device model (CDM)	[3]	-	500	V

[1] Output pin; not to be voltage driven.
[2] Human body model: Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
[3] Charged device model: Equivalent to charging the IC and discharging each pin over a 1 Ω resistor.

10 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.75	38	V
T_j	junction temperature		−40	+125	°C

11 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8 package; PCB 1 layer; 35 µm Cu; 60 mm x 125 mm	135	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	SO8 package	50	K/W

12 Characteristics

Table 7. Characteristics

T_{amb} = 25 °C; V_{CC} = 12 V; C_{GDA}/C_{GDB} = 10 nF (capacitors between GDA and GND and between GDB and GND). All voltages are measured with respect to ground (pin 2). Currents are positive when flowing into the IC, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage management (pin V_{CC})						
V_{start}	start voltage		4.3	4.5	4.7	V
V_{stop}	stop voltage		4.0	4.2	4.4	V
$I_{CC(oper)}$	operating supply current	energy-save	60	80	100	µA
		normal operation (without gate charge)	0.6	0.8	1.1	mA
$t_{act(es)}$	energy save mode activation time		85	110	135	µs
Synchronous rectification sense input (pins DSA, SSA, DSB, and SSB)						
$V_{act(drv)}$	driver activation voltage	$V_{sense(S)A}$/$V_{sense(S)B}$ = 0 V	−450	−400	−350	mV
$V_{reg(drv)}$	driver regulation voltage	$V_{sense(S)A}$/$V_{sense(S)B}$ = 0 V	−36	−29	−23	mV
V_{swoff}	switch-off voltage	$V_{sense(S)A}$/$V_{sense(S)B}$ = 0 V	60	150	200	mV
$t_{d(act)(drv)}$	driver activation delay time	$V_{sense(S)A}$/$V_{sense(S)B}$ = 0 V; normal operation; time from step on V_{DSA}/V_{DSB} (2 V to −0.5 V) to rising of V_{GDA}/V_{GDB} at 10 % of end value	-	80	-	ns
$t_{d(deact)(drv)}$	driver deactivation delay time	$V_{sense(S)A}$/$V_{sense(S)B}$ = 0 V; normal operation; time from step on V_{DSA}/V_{DSB} (−0.5 V to 2 V) to falling of V_{GDA}/V_{GDB} at 90 % of begin value	-	40	-	ns
t_d	delay time	interlock delay time	-	200	-	ns
Gate driver (pins GDA and GDB)						
I_{source}	source current	peak current at V_{DS} = −0.5 V; V_G = 0 V	-	−0.3	-	A
I_{sink}	sink current	regulation current at V_{DS} = 0 V; V_G = 5 V	-	1	-	A
		peak current at V_{DS} = 0.25 V; V_G = 5 V	-	2	-	A
$R_{pd(G)}$	gate pull-down resistance	V_{DS} = 12 V; I_G = 100 mA	2	2.5	3	Ω
$V_{G(max)}$	maximum gate voltage	V_{GDA}/V_{GDB} at V_{CC} = 5 V	4.98	4.99	5	V
		V_{GDA}/V_{GDB} at V_{CC} = 12 V	10.4	10.7	11.0	V
		V_{GDA}/V_{GDB} at V_{CC} = 38 V	10.6	10.9	11.2	V

13 Application information

A resonant switched mode power supply with the TEA2096T consists of a primary side half-bridge, a transformer, a resonant capacitor, and an output stage. To obtain low conduction loss rectification, SR MOSFETs are used in the output stage. The TEA2096T controls these SR MOSFETs.

The gate drive voltage for the SR switch is derived from the voltage difference between the corresponding drain sense and source sense pins.

Special attention must be paid to the connection of the drain sense and source sense pins. The voltages measured on these pins are used for gate drive voltage. Wrong measurement results in a less efficient gate drive because the gate voltage is either too low or too high. The connections to these pins must not interfere with the power wiring. The power wiring conducts currents with high dI/dt values. It can easily cause measurement errors resulting from induced voltages due to parasitic inductances. The separate source-sense pins enable the direct sensing of the source voltage of the external MOSFETs. Using the current carrying power ground tracks is not allowed.

For output voltages below 38 V, the V_{CC} pin can be connected to V_{out} directly.

For output voltages exceeding 38 V, the V_{CC} voltage can be generated via a linear or a discrete regulator (see Figure 6). Or it can be generated via a dedicated supply (see Figure 7).

13.1 Resonant application

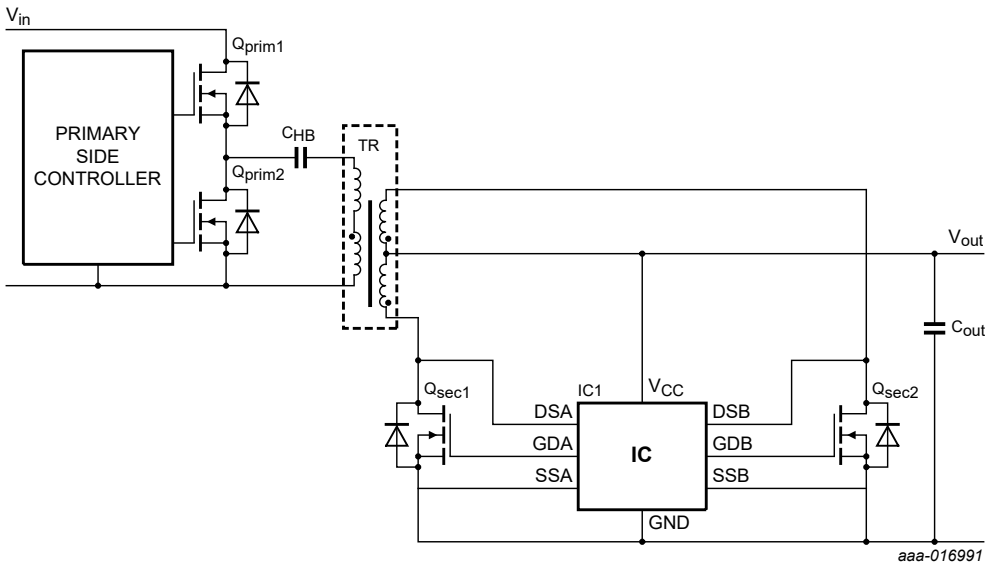


Figure 5. Typical resonant application with TEA2096T

13.2 Application with a discrete V_{CC} supply

With the addition of a small signal MOS transistor, a disable/enable input can be added to the application with a discrete V_{CC} supply. The transistor pulls down the V_{CC} supply and disables the SR operation in situations where synchronous rectification is not desired.

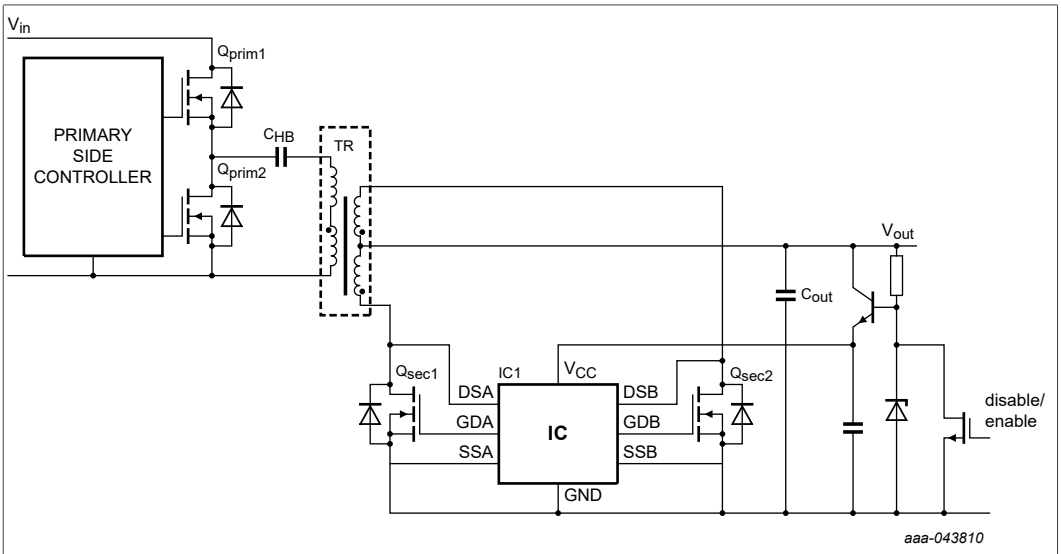


Figure 6. TEA2096T application with a discrete V_{CC} supply and disable/enable input

13.3 Application with dedicated V_{CC} supply

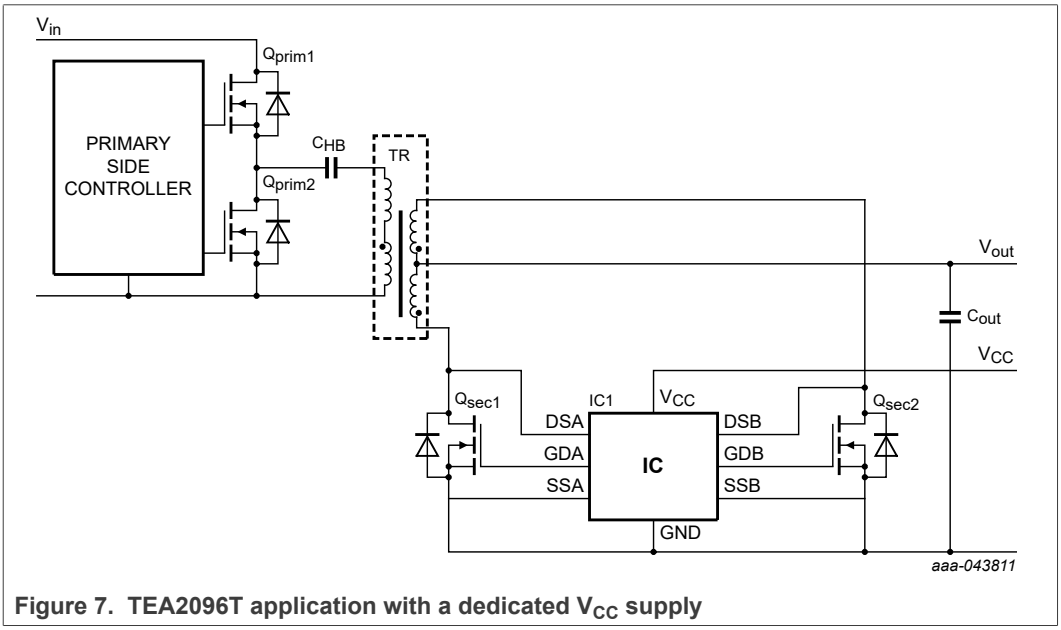
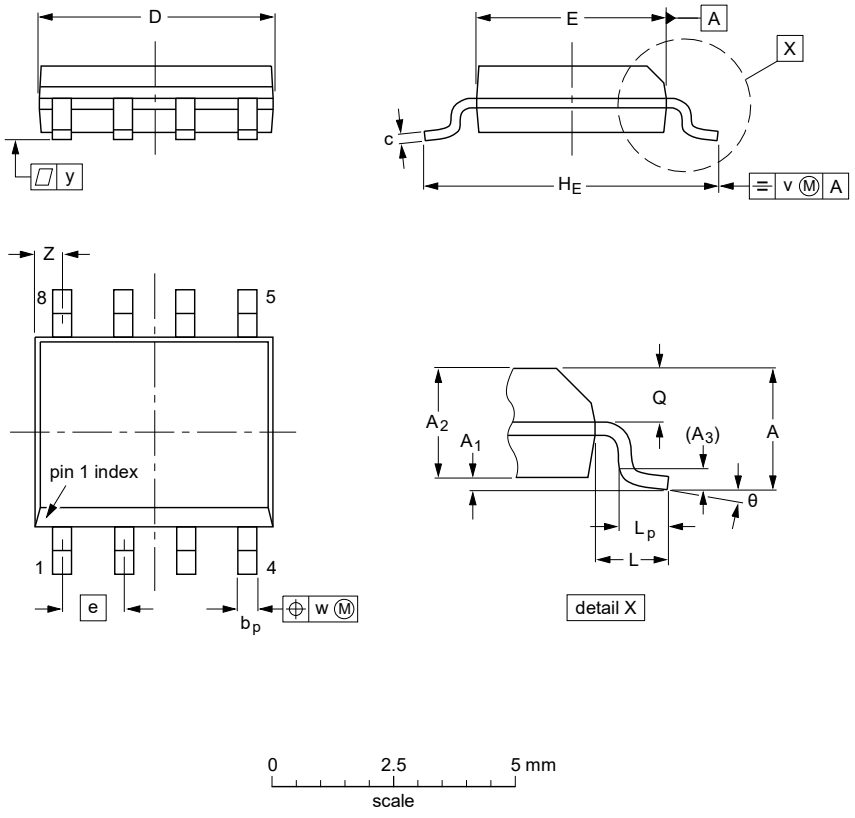


Figure 7. TEA2096T application with a dedicated V_{CC} supply

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 8. Package outline SOT96-1 (SO8)

15 Abbreviations

Table 8. Abbreviations

Acronym	Description
CDM	charged device model
ESD	electrostatic discharge
HBM	human body model
MM	machine model
MOSFET	metal-oxide-semiconductor field-effect transistor
SOI	silicon-on-insulator
SR	synchronous rectification
UVLO	undervoltage lockout

16 Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA2096T v.1	20220909	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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