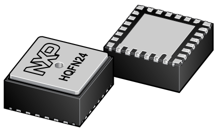


NBP8

Battery pressure monitor sensor

Rev. 2.4 — 11 March 2022

Product data sheet

1 General description

The NBP8 family is a fully integrated battery pressure monitoring sensor (BPMS). The NBP8 BPMS solution integrates an 8-bit central processing unit (CPU) running on factory-embedded firmware with serial data interface to create the ready-to-use battery pressure monitor sensor.

The NBP8 includes unique autonomous features such as periodic data management with host notification, pressure change detection with host wake up, and self-test.

The NBP8 is packaged in a small 4 mm x 4 mm x 1.98 mm wettable-flank QFN, and is qualified to AEC-Q100 grade 1 and MSL 3 classifications.

2 Features and benefits

- Transducer measurement interfaces with low-power AFE:
  - 10-bit compensated pressure sense element
  - 8-bit compensated internal device temperature measurement
  - 8-bit compensated internal device voltage measurement
- 12-entry pressure FIFO
- Selectable host wake-up indications:
  - fixed pressure threshold
  - relative pressure threshold
  - pressure rate of change threshold
- Client SPI to support host access to internal peripherals, registers, and memory
- Qualified in compliance with AEC-Q100, Rev. H
- User-selectable sampling interval
- Low-voltage detection

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NBP8	VSON	plastic thermal enhanced quad flat package; no leads, 0.1 dimple wettable flank; 24 terminals; 0.5 mm pitch, 4 mm x 4 mm x 1.98 mm body	SOT1931-1(D)

Table 2. Ordering options

Part Number	Pressure Range	Pressure tolerances
NBP8FD4T1	40 kPa to 250 kPa	Standard tolerances

4 Block diagram

Figure 1 presents the main blocks of the device and their signal interactions. Power management controls and bus control signals are not shown in this block diagram for clarity.

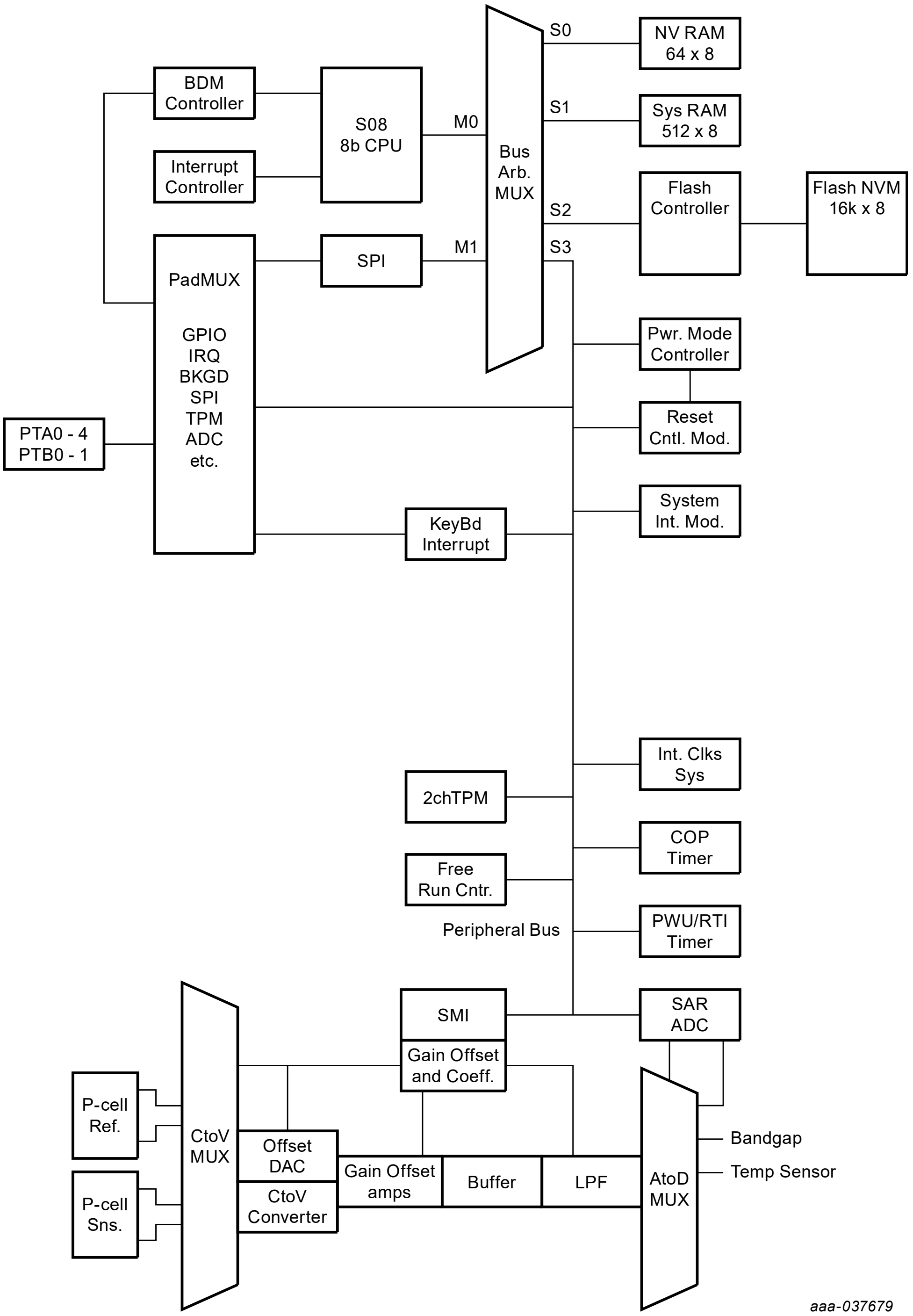


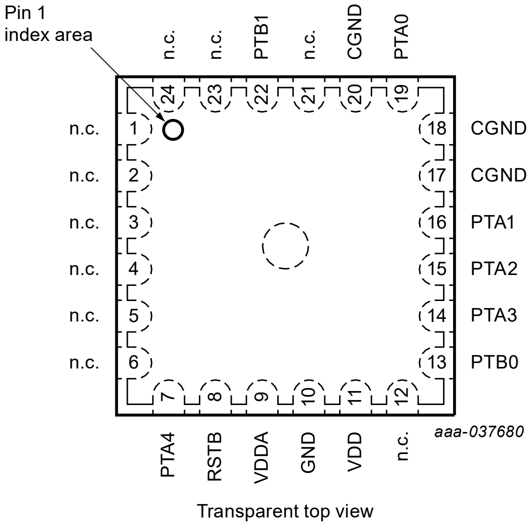
Figure 1. Block diagram

5 Pinning information

This section describes the pin layout and general function of each pin.

5.1 Pinning

The device pinout is shown in Figure 2 for the orientation of the pressure port up.



Note: *Pins 1-6 are mechanically and electrically connected to the central flag; See Section 12 for details. If additional ground is desired, any of the pins 1-6 may be routed to circuit board ground plane, or the central flag may be connected to circuit board ground plane with vias.*

Figure 2. Pin configuration

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Function	Description
n.c.	1	—	Do not connect electrical signals to this pin; solder joint only.
n.c.	2	—	Do not connect electrical signals to this pin; solder joint only.
n.c.	3	—	Do not connect electrical signals to this pin; solder joint only.
n.c.	4	—	Do not connect electrical signals to this pin; solder joint only.
n.c.	5	—	Do not connect electrical signals to this pin; solder joint only.
n.c.	6	—	Do not connect electrical signals to this pin; solder joint only.

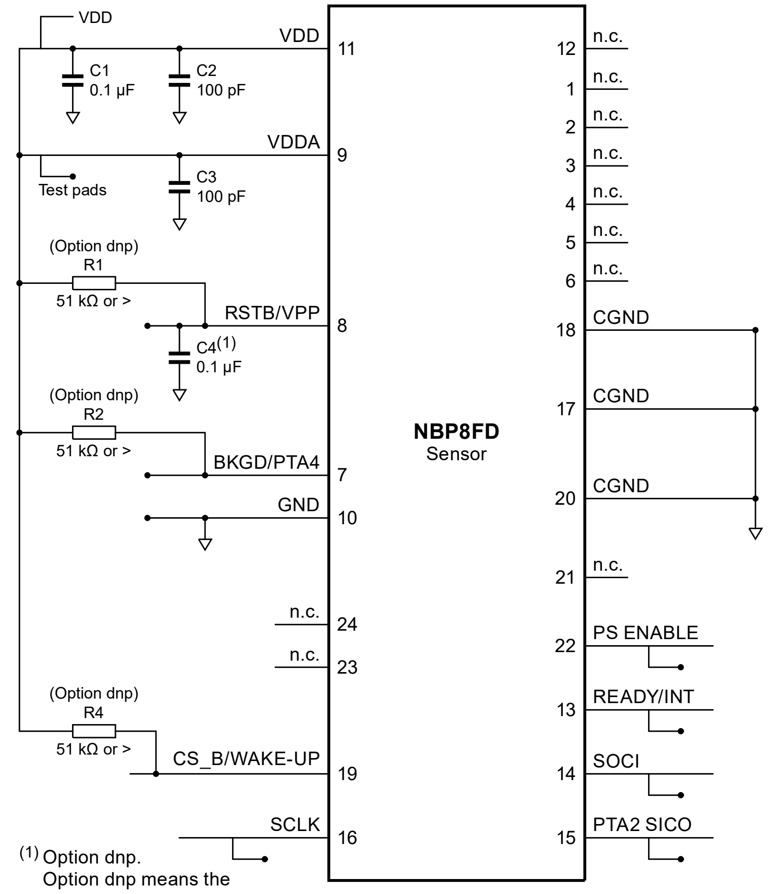
Table 3. Pin description*...continued*

Symbol	Pin	Function	Description
PTA4	7	PTA4 / BKGD	PTA4 Pin - The PTA4 pin places the device in the BACKGROUND DEBUG mode (BDM) to evaluate CPU code and transfer data to/from the internal memory. If the BKGD/PTA4 pin is held low when the device comes out of a power-on-reset (POR), the device switches into the ACTIVE BACKGROUND DEBUG mode (BDM). The BKGD/PTA4 pin has an internal pullup device or can be connected to VDD in the application, unless there is a need to enter BDM operation after the device as been soldered into the PWB. If in-circuit BDM is desired, the BKGD/PTA4 pin should be connected to VDD through a resistor (~10 kΩ or greater) which can be over-driven by an external signal. This resistor reduces the possibility of inadvertently activating the debug mode in the application due to an EMC event. When the application programs port A to GPIOs, PTA4 becomes output-only.
RST_B	8	Reset / V_{PP} programming voltage	The RST_B pin is used for test and establishing the BDM condition and providing the programming voltage source to the internal FLASH memory. This pin will only be used by customers who intend to reprogram the NBP. The RST_B pin has an internal pullup device and can be connected to VDD in the application unless there is a need to enter BDM operation after the device as been soldered to the PWB. If in-circuit BDM is desired, the RST_B pin can be left unconnected; but should be connected to VDD through a low impedance resistor (<10 kΩ) which can be over-driven by an external signal. This low impedance resistor reduces the possibility of getting into the debug mode in the application due to an EMC event. Activation of the external reset function occurs when the voltage on the RST_B pin goes below 0.3 × V_{DD} for at least 100 ns before rising above 0.7 × V_{DD}.
VDDA	9	Analog supply	The analog circuits operate from a single power supply connected to the unit through the VDDA pin. VDDA is the positive supply and GND is the ground. The conductors to the power supply should be connected to the VDDA and GND pins and locally decoupled. Care should be taken to reduce measurement signal noise by separating the VDD, GND, VDDA, and no RFGND pins using a “star” connection such that each metal trace does not share any load currents with other external devices.
GND	10	Digital and analog ground	The digital circuits operate from a single power supply connected to the unit through the VDD and GND pins. GND is the ground. Care should be taken to reduce measurement signal noise by separating the GND pins using a “star” connection such that each metal trace does not share any load currents with other external devices.
VDD	11	Digital supply	The digital circuits operate from a single power supply connected to the unit through the VDD and GND pins. VDD is the positive supply. The conductors to the power supply should be connected to the VDD and GND pins and locally decoupled.
n.c.	12	—	Do not connect electrical signals to this pin; solder joint only.
PTB0	13	PTB0 / TPMCH0 / AD3	The PTB[0] pin is a general-purpose I/O pin. This pin can be configured as a nominal bidirectional I/O pin with programmable pullup devices. User software must configure the general-purpose I/O pin (PTB[1:0]) so that they do not result in “floating” inputs. PTB0 can be mapped to TPM channel 0, or to ADC channel 3.

Table 3. Pin description*...continued*

Symbol	Pin	Function	Description
PTA3	14	PTA3 / KBI3 / SOCI	The PTA[3] pin is a general-purpose I/O pin. The pulldown devices can only be activated if the wake-up interrupt capability is enabled. User software must configure the general-purpose I/O pins so that they do not result in “floating” inputs. PTA[3] maps to keyboard interrupt function bit [3]. When SPI is enabled, PTA[3] serves as SOCI.
PTA2	15	PTA2 / KBI2 / SICO	The PTA[2] pin is a general-purpose I/O pin. The pulldown devices can only be activated if the wake-up interrupt capability is enabled. User software must configure the general-purpose I/O pins so that they do not result in “floating” inputs. PTA[2] maps to keyboard interrupt function bit [2]. When SPI is enabled, PTA[2] serves as SICO.
PTA1	16	PTA1 / KBI1 / SCLK	The PTA[1] pin is a general-purpose I/O pin. The pulldown devices can only be activated if the wake-up interrupt capability is enabled. User software must configure the general-purpose I/O pins so that they do not result in “floating” inputs. PTA[1] maps to keyboard interrupt function bit [1]. When SPI is enabled, PTA[1] serves as SCLK
CGND	17	—	To be connected to ground by the application.
CGND	18	—	To be connected to ground by the application.
PTA0	19	PTA0 / KBI0 / CS_B / IRQ	The PTA[0] pin is a general-purpose I/O pin. PTA[0] can be configured as a normal bidirectional I/O pin with programmable pullup or pulldown devices and/or wake-up interrupt capability. PTA[0] can be configured for external interrupt (IRQ). The pulldown devices can only be activated if the wake-up interrupt capability is enabled. User software must configure the general-purpose I/O pins so that they do not result in “floating” inputs. PTA[0] maps to keyboard interrupt function bit [0]. When SPI is enabled, PTA0 serves as CS_B.
CGND	20	—	To be connected to ground by the application.
n.c.	21	—	Do not connect electrical signals to this pin; solder joint only.
PTB1	22	PTB1 / TPMCH1 / AD4	The PTB[1] pin is a general-purpose I/O pin. This pin can be configured as a nominal bidirectional I/O pin with programmable pullup devices. User software must configure the general-purpose I/O pins (PTB[1:0]) so that they do not result in “floating” inputs. PTB1 can be mapped to TPM channel 1, or to ADC channel 4.
n.c.	23	—	Do not connect electrical signals to this pin; solder joint only.
n.c.	24	—	Do not connect electrical signals to this pin; solder joint only.

5.3 Application



(1) Option dnp.
Option dnp means the component may not be needed in all uses. The application circuit could include footprints where the EMI has to be improved at the board.

Figure 3. NBP8 application

6 Functional description

6.1 Communication between the NBP8 and external host

An example block diagram of NBP8 with an external host is shown in Figure 4:

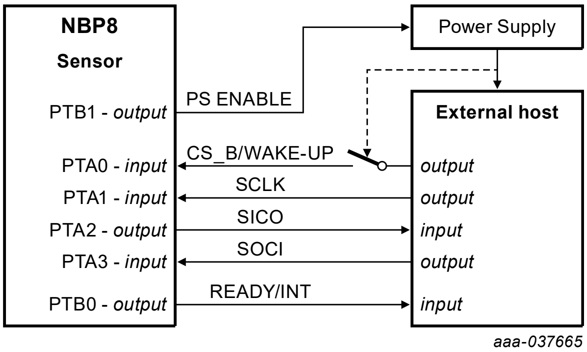


Figure 4. Connections between the NBP8 and external host

Table 4. Connection pins description

Pin	Description	Remarks
PS ENABLE (PTB1)	Power supply enable.	When enabled, the NBP8 asserts the PS ENABLE pin before generating a pulse on the INT pin.
CS_B/WAKE UP (PTA0)	• When SPI is enabled: Client Select active low • When SPI is disabled: WAKE-UP / low state triggers an interrupt on NBP8 side (no edge required)	When SPI is disabled, the WAKE-UP signal can be used for the external host to request SPI communication with the NBP8, to read memory and change settings, or trigger a self-test, firmware verification, software reset, or clear flags and user FIFO. When SPI is enabled, Client Select when active low, ready for SCLK clock and data
SCLK (PTA1)	SPI clock	SPI clock from external host
SICO (PTA2)	SPI SICO	Server-In-Client-Out data
SOCI (PTA3)	SPI SOCI	Server-Out-Client-In data
READY / INT (PTB0)	• READY signal: following a WAKE-UP event, the NBP8 indicates to the external host it is ready for the SPI transfers by asserting the pin. • INT signal: the NBP8 notifies the external host that an event requiring attention occurred by generating a pulse on the pin.	The external host should enable a pull up/down to maintain the pin in idle state as long as the NBP8 does not assert it.

Note: *When the NBP8 is in sleep mode, the CS_B/WAKEUP pin is configured as input with pull-up enabled. All other pins are in high impedance state, which means that the NBP8 does not maintain their levels. Specifically, the level of the PS ENABLE pin is not maintained by the NBP8 in sleep, so when this signal is used, its idle level must be maintained by an external circuit.*

Note: *If the external host will be switched off, the CS_B/WAKE UP signal must be isolated to prevent inadvertent assertion; a fixed low level at the NBP8 CS_B/WAKE UP input will cause the sensor to remain waiting for the SPI SCLK, and not collect new pressure measurements.*

6.2 Serial peripheral interface (SPI) module

The SPI module is configured as a standard client SPI which allows a full duplex, synchronous, serial communication between the unit and a server SPI device.

The principal features of the SPI block are summarized as follows:

- Client only mode operation.
- Full-duplex, 4 wire, synchronous serial communication.
- Command-Response communication format.
- SCLK operation up to 10 MHz supported.
- Fixed Clock polarity and phase supported (CPOL=0, CPHA = 0).
  - The SPI module requires the base clock value to be at the low state (CPOL = 0) with data captured on the rising edge of the clock and data propagated on the falling edge of the clock (CPHA = 0).
- Supports 8-bit register read and write operations via 16 clock transfers.
- Even Parity error-checking.
- Alternate bus controller for the system-on-chip (SoC) internal IP Bus system.
  - SPI can be used to access the entire Memory map of the NBP8.
- Contains eight, 8-bit memory mapped registers for user and test mode operations.
- Decodes SPI test mode entry sequence and enables SPI test mode.

As a client, the SPI interface is compatible with SPI interface mode 00, corresponding to CPOL = 0 and CPHA = 0. For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the rising edge (low to high transition) of the clock and data is propagated on the falling edge (high to low transition) of the clock.

As a client, the CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the server toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the rising edge of the colock and propagated on the falling edge (CPHA = 0). Single-byte read and single-byte write operations are completed in two strobes of CS_B of 16 SCLK cycles each; multiple byte reads and writes are completed in additional multiples of 16 SCLK cycles. The first SCLK cycle latches the most significant bit on SOCI to select whether the desired operation is a read (R/W = 1) or a write (R/W = 0). The following 13 SCLK cycles are used to latch the client register read or write address. The final two SCLK cycles are used to latch the parity calculation results.

When memory is secured by SEC[1:0] settings, the SPI may access only the address ranges indicated in Section 6.8 "Read/write targets accessible by the external host via SPI". Other access attempts result in an error status as defined below.

Note: *The SPI and the CPU share the internal address, data, and control bus, and are arbitrated such that the SPI takes priority over the CPU. The user application must account for inhibited execution of CPU instructions during the time the SPI has taken control of the internal bus.*

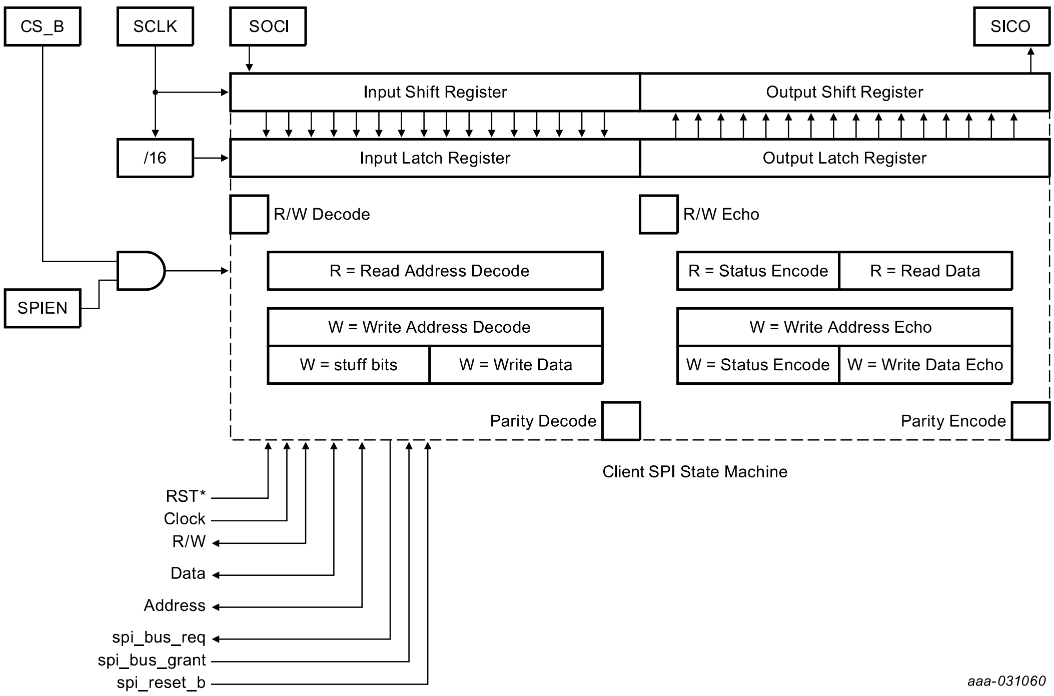


Figure 5. Client SPI state machine

Transaction event schedule; T1 being the first server transmission, R1 being the first client response being concurrent with T2 being the second server transmission:

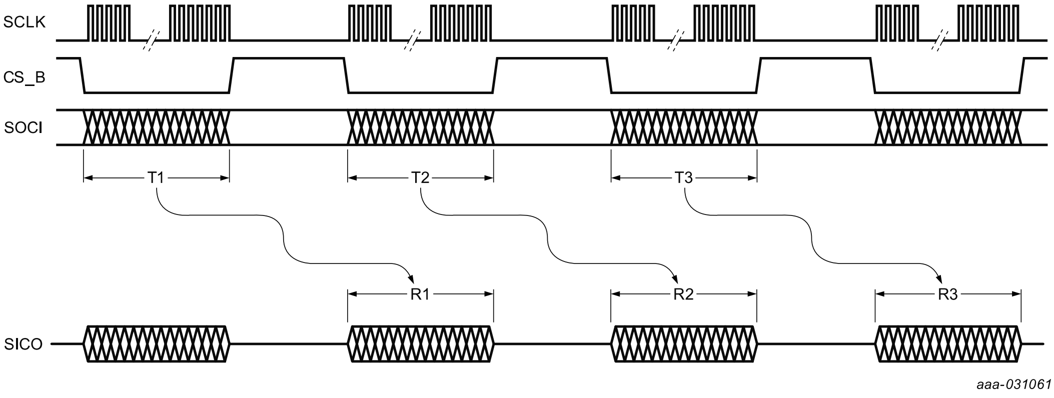


Figure 6. SPI message response protocol

6.2.1 SPI protocol definition

Table 5. SPI protocol architecture

Clock cycle		**c1**	**c2**	**c3**	**c4**	**c5**	**c6**	**c7**	**c8**	**c9**	**c10**	**c11**	**c12**	**c13**	**c14**	**c15**	**c16**
Bit assignment		**b15**	**b14**	**b13**	**b12**	**b11**	**b10**	**b9**	**b8**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Read byte from Address	T1	0	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	p1	p0
	R0	r	s4	s3	s2	s1	s0	r	r	r	r	r	r	r	r	p1	p0
	T2	t	t	t	t	t	t	t	t	t	t	t	t	t	t	p1	p0
	R1	0	s4	s3	s2	s1	s0	d7	d6	d5	d4	d3	d2	d1	d0	p1	p0

Table 5. SPI protocol architecture*...continued*

Clock cycle		c1	c2	c3	c4	c5	c6	c7	c8	c9	c10	c11	c12	c13	c14	c15	c16
Bit assignment		**b15**	**b14**	**b13**	**b12**	**b11**	**b10**	**b9**	**b8**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
Write byte to Address	T1	1	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	p1	p0
	R0	r	s4	s3	s2	s1	s0	r	r	r	r	r	r	r	r	p1	p0
	T2	1	m	m	m	m	m	d7	d6	d5	d4	d3	d2	d1	d0	p1	p0
	R1	1	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	p1	p0
	T3	t	t	t	t	t	t	t	t	t	t	t	t	t	t	p1	p0
	R2	1	s4	s3	s2	s1	s0	d7	d6	d5	d4	d3	d2	d1	d0	p1	p0

Where:

c1 – c16 = SCLK cycles 1 (b15) through 16 (b0), most significant bit first, least significant bit last

b15:0 = bit assignments for each clock cycle, b15 = 0 for read; b15 = 1 for write

a12:0 = 13 LSBs of address being read or written; $0000 to $1FFF is direct; $C000 to $FFFF is indirect

p1:0 = “Even” parity bits, p1 calculated for contents of b15:9; p0 calculated for contents of b8:2

s4:0 = client status:

0 0 0 0 0 = all OK, no need for retry.

1 x x x x = reserved for future fault modes, default to 0 until defined

x 1 x x x =

the response in R0 for first T1 input after reset

in the case of commands ignored by SPI due to error in previous read command; that is, invalid data in response

in the case the write command did not execute

x x 1 x x = clock fault, not enough clocks, or too many clocks per CS_B cycle

x x x 1 x = parity fault from either p1 or p0

x x x x 1 = internal bus contention fault, SPI does not gain access to peripheral bus in the prescribed time, or attempt access illegal or security-blocked address

d7:0 = data being read or written

t = contents of next server transmission T#+1

m = server stuff bits, 0 or 1 by server choice, and included as part of parity calculation

r = contents of previous client response R#-1

6.2.2 SPI signal timing definition

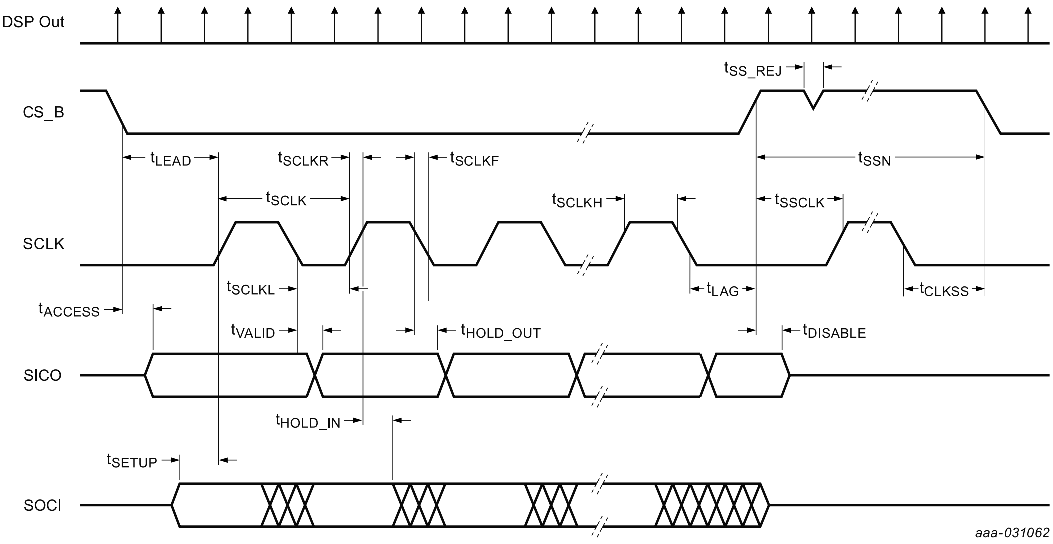


Figure 7. SPI signal timing diagram

Enable SPI by either of the following methods:

1. CPU application software sets the SPIEN control bit at address $1802 to logic 1
2. At power application, an external host holds the PTA0 pin low for greater than the time t_{SPI_EN}

Care must be taken by the user application to assure the SPI is not disabled by writing logic 0 to the SPIEN bit, or by entering a stop mode during an ongoing transmission. SPI can be disabled when CS_B signal is in the inactive state, or high.

6.3 Main features

Table 6. List of the main software-implemented features

Feature	Description	Event occurrence	User configuration
Sensor Data Measurement	The NBP8 takes compensated pressure measurement and can notify the external host that sensor data is available or that measurement completed with errors. The last 12 pressure values are stored in memory.	Periodic	Enable/disable pulse generation when sensor data ready or when acquisition status flag is not clear
			Period selection (ODR)
Pressure Change Detection (PCD)	The NBP8 monitors the pressure change over time and notifies the external host if the pressure change conditions set by the user are met.	Pressure value is verified at the ODR rate	Pressure monitoring options selectable independently
			Programmable warning thresholds
			Programmable debounce counter
Self-test	The NBP8 performs self-test for the ADC and Pressure Measurement Cell (Pcell). In case of failed status, the NBP8 can notify the external host. The result of the last Self-test is stored in memory.	Periodic and/or punctual (triggered by the appropriate command written via SPI)	Enable/Disable periodic self-test
			If enabled, period selection
			Enable/disable pulse generation if an error is detected

Table 6. List of the main software-implemented features*...continued*

Feature	Description	Event occurrence	User configuration
Firmware Integrity Verification	The NBP8 calculates the 16-bit XOR checksum of the entire FLASH memory and compares it with the value stored at production. If values are different, the NBP8 can notify the external host. The result of the last firmware integrity verification is stored in memory.	Triggered by the appropriate command written via SPI	Enable/disable pulse generation if an error is detected

6.4 State-transition diagram

Periodically, the NBP8 takes pressure measurements and completes a compensation. The result is then used for the pressure change detection. Optionally, the host can configure NBP8 for the self-test.

In addition to the periodic events, the external host can request access to the NBP8 memory with the WAKE-UP pin. When the WAKE-UP pin is lowered, the NBP8 enables SPI and remains in RUN mode until the SPI transfers have completed. During the SPI transfers, the external host has read and write access to the NBP8 memory in order to perform operations such as reading status flags, reading sensor data or requesting specific actions to be taken after completion of the SPI transfers.

After completion of the periodic and internally triggered actions, the NBP8 checks whether a condition for pulse generation was met. If so, the bit STATUS_INTF is set, the NBP8 enables SPI, optionally asserts the PS ENABLE pin, and triggers a pulse on the INT pin to notify the external host that an event requiring attention occurred. Then it remains in RUN mode while the SPI transfers have not completed.

Typically, the external host accesses the NBP8 memory and reads the STATUS register to identify the event requiring attention. Depending on the type of event, additional registers (such as SENSTATUS, the pressure FIFO, and so forth) may also be read. To acknowledge the event, the CMD_ACKINTF bit must be set by the external host.

Figure 8 illustrates the state-transition diagram.

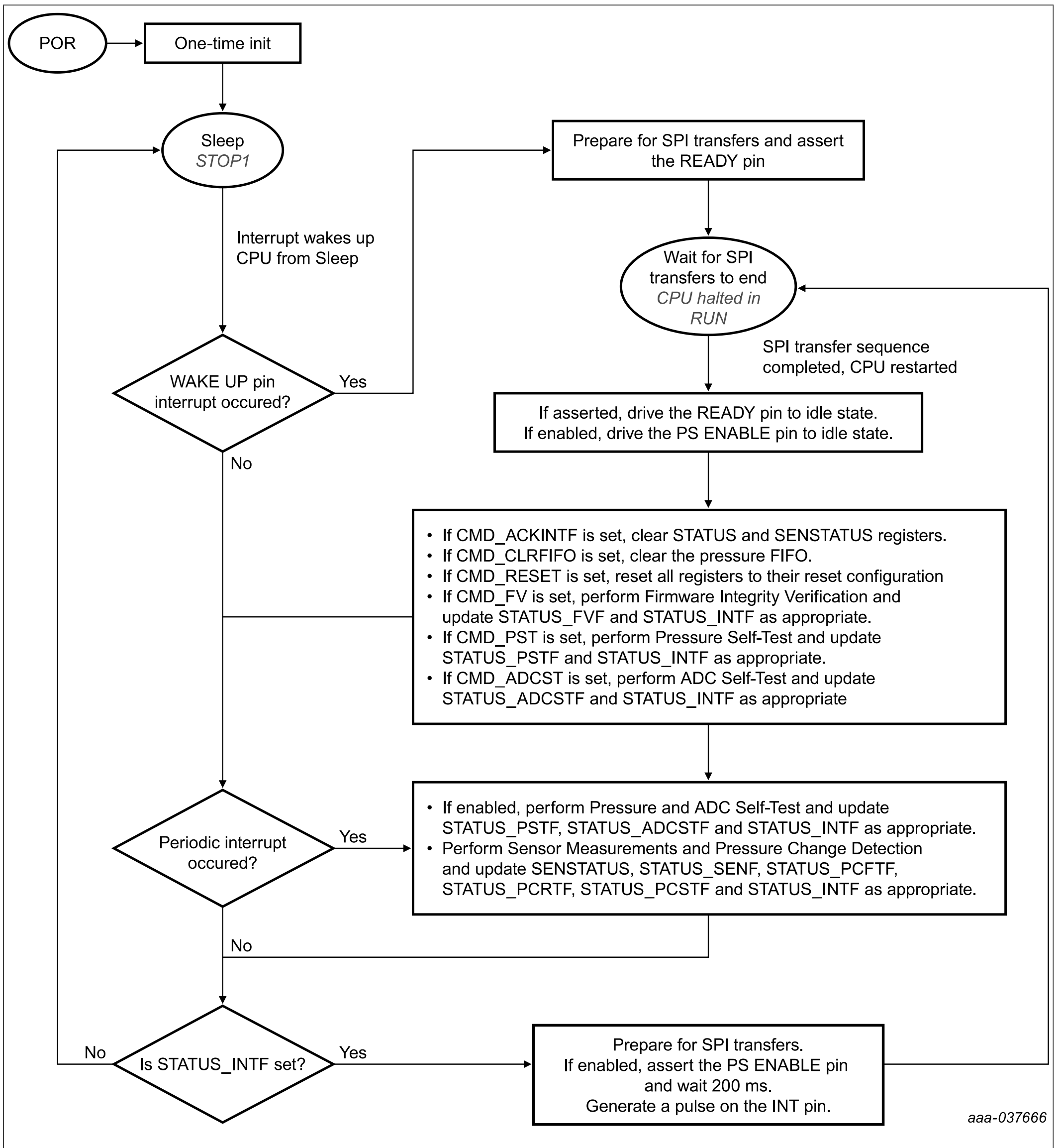


Figure 8. State-transition diagram

6.5 Pressure change detection description

6.5.1 Overview

Pressure measurements are taken at a period configured by the user. The last 12 measurements are stored in the pressure FIFO. The pressure FIFO acts like a rolling buffer and is described later in this section.

Several options with configurable settings are available to monitor pressure variation and determine when the external host should be notified that pressure change conditions have been met. The following three options are available and can be enabled independently. When more than one option is enabled, the program checks whether at least one option has met the condition, and if so, raises the appropriate flags and notifies the external host via the INT pin.

- Option to monitor the pressure vs. a fixed threshold: If pressure value has exceeded the fixed threshold set by the user, the flag STATUS_PCFTF is raised.
- Option to monitor the pressure vs. a relative threshold: The NBP8 monitors when pressure is rising and raises the STATUS_PCRTF flag when the pressure increase ΔPressure has exceeded the relative threshold set by the user.
- Option to monitor the pressure rate of change vs. a rate of change threshold: The NBP8 monitors when pressure is rising. When pressure has been rising for a certain time, configured by the user, the slope Δpressure/Δtime is calculated. If the slope is greater than the threshold configured by the user, the flag STATUS_PCSTF is raised.

After each new sample taken, when the program has executed all algorithms of the enabled options, the STATUS_INTF flag is raised if at least one of the pressure change STATUS flags (STATUS_PCFTF, STATUS_PCRTF or STATUS_PCSTF) is raised. When STATUS_INTF is set, the external host is notified that pressure change conditions have been met and is notified via the INT pin.

Each option is detailed in Section 6.5.2 through Section 6.5.5.

6.5.2 Description of the fixed threshold option

This option is enabled when bit PCCFG_FTEN is set. When a new pressure measurement is available, the pressure value is compared with the fixed threshold Pfix_T configured by the user. If the pressure value exceeds the threshold, the debounce counter Deb_FT_cnt is incremented. Otherwise, Deb_FT_cnt is decremented. When the Deb_FT_cnt exceeds the Debounce_T value configured by the user, the STATUS_PCFTF flag is raised.

The purpose of Deb_FT_cnt is to make sure that the flag is raised only after the condition has been met for a minimum number of samples. This filtering avoids the possibility of a false-alarm occurring when a single-measurement meets the condition due to a coincidental event, such as noise, affecting the measurement.

The algorithm flow is show in Figure 9.

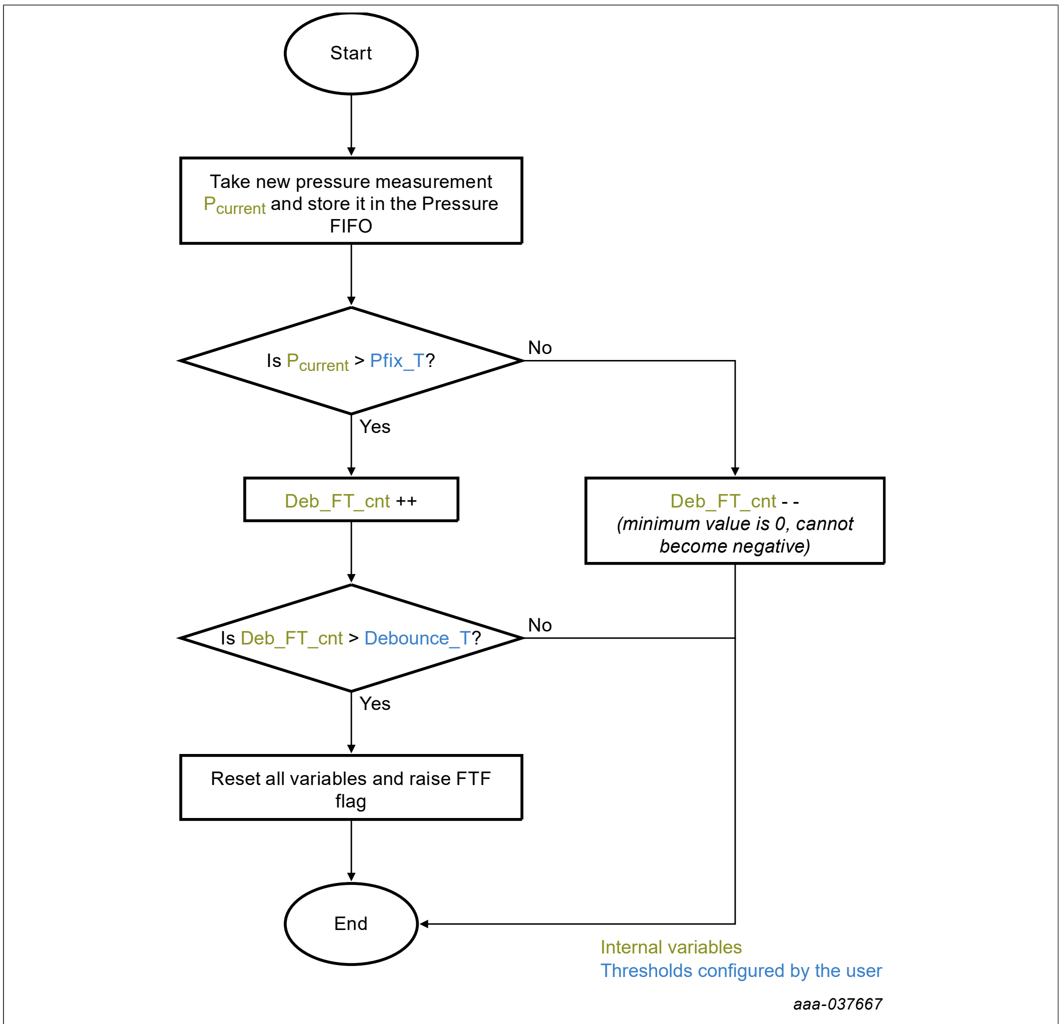


Figure 9. Fixed Threshold algorithm flow

The variables and thresholds used in the flow are described below:

- $P_{current}$: variable internal to the NBP8 program that holds the latest pressure measurement.
- Pfix_T: user-configurable threshold. The value is stored in PCFIXTH/L registers. No flag is raised as long as pressure does not consistently exceed this threshold.
- Deb_FT_cnt: counter internal to the NBP8 program updated every time a new pressure measurement is taken. The counter is incremented if the pressure exceeds the threshold Pfix_T. It is decremented otherwise. When the counter reaches 0, it cannot be further decremented.
- Debounce_T: user-configurable threshold. The value is stored in PCDEBT register. When the value in Deb_FT_cnt exceeds this threshold, pressure is considered to be consistently above Pfix_T, so the FTF flag is raised and external host notified.

An example of algorithm execution is shown in Figure 10. In this example, the sample rate is set to 100 ms. The pressure FIFO depth is 12 measurements; the gray dots represent the pressure values not available in the FIFO anymore when the flag is raised; the black and green dots represent the pressure values available in the FIFO when the flag is raised; the green dot represents the latest pressure measurement added to the FIFO when the flag is raised.

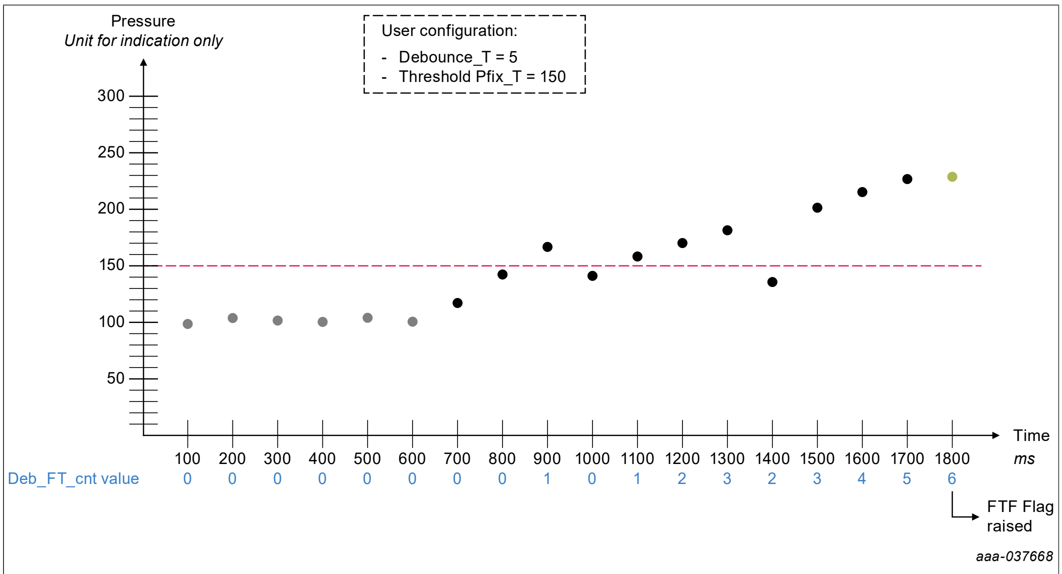


Figure 10. Example of execution of the fixed threshold algorithm

6.5.3 Description of the relative threshold option

The relative threshold option is enabled when bit PCCFG_RTEN is set. The algorithm monitors pressure rising, and whether the pressure increase has exceeded the threshold set by the user. To check for pressure rise, the current pressure measurement $P_{current}$ is compared with the previous measurement $P_{previous}$: the current measurement must be greater than the previous one, by the number of counts Min_T, configurable by the user. This check is to ensure that pressure is actually increasing, and that an increase of the pressure value is not due to sensor drift only. When pressure is increasing, that is, when $P_{current} > P_{previous} + Min\_T$, a counter Incr_cnt is incremented. It is decremented otherwise.

If pressure has been rising, the pressure increase $\Delta P = P_{current} - P_{ref}$ is compared with the user threshold Prel_T. If greater, the counter Deb_RT_cnt is incremented. Otherwise, Deb_RT_cnt is decremented. When Deb_RT_cnt is greater than the user threshold Debounce_T, a flag is raised.

If both the Deb_RT_cnt and Incr_cnt are equal to 0, the current pressure value $P_{current}$ is set as the reference value P_{ref}.

The purpose of Deb_RT_cnt is to make sure that the flag is raised only after the condition has been met for a minimum number of samples. This filtering avoids the possibility of a false-alarm occurring when a single-measurement meets the condition due to a coincidental event, such as noise, affecting the measurement.

The algorithm flow is shown in Figure 11.

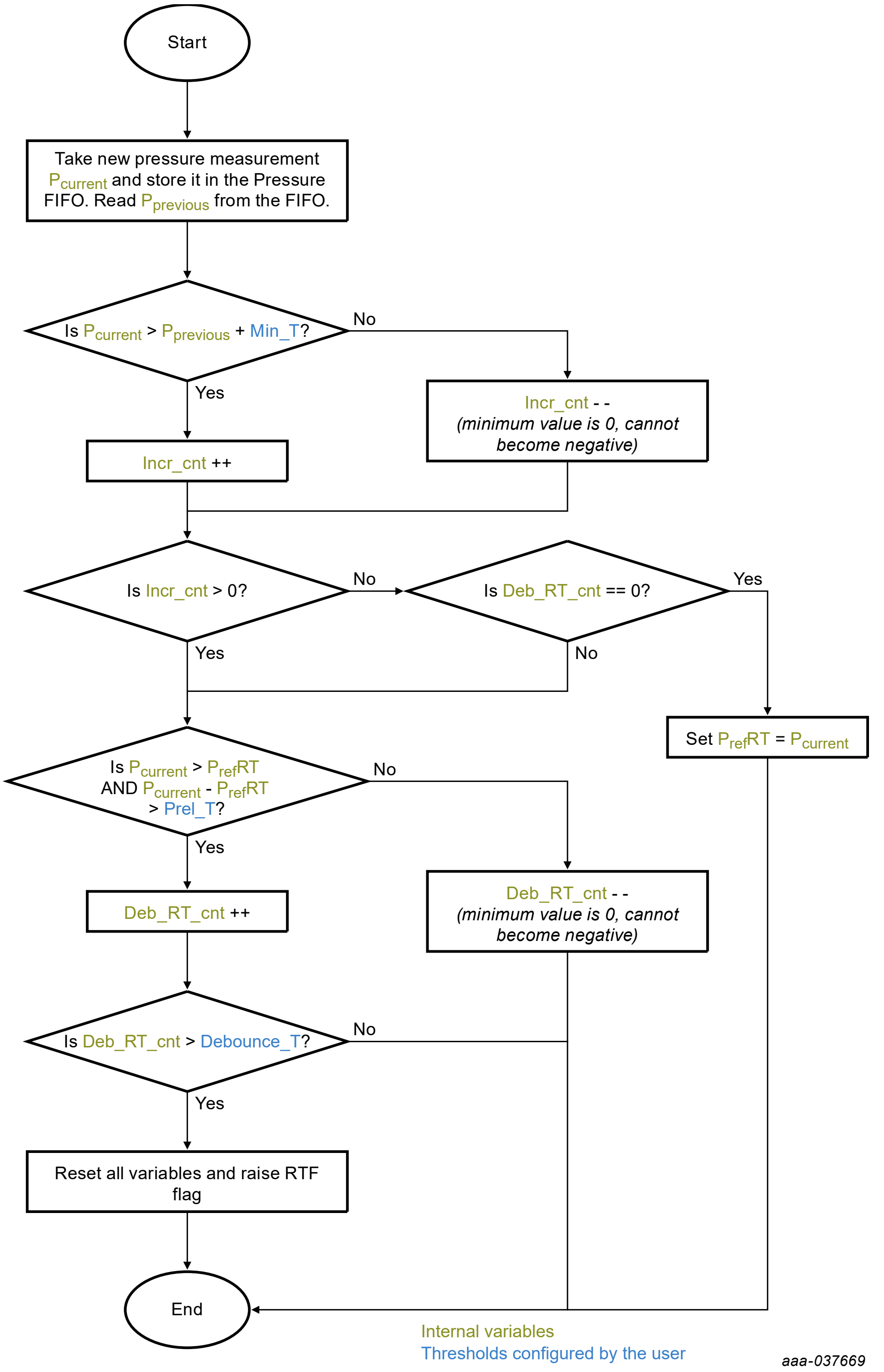


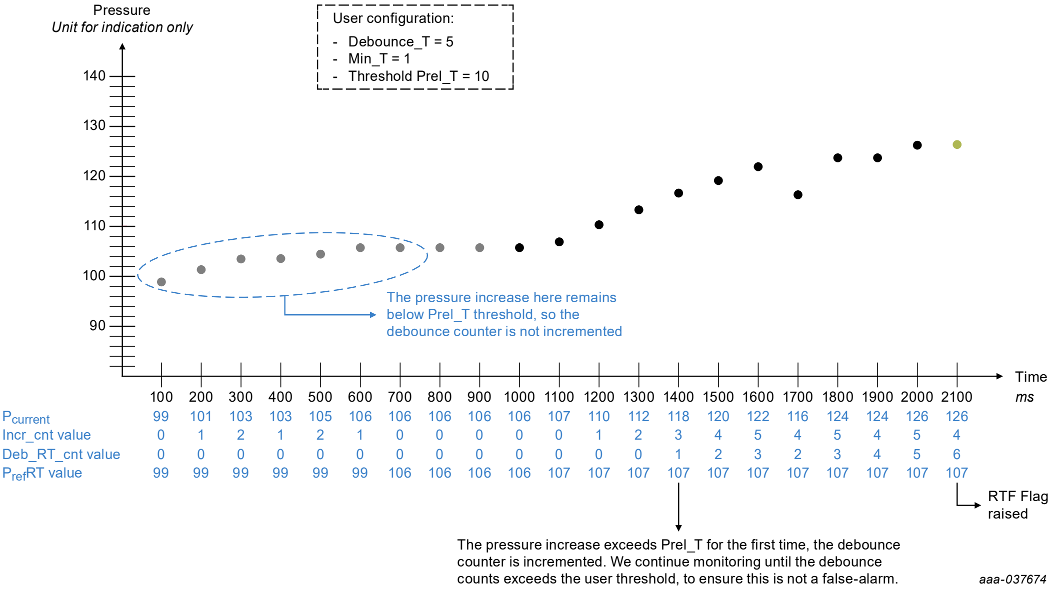
Figure 11. Relative threshold algorithm flow

The variables and thresholds used in the flow are described below:

- $P_{current}$: variable internal to the NBP8 program that holds the latest pressure measurement.
- $P_{previous}$: variable internal to the NBP8 program that holds the previous pressure measurement.

- $P_{ref}RT$: variable internal to the NBP8 program that stores the last pressure value before the pressure started to rise.
- Min_T: user-configurable threshold that defines the minimum number of counts by which the current pressure value must exceed the previous pressure value, for the NBP8 program to consider that the pressure is rising. The value is stored in PCMINT register.
- Incr_cnt: variable internal to the NBP8 incremented when pressure is rising, and decremented otherwise.
- Prel_T: user-configurable threshold. When pressure is rising, the pressure increase $\Delta P = P_{current} - P_{ref}RT$ is compared with Prel_T. If the pressure increase exceeds Prel_T, the debounce counter is incremented. It is decremented otherwise The value is stored in PCRELTH/L registers.
- Deb_RT_cnt: counter internal to the NBP8 program incremented when the pressure increase exceeds the Prel_T. If pressure is still rising but the pressure increase remains below Prel_T, Deb_RT_cnt is decremented. When the counter reaches 0, it cannot be further decremented.
- Debounce_T: user-configurable threshold. When the value in Deb_RT_cnt exceeds this threshold, the pressure increase is considered to be consistently above Prel_T, so the RTF flag is raised and external host notified. The value is stored in PCDEBT register.

Figure 12 shows an example algorithm execution. In this example, the sample rate is set to 100 ms. The pressure FIFO depth is 12 measurements; the gray dots represent the pressure values not available in the FIFO anymore when the flag is raised; the black and green dots represent the pressure values available in the FIFO when the flag is raised; the green dot represents the latest pressure measurement added to the FIFO when the flag is raised.



User configuration:
- Debounce_T = 5
- Min_T = 1
- Threshold Prel_T = 10

The pressure increase here remains below Prel_T threshold, so the debounce counter is not incremented

Time ms	100	200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500	1600	1700	1800	1900	2000	2100
$P_{current}$	99	101	103	103	105	106	106	106	106	106	107	110	112	118	120	122	116	124	124	126	126
Incr_cnt value	0	1	2	1	2	1	0	0	0	0	0	1	2	3	4	5	4	5	4	5	4
Deb_RT_cnt value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	2	3	2	3	4	5	6
$P_{ref}RT$ value	99	99	99	99	99	99	106	106	106	106	107	107	107	107	107	107	107	107	107	107	107

RTF Flag raised

The pressure increase exceeds Prel_T for the first time, the debounce counter is incremented. We continue monitoring until the debounce counts exceeds the user threshold, to ensure this is not a false-alarm.

aaa-037674

Figure 12. Example of execution of the relative threshold algorithm

6.5.4 Description of the rate of change threshold option

This option is enabled when PCCFG_STEN is enabled. When a new measurement $P_{current}$ is taken, it is compared with the previous value $P_{previous}$. The current measurement must be greater than the previous one, by the number of counts Min_T, configurable by the user, to consider that the pressure is rising. This check is to ensure that pressure is actually increasing, and that an increase of the pressure value is not due to sensor drift only. When pressure is increasing, that is, when $P_{current} > P_{previous} + Min\_T$, the counter Deb_ST_cnt is incremented. It is decremented otherwise. When Deb_ST_cnt exceeds the threshold value Debounce_T set by the user, the Slope = Δpressure/Δtime is calculated and compared with the threshold Slope_T configured by the user. If Slope > Slope_T then a flag is raised.

The algorithm flow is shown in Figure 13.

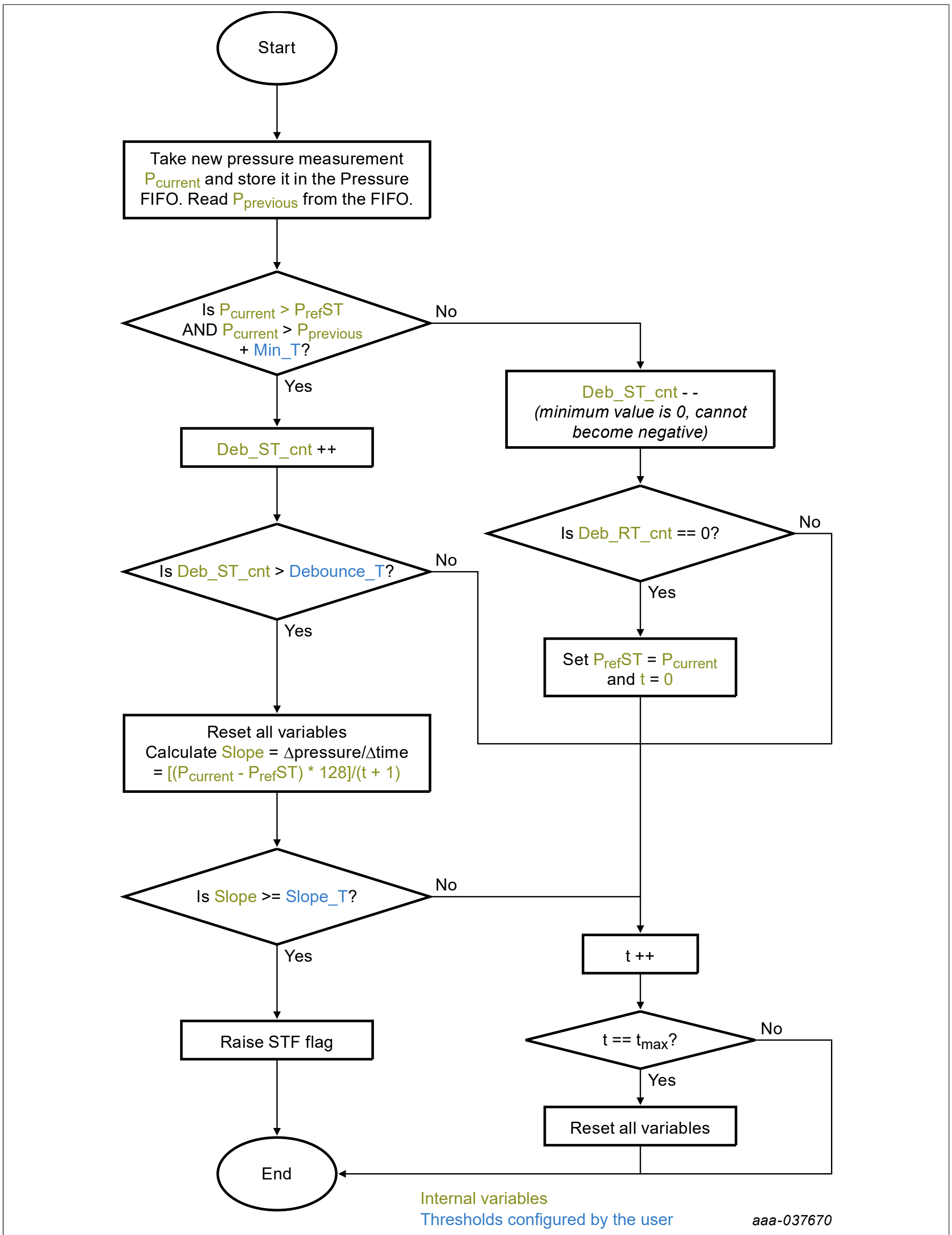
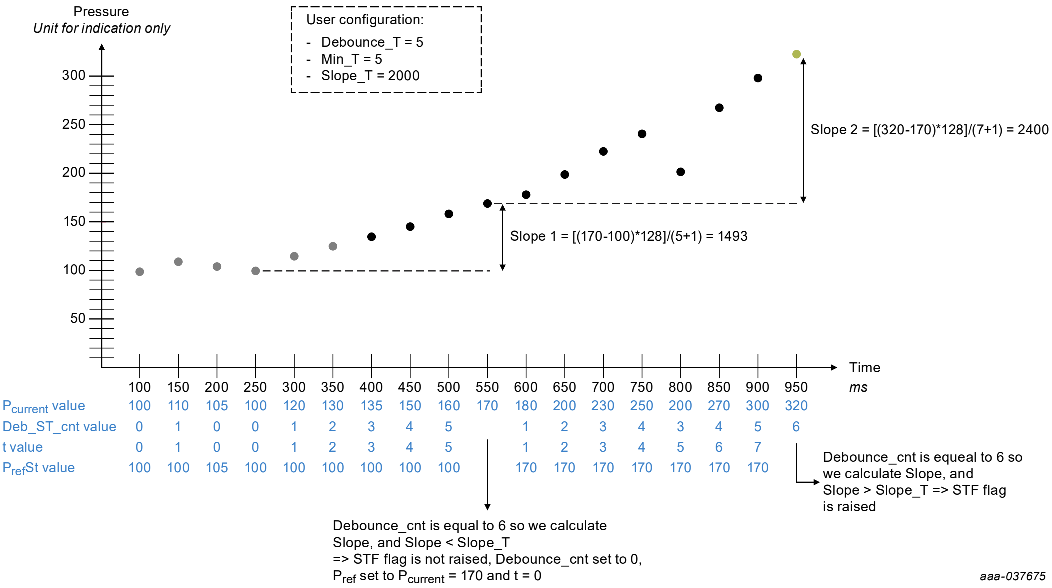


Figure 13. Slope threshold algorithm flow

The different variables and thresholds correspond to the following:

- $P_{current}$: variable internal to the NBP8 program that holds the latest pressure measurement. Pressure measurements are taken at a sample rate configured by the user.
- $P_{previous}$: variable internal to the NBP8 program that holds the previous pressure measurement.
- P_{ref}ST: variable internal to the NBP8 program that stores the last pressure value before the pressure started to rise.
- t: 16-bit variable internal to the NBP8 that is incremented periodically at the pressure sample rate when the pressure has been rising (that is, when Deb_ST_cnt is greater than 0) to keep track of the number of sampling periods during which pressure has been rising.
  If t value reaches its maximum value 65535, the pressure has been increasing over the last 65535 sampling periods but the Debounce counter has not reached the Debounce threshold. Reaching a t value of 65535 only happens if the Debounce threshold is set to a very high value and pressure increases extremely slowly. When such a situation occurs, the process resets in order to avoid rollover and a potentially incorrect slope calculation.
- Min_T: user-configurable threshold that defines the minimum number of counts by which the current pressure value must exceed the previous pressure value, for the NBP8 program to consider that the pressure is rising. The value is stored in PCMINT register.
- Deb_ST_cnt: counter internal to the NBP8 program updated every time a new pressure measurement is taken. The counter is incremented if the pressure is considered to be increasing, following the condition described above. It is decremented otherwise. When the counter reaches 0, it cannot be further decremented.
- Debounce_T: user-configurable threshold. The value is stored in PCDEBT register. When the value in Deb_ST_cnt exceeds this threshold, the pressure increase is considered consistent and the slope of pressure versus time is calculated to check whether the pressure increase should be notified to the external host.
- Slope: variable internal to the NBP8 program that holds the value of the scaled slope $(P_{current} - P_{ref}) * 128 / (t+1)$.
  The coefficient 128 provides improved precision in the slope calculation since all calculations are computed with integer values. Examples of slope calculation are provided in the description of the PCSLOPETH/L registers.
- Slope_T: user-configurable threshold. The value is stored in PCSLOPETH/L registers. When the value in Slope exceeds this threshold, the pressure increase is considered significant and the NBP8 raises the Pressure Change Detection flag before notifying to the external host that an event requiring attention occurred.

Figure 14 shows an example algorithm execution. In this example, the sample rate is set to 50 ms. The Pressure FIFO depth is 12 measurements; the gray dots represent the pressure values not available in the FIFO anymore when the flag is raised; the black and green dots represent the pressure values available in the FIFO when the flag is raised; the green dot represents the latest pressure measurement added to the FIFO when the flag is raised.



	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950
$P_{current}$ value	100	110	105	100	120	130	135	150	160	170	180	200	230	250	200	270	300	320
Deb_ST_cnt value	0	1	0	0	1	2	3	4	5		1	2	3	4	3	4	5	6
t value	0	1	0	0	1	2	3	4	5		1	2	3	4	5	6	7	
P_{ref}St value	100	100	105	100	100	100	100	100	100		170	170	170	170	170	170	170	

Debounce_cnt is equal to 6 so we calculate Slope, and Slope < Slope_T => STF flag is not raised, Debounce_cnt set to 0, P_{ref} set to $P_{current}$ = 170 and t = 0

Debounce_cnt is equeal to 6 so we calculate Slope, and Slope > Slope_T => STF flag is raised

Figure 14. Example of slope threshold algorithm flow

6.5.5 Description of the pressure FIFO

The last twelve pressure measurements are stored in the pressure FIFO. Pressure measurements are stored on two bytes, so the FIFO depth is 24 bytes. The FIFO is implemented as a rolling buffer: the most recent pressure measurement overwrites the oldest one. An 8-bit index INDFIFO holds the value of the last address written.

The FIFO starts at address $0076 and ends at address $008D. Addresses that have not yet been written contain the value 0x00. Measurements are written from the lower to the higher addresses, Most Significant Byte first. When the highest address has been written, the next sample is written at the lowest address.

Figure 15 shows how the program fills FIFO, for the first 25 samples. The index value after the sample Pn - the nth sample - has been written is also indicated.

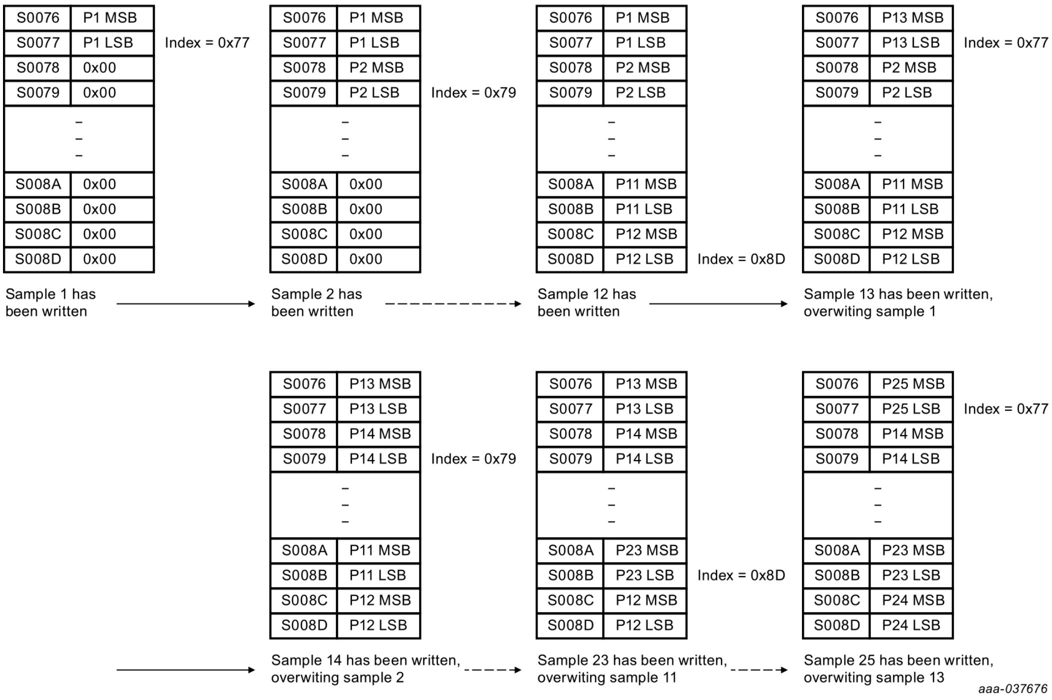


Figure 15. Pressure FIFO filled for the first 25 samples

6.6 SPI transfer sequence

6.6.1 SPI transfer requested by the external host via the WAKE-UP pin

At any time, the external host can request SPI communication by lowering the WAKE-UP pin, which triggers an interrupt on the NBP8 side. When the NBP8 is ready for the transfers, it asserts the READY pin. The polarity of the READY/INT pin is configured with the bit INTTRIG_INTPOL. After asserting the READY pin, the NBP8 writes in the SPIOPS register to halt itself, in order to avoid any memory access contention with the SPI server. Note that the NBP8 remains halted for a maximum of 2048 ms (SPI timeout), so the duration of the transfers should not exceed this time. The SPI server should poll the READY pin and start the SPI transfers only after this pin was asserted by the NBP8. During the SPI transfers, the SPI server can perform read and write access to the NBP8 memory. The list of addresses relevant for the application is given later in this document.

If the status of the SPI transfer corresponds to “internal bus contention fault”, the external host must recognize that it has started the SPI transfers while the NBP8 was generating the pulse on the INT pin. If such event occurs, the External MCU should wait for the INT pin to come back to idle state before resuming the SPI transfers.

If the NBP8 wakes up from the CS_B being driven low and then back to high state by the external host, the SPI status indicates the clock fault status due to the missing SCLK cycles. Therefore, the external host must treat the first command as a dummy to clear the SPI error status. Normal responses will remain after the first successful SPI command.

When the SPI server has completed all read and write accesses, it should perform a last write access to the NBP8 memory in order to clear the SPIOPS register. After the register has been cleared, the NBP8 resumes operation and drives the READY pin to inactive state before disabling the SPI block. If the SPI server does not clear the SPIOPS register, the NBP8 will automatically resume operations after the timeout duration.

The timing is described in Figure 16.

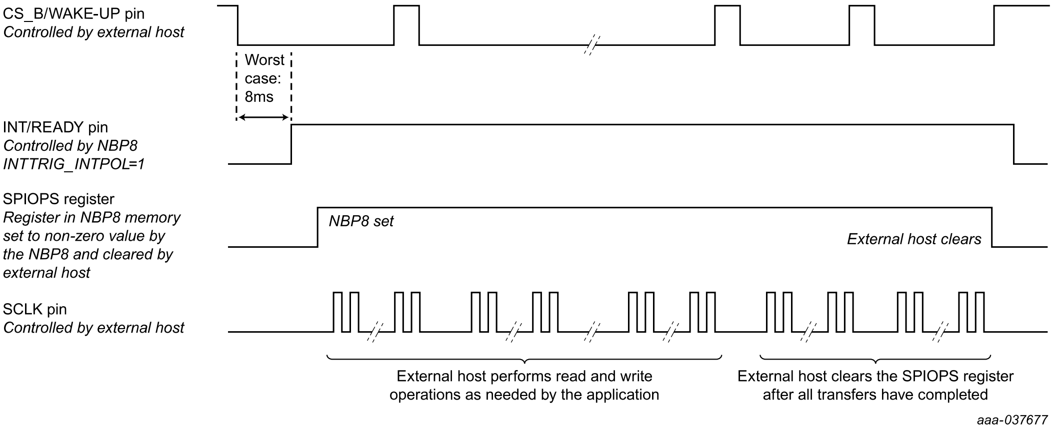


Figure 16. SPI timing description when transfers are requested by the external host via the WAKE-UP pin, with INTTRIG_INTPOL=1

Important note: Figure 16 shows that the CS_B / WAKE-UP pin is held low by the external host from the moment the external host lowers the pin to request a transfer, until the end of the first SPI transfer. In reality, the actual sequence implemented by the external host may be different, taking into account the possible software implementation described below.

To trigger the transfer request, the external host application may configure the CS_B / WAKE-UP pin as GPIO output low, and hold the pin in low state while polling the NBP8 READY pin. When the READY pin is asserted by the NBP8, the external host can start the SPI transfers. To start the transfers, the external host application must configure the CS_B / WAKE-UP signal as an SPI CS_B function. At that moment, the SPI transfers have not yet started and the CS_B / WAKE-UP must be driven back to high state by the external host hardware SPI block, before being driven low again when the first transfer starts.

The sequence means there may be a duration during which the CS_B / WAKE-UP pin is driven to low state and then back to high state again, before the SPI transfers start, as illustrated in Figure 17 below. The NBP8 logic considers this duration as a failed SPI transfer due to a clock fault error (CS_B pin lowered but no SCLK signal). After generating a clock fault error, the NBP8 needs one 16-bit transfer to clear the error before continuing normal operations. Consequently, the command inside the first 16-bit transfer performed by the external host is ignored by the NBP8. The first transfer is used by the NBP8 to clear the clock fault error only. So, the external host has to consider the first transfer to be a dummy transfer, during which the command is not taken into account. It is only from the second transfer that the READ or WRITE commands are processed by the NBP8.

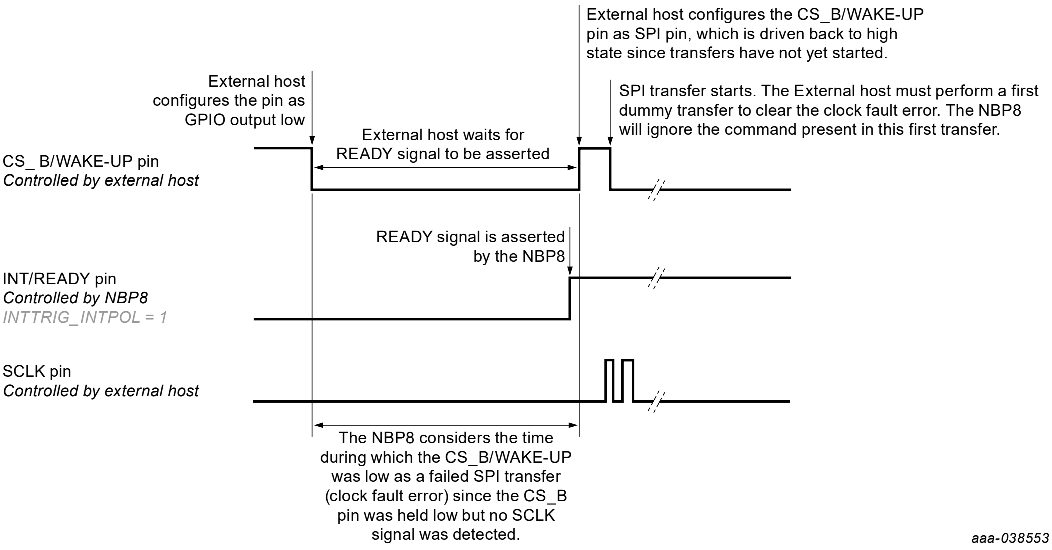


Figure 17. Sequence leading to a clock fault error on the NBP8 side

6.6.2 SPI transfer requested by the NBP8, when an event requiring attention occurred

When an event requiring attention has occurred, the NBP8 notifies the external host in order to establish SPI communication. For that, the NBP8 first enables SPI and then generates a pulse on the INT pin. If PS ENABLE pin is enabled in the PINCFG register, the NBP8 asserts PS ENABLE pin and waits 200 ms before generating the pulse on the INT pin. The polarity and duration of the pulse are configured with INTTRIG_INTPOL and INTTRIG_INTDUR bits. Following the pulse, the NBP8 writes in the SPIOPS register to halt itself, in order to avoid any memory access contention with the SPI server. Note that the NBP8 remains halted for a maximum of 2048 ms (SPI timeout), so the duration of the transfers should not exceed this time. The SPI server should poll the INT pin and start the SPI transfers only after the pulse ended, so after this pin was driven back to idle state by the NBP8. During the SPI transfers, the SPI server can perform read and write access to the NBP8 memory. The list of addresses relevant for the application is given later in this document. Typically, the external host would start by reading the STATUS register in order to know the origin of the event. The external host must set the CMD_ACKINTF bit to acknowledge the flags, which will be cleared by the NBP8 after completion of the SPI transfers.

When the SPI server has completed all read and write accesses, it should perform a last write access to the NBP8 memory in order to clear the SPIOPS register. After the register has been cleared, the NBP8 resumes operation. If the SPI server does not clear the SPIOPS register, the NBP8 will automatically resume operations after the timeout duration.

The timing is shown in Figure 18.

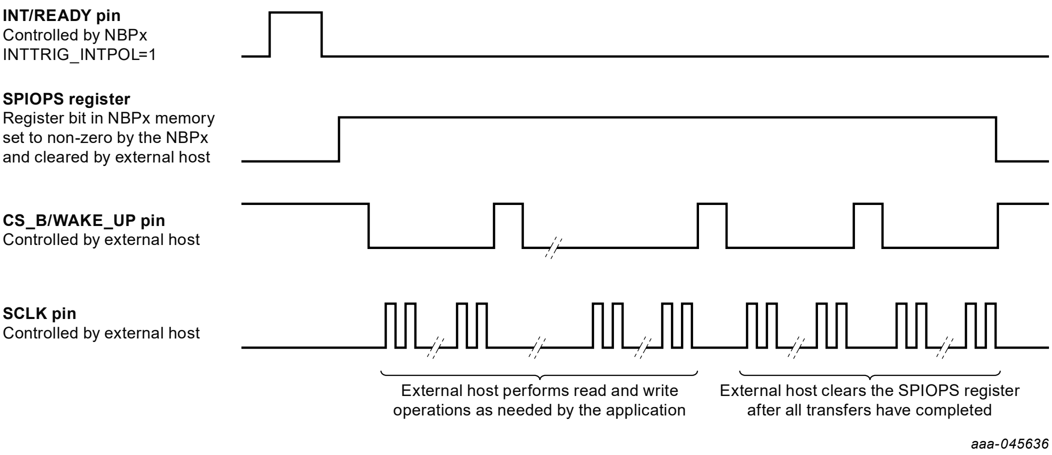


Figure 18. SPI timing description when transfers are requested by the NBP8 via the INT pin, with INTTRIG_INTPOL=1

Figure 19 shows the case where PS ENABLE pin is enabled.

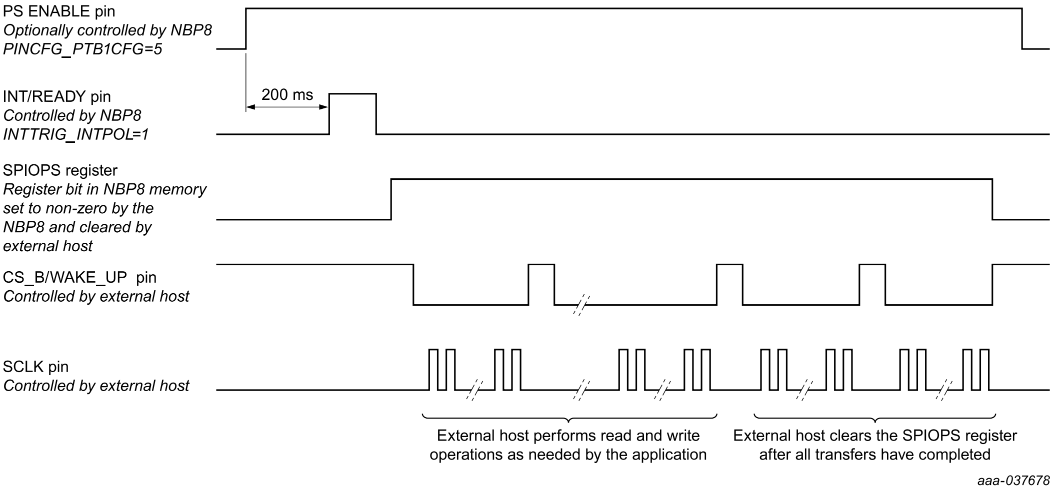


Figure 19. SPI timing description when transfers are requested by the NBP8 via the INT pin, with PINCFG_PTB1CFG = 5 and INTTRIG_INTPOL=1

6.7 Typical sequence timings

6.7.1 Periodic events

Figure 20 illustrates a sequence of periodic events. The sampling period configured in the PSP register corresponds to the execution time of the sensor measurements, pressure change algorithm(s) execution, and sleep duration. The available sampling periods are achieved by adjusting the sleep time.

The execution time of the periodic ADC and Pcell Self-Test is not included in the sampling period. The duration of the Self-Test is indicated at the end of this section. The power consumption of sensor measurements is indicated in Table 51.

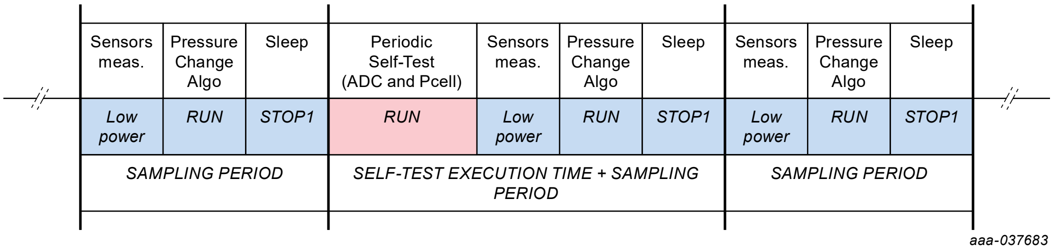


Figure 20. Sequence of periodic events

6.7.2 NBP8 notifying the external host

Figure 21 and Figure 22 illustrate a sequence of periodic events during which the NBP8 notifies the External host that an event requiring attention has occurred. When such an event occurs, the NBP8 generates a pulse on the INT pin and then waits until either the External host clears the SPIOPS register via SPI or the 2048 ms timeout period expires.

In the first example, the External host clears the SPIOPS during the last SPI transfer. The NBP8 then executes the commands that have been configured by the External host in the CMD register.

The duration of the INT pulse is configured by the user with the INTTRIG_INTDUR bit. The time during which the NBP8 waits after generating the INT pulse depends on the time needed by the External host to start the SPI transfers and the duration of the SPI transfers, which itself depends on the SPI baud rate configured on the external host side and the number of transfers performed. The execution time of the commands performed by the NBP8 is indicated at the end of this section. The duration of the Self-Test is indicated at the end of this section. The power consumption of sensor measurements is indicated in Table 51.

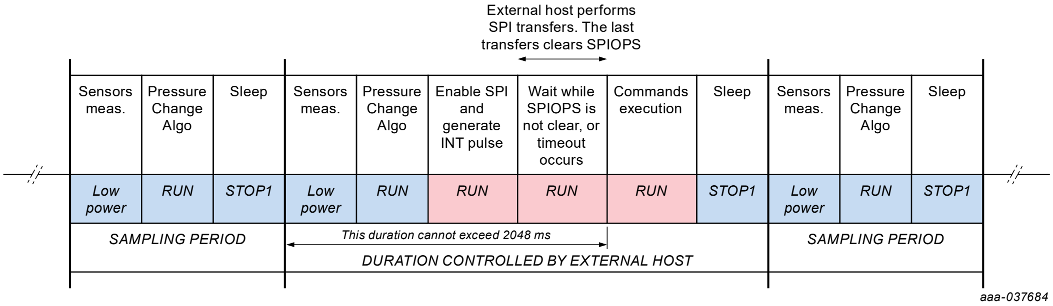


Figure 21. Sequence of events when NBP8 notifies the external host of an event and the external host clears the SPIOPS register

The second example illustrates the sequence of events when the external host does not clear the SPIOPS register via SPI. In that case, the NBP8 exits the waiting state on timeout before entering the sleep state. Note that in this situation, the NBP8 does not execute the potential commands that could have been written in the CMD register. This is because exiting on timeout is not the expected sequence of events, indicating that a problem occurred on the external host side.

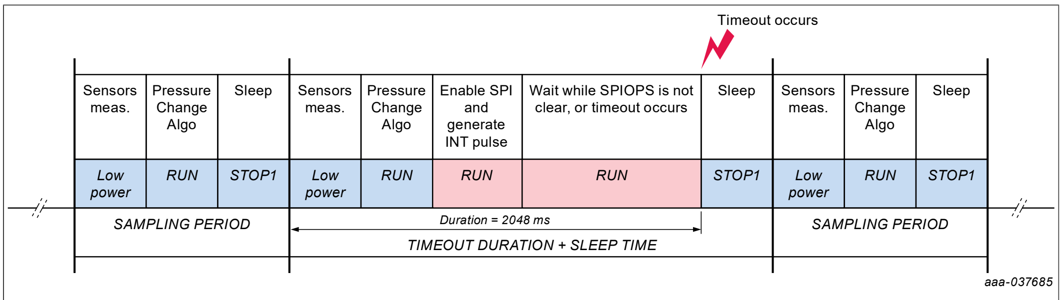


Figure 22. Sequence of events when NBP8 notifies the external host of an event but the external host does not clear the SPIOPS register

6.7.3 External host requesting an SPI transfer

Figure 23 and Figure 24 illustrate a sequence of periodic events during which the external host triggers an interrupt on the NBP8 side via the WAKE-UP pin in order to request SPI transfers.

If the WAKE-UP interrupt is triggered while the NBP8 is in the sleep state (as in the example below), the NBP8 wakes up immediately, enables SPI, and raises the READY pin. That series of events (wake up, enable SPI, and raise the READY pin) takes 125 µs.

If the WAKE-UP interrupt is triggered while the NBP8 performs sensor measurements, self-test, or any of the actions triggered by the CMD register, the NBP8 first completes the ongoing action before enabling SPI, and raising the READY pin. Raising the READY pin can take up to 8 ms (or up to 132 ms, if the NBP8 if performing firmware verification).

In the first example, the external host clears the SPIOPS register during the last SPI transfer. After exiting the wait state, the NBP8 executes the commands configured by the external host in the CMD register before continuing the periodic sequence of events.

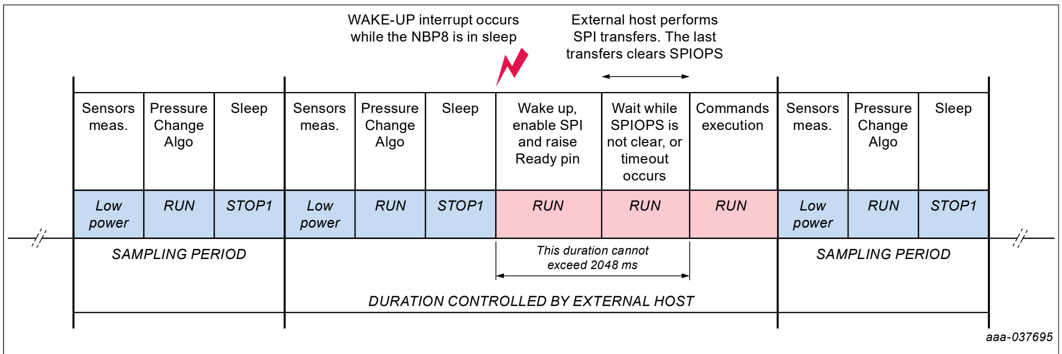


Figure 23. External host requests SPI transfers and then clears the SPIOPS register

In the second example, the external host does not clear the SPIOPS register during the SPI transfers, so the NBP8 exits the wait state on timeout before entering the sleep state. Note in this situation, the NBP8 does not execute the potential commands that could have been written in the CMD register due to exiting on timeout. The timeout indicates that a problem occurred on the external host side.

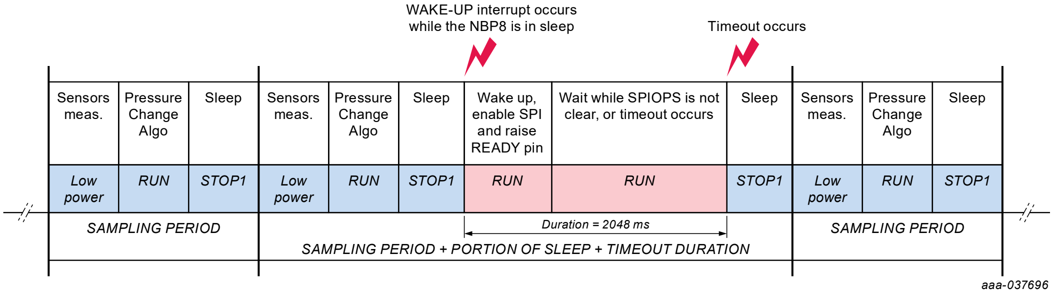


Figure 24. External host requests SPI transfers but does not clear the SPIOPS register

6.7.4 Summary of execution times

Table 7 summarizes the execution times of the different actions. Sensor measurements include raw pressure, raw temperature, and raw voltage readings, followed by pressure, temperature, and voltage compensations.

Table 7. Summary of execution times

Action	Periodic/Triggered	Duration
Sensor measurements	Periodic	4.4 ms
Pressure change algorithm	Periodic	100 μs
ADC and Pcell self-test	Periodic	3.47 ms
ADC self-test	Triggered by CMD_ADCST	455 μs
Pcell self-test	Triggered by CMD_PST	3.32 ms
Firmware verification	Triggered by CMD_FV	132 ms
Reset registers	Triggered by CMD_RESET	206 μs
Clear FIFO	Triggered by CMD_CLRFIFO	185 μs
Acknowledge INTF	Triggered by CMD_ACKINTF	18 μs

6.8 Read/write targets accessible by the external host via SPI

This section details the addresses of the NBP8 accessible by the external host via SPI.

Table 8. Read and write addresses summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0038	SPIOPS	reserved	reserved	reserved	reserved	reserved	CORE_TR_HOLD	reserved	reserved
$0050	PSP	PSP[7:0]							
$0051	STPER	STPER[7:0]							
$0052	PINCFG	reserved	reserved	reserved	reserved	reserved	PINCFG[2:0]		
$0053	INTTRIG	reserved	reserved	INTPOL	INTDUR	FVERR	STERR	SENSERR	SENSRDY
$0054	PCCFG	reserved	reserved	reserved	reserved	reserved	STEN	RTEN	FTEN
$0055	STATUS	INTF	PCSTF	PCRTF	PCFTF	FVF	PSTF	ADCSTF	SENSF
$0056	SENSTATUS	ADCERR	LVW	POVER	PUNDER	TOVER	TUNDER	VOVER	VUNDER
$0057	CMD	ACKINTF	reserved	reserved	CLRFIFO	RESET	FV	PST	ADCST

Table 8. Read and write addresses summary*...continued*

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0058	PCDEBT	PCDEBT[7:0]							
$0059	PCFIXTH	PCFIXT[15:8]							
$005A	PCFIXTL	PCFIXT[7:0]							
$005B	PCMINT	PCMINT[7:0]							
$005C	PCRELTH	PCRELT[15:8]							
$005D	PCRELTL	PCRELT[7:0]							
$005E	PCSLOPETH	PCSLOPET[15:8]							
$005F	PCSLOPETL	PCSLOPET[7:0]							
$0070:	TCODE	TCODE[7:0]							
$0071	VCODE	VCODE[7:0]							
$0075	INDFIFO	INDFIFO[7:0]							
$0076 to $008D	PFIFOH 1[15:8] PFIFOL1[7:0] to PFIFOH12[15:8] PFIFOL12[7:0]	PFIFO1[15:0] through PFIFO12[15:0]							

The detail of the read/write targets is given below.

Table 9. SPI Operations (SPIOPS) (address 0x0038)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	CORE_ TR_ HOLD	Bit1	Bit0
POR or User Reset ($0)	0	0	0	0	0	0	0	0

Table 10. SPIOPS fields description

Fields	Description
7 to 3	Reserved
2 SPIOPS[2]	SPIOPS[2] CORE_TR_HOLD - Core read/write accesses on hold. This bit is used to ensure that SPI becomes the only internal bus server with unhindered access to the system registers. 0 = internal bus normal; SPI is granted access only if the internal CPU is not accessing the same sub-bus modules; Result of Reset. 1 = internal CPU on hold; SPI has unhindered access to the system registers, for the external host SPI server to read or write as needed. Must be cleared to 0 at the end of the external host SPI server transaction, to release the internal CPU.
1 to 0	Reserved

Table 11. Pressure Sampling Period (PSP) (address 0x0050)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($4)	0	0	0	0	0	1	0	0

Table 12. PSP fields description

Fields	Description
7 to 0 PSP[7:0]	The PSP[7:0] configures the period at which pressure measurement is triggered. The operating range of PSP[7:0] is $00 to $06, resulting in the following sampling periods: PSP[7:0] = $00: SAMPLING PERIOD = 10 ms PSP[7:0] = $01: SAMPLING PERIOD = 20 ms PSP[7:0] = $02: SAMPLING PERIOD = 40 ms PSP[7:0] = $03: SAMPLING PERIOD = 70 ms PSP[7:0] = $04: SAMPLING PERIOD = 135 ms PSP[7:0] = $05: SAMPLING PERIOD = 510 ms PSP[7:0] = $06: SAMPLING PERIOD = 1000 ms PSP[7:0] = $07 to $FF = same as $06. The typical sampling periods may vary due to the LFO clock tolerance listed in Section 9 "Electrical specifications". The reset value is $04, resulting in a 135 ms period. When the PSP value is changed by the External Host, the Pressure FIFO is cleared after completion of the SPI transfers

Table 13. Self-Test Execution Period (STPER) (address 0x0051)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($FF)	1	1	1	1	1	1	1	1

Table 14. STPER fields description

Fields	Description
7 to 0 STPER[7:0]	The STPER[7:0] configures the period at which ADC and Pcell Self-Test is performed. The operating range of STPER[7:0] is $00 to $FF. A value of $00 disables the periodic Self-Test. Any other value gives a range of Self-Test execution period from 1 to 255 x SAMPLING PERIOD. Depending on the value of the bits for the PSP[7:0], the Self-Test execution period can nominally be from 2.55 s to 255 s. The conversion from the decimal value of STPER[7:0] to the period in milliseconds is given as described by the following equation. SELF TEST PERIOD = STPER[7:0] * SAMPLING PERIOD

Table 15. PIN Configuration (PINCFG) (address 0x0052)

Bit	7	6	5	4	3	2	1	0
R/W	—	—	—	—	—	PINCFG2	PINCFG1	PINCFG0
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 16. PINCFG fields description

Fields	Description
7 to 3 Reserved	Reserved bits—not for user access
2 to 0 PINCFG[2:0]	The PINCFG[2:0] configures the PTB1 pin function as described below: PINCFG[2:0] = 0 0 0: the pin is disabled PINCFG[2:0] = 0 0 1: the pin is disabled PINCFG[2:0] = 0 1 0: the pin is disabled PINCFG[2:0] = 0 1 1: the pin is disabled PINCFG[2:0] = 1 0 0: the PS ENABLE function is enabled and the pin is idle at logic 1, asserted at logic 0 PINCFG[2:0] = 1 0 1: the PS ENABLE function is enabled and the pin is idle at logic 0, asserted at logic 1 PINCFG[2:0] = 1 1 0: the pin is disabled PINCFG[2:0] = 1 1 1: the pin is disabled

Table 17. Interrupt pulse Trigger (INTTRIG) (address 0x0053)

Bit	7	6	5	4	3	2	1	0
R/W	—	—	INTPOL	INTDUR	FVERR	STERR	SENSERR	SENSRDY
POR or User Reset ($3E)	—	—	1	1	1	1	1	0

Table 18. INTTRIG fields description

Fields	Description
7 to 6	Reserved bits—not for user access
5 INTPOL	INT pin Polarity – Selects the polarity of the INT/READY pin. 0 The pin is asserted to logic 0 during the pulse, and idle at logic 1 1 The pin is asserted to logic 1 during the pulse, and idle at logic 0
4 INTDUR	INT pulse Duration - Selects the duration of the pulse generated by the NBP8 on the INT pin. 0 Pulse on the INT pin has a duration of 4 ms 1 Pulse on the INT pin has a duration of 8 ms
3 FVERR	Firmware Verification Error – Selects whether the NBP8 generates a pulse on the INT pin when the Firmware Verification execution completes with errors. 0 No pulse generated on the INT pin when the Firmware Verification execution completes with errors 1 Pulse generated on the INT pin when the Firmware Verification execution completes with errors
2 STERR	Self-Test Error – Selects whether the NBP8 generates a pulse on the INT pin when the Pcell or ADC Self-Test execution completes with errors. 0 No pulse generated on the INT pin when the Self-Test execution completes with errors 1 Pulse generated on the INT pin when the Self-Test execution completes with errors
1 SENSERR	Sensor Error – Selects whether the NBP8 generates a pulse on the INT pin when the sensor data acquisition completed with errors. 0 No pulse generated on the INT pin when the sensor data acquisition completed with errors 1 Pulse generated on the INT pin when the sensor data acquisition completed with errors

Table 18. INTTRIG fields description*...continued*

Fields	Description
0 SENSRDY	Sensor Data Ready – Selects whether the NBP8 generates a pulse on the INT pin when the sensor data acquisition completed, and new sensor data is available. 0 No pulse generated on the INT pin when the sensor data acquisition completed, and new sensor data is available 1 Pulse generated on the INT pin when the sensor data acquisition completed, and sensor data is available

Table 19. Pressure Change Configuration (PCCFG) (address $0054)

Bit	7	6	5	4	3	2	1	0
R/W	--	--	--	--	--	STEN	RTEN	FTEN
POR or User Reset ($01)	0	0	0	0	0	0	0	1

Table 20. PCCFG fields description

Fields	Description
7 to 3 Reserved	Reserved bits – Not for user access.
2 STEN	Slope Threshold Enable – Enables the option to monitor the pressure change of rate vs. a change of rate threshold. 0 Option disabled 1 Option enabled
1 RTEN	Relative Threshold Enable – Enables the option to monitor the pressure vs. a relative threshold. 0 Option disabled 1 Option enabled
0 FTEN	Fixed Threshold Enable – Enables the option to monitor the pressure vs. a fixed threshold. 0 Option disabled 1 Option enabled

Table 21. Status of the latest executions (STATUS) (address 0x0055)

Bit	7	6	5	4	3	2	1	0
R	INTF	PCSTF	PCRTF	PCFTF	FVF	PSTF	ADCSTF	SENSF
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 22. STATUS fields description

Fields	Description
7 INTF	INT pin Flag – Indicates whether a condition for pulse generation is met, and a pulse on the INT pin is generated. 0 No pulse on the INT pin is generated 1 Pulse on the INT pin is generated. Events that occurred are detailed in bits 6:0. Including INTF, each of the bits are cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
6 PCSTF	Pressure Change Slope Threshold Flag – Indicates whether the pressure rate of change has exceeded the rate of change threshold PCSLOPET. 0 Condition is not met, the pressure rate of change has not exceeded the threshold 1 Condition is met, the pressure rate of change has exceeded the threshold. STATUS_INTF is set and a pulse is generated on the INT pin.
5 PCRTF	Pressure Change Relative Threshold Flag – Indicates whether the pressure has exceeded the relative threshold PCRELT. 0 Condition is not met, the pressure has not exceeded the threshold 1 Condition is met, the pressure has exceeded the threshold. STATUS_INTF is set and a pulse is generated on the INT pin.
4 PCFTF	Pressure Change Fixed Threshold Flag – Indicates whether the pressure has exceeded the fixed threshold PCFIXT. 0 Condition is not met, the pressure has not exceeded the threshold 1 Condition is met, the pressure has exceeded the threshold. STATUS_INTF is set and a pulse is generated on the INT pin.
3 FVF	Firmware Verification Flag– Indicates the status of the latest firmware verification. 0 The latest firmware verification completed with no errors 1 The latest firmware verification completed with errors. If INTTRIG_FVERR is set, STATUS_INTF is set and a pulse is generated on the INT pin.
2 PSTF	Pcell Self-Test Flag – Indicates the status of the latest Pcell Self-Test. 0 The latest Pcell Self-Test completed with no errors 1 The latest Pcell Self-Test completed with errors. If INTTRIG_STERR is set, STATUS_INTF is set and a pulse is generated on the INT pin.
1 ADCSTF	ADC Self-Test Flag – Indicates the status of the latest ADC Self-Test. 0 The latest ADC Self-Test completed with no errors 1 The latest ADC Self-Test completed with errors. If INTTRIG_STERR is set, STATUS_INTF is set and a pulse is generated on the INT pin.
0 SENSF	Sensor Flag – Indicates the status of the latest sensor acquisition. 0 The latest sensor acquisition completed with no errors, the SENSTATUS fields are all clear. If INTTRIG_SENSRDY is set, a pulse is generated on the INT pin after completion of the acquisition 1 The latest sensor acquisition completed with errors detailed in the SENSTATUS fields. If INTTRIG_SENSERR or INTTRIG_SENSRDY is set, STATUS_INTF is set and a pulse is generated on the INT pin after completion of the acquisition.

Table 23. Sensor Status (SENSTATUS) (address 0x0056)

Bit	7	6	5	4	3	2	1	0
R	ADCERR	LVW	POVER	PUNDER	TOVER	TUNDER	VOVER	VUNDER
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 24. SENSTATUS fields description

Fields	Description
7 ADCERR	ADC Error – Indicates whether an ADC error occurred during the latest sensor acquisition. 0 No ADC error occurred during the latest sensor acquisition 1 An ADC error occurred during the latest sensor acquisition. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
6 LVW	Low Voltage Warning – Indicates whether the voltage is suspected to be below operating range for pressure measurement. 0 Voltage is in-range 1 Voltage is suspected to be below operating range, pressure accuracy is not guaranteed. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
5 POVER	Pressure Overflow – Indicates whether the latest pressure acquisition resulted in an overflow. 0 The latest pressure measurement did not overflow 1 The latest pressure measurement resulted in an overflow. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
4 PUNDER	Pressure Underflow – Indicates whether the latest pressure acquisition resulted in an underflow. 0 The latest pressure measurement did not underflow 1 The latest pressure measurement resulted in an underflow. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
3 TOVER	Temperature Overflow – Indicates whether the latest temperature acquisition resulted in an overflow. 0 The latest temperature measurement did not overflow 1 The latest temperature measurement resulted in an overflow. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
2 TUNDER	Temperature Underflow – Indicates whether the latest temperature acquisition resulted in an underflow. 0 The latest temperature measurement did not underflow 1 The latest temperature measurement resulted in an underflow. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
1 VOVER	Voltage Overflow – Indicates whether the latest voltage acquisition resulted in an overflow. 0 The latest voltage measurement did not overflow 1 The latest voltage measurement resulted in an overflow. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.
0 VUNDER	Voltage Underflow – Indicates whether the latest voltage acquisition resulted in an underflow. 0 The latest voltage measurement did not underflow 1 The latest voltage measurement resulted in an underflow. The bit is cleared after completion of the SPI transfers, if the external host set CMD_ACKINTF.

Table 25. Command (CMD) (address 0x0057)

Bit	7	6	5	4	3	2	1	0
R/W	ACKINTF	--	--	CLRFIFO	RESET	FV	PST	ADCST
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 26. CMD fields description

Fields	Description
7 ACKINTF	Acknowledge INT Flag – If the external host writes logic 1 to this bit, the STATUS, and SENSTATUS registers will be cleared after completion of the SPI transfers. 0 No effect 1 Clearing the STATUS, and SENSTATUS registers is requested. The NBP8 clears this bit after completion of the command
6 to 5	Reserved bits – Not for user access.
4 CLRFIFO	Clear FIFO - If the external host writes logic 1 to this bit, the Pressure FIFO will be cleared after completion of the SPI transfers. 0 No effect 1 Clearing the Pressure FIFO is requested. The NBP8 clears this bit after completion of the command
3 RESET	Reset – Indicates to the NBP8 whether a one-time register reset is requested after completion of the on-going SPI transfer sequence. Register reset sets all read/write user targets to their reset values. 0 No register reset requested 1 Register reset is requested. The NBP8 clears this bit after completion of the command
2 FV	Firmware Verification – Indicates to the NBP8 whether a one-time Firmware Verification is requested after completion of the on-going SPI transfer sequence. 0 No Firmware Verification requested 1 Firmware Verification requested. The NBP8 clears this bit after completion of the command
1 PST	Pressure cell Self-Test – Indicates to the NBP8 whether a one-time pressure cell Self-Test is requested after completion of the on-going SPI transfer sequence. 0 No pressure cell Self-Test requested 1 Pressure cell Self-Test requested. The NBP8 clears this bit after completion of the command
0 ADCST	ADC Self-Test – Indicates to the NBP8 whether a one-time ADC Self-Test is requested after completion of the on-going SPI transfer sequence. 0 No ADC Self-Test requested 1 ADC Self-Test requested. The NBP8 clears this bit after completion of the command

Table 27. Pressure Change Debounce Threshold (PCDEBT) (address 0x0058)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($05)	0	0	0	0	0	1	0	1

Table 28. PCDEBT fields description

Fields	Description
7 to 0 PCDEBT[7:0]	The PCDEBT[7:0] debounce threshold defines the minimum debounce value to consider that a Pressure Change condition has been met. The operating range of PCDEBT[7:0] is 0 to 254. If this register is configured to value 255 by the External host during an SPI transfer, the value will be changed to 254 after completion of the SPI transfers.

Table 29. Pressure Change Fixed Threshold High (PCFIXTH) (address 0x0059)

Bit	7	6	5	4	3	2	1	0
R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
POR or User Reset ($03)	0	0	0	0	0	0	1	1

Table 30. Pressure Change Fixed Threshold Low (PCFIXTL) (address 0x005A)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($20)	0	0	1	0	0	0	0	0

Table 31. PCFIXTH/L fields description

Fields	Description
15 to 0 PCFIXT[15:0]	The two PCFIXT[15:0] define the fixed threshold value used in the Fixed Threshold algorithm. When PCCFG_FTEN is set, the flag STATUS_PCFTF is raised when pressure is consistently above this threshold.

Table 32. Pressure Change Minimum Threshold (PCMINT) (address $005B)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($03)	0	0	0	0	0	0	1	1

Table 33. PCMINT fields description

Fields	Description
7 to 0 PCMINT[7:0]	The PCMINT[7:0] defines the minimum number of counts by which the current pressure value must exceed the previous pressure value, for the NBP8 program to consider that the pressure is increasing.

Table 34. Pressure Change Relative Threshold High (PCRELTH) (address $005C)

Bit	7	6	5	4	3	2	1	0
R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 35. Pressure Change Relative Threshold Low (PCRELTL) (address $005D)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Table 35. Pressure Change Relative Threshold Low (PCRELTL) (address $005D)*...continued*

Bit	7	6	5	4	3	2	1	0
POR or User Reset ($32)	0	0	1	1	0	0	1	0

Table 36. PCRELTH/L fields description

Fields	Description
15 to 0 PCRELT[15:0]	The two PCRELT[15:0] define the relative threshold value used in the Relative Threshold algorithm. When PCCFG_RTEN is set, the flag STATUS_PCRTF is raised when pressure increase is consistently above this threshold.

Table 37. Pressure Change Slope Threshold High (PCSLOPETH) (address 0x005E)

Bit	7	6	5	4	3	2	1	0
R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 38. Pressure Change Slope Threshold Low (PCSLOPETL) (address 0x005F)

Bit	7	6	5	4	3	2	1	0
R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($40)	0	1	0	0	0	0	0	0

Table 39. PCSLOPETH/L fields description

Fields	Description
15 to 0 PCSLOPET[15:0]	The two PCSLOPET[15:0] define the rate of change threshold value used in the Slope Threshold algorithm. When PCCFG_STEN is set, the flag STATUS_PCSTF is raised when the pressure rate of change exceeds this threshold. Calculate the slope by *ΔP * 128* / *number sampling periods* where: –*ΔP* is the pressure increase, in counts –*128* is a multiplication coefficient, to scale the slope –*number sampling periods* is the number of sampling periods during which the pressure has been increasing until the slope is calculated Note the slope value is expressed in pressure counts per sampling period. The conversion to kPa/s depends on the pressure sensitivity and the user-selected sampling period value. *Example:* For a pressure sensitivity equal to 0.2 kPa/LSB and a sampling period selected as 135 ms, a pressure increase of 10 kPa over 1 second corresponds to a pressure increase of 50 pressure counts over 7.4 sampling periods, resulting in a slope value of 50*128/7.4 = 864. If the sampling period is selected as 70 ms, then a pressure increase of 10 kPa over 1 second corresponds to a pressure increase of 50 pressure counts over 14.3 sampling periods, resulting in a slope value of 50*128/14.3 = 447.

Table 40. Temperature measurement (TCODE) (address $0070)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($70)	0	0	0	0	0	0	0	0

Table 41. TCODE fields description

Fields	**Description**
7 to 0 TCODE[7:0]	The TCODE[7:0] stores the most recent compensated internal device temperature measurement, and can be converted to °C by the transfer function *T °C = (1 °C / LSB × TCODE) – 55 °C*

Table 42. Voltage measurement (VCODE) (address $0071)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($70)	0	0	0	0	0	0	0	0

Table 43. Voltage measurement fields description

Fields	**Description**
7 to 0 VOCODE[7:0]	The VCODE[7:0] stores the most recent compensated internal device voltage measurement, and can be converted to V using the transfer function *V = (0.01 V / LSB × VCODE) + 1.22 V.*

Table 44. Index of the pressure FIFO (INDFIFO) (address $0075)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POR or User Reset ($76)	0	1	1	1	0	1	1	0

Table 45. INDFIFO fields description

Fields	**Description**
7 to 0 INDFIFO[7:0]	The INDFIFO[7:0] stores the address of the last byte written in the pressure PFIFO.

Table 46. Pressure FIFO (PFIFOH/Lx) (addresses $0076 - $008D)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Table 46. Pressure FIFO (PFIFOH/Lx) (addresses $0076 - $008D)*...continued*

Bit	7	6	5	4	3	2	1	0
POR or User Reset ($00)	0	0	0	0	0	0	0	0

Table 47. PFIFOH/Lx fields description

Fields	Description
15 to 8 PFIFOHx[15:8] 7 to 0 PFIFOLx[7:0][1]	The PFIFO stores the 12 latest pressure measurements. The PFIFO is implemented as a rolling buffer: the most recent pressure measurement overwrites the oldest one. The INDFIFO index holds the value of the last address written. Each entry shall occupy two bytes, high byte at first address and low byte at second address, for a total of 24 bytes.

[1] Where x = 1 to 12.

7 Limiting values

Limiting values are the extreme limits the device can be exposed to without permanently damaging it. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than the values shown in Table 48. Keep V_{IN} and V_{OUT} within the range $V_{SS} \leq (V_{IN}$ or $V_{OUT}) \leq V_{DD}$.

Table 48. Maximum ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{DD}	V_{DD} or V_{DDA} to V_{SS}	$T_L \leq T_A \leq T_h$	–0.3	—	3.8	V	C
V_{IO}	IO pin current, each pin vs V_{DD} / V_{DDA} or V_{SS}	T_{AS} Min ≤ T_A ≤ T_A Max	V_{ss} – 0.3	—	V_{dd} + 0.3	V	C
I_{IO}	IO pin current, pin vs V_{DD} / V_{DDA} or V_{SS}	$T_L \leq T_A \leq T_H$, V_{DDR} Min ≤ V_{DD} ≤ V_{DDR} Max	–10	—	10	mA	C
I_{SUBIO}	Substrate current injection, all IO pins current from pin to V_{SS} – 0.3 V	$T_L \leq T_A \leq T_H$, V_{DDR} Min ≤ V_{DD} ≤ V_{DDR} Max	—	600	—	µA	C
I_{LATCH}	Latch-up current, current to/from pin to V_{DD} / V_{DDA} + 0.3 V	$T_L \leq T_A \leq T_H$, V_{DDR} Min ≤ V_{DD} ≤ V_{DDR} Max	–100	—	100	mA	C
ESD_{HBM}	Electrostatic discharge, human body model (HBM), all pins	T_A = 25 °C, V_{DD} = 3.0 V	–2000	—	2000	V	C
ESD_{CDM}	Electrostatic discharge, charged device model (CDM), all pins	T_A = 25 °C, V_{DD} = 3.0 V	–500	—	500	V	C
T_{STG}	Unpowered storage, temperature range	—	–50	—	150	°C	C

8 Recommended operating conditions

The limits normally expected in the application that define the range of operation.

Table 49. Operating range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{DDR}	Operating voltage range, Parameter register retention where Min = V_L, Typ = 3.0 V, Max = V_H	T_{AS} Min ≤ T_A ≤ T_{AS} Max	1.2	3.0	3.6	V	C

Table 49. Operating range*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{DDS}	Operating voltage range, CPU and SW, Flash Read, Voltage Measurement where Min = V_L, Typ = 3.0 V, Max = V_H	T_{AS} Min ≤ T_A ≤ T_{AS} Max	1.8	3.0	3.6	V	C
V_{DDM}	Operating voltage range, pressure, and temperature measurements where Min = V_L, Typ = 3.0 V, Max = V_H	T_{AS} Min ≤ T_A ≤ T_{AS} Max	2.1	3.0	3.6	V	C
V_{DDF}	Operating voltage range, Flash Programming where Min = V_L, Typ = 3.0 V, Max = V_H	–20 °C ≤ T_A ≤ 85 °C	2.1	3.0	3.6	V	C
T_{AS}	Operating temperature range, Full functionality except Flash Programming where Min = T_L, Typ = 25 °C, Max = T_H	V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max	–40	25	125	°C	C
T_{AF}	Operating temperature range, Operating voltage range, Full functionality, including Flash programming	V_{DDF} Min ≤ V_{DD} ≤ V_{DDF} Max	–20	25	85	°C	C
$T_{A\text{-}EXC}$	Operating temperature range excursion; 12 excursions of 15 minutes ea. (all Tolerances may be out of spec)	V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max	—	—	150	°C	C
I_{DD1}	Supply Current; Stop1 Mode (only LFO, PWU, and param. reg. On)	Typ = 25 °C, 3.0 V, Max = T_{AS} Min to Max and V_{DDR} Min to Max	—	0.18	18	µA	B
I_{DDR4M}	Supply Current; CPU Run 4 MHz	Typ = 25 °C, 3.0 V, Max = T_{AS} Min to Max and V_{DDS} Min to Max	—	2.1	2.5	mA	B

9 Electrical specifications

Tables in the electrical and mechanical specification sections of this data sheet may contain hyperlinked note references in the last cell of the row. The hyperlinks are linked to and defined in Table 50.

Table 50. Electrical and mechanical specification note definition table

Note identifier	Description
A	Parameters tested 100 % at final test.
B	Parameters tested 100 % at unit probe.
C	Verified by characterization, not tested in production.
D	For information only, may be determined by simulation.

9.1 Charge consumptions

Table 51. Charge consumptions

$T_L \le T_A \le T_H$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
Q_{wake}	Stop1 to run charge consumption, F_{bus} set for 4 MHz	V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max	—	0.10	—	µA-sec	C
QPA_{r2584}	Pressure charge consumption; Raw 2584 µs settling per sample	V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max	—	1.9	—	µA-sec	D
QP_{c3}	Pressure charge consumption; Compensation third order per sample	V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max	—	1.77	—	µA-sec	D
QVT_{r50}	Voltage or temperature charge consumption; Raw 50 µs conversion per sample	V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max	—	0.2	—	µA-sec	C
QVT_{c250}	Voltage or temperature charge consumption; Compensation ~0.25 ms per sample	V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max	—	0.50	—	µA-sec	D

9.2 Clocks and thresholds

Table 52. Clocks and thresholds

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
f_{BUS}	CPU bus frequency multiple of HFO	V_{DD} > 2.1 V	—	0.5	—	x HFO	D
f_{HFO}	High frequency oscillator, multiple of MFO	V_{DD} > 2.1 V	—	64	—	x MFO	D
t_{HFOST}	Stabilization time	—	—	300	1000	µs	D
f_{MFO}	Medium frequency oscillator	V_{DD} > 2.1 V	107	125	135	kHz	A
f_{LFO}	Low frequency oscillator	—	504	—	1512	Hz	B
t_{STOP1}	CPU wake-up time	From Stop1 to 1st instruction, 4 MHz	—	50	70	µs	C
t_{STOP4}	CPU wake-up time	From Stop4 to 1st instruction, 4 MHz	—	25	35	µs	C
t_{LV}	Low voltage times	V_{DD} < V_{LVx}	—	—	10	µs	D

Table 52. Clocks and thresholds*...continued*

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{LVWLF}	Low voltage warning (LVW)	Lower threshold, V_{DD} falling	1.95	—	2.2	V	C
V_{LVWLR}	Low voltage warning (LVW)	Lower threshold, V_{DD} rising	2.02	—	2.1	V	C
V_{LVWHF}	Low voltage warning (LVW)	Higher threshold, V_{DD} falling	2.28	—	2.54	V	C
V_{LVWHR}	Low voltage warning (LVW)	Higher threshold, V_{DD} rising	2.34	—	2.61	V	C
V_{LVDLF}	Low voltage detection (LVD)	Lower threshold, V_{DD} falling	1.79	—	1.96	V	C
V_{LVDLR}	Low voltage detection (LVD)	Lower threshold, V_{DD} rising	1.87	—	2.03	V	C
V_{LVDHF}	Low voltage detection (LVD)	Higher threshold, V_{DD} falling	1.95	—	2.2	V	C
V_{LVDHR}	Low voltage detection (LVD)	Higher threshold, V_{DD} rising	2.02	—	2.1	V	C
T_{FDR}	Flash memory data retention	—	10	—	—	Yr	D

9.3 Power-on reset operation

When power is initially applied to the device, or when the supply voltage drops below the V_{POR} level, the POR circuit causes a reset condition. As the supply voltage rises, the LVD circuit holds the chip in reset until the supply has risen above the level determined by LVDV bit. Both the POR bit and the LVD bit in SRS are set following a POR.

Table 53. Power-on reset

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
t_R	Power on reset (POR)	V_{DD} risetime to avoid latch up	—	—	1	s	C
t_{POR}	Power on reset (POR)	Time for V_{DD} < 0.5 V to assure POR	70	—	—	µs	C
V_{PORR}	Power on reset (POR)	Rising voltage to release reset	—	—	2.1	V	C
V_{PORA}	Power on reset (POR)	Falling voltage to assert reset	0.8	—	—	V	C

9.4 GPIO port pins

Table 54. GPIO port pins

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{OH}	Output high voltage	I_{LOAD} = 5 mA	V_{DD} – 0.35	—	—	V	D
V_{OL}	Output low voltage	I_{LOAD} = 5 mA	—	—	V_{SS} + 0.35	V	D
V_{IHn}	Input high voltage	2.3 V ≤ V_{DD} ≤ V_H, T_A = T_L, T_H	0.7 × V_{DD} / V_{DDA}	—	V_{DD} / V_{DDA}	V	D
V_{IHlv}	Input high voltage	V_{DD} ≤ 2.3 V, T_A = 25 °C	0.85 × V_{DD} / V_{DDA}	—	V_{DD} / V_{DDA}	V	D
V_{ILn}	Input low voltage	2.3 V ≤ V_{DD} ≤ V_H, T_A = T_L, T_H	V_{SS}	—	0.35 × V_{DD} / V_{DDA}	V	D
V_{ILlv}	Input low voltage	V_{DD} ≤ 2.3 V, T_A = 25 °C	V_{SS}	—	0.28 × V_{DD} / V_{DDA}	V	D

Table 54. GPIO port pins*...continued*

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
I_{IH}	Input high current, PTA0:3	Pulldown disabled; V_{IH} Min	–1	—	+1	μA	D
I_{IHp}	Input high current, PTA0:3	Pulldown enabled; V_{IH} Min	0	—	120	μA	D
I_{IL}	Input low current, PTA0:3	Pullup disabled; V_{IL} Max	–1	—	+1	μA	D
I_{ILp}	Input low current PTA0:3	Pullup enabled; V_{IL} Max	–120	—	0	μA	D
$I_{IH\text{-}IL}$	Input current PTA4 only	V_{IH} Min and V_{IL} Max	–120	—	120	μA	D
C_{IO}	Pin capacitance	V_{DD} = 3.0 V	0	—	15	pF	D
C_{SICO}	SICO load capacitance	V_{DD} = 3.0 V	—	—	50	pF	D

9.5 SPI timing characteristics

Table 55. SPI timing

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
t_{SSMIN}	CS_B asserted period	f_{BUS} = 4 MHz	1	—	—	f_{BUS} period	
t_{ACCESS}	CS_B low to SICO	—	—	—	50	ns	D
t_{LEAD}	CS_B low to SCLK start	—	50	—	—	ns	D
t_{SETUP}	SOCI to SCLK start	—	20	—	—	ns	D
t_{SCLK}	SCLK period	—	100	—	—	ns	D
t_{SCLKH}	SCLK high portion	—	35	—	—	ns	D
t_{SCLKL}	SCLK low portion	—	35	—	—	ns	D
t_{SCLKR}	SCLK risetime	—	—	10	25	ns	D
t_{SCLKF}	SCLK fall time	—	—	10	25	ns	D
t_{VALID}	SICO valid transition time	—	—	—	30	ns	D
t_{HOLD_IN}	SOCI hold time	—	10	—	—	ns	D
t_{HOLD_OUT}	SCLK high to SICO transition start	—	0	—	—	ns	D
t_{LAG}	Final SCLK low to CS_B high	—	60	—	—	ns	D
$t_{DISABLE}$	CS_B high to SICO 3-state	—	—	—	60	ns	D
t_{SS_REJ}	CS_B noise rejection period	—	—	—	5	ns	D
t_{SSCLK}	CS_B high to SCLK high	—	50	—	—	ns	D
t_{CLKSS}	SCLK high to SCLK low	—	50	—	—	ns	D
t_{SSN}	CS_B not asserted period	f_{BUS} = 4 MHz	6	—	—	f_{BUS} period	D
$t_{LEAD\text{-}WU}$	Wake-up by CS_B low to SCLK start	—	1	—	—	ms	D
t_{SPI_EN}	SPI enable by CS_B low after V_{DD} > V_{PORR}	—	200	—	—	μs	D

9.6 Temperature measurement characteristics

Table 56. Temperature measurement

V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.
Transfer function: T °C = ($\Delta T_{MAX–MIN}$ °C / LSB × T_{CODE}) – 55 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
$\Delta T_{MAX\text{-}MIN}$	Sensitivity	—	0.93	1	1.08	°C / LSB	C
T_{ERROR}	Error	—	—	0	—	LSB	C
T_{UNDER}	Underflow	—	—	1	—	LSB	C
T_{OVER}	Overflow	—	—	255	—	LSB	C
T_{MIN}	Temperature measurement	T_A = –50 °C	0	5	10	LSB	C
$T_{RATE\text{-}MIN}$	Temperature measurement	T_A = –40 °C	11	15	19	LSB	C
T_{CODE}	Temperature measurement	T_A = –20 °C	32	35	38	LSB	A
T_{CODE}	Temperature measurement	T_A = 0 °C	52	55	58	LSB	C
T_{CODE}	Temperature measurement	T_A = 25 °C	77	80	83	LSB	A
T_{CODE}	Temperature measurement	T_A = 70 °C	122	125	128	LSB	C
T_{CODE}	Temperature measurement	T_A = 85 °C	137	140	143	LSB	A
T_{CODE}	Temperature measurement	T_A = 105 °C	156	160	164	LSB	C
$T_{RATE\text{-}MAX}$	Temperature measurement	T_A = 125 °C	175	180	185	LSB	B
T_{MAX}	Temperature measurement	T_A = 150 °C [1]	195	205	215	LSB	C
T_{DRIFT}	Temperature measurement drift	—	–2	—	+2	LSB	C

[1] Temperature excursions, time at T_{MAX} must not exceed 12 events of 15 minutes duration during the product lifetime.

9.7 Voltage measurement characteristics

Table 57. Voltage measurement characteristics

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.
Transfer function: V = ($\Delta V_{MAX–MIN}$ V / LSB × V_{CODE}) + 1.22 V
Interpolated limits between –40 °C to 0 °C and between 50 °C to 125 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
$\Delta V_{MAX\text{-}MIN}$	Sensitivity	—	9	10	12	mV / LSB	C
V_{ERROR}	Error	—	—	0	—	LSB	C
V_{UNDER}	Underflow	—	—	1	—	LSB	C
V_{OVER}	Overflow	—	—	255	—	LSB	C
V_{CODE}	V_{DD} voltage, 2.8 V	0 °C ≤ T_A ≤ 50 °C, V_{DD} = 2.8 V	153	158	163	LSB	C
V_{CODE}	V_{DD} voltage, 3.0 V	0 °C ≤ T_A ≤ 50 °C, V_{DD} = 3.0 V	173	178	183	LSB	C
V_{CODE}	V_{DD} voltage, 3.3 V	0 °C ≤ T_A ≤ 50 °C, V_{DD} = 3.3 V	203	208	213	LSB	C
V_{MIN}	V_{DD} voltage, 1.8 V	—	38	58	78	LSB	C
V_{CODE}	V_{DD} voltage, 2.1 V	—	68	88	108	LSB	B
V_{CODE}	V_{DD} voltage, 2.3 V	–40 °C ≤ T_A ≤ 0 °C or 50 °C ≤ T_A ≤ 125 °C, V_{DD} = 2.3 V	98	108	118	LSB	C
V_{CODE}	V_{DD} voltage, 2.8 V	–40 °C ≤ T_A ≤ 0 °C or 50 °C ≤ T_A ≤ 125 °C, V_{DD} = 2.8 V	148	158	168	LSB	C

Table 57. Voltage measurement characteristics*...continued*

V_{DDS} Min ≤ V_{DD} ≤ V_{DDS} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.
Transfer function: V = (Δ $V_{MAX–MIN}$ V / LSB × V_{CODE}) + 1.22 V
Interpolated limits between –40 °C to 0 °C and between 50 °C to 125 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V_{CODE}	V_{DD} voltage, 3.0 V	–40 °C ≤ T_A ≤ 0 °C or 50 °C ≤ T_A ≤ 125 °C, V_{DD} = 3.0 V	168	178	188	LSB	B
V_{CODE}	V_{DD} voltage, 3.3 V	–40 °C ≤ T_A ≤ 0 °C or 50 °C ≤ T_A ≤ 125 °C, V_{DD} = 3.3 V	198	208	218	LSB	C
V_{MAX}	V_{DD} voltage, 3.6 V	—	228	238	248	LSB	C
V_{DRIFT}	Voltage drift	—	–2	—	+2	LSB	C

9.8 Pressure measurement characteristics

Unless otherwise noted, stated tolerances are valid only with internal sequence timing as described in Section 6.7.4 "Summary of execution times".

9.8.1 Pressure measurement characteristic (40 kPa to 250 kPa) range

Table 58. Pressure measurement characteristics (40 kPa to 250 kPa) range, standard tolerances

V_{DDM} Min ≤ V_{DD} ≤ V_{DDM} Max, T_{AS} Min ≤ T_A ≤ T_{AS} Max, unless otherwise specified.
Transfer function: P kPa = ($\Delta P_{MAX–MIN}$ kPa / LSB × P_{CODE}) + 39.6 kPa

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
$\Delta P_{MAX\text{-}MIN}$	Sensitivity	–20 °C ≤ TA ≤ 85 °C	0.20	0.206	0.21	kPa / LSB	C
P_{ERROR}	Error	—	—	0	—	LSB	C
P_{UNDER}	Underflow	FW error status bit 0 = 1	—	1	—	LSB	C
P_{OVER}	Overflow	FW error status bit 0 = 1	—	1023	—	LSB	C
P_{MIN}	Proof pressure, 40 kPa	–40 °C to 125 °C	—	2	17	LSB	C
P_{CODE}	Proof pressure, 75 kPa	–40 °C to 125 °C	162	172	187	LSB	C
P_{CODE}	Proof pressure, 110 kPa	–40 °C to 125 °C	332	342	357	LSB	C
P_{CODE}	Proof pressure, 145 kPa	–40 °C or 125 °C	502	512	527	LSB	C
P_{CODE}	Proof pressure, 180 kPa	–40 °C to 125 °C	672	682	697	LSB	C
P_{CODE}	Proof pressure, 215 kPa	–40 °C to 125 °C	842	852	867	LSB	C
P_{MAX}	Proof pressure, 250 kPa	–40 °C to 125 °C	1012	1022	—	LSB	C

10 Mechanical specifications

10.1 Maximum ratings (mechanical)

Maximum ratings are the extreme limits the device can be exposed without permanent damage. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than the values shown in Table 59. Keep V_{IN} and V_{OUT} within the range V_{SS} ≤ (V_{IN} or V_{OUT}) ≤ V_{DD}.

Table 59. Maximum ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
$P_{burst1k}$	Pressure transducer, minimum burst pressure	≤ 1000 kPa rating	2000	—	—	kPa	D
f_{P0}	Pressure transducer, minimum natural resonance frequency	—	—	5	—	MHz	D
Q_P	Pressure transducer damping ratio	—	—	1	—	—	D
PA_N	Pressure transducer, sensitivity to vertical acceleration	–500 g ≤ A ≤ +500 g	—	0	—	Pa / g	C
PA_{neg}	Pressure transducer, sensitivity to vertical acceleration	A < –500 g	2	4.5	6.5	Pa / g	C
m	Package Mass	—	—	0.2	—	gram	D

10.2 Media compatibility

Media compatibility is based on the media and test methods described in NXP specification NXPOMS-1719007347-3772.[1] Consult your sales representative for more details and specific requirements.

11 Mounting recommendations

The package should be mounted with the pressure port pointing away from sources of debris which might otherwise plug the sensor.

A plugged port exhibits no change in pressure and can be cross-checked in the user software.

Refer to application note AN1902[2] for proper printed circuit board attributes and recommendations.

12 Package outline

Consult the most recently issued drawings before initiating or completing a design. The drawings are available for download at https://www.nxp.com/packages/SOT1931-1(D).

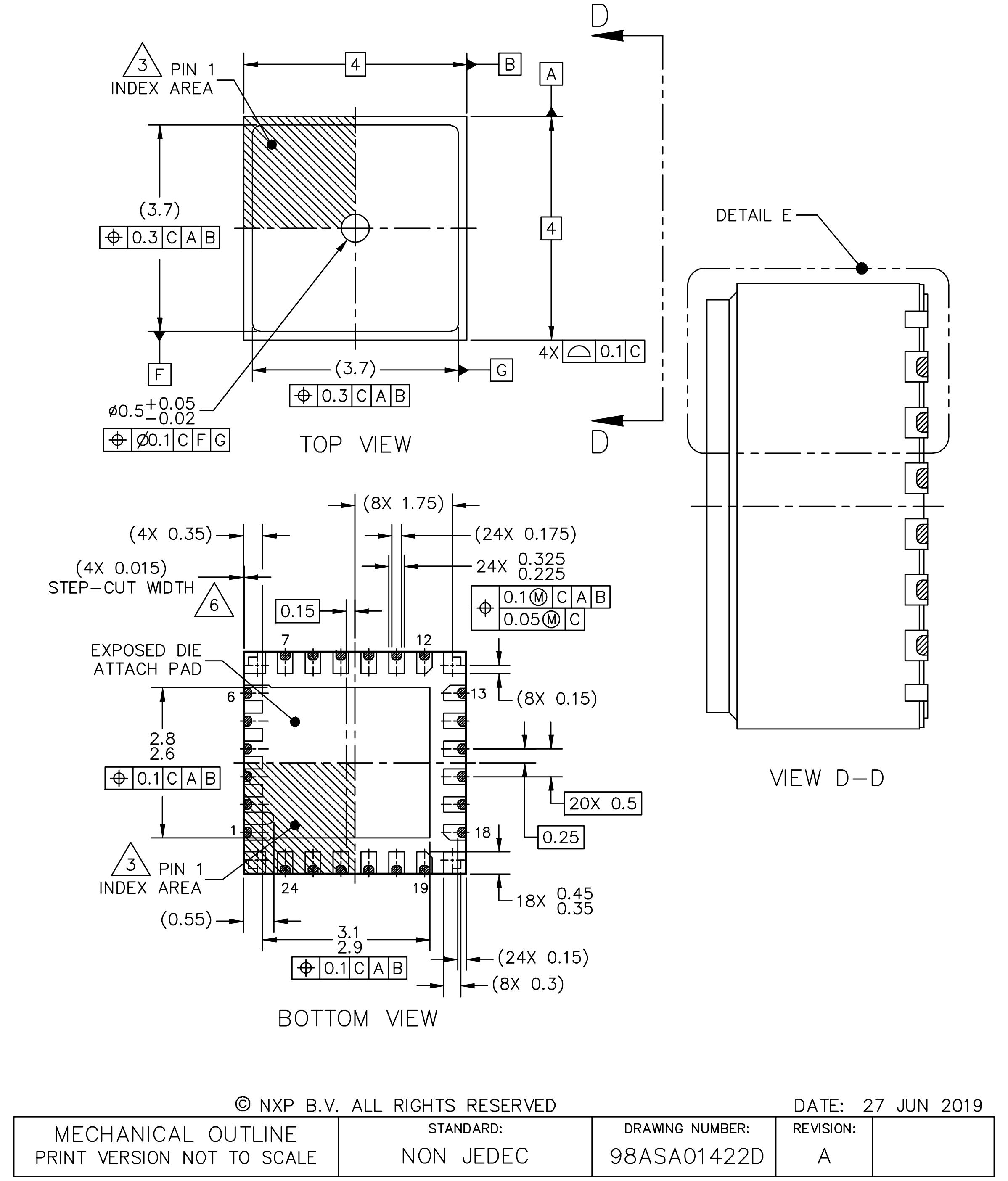
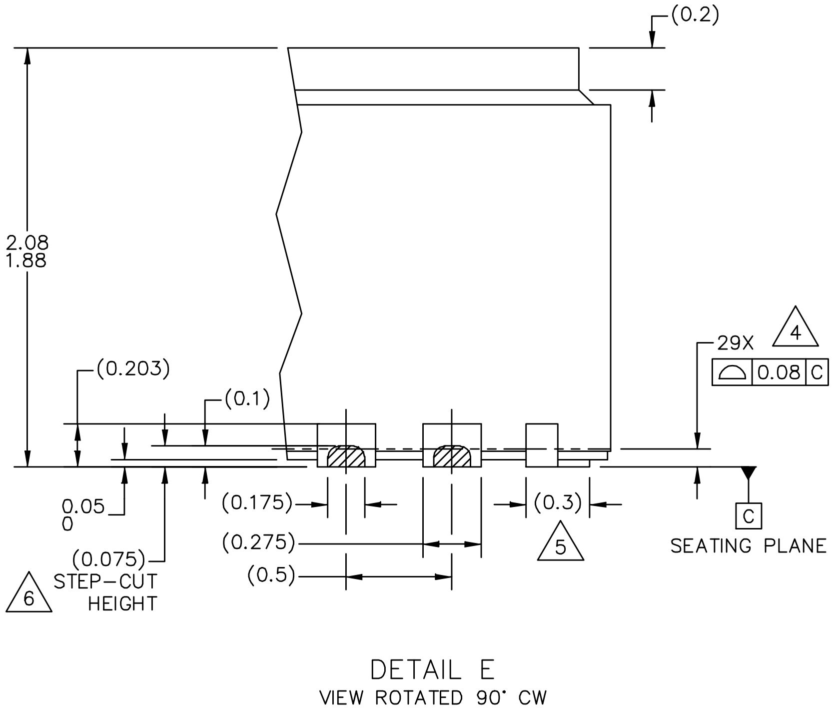


Figure 25. Package outline HQFN24 (SOT1931-1(D))



DATE: 27 JUN 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01422D	REVISION: A	

Figure 26. Package outline detail HQFN24 (SOT1931-1(D))

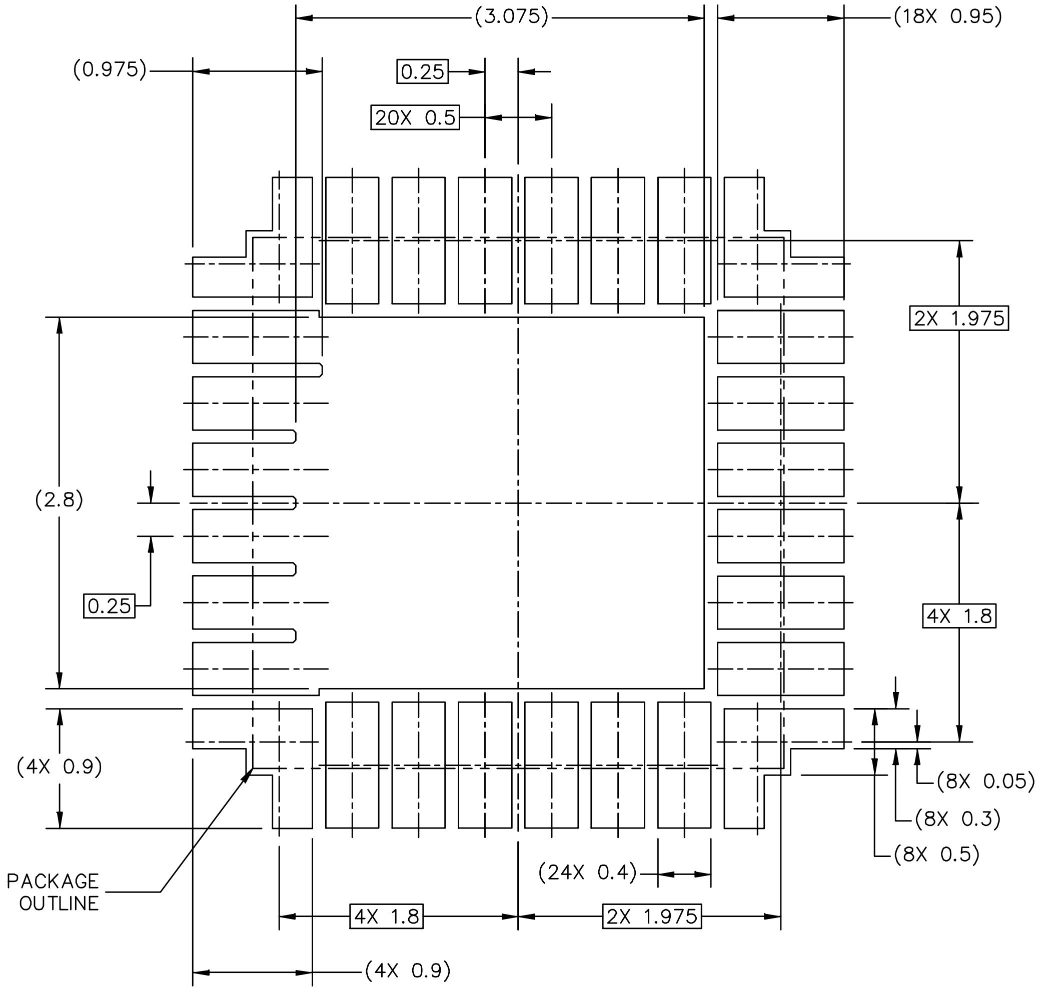


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Figure 27. Reflow soldering footprint part1 for HQFN24 (SOT1931-1(D))

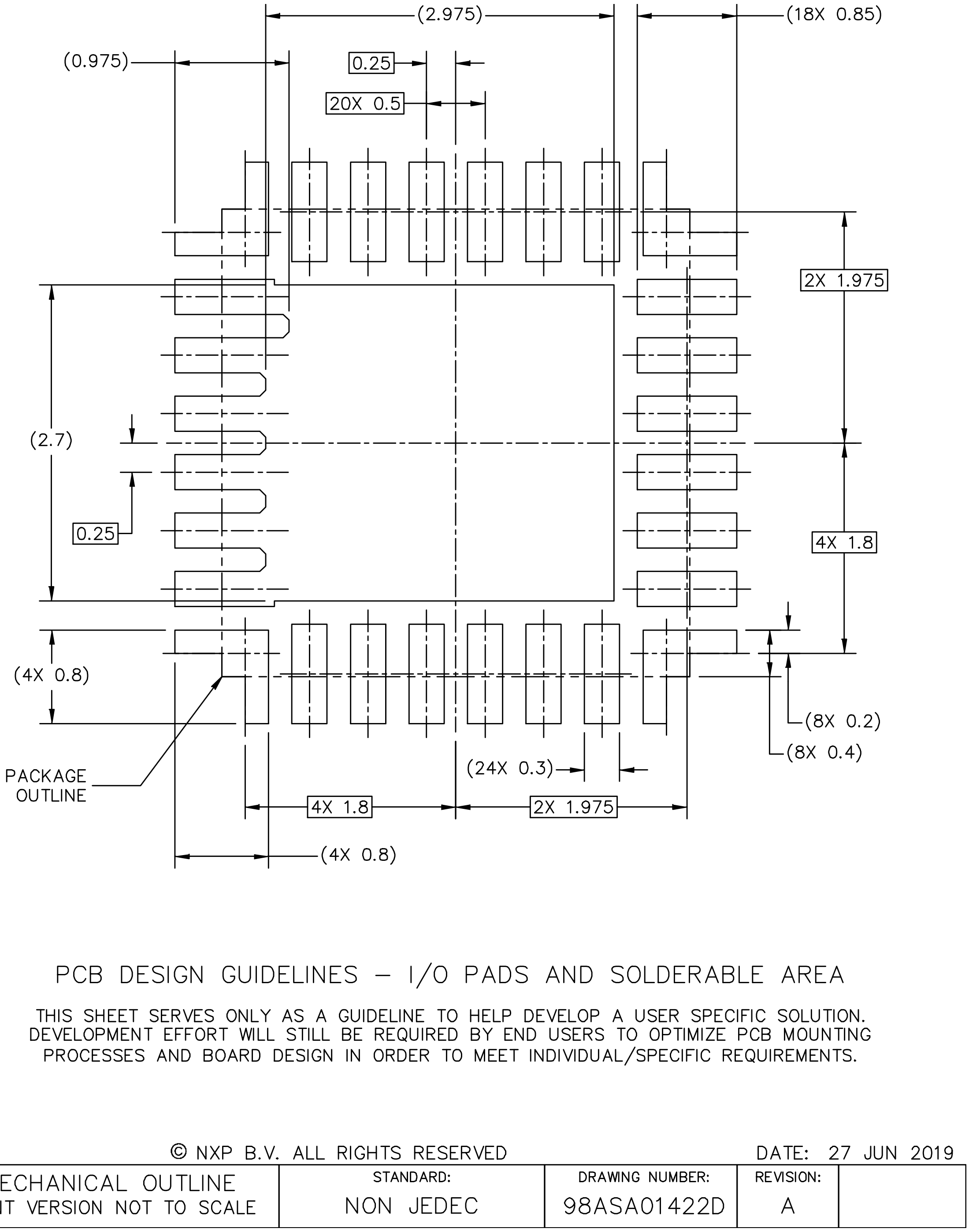

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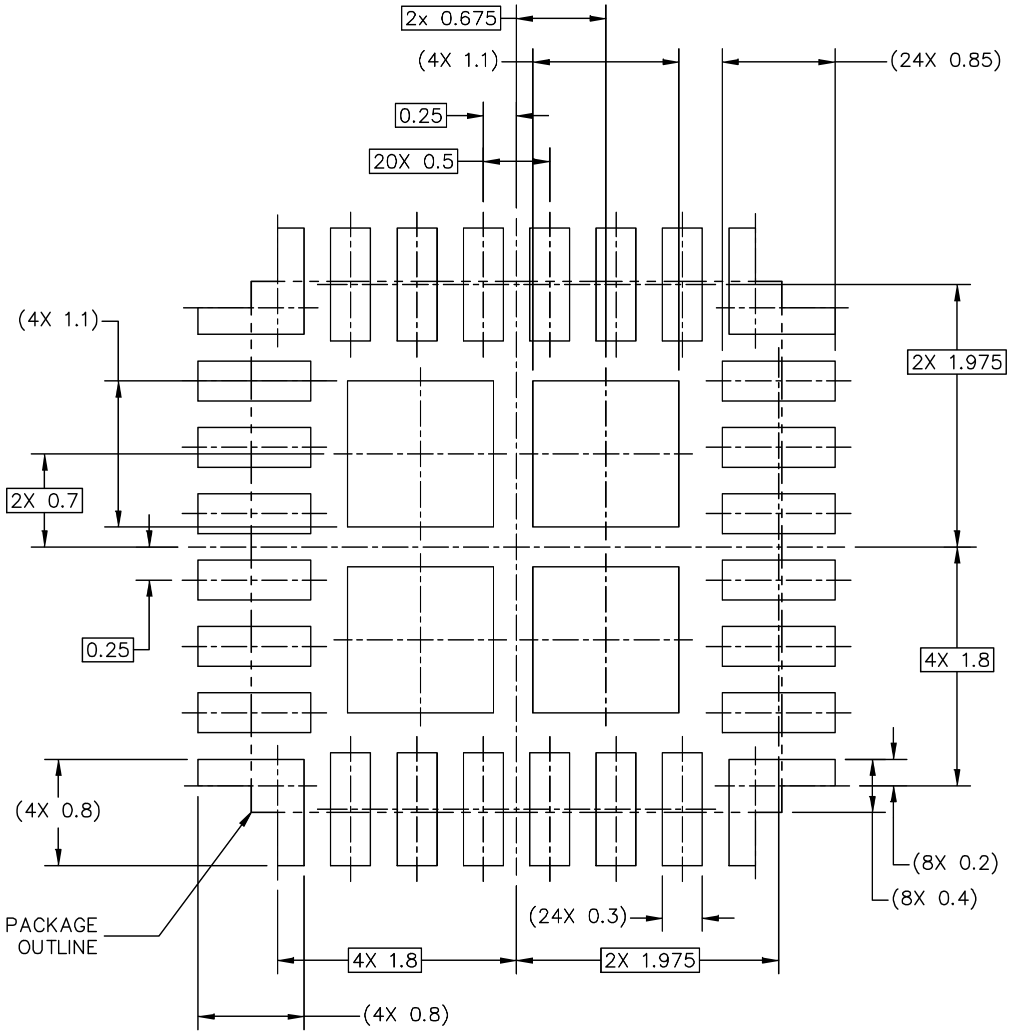
Figure 28. Reflow soldering footprint part2 for HQFN24 (SOT1931-1(D))



RECOMMENDED STENCIL THICKNESS 0.125

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Figure 29. Reflow soldering footprint part3 for HQFN24 (SOT1931-1(D))

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON−FUNCTIONAL PADS.
5. ANCHORING PADS.
6. STEP−CUT IS APPLIED FOR BURR REMOVAL ONLY.

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Figure 30. Package outline notes HQFN24 (SOT1931-1(D))

13 References

NXP reference documents

[1] NXP Specification NXPOMS-1719007347-3772, *Media Test for Automotive Pressure Sensors*

[2] AN1902, *Assembly guidelines for QFN (quad flat no-lead) and SON (small outline no-lead) packages*

14 Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NPB8 v.2.4	20220311	Product data sheet	—	NBP8 v.2.3
Modifications	• Section 6.5.3, revised the content for "Prel_T". • Section 6.6.2, revised the content and added new Figure 18. • Section 6.8, Table 22, revised "CMD_ACKF" to "CMD_ACKINTF" in the Bit 7 description. • Section 6.8, Table 24, revised "CMD_ACKF" to "CMD_ACKINTF" in all descriptions.			
NBP8 v.2.3	20210927	Product data sheet	—	NBP8 v.2.2
NBP8 v.2.2	20210727	Product data sheet	—	NBP8 v.2.1
NBP8 v.2.1	20210604	Product data sheet	—	NBP8 v.2
NBP8 v.2	20210507	Product data sheet	—	NBP8 v.1.2
NBP8 v.1.2	20200819	Objective data sheet	—	NBP8xD v.1.1
NBP8 v.1.1	20200420	Objective data sheet	—	NBP8xD v.1
NBP8xD v.1	20200319	Objective data sheet	—	—

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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