NXP Semiconductors
Reference Manual

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Layerscape FRWY-LS1046A Board Reference Manual

Supports FRWY-LS1046A Board Revision B

Contents

Chapter 1
FRWY-LS1046A Overview

The Layerscape® LS1046A Freeway (FRWY-LS1046A) board is a high-performance development platform that supports the QorIQ® LS1046A architecture processor capable of supporting more than 32000 CoreMark® performance. The FRWY-LS1046A board supports the QorIQ LS1046A processor, onboard DDR4 memories, multiple Gigabit Ethernet ports, USB 3.0 ports, M.2 Key-E slots for Wi-Fi, and expansion board options via a mikroBUS™ socket.

The FRWY-LS1046A comes pre-loaded with a board support package (BSP) based on a standard Linux kernel. The board is lead-free and RoHS-compliant.

Following are orderable part numbers for the board:

- FRWY-LS1046A-PA
- FRWY-LS1046A-AC

This document provides detailed information about FRWY-LS1046A board interfaces, power supplies, clocks, DIP switch, and LEDs.

1.1 Acronyms and abbreviations

The table below lists and explains the acronyms and abbreviations used in this document.

Table 1. Acronyms and abbreviations

Term	Description
CD	Card detect
CTS	Clear to send
DDR	Double data rate
DIP	Dual inline package
DQS	Data strobe
DUT	Device under test
ECC	Error correcting code
EMI	Ethernet management interface
eSDHC	Enhanced secure digital host controller
GIC	Generic interrupt controller
GPIO	General purpose input/output
I2C	Inter-integrated circuit
IFC	Integrated flash controller
JTAG	Joint Test Action Group (IEEE® Standard 1149.1™)
MAC	Media access control
MT/s	MegaTransfers/second
NFC	Near field communication

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Table 1. Acronyms and abbreviations (continued)

Term	Description
PBL	Pre-boot loader
PLL	Phase-locked loop
PMIC	Power management integrated circuit
POR	Power-on reset
PWM	Pulse width modulation
QSGMII	Quad serial gigabit media independent interface
QSPI	Quad serial peripheral interface
RCW	Reset configuration word
RTC	Real-time clock
RTS	Request to send
SDHC	Secure digital host controller
SDRAM	Synchronous dynamic random-access memory
SerDes	Serializer/deserializer
SPD	Serial presence detect
SPI	Serial peripheral interface
TSN	Time-sensitive networking
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
WP	Write protect

1.2 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on the FRWY-LS1046A. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document	Description	Link / how to access
Layerscape FRWY-LS1046A Board Getting Started Guide	Describes the FRWY-LS1046A board settings and explains steps to set up and boot the board	FRWY-LS1046AGSG.pdf
Layerscape FRWY-LS1046A Board Errata	Describes known errata and workarounds for the FRWY-LS1046A board	Contact FAE / sales representative
QorIQ LS1046A Product Brief	Provides a brief overview of the LS1046A processor	LS1046APB.pdf

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Table 2. Related documentation (continued)

Document	Description	Link / how to access
QorIQ LS1046A Data Sheet	Provides information about LS1046A electrical characteristics, hardware design considerations, and ordering information	LS1046A.pdf
QorIQ LS1046A Reference Manual	Provides a detailed description about the QorIQ LS1046A multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information	LS1046ARM.pdf
QorIQ LS1046A Chip Errata	Lists the details of all known silicon errata for the LS1046A	Contact FAE / sales representative
QorIQ LS1046A Design Checklist (AN5252)	This document provides recommendations for new designs based on the LS1046A. This document can also be used to debug newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.	AN5252.pdf
Layerscape FRWY-LS1046A BSP User Guide	This document describes how to work with FRWY-LS1046A board support package (BSP) to be used with FRWY-LS1046A board.	FRWY-LS1046ABSPUG.pdf
CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA, Targeting Manual	This manual explains how to use the CodeWarrior Development Studio for QorIQ LS series - ARM V8 ISA product.	CWARMv8TM.pdf
CodeWarrior TAP Probe User Guide	Provides details of CodeWarrior® TAP, which enables target system debugging through a standard debug port (usually JTAG) while connected to a developer workstation through Ethernet or USB	CWTAPUG.pdf

1.3 Block diagram

The figure below shows the FRWY-LS1046A block diagram.

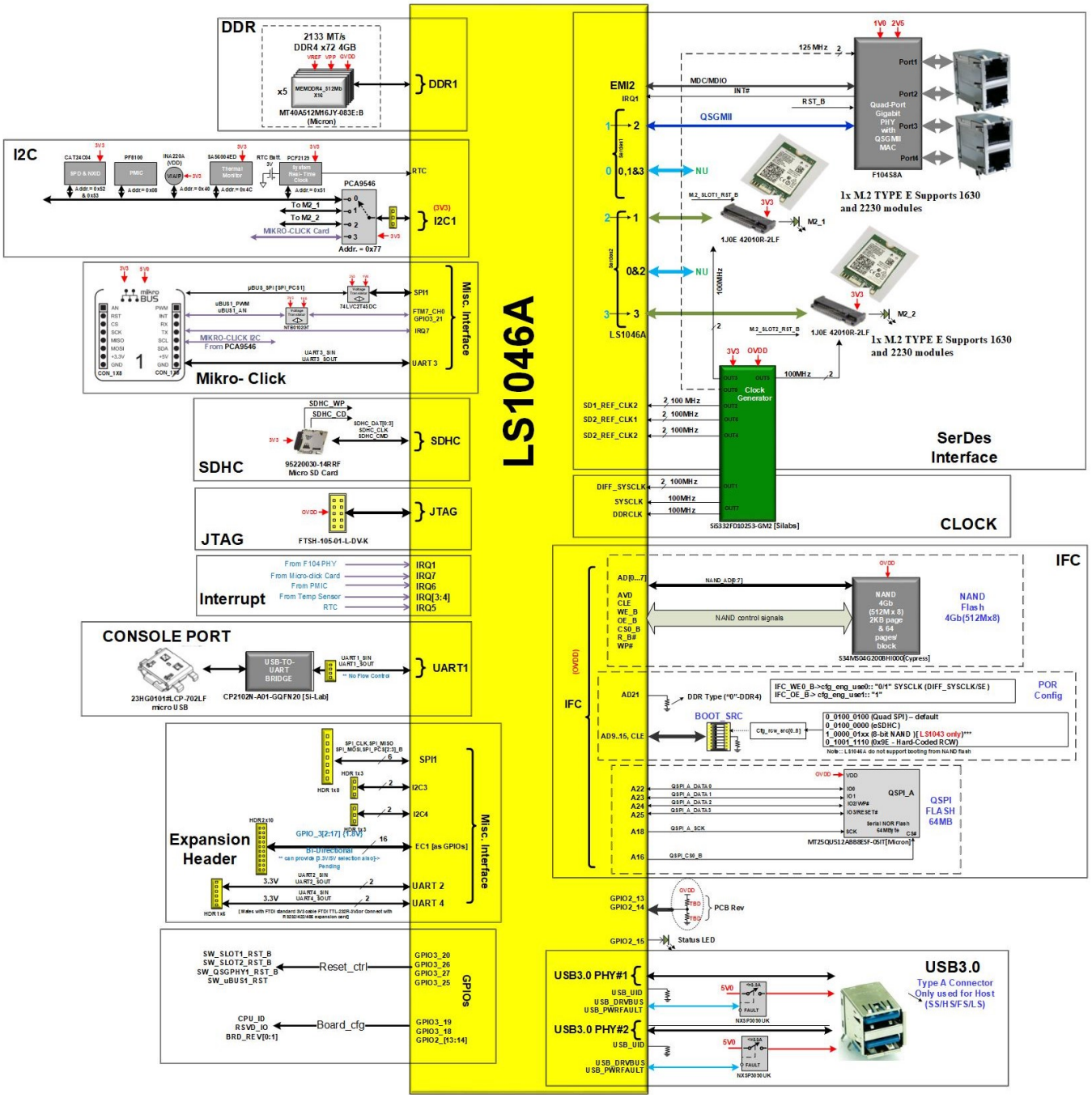

Figure 1. FRWY-LS1046A block diagram

1.4 Board features

The table below describes the features of the FRWY-LS1046A.

Table 3. FRWY-LS1046A features

Board feature	Processor feature used	Description
Processor		QorIQ LS1046A processor **NOTE** For details on the LS1046A processor, see *QorIQ LS1046A Reference Manual*.
DDR	One 32-/64-bit DDR4 SDRAM memory controller with ECC	• Supports data rates of up to 2133 MT/s • Supports 64-bit data bus • Supports five onboard 512 Mbit x16 discrete memory modules (eight data byte lanes + ECC) • Supports double-bit error detection and single-bit error correction ECC (8-bit check word across 64-bit data) • Supports single chip select
SerDes	Two SerDes modules (SerDes1 and SerDes2), each having four lanes with speeds of up to 10 Gbit/s	SerDes1: • Lane 2: Supports a QSGMII PHY, provides four 1.25 GbE ports SerDes2: • Lane 1: Supports a PCIe x1 (Gen 1/2/3) M.2 Key-E slot for 1630/2230 Wi-Fi module • Lane 3: Supports a PCIe x1 (Gen 1/2/3) M.2 Key-E slot for 1630/2230 Wi-Fi module
Ethernet	QSGMII interface	• Supports four 1G/100M/10BaseT Ethernet ports through two 1x2 RJ45 connectors with link and activity status
USB 3.0	Two USB 3.0 controllers (USB1 and USB2) with integrated PHYs	• Supports super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations • Two USB 3.0 ports are configured as host with a 1x2 USB Type A connector
IFC 2.0	Integrated flash controller (NOR, NAND)	• 64 MB onboard QSPI NOR flash memory (1.8 V) - as boot source • 4 Gbit (512 Mbit x 8) SLC NAND flash memory (1.8 V) with ECC support
SDHC	One enhanced secure digital host controller (eSDHC)	• Supports a micro-SDHC connector for connecting an external micro-SD 3.0 card • Operates at 3.3 V

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Table 3. FRWY-LS1046A features (continued)

Board feature	Processor feature used	Description
UART	Two DUART modules (DUART1 and DUART2), each containing two UARTs	DUART1: • UART1 is routed to USB-UART bridge and supports USB port to access the serial port as console, requires a jumper to be placed on a header • UART1 can be used without flow control on an expansion header, requires the jumper to be removed from the header • UART3 can be used to interface with a click board plugged-in into mikroBUS socket DUART2: • UART2 can be used with/without flow control on an expansion header • UART4 can be used on the same expansion header
SPI	One serial peripheral interface (SPI)	• Connects to a click board plugged-in into mikroBUS socket using PCS0 (3.3 V) • Supports SPI expansion header using PCS[1:3] (3.3 V)
I2C	Three I2C controllers (I2C1, I2C3, and I2C4)	• I2C1: Controls all system devices and can be accessed remotely through an I2C expansion header (I2C1) • I2C3: Can be accessed remotely through an I2C expansion header (I2C3) • I2C4: Can be accessed remotely through an I2C expansion header (I2C4)

Table continues on the next page...

Table 3. FRWY-LS1046A features (continued)

Board feature	Processor feature used	Description
Power supply		• 12 V input power from DC input adapter • 1/0.9 V for core VDD, USB_SVDD, USB_SDVDD, and SVDD • 1.2 V for DDR4 G1VDD • 0.6 V for DDR4 VTT/VREF • 2.5 V for DDR4 VPP • 3.3 V for DVDD • 3.3 V for EVDD • 3.3 V for USB_HVDD • 1.8 V for OVDD and LVDD • 1.35 V for XVDD • 2.5 V for TVDD • 1.8 V / GND for TA_PROG_SFP (GPIO-controlled) • 1/0.9 V for TA_BB_VDD • 2.5 V for QSGMII PHY VDD25, VDD25A • 2.1 V for QSGMII PHY core • 3.3 V for M.2 Key-E slots • 5 V for USB port • 5 V and 3.3 V for mikroBUS socket
Clock		SYSCLK: • Supports single-ended SYSCLK and DDRCLK clock input = 100 MHz (fixed) • Supports single-source differential DIFF_SYCLK = 100 MHz (fixed) SerDes: • Provides clocks to all SerDes blocks and slots • 100 MHz for SD1_REF_CLK2 • 100 MHz for SD2_REF_CLK1 and SD2_REF_CLK2 • 100 MHz for M.2 Key-E slots M2_1_REFCLK and M2_2_REFCLK RTC: • Supports 32.768 kHz for LS1046A RTC Ethernet: • Supports differential 125 MHz for F104S8A QSGMII PHY

Table continues on the next page...

Table 3. FRWY-LS1046A features (continued)

Board feature	Processor feature used	Description
Debug		• Supports Arm Cortex 10-pin JTAG connector • Supports micro-USB port to access serial port as console for debug
GPIO		• Supports a 2x10 GPIO header (1.8 V) • Supports bi-directional (configurable) inputs/outputs

1.5 Board top/bottom views

The figure below shows the top-side view of the FRWY-LS1046A.

Figure 2. FRWY-LS1046A top view

The figure below shows the bottom-side view of the FRWY-LS1046A.

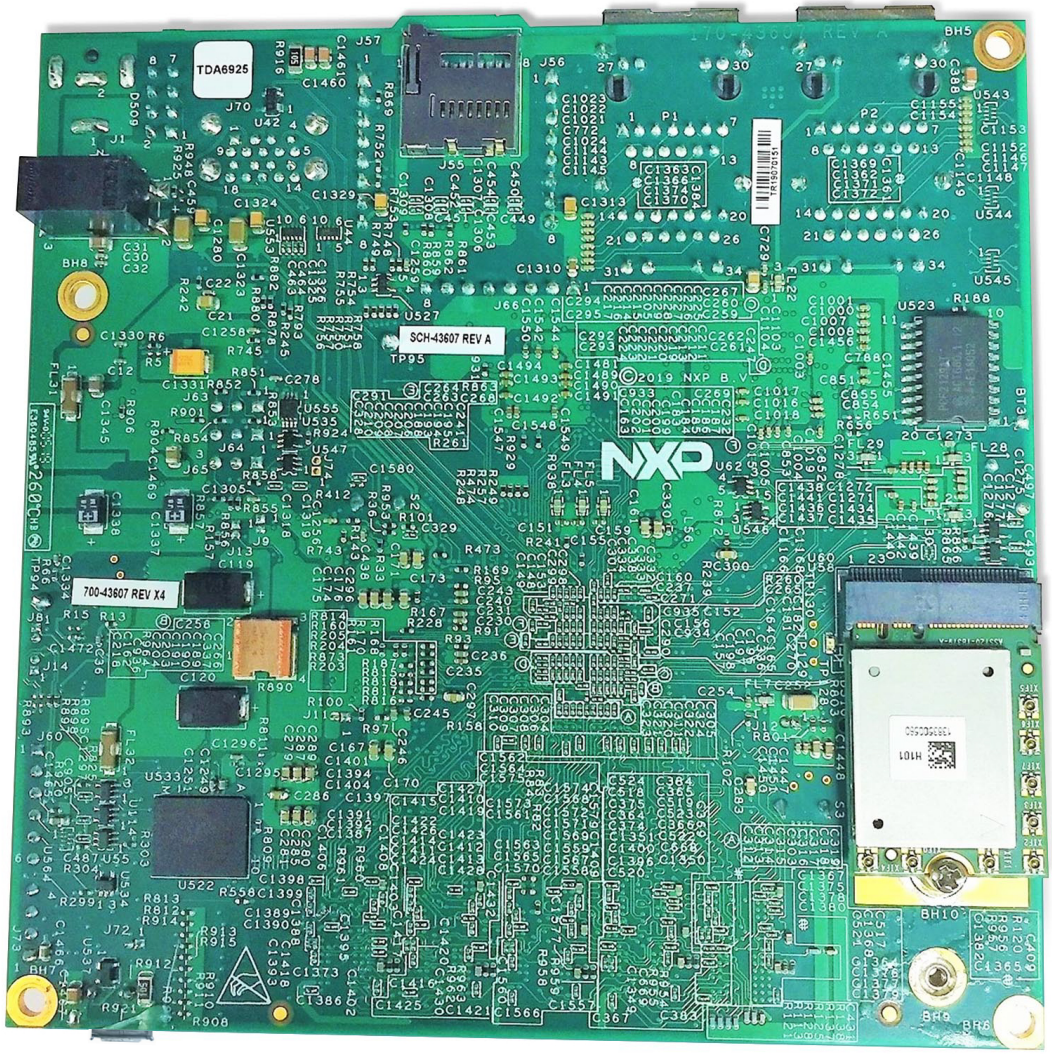

Figure 3. FRWY-LS1046A bottom view

Chapter 2
FRWY-LS1046A Functional Description

This chapter describes the features and functions of the FRWY-LS1046A. For details of the LS1046A processor features, see *QorIQ LS1046A Reference Manual*.

The chapter is divided into the following sections:

2.1 Power supplies

The FRWY-LS1046A gets 12 V input power from an external DC power supply. The power supply devices on the board use the 12 V power to generate required power supplies for the LS1046A processor, DDR4 SDRAMs, PHY, and numerous other peripherals. The figure below shows the FRWY-LS1046A power supply block diagram.

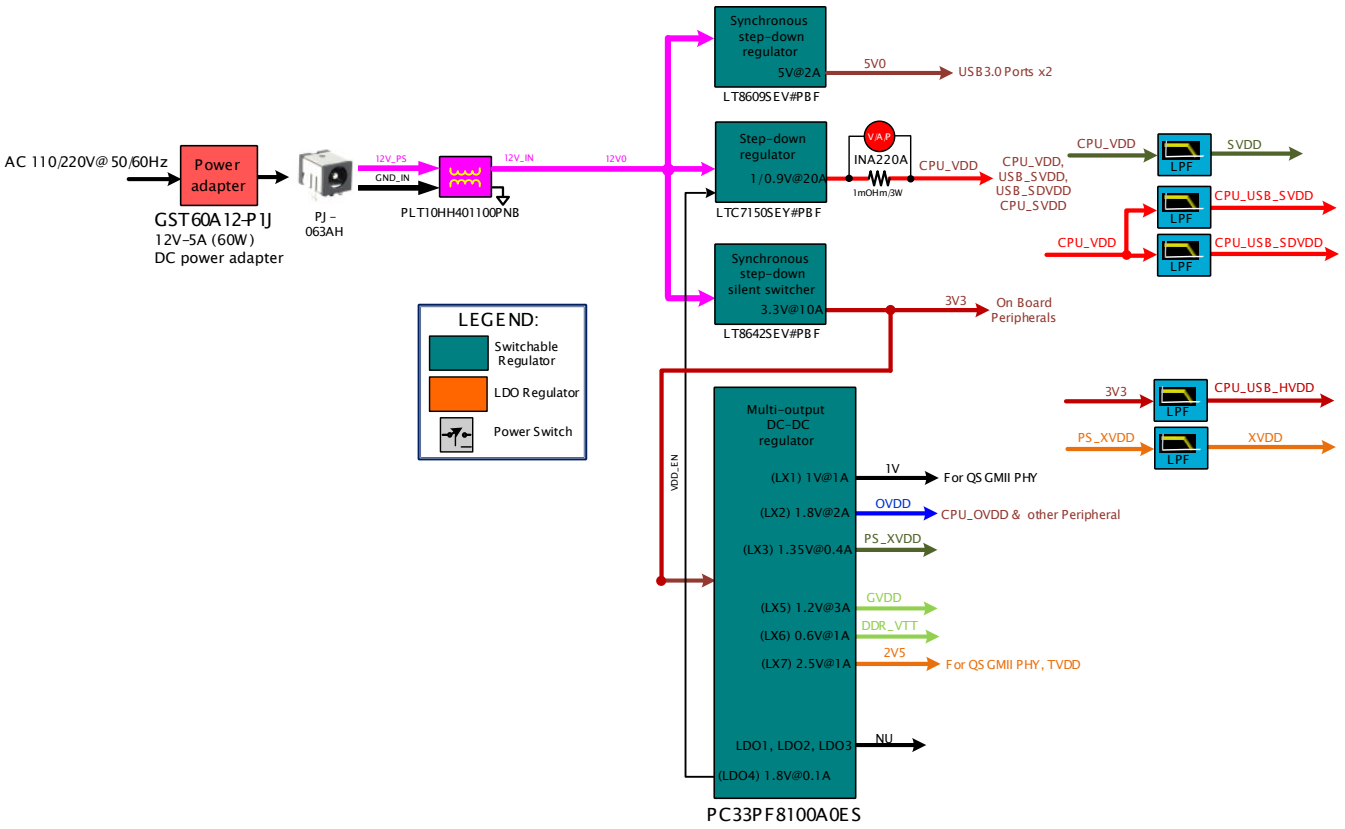

Figure 4. Power supply block diagram

Note that several power supplies have onboard low-pass filters to prevent board switching noise from coupling into sensitive analog supplies. The figure below shows the filters used.

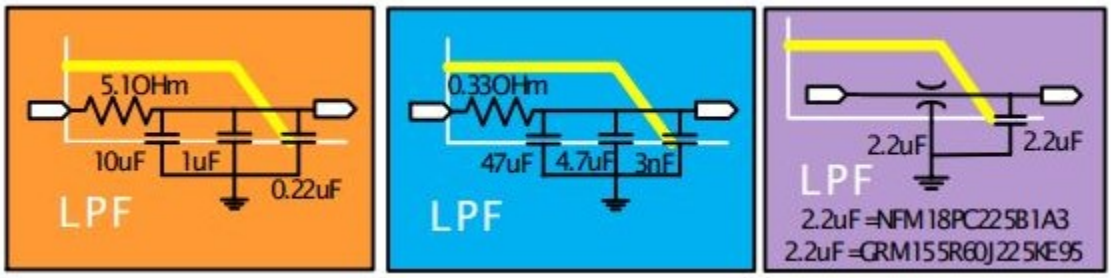

Figure 5. Low-pass filters

2.1.1 Primary power supply

The FRWY-LS1046A is powered up using an external 12 V DC power adapter. The table below describes the 12 V power adapter.

Table 4. 12 V power adpater

Part number	Input power specifications	Output power specifications
GST60A12-P1J (MEAN WELL)	• Input: 110 - 230 VAC, 50 - 60 Hz • 3-pole AC inlet (IEC 320 C14)	• Output: 12 V, 0 - 5 A DC power supply adapter (160 W) - standard • DC jack (2-pin, 2.1 mm x 5.5 mm x 11 mm)

The table below shows the details of the power jack on the board to connect external 12 V power adapter.

Table 5. Power jack

Part identifier	Part number	Description
J1	PJ-063AH	Plug/mating plug specifications: • Inside diameter: 2.1 mm • Outside diameter: 5.5 mm • Rating: 8 A

2.1.2 Secondary power supplies

The table below describes the FRWY-LS1046A power supply devices that generate secondary power supplies for the board.

Table 6. FRWY-LS1046A power supply devices

Reference designator	Device	Power supply voltage	Description
	(From 12 V power adapter)	12V0 (12 V at 5 A)	Supply for LTC7150S, LT8609SEV, and LT8642SEV power supply devices
U557	LTC7150S (Linear Technology)	CPU_VDD (1/0.9 V ±3% at 20 A)	• Supply for processor cores and platform (VDD) • Filtered VDD also powers USB (USB_SDVDD and USB_SVDD) and SerDes (SVDD) power supplies of the LS1046A processor • Jumper-enabled VDD also powers TA_BB_VDD and FA_VL supplies of the LS1046A processor • VDD is 1 V or 0.9 V depending on the jumper setting on header J8
U1	LT8609SEV (Linear Technology)	5V0 (5 V at 2 A)	• Supply for dual-port USB 3.0 connector • Supply for mikroBUS socket connector J57

Table continues on the next page...

Table 6. FRWY-LS1046A power supply devices (continued)

Reference designator	Device	Power supply voltage	Description
U560	LT8642SEV (Linear Technology)	3V3 (3.3 V at 10 A)	• Supply for processor DVDD and EVDD • Filtered 3V3 power for USB (USB_HVDD) power supply of the LS1046A processor • Supply for the following board components: — Si5332FD10253-GM2 clock generator — M.2 Key-E slots — Micro-SDHC connector — RTC — I2C EEPROM — Current monitor (INA220A) — Temperature sensor (SA56004ED) — UART and SPI expansion headers — MikroBUS socket connector J56 — CP2102N UART-USB bridge — Misc. components (buffers and translators) • Supply for PC33PF8100EAES PMIC
U561	PC33PF8100EAES (NXP Semiconductors)[1]	Multi-output DC-DC regulator with six switched outputs, one LDO output (VDD enable), and one reset control output to the LS1046A processor. Six switched outputs are given below:	
		SW1LX: 1V0_F104 (1 V at 1 A)	Supply for the QSGMII PHY VDD and VDDA
		SW2LX: OVDD (1.8 V at 2 A)	• Supply for processor OVDD, LVDD, and TH_VDD • Filtered OVDD powers for processor AVDD_CGA[1:2], AVDD_PLAT, and AVDD_D1 • Supply for GPIO3_24 controlled processor power TA_PROG_SFP (for fuse programming) • Jumper-enabled OVDD also powers PROG_MTR • OVDD for board components: — SLC NAND and QSPI memories — Si5332FD10253-GM2 clock generator VDDO5 — Misc. components (buffers and translators)
		SW3LX: 1V35 (1.35 V at 400 mA)	Filtered 1.35 V is supplied to processor XVDD, AVDD_SD[1:2]_PLL1, and AVDD_SD[1:2]_PLL2

Table continues on the next page...

Table 6. FRWY-LS1046A power supply devices (continued)

Reference designator	Device	Power supply voltage	Description
		SW5LX: GVDD (1.2 V 3 A)	• Supply for DDR controller input/output (GVDD) • Supply for DDR4 SDRAM memory chips
		SW6LX: DDR_VTT (0.6 V at 1 A)	Supply for DDR address and control bus termination (VTT) **NOTE** VTT_Mode is enabled (sink current is up to 700 mA (typical)).
		SW7LX: 2V5 (2.5 V at 1 A)	• Supply for processor TVDD • Supply for QSGMII PHY VDD25, VDD25A, and DDR4 memory VPP

1. The PC33PF8100EAES is a programmable PMIC that generates most of the LS1046A power. Power configurations are stored in its one-time programmable (OTP) memory. The configuration in volatile memory can be changed through the I2C1_CH0 interface. The device is accessible at 0x08 I2C 7-bit address.

2.1.3 Power supply sequence

The FRWY-LS1046A is configured to switch ON automatically when the 12 V power adapter (12 V power supply source) is switched ON and is connected to power jack (J1) on the board. When the 12 V supply is available to power regulators on the board, the power good signals of these regulators enable all board power supplies in correct sequence.

NOTE

The board does not have a power ON/OFF switch. To power ON/OFF the board, plug/unplug the 12 V power adapter to/from the board.

The figure below shows the FRWY-LS1046A power supply sequence.

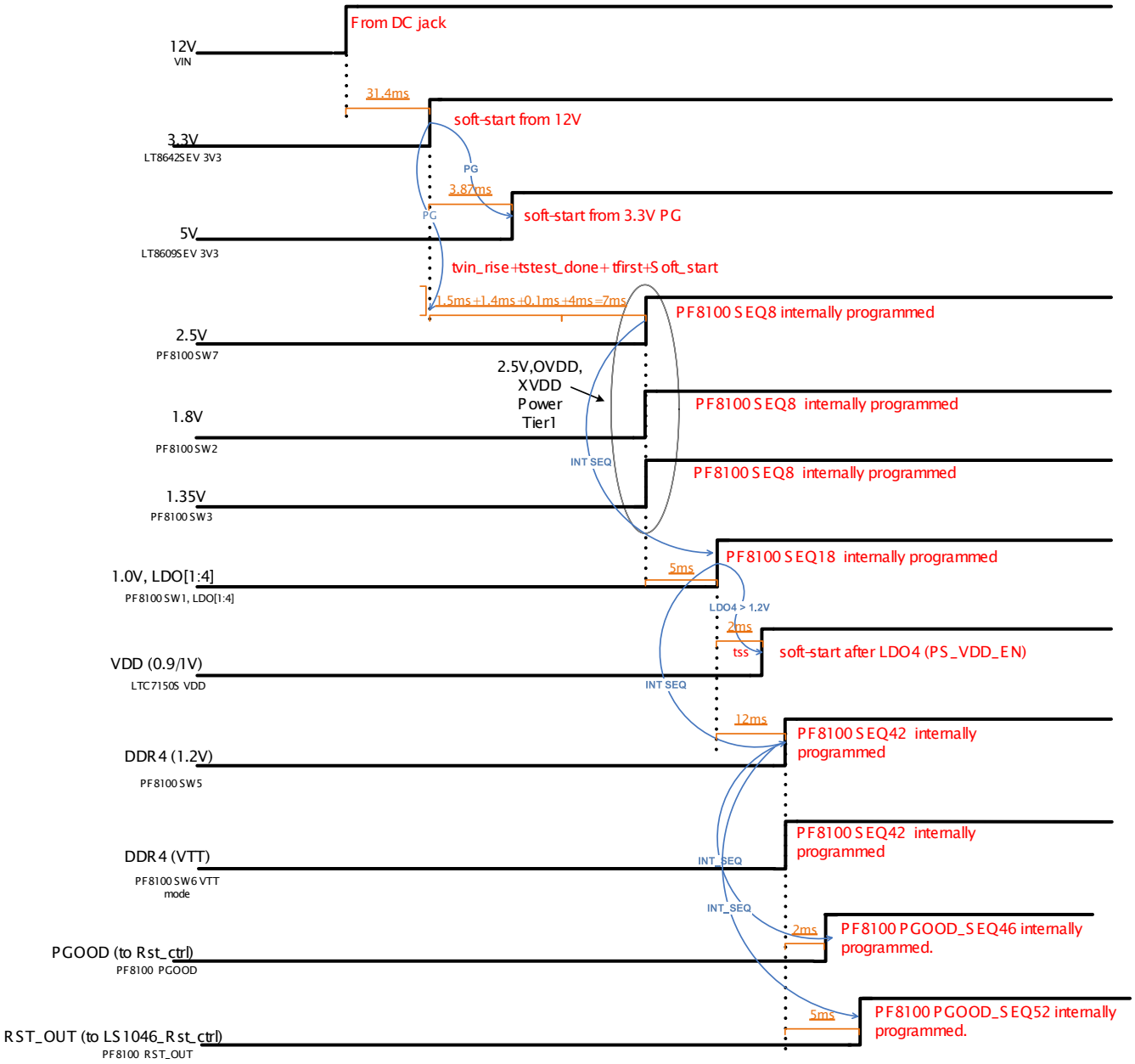

Figure 6. Power supply sequence

NOTE

The FRWY-LS1046A follows the power supply sequencing requirements mentioned in *QorIQ LS1046A Data Sheet*.

2.1.4 VDD current/power measurement

The FRWY-LS1046A facilitates onboard measurement of current and power for its VDD power supply. Current/power measurement facility is not available for other power supplies as they are considered as low-current/incidental supplies. The table below provides details of VDD current/power measurement.

Table 7. VDD current/power measurement

Measurement device	Shunt resistor value	Notes
INA220AIDGST	0.001	The VDD supply powers the LS1046A core (1/0.9 V), USB (USB_SDVDD and USB_SVDD), and SerDes (SVDD) power supplies

2.2 Clocks

The FRWY-LS1046A has a clock generator (Si5332FD10253-GM2), which generates most of the clocks required for the functioning of the LS1046A processor and different board peripherals. The figure below shows the clock diagram of the FRWY-LS1046A.

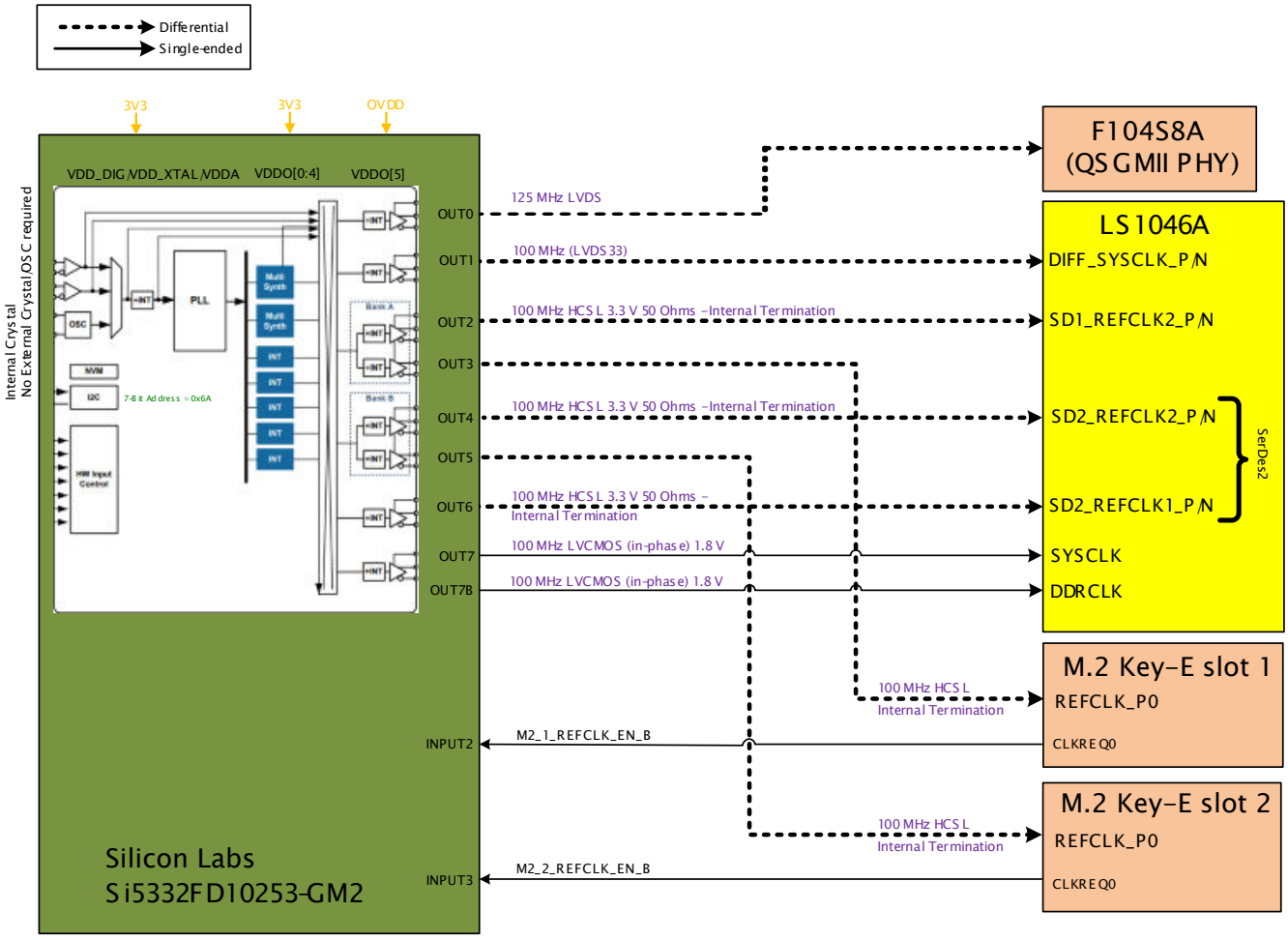

Figure 7. FRWY-LS1046A clock diagram

NOTE

Si5332FD10253-GM2 uses an internal 50 MHz crystal oscillator to generate different frequencies.

The table below provides details of different clocks of the FRWY-LS1046A.

Table 8. FRWY-LS1046A clocks

Clock generator	Clocks	Specifications	Destination
U50: Si5332FD10253-GM2	OUT0: QSGPHY_REFCLK_125M_[P,N]	• Frequency: 125 MHz • Output type: LVDS • Operating voltage: 3.3 V	QSGMII PHY
	OUT1: DIFF_SYSCLK_[P, N]	• Frequency: 100 MHz • Output type: LVDS • Operating voltage: 3.3 V	DIFF_SYSCLK
	OUT2: SD1_REFCLK2_[P, N]	• Frequency: 100 MHz • Output type: HCSL • Operating voltage: 3.3 V	SerDes1 controller (PLL 2)
	OUT3,5[1]: M2_1_REFCLK_[P,N] M2_2_REFCLK_[P,N]	• Frequency: 100 MHz • Output type: HCSL • Operating voltage: 3.3 V	M.2 PCIe x1 slot 1 and slot 2
	OUT4,6: SD2_REFCLK2_[P, N] SD2_REFCLK1_[P, N]	• Frequency: 100 MHz • Output type: HCSL • Operating voltage: 3.3 V	SerDes2 controller (PLL 2 and PLL 1)
	OUT7: SYS_CLK_100MHz_LVCMOS DDR_CLK_100MHz_LVCMOS	• Frequency: 100 MHz • Output type: LVCMOS • Operating voltage: 1.8 V	SYSCLK DDRCLK
U523: PCF2129AT	CLK_32KHZ	• Frequency: 32.768 kHz • Operating voltage: 3.3 V	LS1046A RTC

1. The clock generator also controls the enable/disable for 100 MHz clocks to M.2 PCIe x1 slots. When the clock generator detects a card in any of the M.2 slots, it enables clocks to the slots. Clocks are enabled for both slots even if only one slot is populated with a card.

2.3 DDR interface

The FRWY-LS1046A has five onboard x16 DDR4 SDRAM memory chips with four chips supporting data transfer and one chip supporting ECC. The figure below shows the DDR diagram of the FRWY-LS1046A.

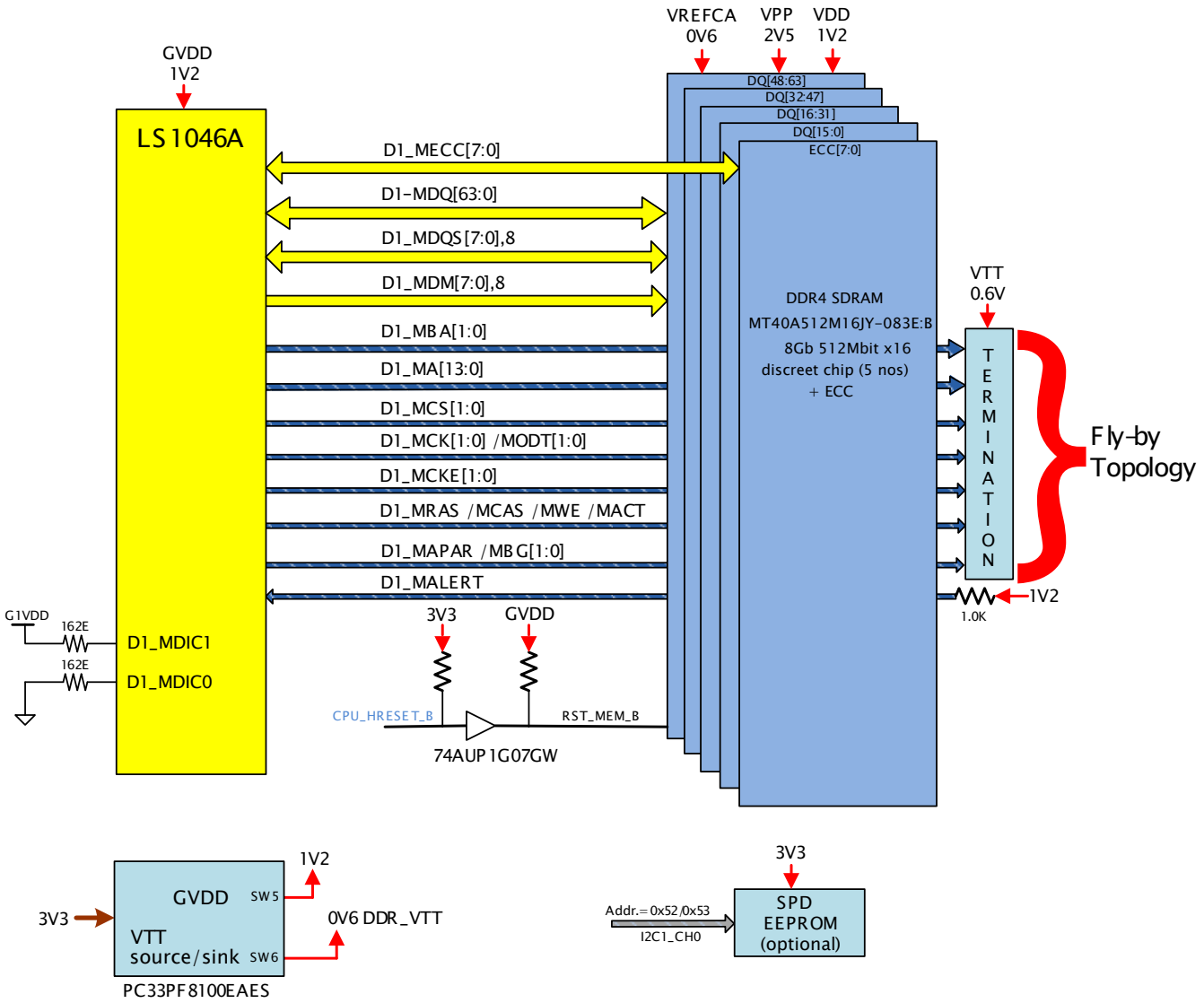

Figure 8. DDR diagram

The part number of the SDRAM memory chips is MT40A512M16JY-083E:B (from Micron Technology). Following are the characteristics of the FRWY-LS1046A DDR interface:

- Supports data rates of up to 2133 MT/s
- Supports 64-bit data bus
- Supports x16 discrete memory modules (eight data byte lanes + ECC)
- Supports double-bit error detection and single-bit error correction ECC (8- bit check word across 64-bit data)
- Supports single chip select (D1_MCS0_B)

The address and control signals to the DDR4 SDRAM memory chips are routed as per Fly-by topology and are terminated at VTT (0.6 V). The data bus and associated signals, such as MDM and MDQS have one-to-one connections with individual x16 DDR4 memories. The ECC nibble goes to the fifth DDR4 memory.

The different components of the FRWY-LS1046A DDR interface are powered by the following power supplies generated by the PF8100 power management integrated circuit (PMIC):

- 1.2 V (GVDD) for DDR controller input/output

- 1.2 V and 2.5 V (VPP) for DDR4 SDRAM memory chips
- 0.6 V (VTT) for DDR address and control bus termination

For more information on board power supplies, see Secondary power supplies on page 14.

2.4 SerDes interface

The FRWY-LS1046A supports serializer/deserializer (SerDes) connections on three of the eight lanes of SerDes1 and SerDes2 modules of the LS1046A processor. The figure below shows the SerDes diagram of the FRWY-LS1046A.

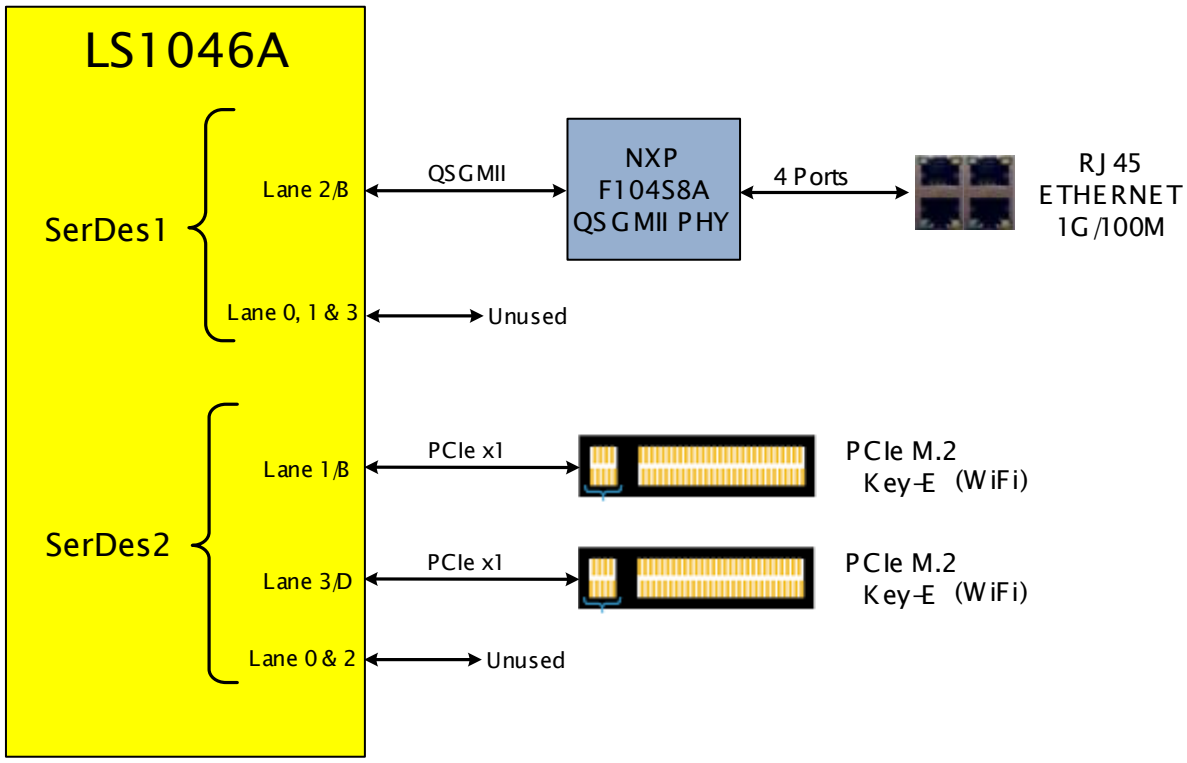

Figure 9. SerDes diagram

The table below describes the FRWY-LS1046A SerDes assignments.

Table 9. SerDes assignments

SerDes module	Lane	Connectivity	Port
SerDes1	Lane 2	NXP F104S8A 1.25 GbE quad-port QSGMII PHY	Two 1.25 GbE 1x2 RJ45 ports on QSGMII MAC interface
SerDes2	Lane 1	PCIe (Gen 1/2/3)	PCIe x1 M.2 Key-E slot for 1630/2230 Wi-Fi module
	Lane 3	PCIe (Gen 1/2/3)	PCIe x1 M.2 Key-E slot for 1630/2230 Wi-Fi module

The figure below shows the possible SerDes1 protocol combinations that can be used on the FRWY-LS1046A.

SRDS_PRTCL_S1 RCW[128-143] (in hex)	D SD1_RX0_P/N SD1_TX0_P/N	C SD1_RX1_P/N SD1_TX1_P/N	B SD1_RX2_P/N SD1_TX2_P/N	A SD1_RX3_P/N SD1_RX3_P/N	PCIe Gen1/2 PLL Mapping	PCIe Gen3 PLL Mapping
3040	SGMII.9	Unused	QSGMII. 6,5,10,1	Unused	2222	not available

Figure 10. SerDes1 protocol combinations

The figure below shows the possible SerDes2 protocol combinations that can be used on the FRWY-LS1046A.

SRDS_PRTCL_S2 RCW[144-159]	A SD2_RX0_P/N SD2_RX0_P/N	B SD2_RX1_P/N SD2_RX1_P/N	C SD2_RX2_P/N SD2_RX2_P/N	D SD2_RX3_P/N SD2_RX3_P/N	PCIe Gen1/2 PLL Mapping	PCIe Gen3 PLL Mapping
0506	Unused	PCIe.2 x1	Unused	PCIe.3 x1	2222	1111

Figure 11. SerDes2 protocol combinations

2.4.1 Ethernet interface

The onboard Ethernet PHY, NXP F104S8A PHY (U123), connects to the TSN switch of the LS1046A processor using QSGMII protocol over SerDes1 lane 2/B. The figure below shows the FRWY-LS1046A Ethernet diagram.

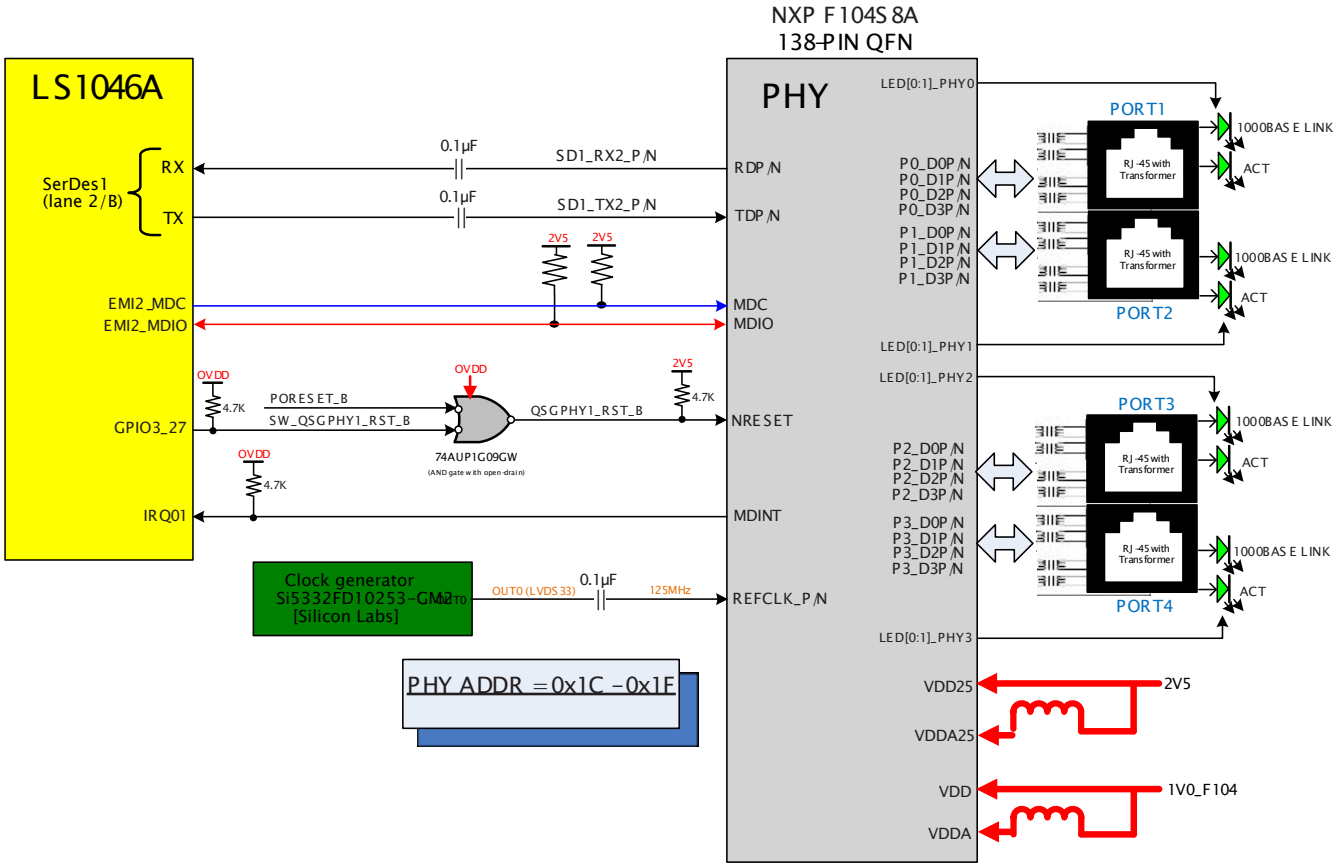

Figure 12. Ethernet diagram

The EMI2 MDIO/MDC signals control the QSGMII PHY transceiver. EMI2 operates at TVDD (2.5 V) levels. The figure below shows the EMI connections.

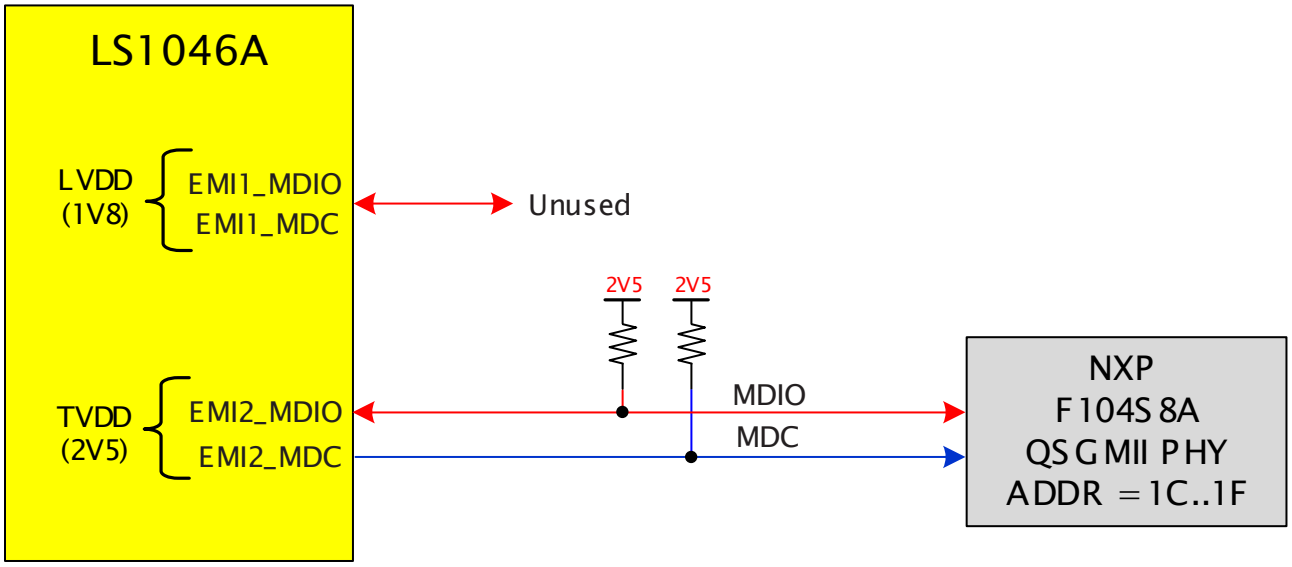

Figure 13. EMI connections

The table below shows the hardware bootstrap settings required for the QSGMII PHY. These configuration settings are controlled through onboard resistors.

Table 10. Hardware bootstrap settings for QSGMII PHY

Feature	Settings
PHY address	PHYADD[4:2] = 0x1C - 0x1F
REFCLK selection	REFCLK_SEL[1:0] = 00: 125 MHz clock is used as REFCLK
COMA_MODE	COMA_MODE = 0: PHY comes out of reset as soon as reset is de-asserted

2.4.2 M.2 PCIe slots

The FRWY-LS1046A supports two M.2 Key-E slots (J46 and J52), which are supported through SerDes2 lane 1 and lane 3, respectively. These connectors support only 1630 and 2230 PCIe Gen 1/2/3 card types to provide wireless connectivity, including Wi-Fi and NFC. Note that:

- M.2 connectors have PCIe x1 (upto Gen 3) connectivity through the LS1046A processor
- M.2 connectors do not have UART, SDIO, or USB 2.0 connectivity through the LS1046A processor. Therefore, it could be possible that some of the features related to these interfaces would not work in plugged-in M.2 modules.
- M.2 connectors have test points for coexistence signals. Because coexistence signal assignments on M.2 connectors is vendor dependent, refer to vendor-specific documentation of M.2 modules for details.

2.4.2.1 Adapters for M.2 PCIe slots

You can use an adapter to convert an M.2 PCIe slot to a slot that supports PCIe Gen 1 and Gen 2 compliant endpoints. See links below for more detail on such adapters:

- P11S-P11F - Duo PCI-E to M.2 (NGFF) Extender Board
- P11S-P11F - M.2 (NGFF) to PCI-E Extender Board

2.5 USB interface

The FRWY-LS1046A supports universal serial bus (USB) 3.0 connections with USB1 and USB2 controllers of the LS1046A processor through a dual-port USB Type A connector. The figure below shows the USB diagram of the FRWY-LS1046A.

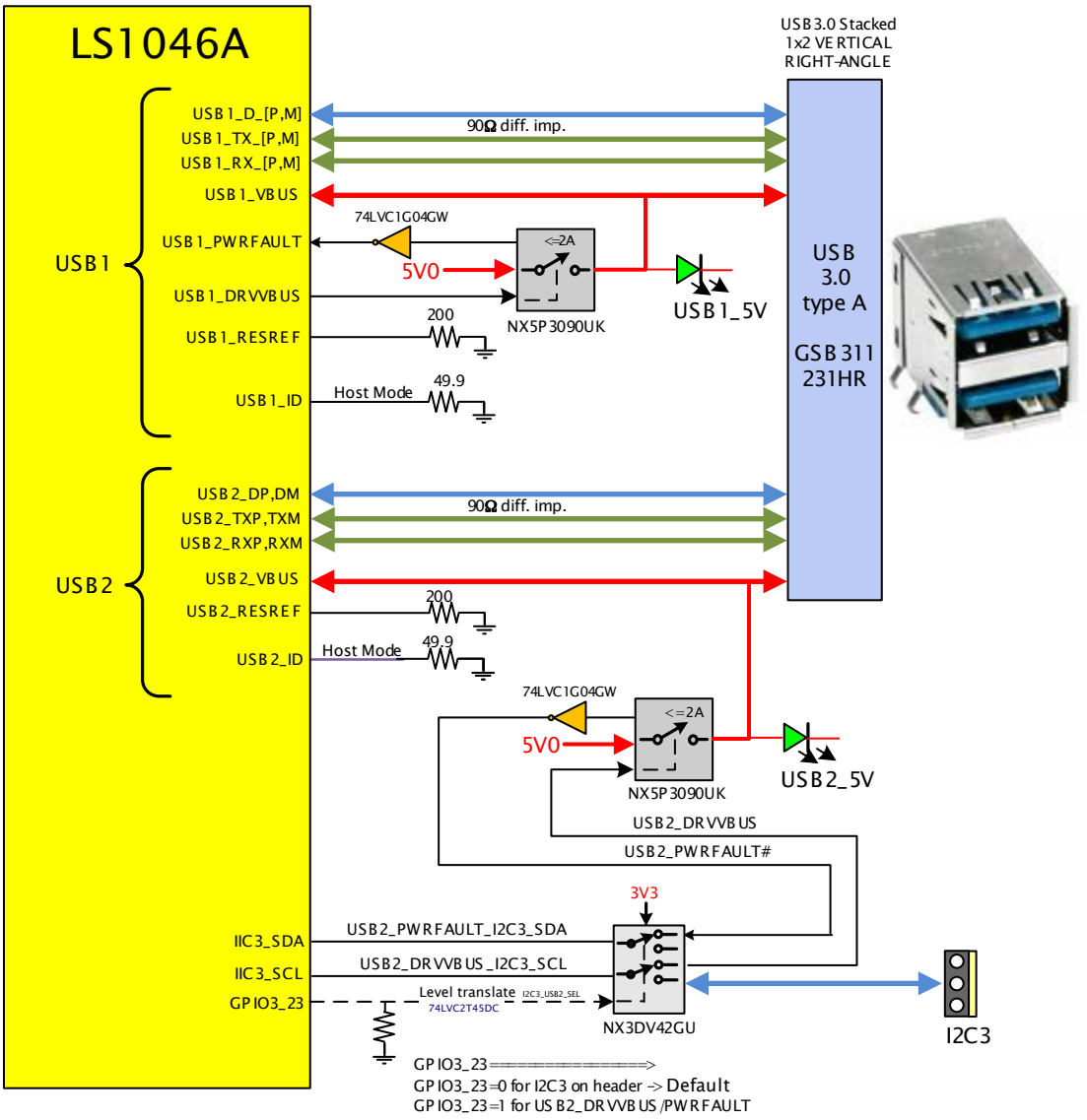

Figure 14. USB diagram

The table below describes the FRWY-LS1046A USB connections.

Table 11. USB connections

USB controller	Connector	Supported mode	Supported speed
USB1	Stacked 1x2 USB 3.0 Type A connector (J70: GSB311231HR)	Host	Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s)
USB2		Host	Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s)

The USBx_DRVVBUS and USBx_PWRFAULT pins of each USB controller are connected to a programmable-current USB switch, NX5P3090UK (U40 and U550), for individual port management. Each USB switch is powered from the 5 V power supply. To indicate power fault conditions, a USB switch sends a PWRFAULT signal to the corresponding USB controller. For each port of the dual-port USB connector, the corresponding USB switch drives a VBUS signal when USBx_DRVVBUS = 1.

The USB2_DRVVBUS and USB2_PWRFAULT signals are muxed with I2C3_SCL and I2C3_SDA signals, respectively. A multiplexer NX3DV42GU (from NXP) is used to demux the muxed signals. The GPIO3_23 signal (I2C3_USB2_SEL) controls the routing of the demuxed signals to the appropriate board peripheral, as follows:

- I2C3_USB2_SEL = 0: I2C3_SCL/SDA signals are routed to I2C3 header J64 (default setting)
- I2C3_USB2_SEL = 1: USB2_DRVVBUS/PWRFAULT signals are routed to USB2 port management switch U550

The maximum allowed current consumption of a USB connected device is 900 mA per channel.

Each port of the dual-port USB connector has an LED (USB1_5V and USB2_5V) to indicate its status, the LED is active when the 5 V power supply is enabled for the port.

2.6 IFC interface

The FRWY-LS1046A supports integrated flash controller (IFC) 2.0 connections with the LS1046A processor through NAND flash and QSPI NOR flash memories. The figure below shows the IFC diagram of the FRWY-LS1046A.

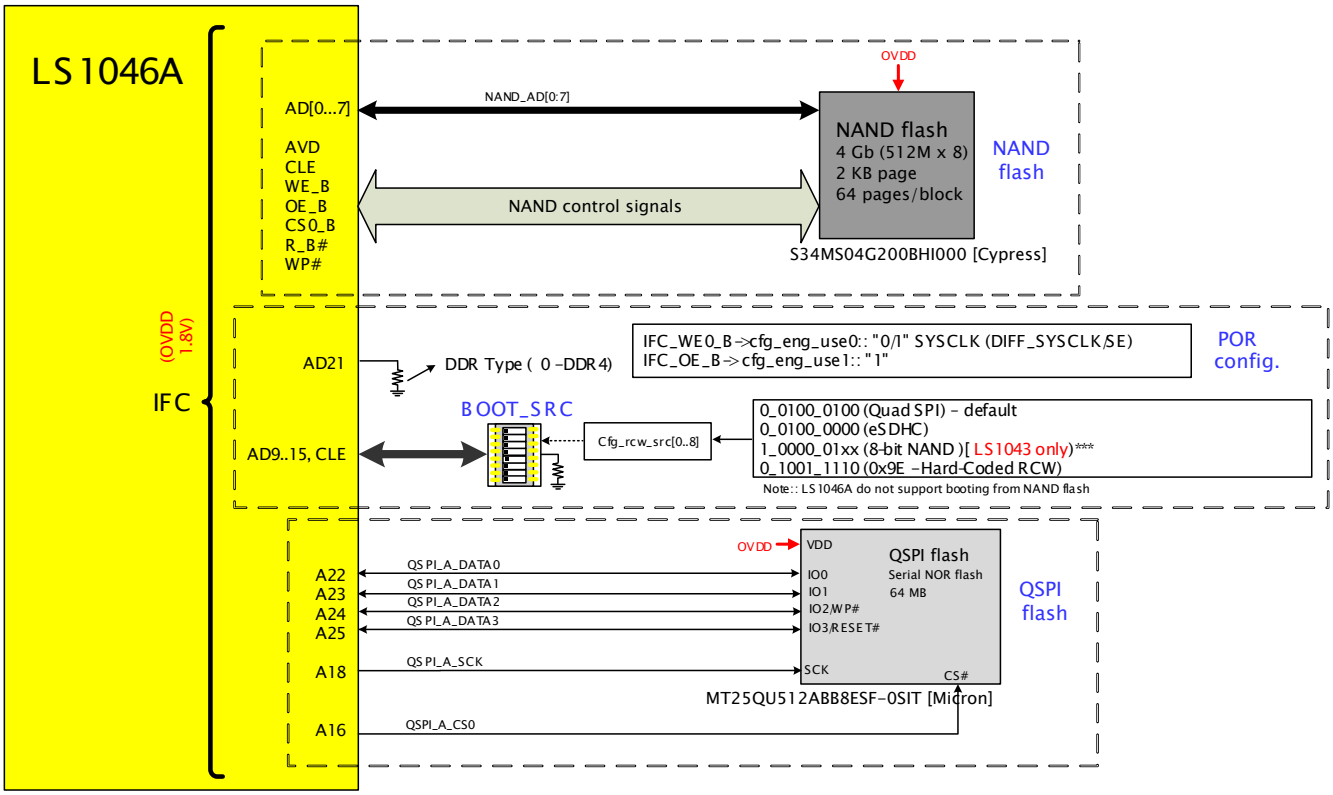

Figure 15. IFC diagram

The subsections below describe the IFC devices supported by the FRWY-LS1046A:

- NAND flash memory on page 27
- QSPI NOR flash memory on page 26

2.6.1 QSPI NOR flash memory

The FRWY-LS1046A supports QSPI as the primary system boot source. The table below describes the QSPI NOR flash memory used in FRWY-LS1046A.

Table 12. QSPI NOR flash memory

Part identifier	Part number	Description
U532	MT25QU512ABB8ESF-0SIT	• Type: Serial NOR flash memory • Density: 512 Mbit (64 MB) • Operating voltage: 1.8 V

2.6.2 NAND flash memory

The table below describes the NAND flash memory used in FRWY-LS1046A.

Table 13. NAND flash memory

Part identifier	Part number	Description
U522	S34MS04G200BHI000	• Type: SLC NAND flash memory • Density: 4 Gbit • I/O bus width: 8 bits (x8) • Page size: (2048+128) bytes • Block size: 64 pages • Device size: 512 MB

2.7 SDHC interface

The FRWY-LS1046A supports connections with the enhanced secure digital host controller (eSDHC) of the LS1046A processor through a micro-SDHC connector that accepts an external micro-SD 3.0 card. The micro-SD card is one of the primary boot sources of the board. The figure below shows the SDHC diagram of the FRWY-LS1046A.

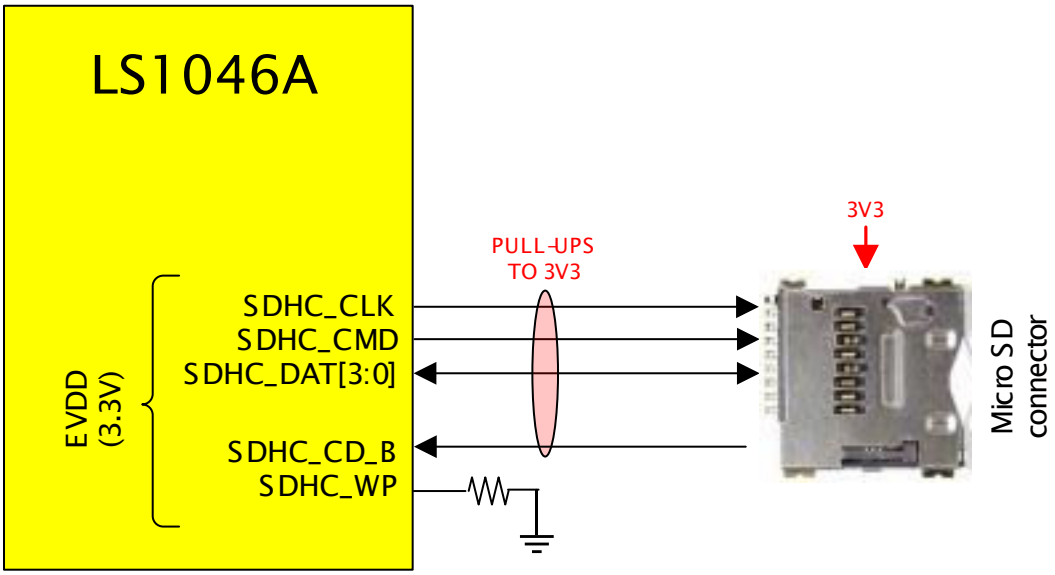

Figure 16. SDHC diagram

NOTE

The micro-SD card available with the board does not support ultra high-speed (UHS) modes.

The part number of the micro-SDHC connector J55 is 95220030-14RRF. The table below shows the pinout details of the micro-SDHC connector.

Table 14. Micro-SDHC connector pinout

Pin number	SDHC signals	Direction with respect to LS1046A	I/O voltage
1	SD_DATA2	Bidirectional	3.3 V
2	SD_DATA3	Bidirectional	
3	SD_CMD	From LS1046A	
4	3V3		
5	SD_CLK	From LS1046A	
6	GND		
7	SD_DATA0	Bidirectional	
8	SD_DATA1	Bidirectional	
9	SDHC_CD_B	To LS1046A	

The SDHC_CD_B signal of the micro-SDHC connector indicates presence/absence of card in the connector slot. This signal goes to I2C2 controller through the IIC2_SCL pin of the controller. The IIC2_SCL pin must be programmed in RCW (by setting RCW[I2C2_EXT] to 001) to serve as the SDHC_CD_B pin for the eSDHC controller. This happens automatically when the micro-SD card is selected as the boot source for the board.

2.8 UART interface

The LS1046A processor has two dual universal asynchronous receiver/transmitter (DUART) modules, DUART1 and DUART2, each containing two UARTs. Each DUART module can work as one UART with flow control or two UARTs without flow control.

The FRWY-LS1046A supports both DUART modules of the LS1046A processor; however, it does not support flow control on DUART1 module, it means, this DUART module works as two UARTs (UART1 and UART3) on the board. Flow control is supported on DUART2 module, which can work as one UART (UART2) or two UARTs (UART2 and UART4). The figure below shows the UART diagram of the FRWY-LS1046A.

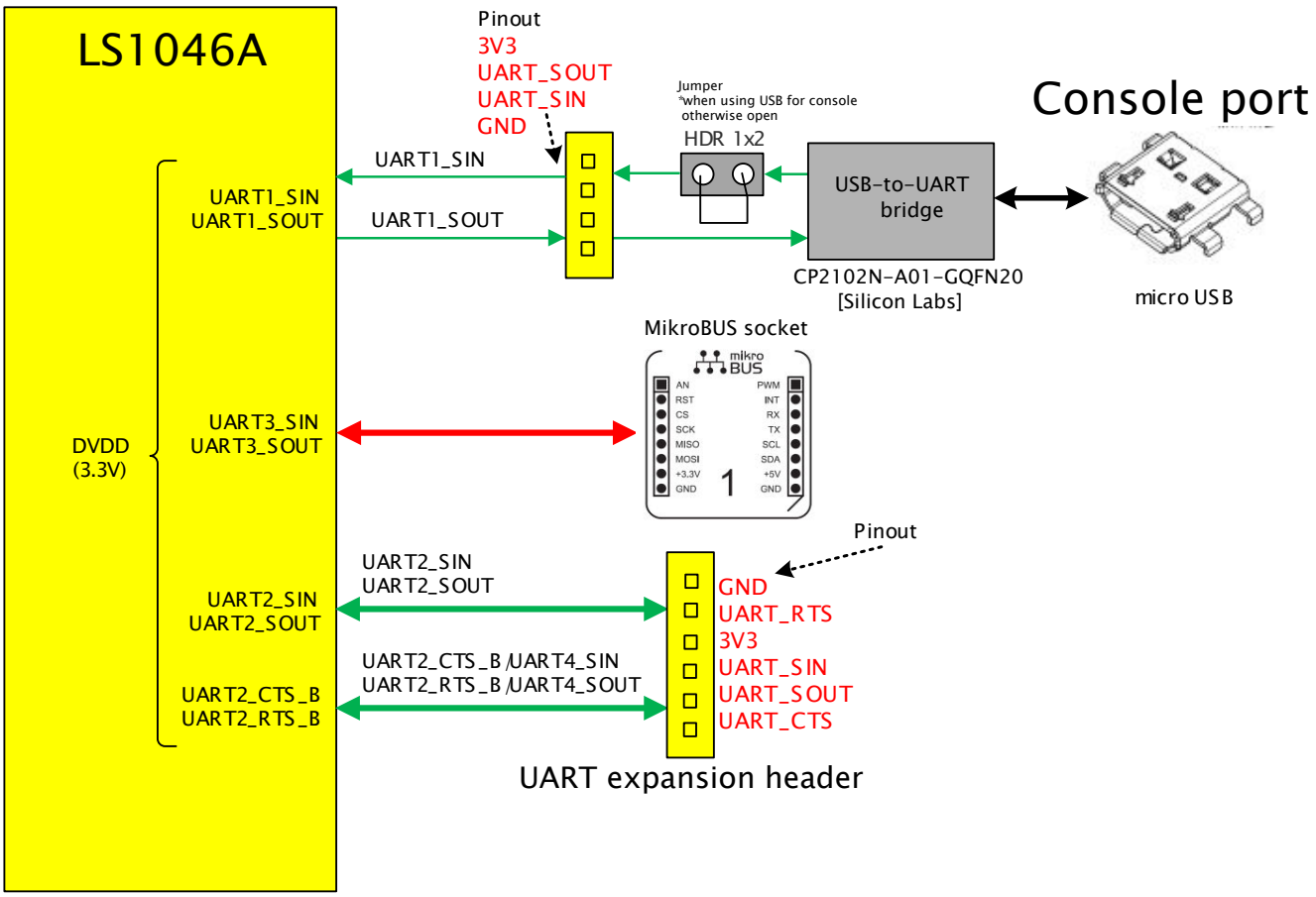

Figure 17. UART diagram

NOTE

It is recommended to use UART1 as a debug port.

The FRWY-LS1046A supports following UART features:

- UART1 is routed to CP2102N USB-UART bridge and supports micro-USB port to access the serial port as console. This connection requires placing a jumper on header J72.
- UART1 can be used without flow control on expansion header J73 (3.3 V). This connection requires removing the jumper from header J72.
- UART3 signals can be used to communicate with click board plugged-in into mikroBUS socket
- UART2 can be used with/without flow control on expansion header J60 (3.3 V). A remote UART connection can be made from the expansion header using an FTDI standard 3.3 V cable (TTL-232R-3V3) or by connecting to an RS-232/RS-485/ RS-422 expansion card.
- UART4 can be used on expansion header J60 (3.3 V)

The table below shows pinout details of UART expansion header J73.

Table 15. UART expansion header J73 pinout

Pin number	UART signals	Direction with respect to LS1046A	I/O voltage
1	3V3		3.3 V

Table continues on the next page...

Table 15. UART expansion header J73 pinout (continued)

Pin number	UART signals	Direction with respect to LS1046A	I/O voltage
2	UART1_SOUT	From LS1046A	
3	UART1_SIN	To LS1046A	
4	GND		

The table below shows pinout details of UART expansion header J60.

Table 16. UART expansion header J60 pinout

Pin number	UART signals	Direction with respect to LS1046A	I/O voltage
1	GND		3.3 V
2	UART2_RTS_B/UART4_SOUT	From LS1046A	
3	3V3		
4	UART2_SIN	To LS1046A	
5	UART2_SOUT	From LS1046A	
6	UART2_CTS_B/UART4_SIN	To LS1046A	

2.9 Serial peripheral interface

The FRWY-LS1046A supports serial peripheral interface (SPI) connections to the LS1046A processor through a mikroBUS socket and SPI expansion header. The figure below shows the SPI diagram of the FRWY-LS1046A.

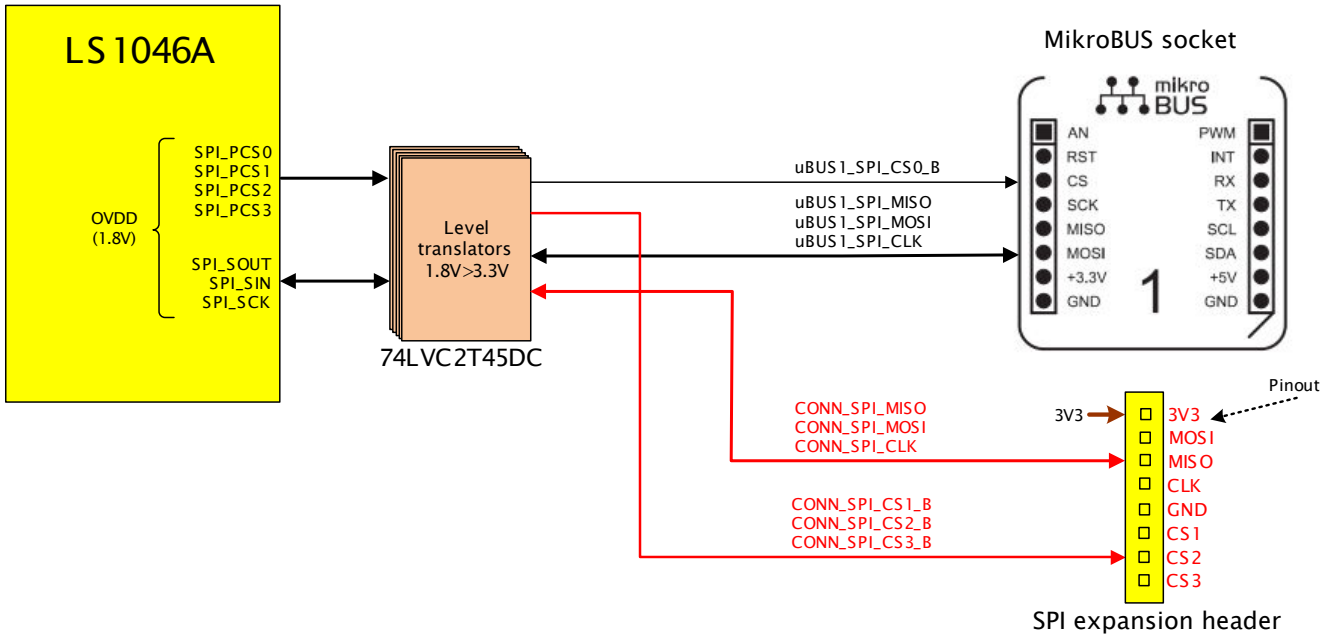

Figure 18. SPI diagram

NOTE

The LS1046A SPI signals are on 1.8 V (OVDD) and they are converted to 3.3 V level using level translators.

The table below describes chip select mapping for FRWY-LS1046A SPI interface.

Table 17. SPI chip select mapping

Chip select	Connected device
SPI_PCS0	MikroBUS socket
SPI_PCS1	Expansion header
SPI_PCS2	Expansion header
SPI_PCS3	Expansion header

The table below shows pinout details of SPI expansion header J66.

Table 18. SPI expansion header J66 pinout

Pin number	SPI signals	Direction with respect to LS1046A	I/O voltage
1	3V3		3.3 V
2	CONN_SPI_MOSI	From LS1046A	
3	CONN_SPI_MISO	To LS1046A	
4	CONN_SPI_CLK	From LS1046A	
5	GND		
6	CONN_SPI_CS1_B	From LS1046A	
7	CONN_SPI_CS2_B	From LS1046A	
8	CONN_SPI_CS3_B	From LS1046A	

2.10 MikroBUS socket

The FRWY-LS1046A provides one mikroBUS socket supporting two connectors, J56 and J57. A mikroBUS socket is a pair of 1×8 female headers with a proprietary pin configuration and silkscreen markings, as shown in the figure below. The mikroBUS socket allows maximum hardware expandability with smallest number of pins.

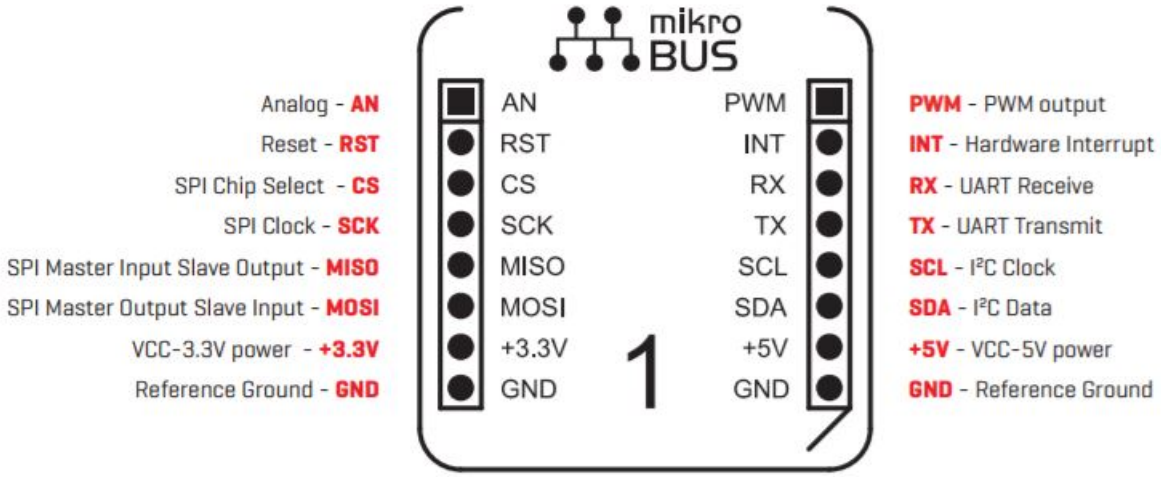

Figure 19. MikroBUS pin specifications

The FRWY-LS1046A mikroBUS socket supports different types of add-on boards, called *click boards*, which can be accessed through SPI, UART3, PWM, or I2C interface. On the FRWY-LS1046A, following interfaces are used with the LS1046A processor for click boards:

- SPI on click boards can be accessed through SPI of the LS1046A processor using CS0
- UART on click boards can be accessed through UART3 of the LS1046A processor
- I2C on click boards can be accessed through I2C1 of the LS1046A processor using I2C multiplexer

The figure below shows the FRWY-LS1046A mikroBUS socket diagram.

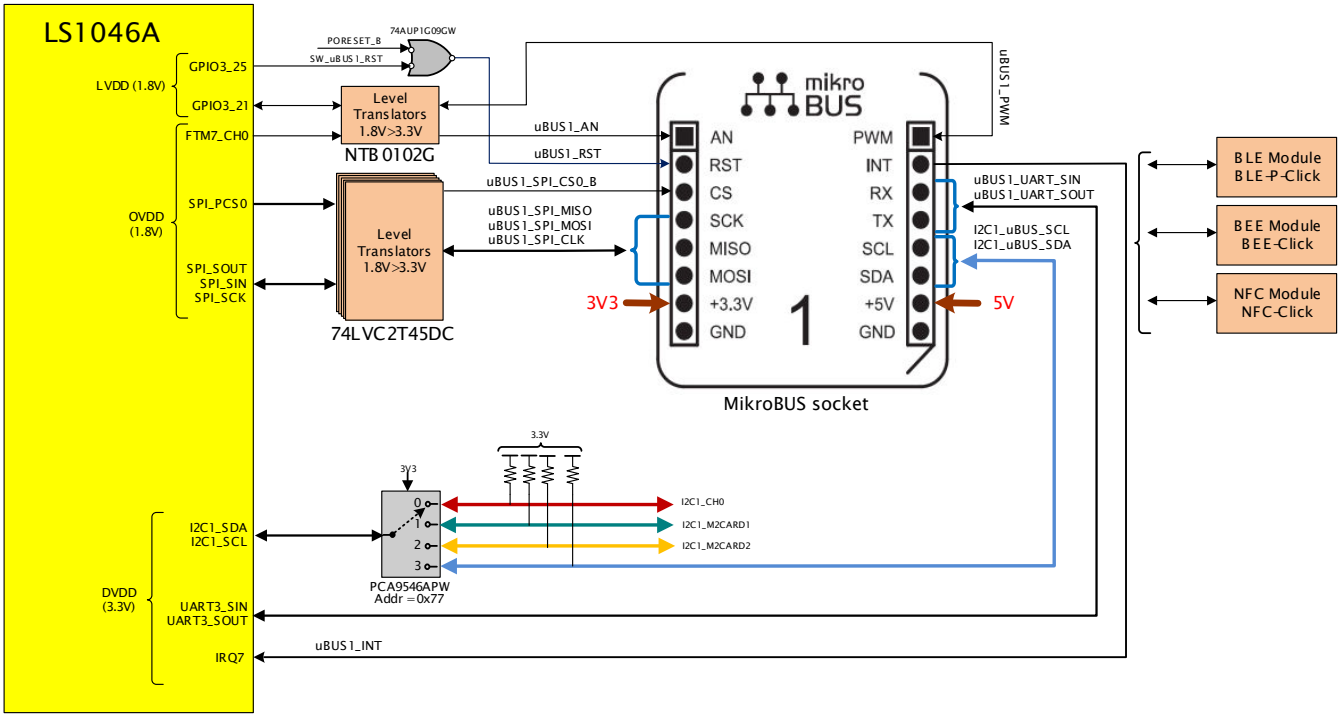

Figure 20. MikroBUS socket diagram

Click boards are plug and play solutions to add new functionality to the board design. A click board has two columns each of eight pins, which connect to the two 1x8 headers of a mikroBUS socket. The table below lists some of the click boards that can be added on the FRWY-LS1046A mikroBUS socket.

Table 19. Supported click boards

Part number	Name	Supported communication interface	Operating voltage	Description
MIKROE-1597	BLE P click	SPI	3.3 V	Contains a Bluetooth® low energy chip. This module communicates with FRWY-LS1046A through SPI (CS, SCK, MISO, MOSI), INT (RDY), and AN (ACT) lines on mikroBUS socket.
MIKROE-987	BEE click	SPI	3.3 V	Contains a 2.4 GHz IEEE 802.15.4 radio transceiver module to support wireless communication applications
MIKROE-2395	NFC click	I2C, GPIO	3.3 V	Contains a near field communication (NFC) controller, PN7120, from NXP
MIKROE-1194	Accel click	I2C, GPIO, SPI	3.3 V	Contains a 3-axis accelerometer module with ultra-low power and high resolution (13-bit) measurement

2.11 I2C interface

The LS1046A processor supports four I2C controllers. However, in the FRWY-LS1046A, all system devices are accessed via I2C1 controller over I2C1 bus. The figure below shows the I2C diagram of the FRWY-LS1046A.

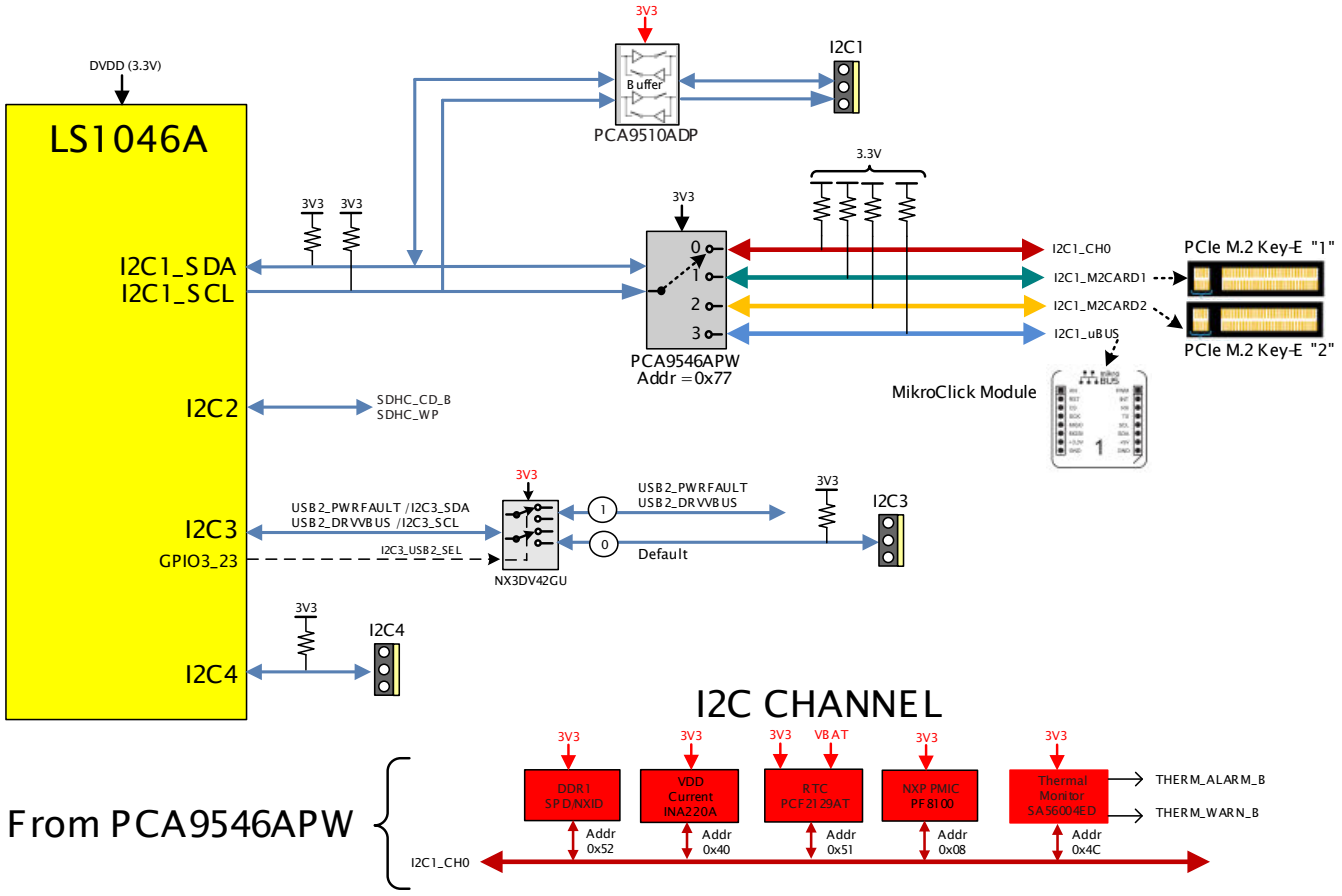

Figure 21. I2C diagram

NOTE

I2C2 should be programmed to be used for SDHC_CD_B and SDHC_WP.

The I2C1 bus has an I2C multiplexer (PCA9546APW) to isolate address conflicts and effectively manage large number of I2C devices. The multiplexer partitions the I2C1 bus into four sub-buses, called "channels". Software must program the multiplexer to access one of the four I2C1 channels. All boot-software-dependant devices are placed on channel 0, or "I2C1_CH0" as it is named. Channel 0 is the default selection upon reset so that software has immediate access to critical resources.

The table below shows the I2C bus device map for the FRWY-LS1046A.

Table 20. I2C bus device map

I2C bus	7-bit address	Device	Description	Notes
(All)	-	FRWY-LS1046A	I2C master	
I2C1	0x77	PCA9546APW	I2C bus multiplexer (U525)	Converts I2C1 bus into four channels
I2C1_CH0	0x08	PF8100	Power management integrated circuit (PMIC) (U561)	Generates 1 V, 1.8 V, 1.2 V, 1.35 V, 0.6 V, 2.5 V, and 1.8 V
	0x40	INA220AIDGST	VDD voltage/current/power monitor (U558)	Reports voltage, current, and power data for VDD

Table continues on the next page...

Table 20. I2C bus device map (continued)

I2C bus	7-bit address	Device	Description	Notes
	0x4C	SA56004ED	Temperature sensor (U28)	Monitors processor thermal diode
	0x51	PCF2129AT	Battery-backed clock (U523)	Provides time and date functionality with battery backup option
	0x52 and 0x53	CAT24C04WI-G	System ID EEPROM (U524)	Stores board-specific data, such as MAC addresses and serial number / errata
I2C1_CH 1	I2C address is defined by the plugged-in PCIe card	PCIe M.2 slot	Key E - based M.2 PCIe x1 slot 1 (J46)	Provides I2C path for J46, which supports Wi-Fi cards on lane 1 of SerDes2 controller
I2C1_CH 2	I2C address is defined by the plugged-in PCIe card	PCIe M.2 slot	Key E - based M.2 PCIe x1 slot 2 (J52)	Provides I2C path for J52, which supports Wi-Fi cards on lane 3 of SerDes2 controller
I2C1_CH 3	I2C address is defined by the plugged-in click board	MikroBUS socket	MikroBUS socket	Provides I2C connectivity to the click board plugged-in into the mikroBUS socket

NOTE

A 7-bit address does not include the read/write (R/W) bit as an address member, though some datasheets might do so. For consistency, all I2C addresses above are of 7 bits only.

The FRWY-LS1046A also provides I2C headers for remotely accessing I2C buses. The table below describes the I2C headers.

Table 21. I2C headers

Part identifier	Header name	Header type	Purpose
J65	I2C1	1x3 connector	To access I2C1 bus remotely
J64	I2C3[1]	1x3 connector	To access I2C3 bus remotely
J63	I2C4	1x3 connector	To access I2C4 bus remotely

1. I2C3_SCL/SDA signals are muxed with USB2_DRVVBUS/PWRFAULT signals and are demuxed with using a multiplexer NX3DV42GU and controlled using GPIO3_23.

2.12 JTAG header

The FRWY-LS1046A provides an Arm JTAG header, which allows connections with a CodeWarrior TAP for debugging the board. The figure below shows the JTAG diagram of the FRWY-LS1046A.

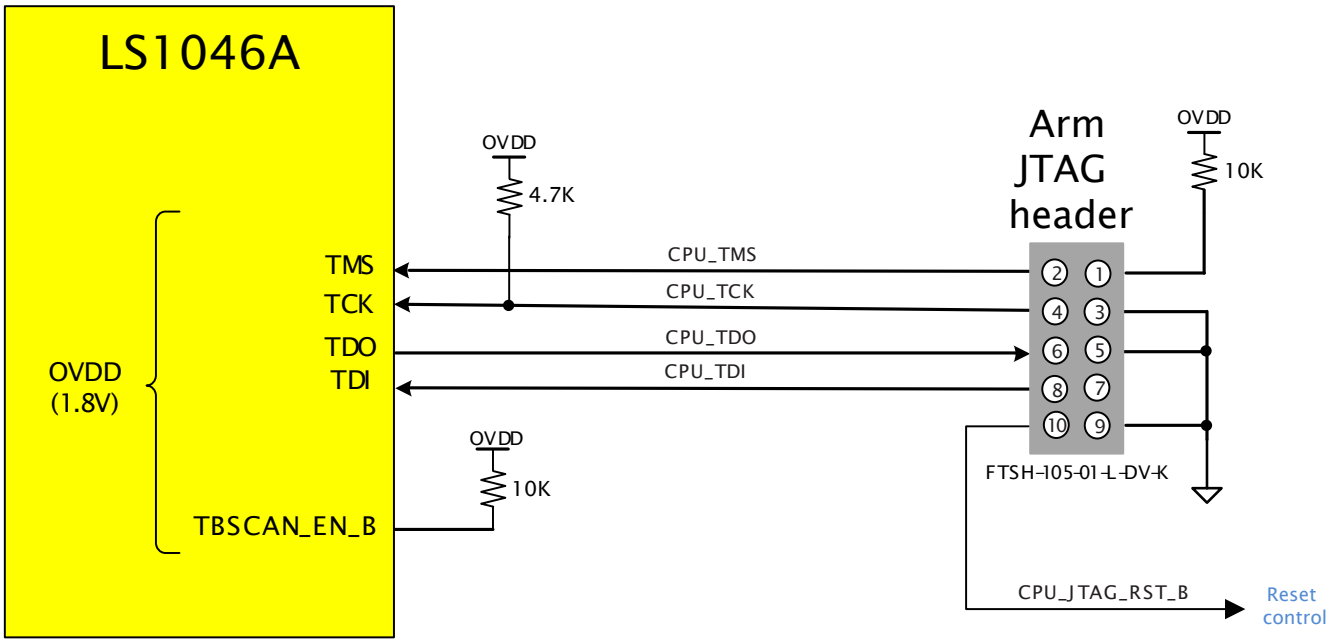

Figure 22. JTAG diagram

The table below describes the JTAG header.

Table 22. JTAG header

Part identifier	Part number	Description	Purpose
J15	FTSH-105-01-L-DV-K	10-pin Arm Cortex JTAG connector	Provides access to the processor for debugging purposes

2.13 GPIOs

The LS1046A processor has no dedicated general-purpose input/output (GPIO) pins. Instead, GPIO functions are multiplexed internally onto other signals, which must be disabled before using the GPIO functions. For the FRWY-LS1046A, GPIO access is provided through the IFC, EC1, and EC2 pins but only when those pins are not used for their primary purposes. The table below shows the GPIO mapping in the FRWY-LS1046A.

Table 23. GPIO mapping

Processor signal		Board function	Description
GPIO function	**Primary function**		
GPIOs for system configuration			
GPIO2_13	IFC_PAR0	BRD_REV0	PCB revision (BRD_REV[1:0]): • 00: Revision A • 01: Revision B
GPIO2_14	IFC_PAR1	BRD_REV1	

Table continues on the next page...

Table 23. GPIO mapping (continued)

Processor signal		Board function	Description
GPIO function	**Primary function**		
GPIO3_19	EC2_TX_EN	CPU_ID	CPU ID (CPU_ID): • 1: LS1046A CPU • 0: Others
GPIO2_15	IFC_PERR_B	SYS_STATUS#	Controls system status LED
GPIO3_21	EC2_GTX_CLK125	uBUS1_PWM	Provides PWM input to mikroBUS socket
GPIO3_23	EC2_RXD2	I2C3_USB2_SEL_IO	Controls the routing of the I2C3_SCL/SDA and USB2_DRVVBUS/PWRFAULT signals: • 0: I2C3_SCL/SDA signals are routed to I2C3 header J64 (default setting) • 1: USB2_DRVVBUS/PWRFAULT signals are routed to USB2 port management switch U550
GPIO3_18	EC2_TXD0	RSV_IO	Reserved for general purpose input/output
GPIOs for reset control			
GPIO3_25	EC2_RXD0	SW_uBUS1_RST	Resets mikroBUS socket
GPIO3_20	EC2_GTX_CLK	SW_SLOT1_RST_B	Resets M.2 PCIe slot 1
GPIO3_26	EC2_RX_CLK	SW_SLOT2_RST_B	Resets M.2 PCIe slot 2
GPIO3_27	EC2_RX_DV	SW_QSGPHY1_RST_B	Resets QSGMII PHY
GPIO for fuse programming			
GPIO3_24	EC2_RXD1	GPIO_FUSE_PROG	Connects to the 1x2 PROG_SFP header (J74). The GPIO_FUSE_PROG signal controls the power supply to the TA_PROG_SFP pin of the processor: • When GPIO_FUSE_PROG is low, power to TA_PROG_SFP pin is 1.8 V (fuse programming enable) • When GPIO_FUSE_PROG is high, power to TA_PROG_SFP pin is 0 V (fuse programming disable) (default value)
GPIO expansion header			
GPIO3_06	EC1_TX_EN	Connect to a 2x10 GPIO header (J67) for general purpose input/output.	
GPIO3_11	EC1_RXD1		
GPIO3_04	EC1_TXD1		
GPIO3_12	EC1_RXD0		
GPIO3_02	EC1_TXD3		

Pin number	Signal name	Direction (type)	I/O voltage
1	GPIO3_06	Bidirectional (input/output)	1.8 V

Table continues on the next page...

Table 23. GPIO mapping (continued)

Processor signal		Board function		Description	
GPIO function	**Primary function**	**Pin number**	**Signal name**	**Direction (type)**	**I/O voltage**
GPIO3_05	EC1_TXD0	2	GPIO3_11	Bidirectional (input/ output)	
GPIO3_03	EC1_TXD2	3	GPIO3_04	Bidirectional (input/ output)	
GPIO3_08	EC1_GTX_CLK125	4	GPIO3_12	Bidirectional (input/ output)	
GPIO3_07	EC1_GTX_CLK	5	GPIO3_02	Bidirectional (input/ output)	
GPIO3_14	EC1_RX_DV	6	GPIO3_05	Bidirectional (input/ output)	
GPIO3_10	EC1_RXD2	7	GND		
GPIO3_15	EC2_TXD3	8	GND		
GPIO3_13	EC1_RX_CLK	9	GPIO3_03	Bidirectional (input/ output)	
GPIO3_16	EC2_TXD2	10	GPIO3_08	Bidirectional (input/ output)	
GPIO3_09	EC1_RXD3	11	GPIO3_07	Bidirectional (input/ output)	
GPIO3_17	EC2_TXD1	12	GPIO3_14	Bidirectional (input/ output)	
		13	GND		
		14	GND		
		15	GPIO3_10	Bidirectional (input/ output)	
		16	GPIO3_15	Bidirectional (input/ output)	
		17	GPIO3_13	Bidirectional (input/ output)	
		18	GPIO3_16	Bidirectional (input/ output)	
		19	GPIO3_09	Bidirectional (input/ output)	
		20	GPIO3_17	Bidirectional (input/ output)	

2.14 Interrupt handling

Apart from handling interrupts from interrupt sources within the processor, the generic interrupt controller (GIC) of the LS1046A processor can handle interrupts from external interrupt sources. In the FRWY-LS1046A, the onboard interrupt sources are connected to interrupt controller through IRQ01, IRQ03-IRQ07 pins of the processor for interrupt controller to handle their interrupt signals. The figure below shows the mapping between the onboard interrupt sources and IRQ pins of the processor.

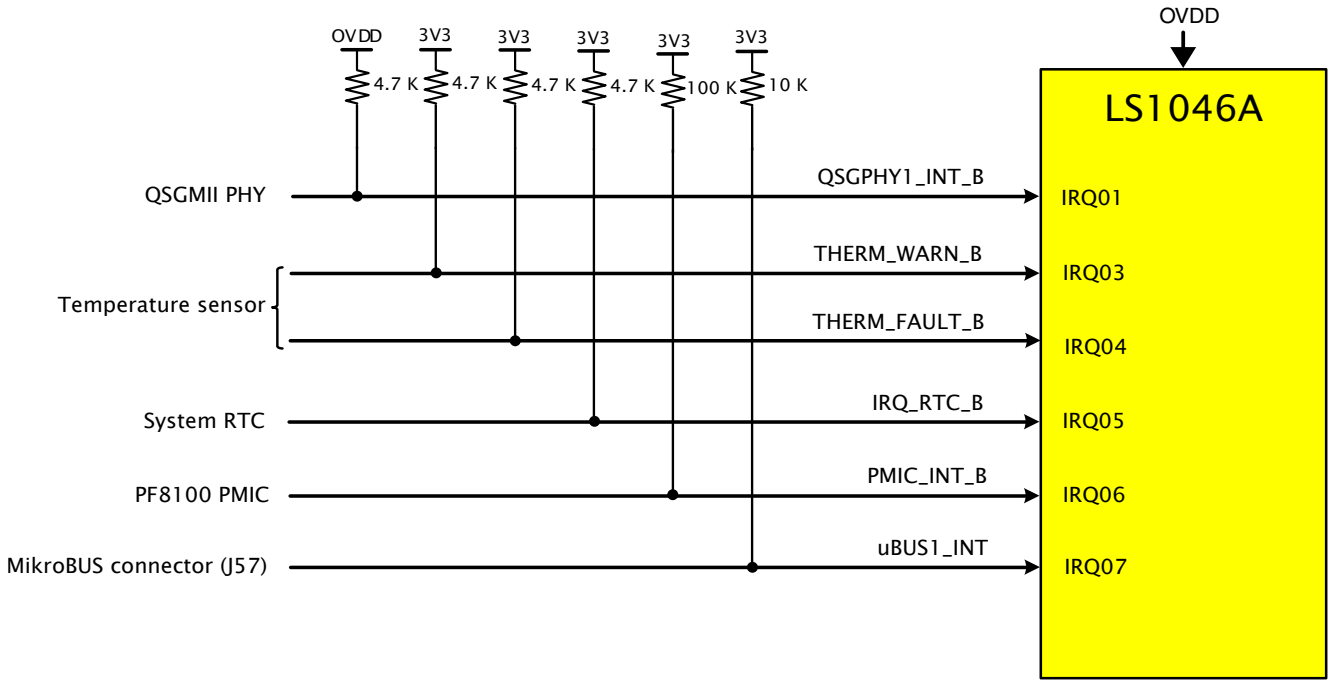

Figure 23. Interrupt assignments

The table below further explains the FRWY-LS1046A interrupt assignments.

Table 24. Interrupt assignments

Interrupt controller signal	Interrupt signal on board	Description
IRQ01	QSGPHY1_INT_B	QSGMII PHY interrupt
IRQ03	THERM_WARN_B	Temperature sensor warning interrupt
IRQ04	THERM_FAULT_B	Temperature sensor fault interrupt
IRQ05	IRQ_RTC_B	RTC interrupt
IRQ06	PMIC_INT_B	PF8100 PMIC interrupt
IRQ07	uBUS1_INT	MikroBUS click board interrupt

2.15 Temperature measurement

The FRWY-LS1046A has a digital temperature sensor (thermal monitor), which can be used to measure the LS1046A die temperature through the thermal diode of the processor. The LS1046A processor sends temperature readings (through

TD1_ANODE and TD1_CATHODE signals) to the temperature sensor. Upon detecting thermal problems, the temperature sensor sends alarm signals (through THERM_WARN_B and THERM_FAULT_B interrupt signals) to the processor. These interrupts can be used to power down the system to protect the processor from over-temperature damage. The figure below shows thermal management in the FRWY-LS1046A.

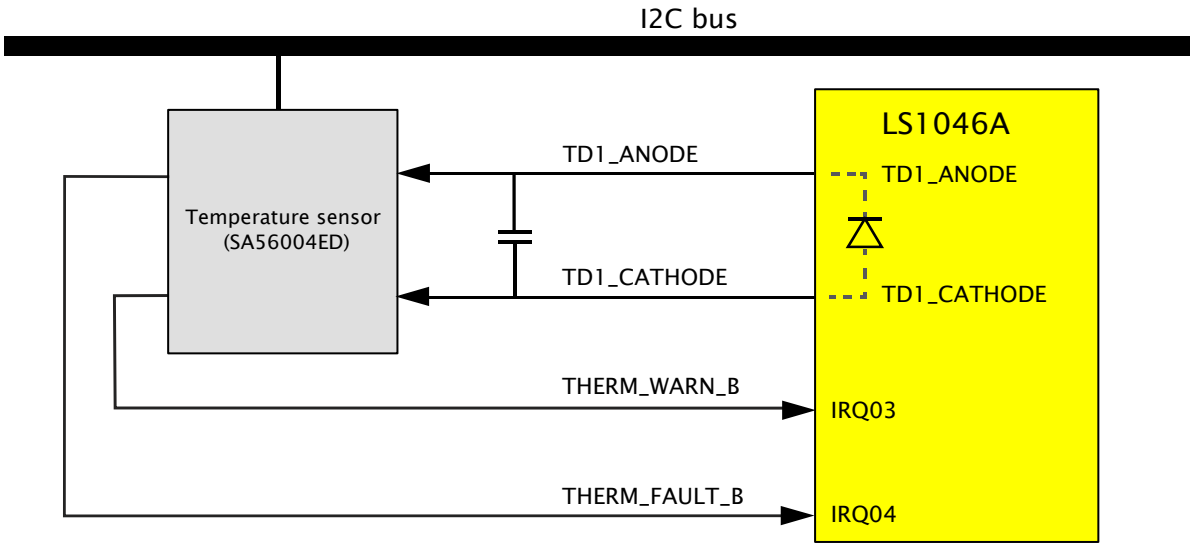

Figure 24. Thermal management

The table below describes the temperature sensor. The I2C address can be used for remotely accessing the temperature sensor.

Table 25. Temperature sensor

Part identifier	Part number	I2C sub-bus	I2C address	Operating voltage
U28	SA56004ED	I2C1_CH0	0x4C	3.3 V

2.16 DIP switch

The FRWY-LS1046A has a 10-pin dual inline package (DIP) switch, SW1, which helps to perform some most common board configuration tasks. For SW1:

- "ON" setting corresponds to 1
- "OFF" setting corresponds to 0

The table below describes SW1 settings.

Table 26. SW1 settings

Switch	Supported function	Settings
SW1[1:9]	RCW fetch location CFG_RCW_SRC[0:8]	• 0_0100_0100: QSPI NOR flash (default setting) • 0_0100_0000: Micro-SD card • 1_0000_01xx: NAND flash (8-bit bus, 2 KB page, 64 pages/block) (LS1043A only)[1] • 0_1001_1110: Hard-coded RCW
SW1[10]	System clock source CFG_ENG_USE0	• 0: DIFF_SYSCLK/DIFF_SYSCLK_B (differential clock) - 100 MHz (fixed) (default setting) • 1: SYSCLK (single-ended clock) - 100 MHz (fixed)

1. The LS1046A processor does not support booting from NAND flash.

2.17 LEDs

The FRWY-LS1046A has light-emitting diodes (LEDs) to monitor system functions, such as power-on, reset, board faults, and so on. The information collected from LEDs can be used for debugging purposes. The table below describes the FRWY-LS1046A LEDs.

Table 27. FRWY-LS1046A LEDs

Reference designator	LED color	LED name	Description (when LED is ON)
D2	Yellow	ASLEEP	The processor has not exited Sleep mode, which generally indicates: • Improper RCW source selection • Boot memory does not contain a valid RCW/PBL • PLL multipliers in the RCW data are not compatible with the fixed SYSCLK, DDRCLK, or SDCLK values
D4	Green	USB1_5V	USB1 port of the dual-port USB connector (J70) is powered with 5 V supply for external USB device
D508	Green	USB2_5V	USB2 port of the dual-port USB connector (J70) is powered with 5 V supply for external USB device
D510[1]	Green	M.2 Card1	The M.2 PCIe module on M.2 PCIe slot 1 (J46) is powered properly and its transmitter is ready to transmit
D511	Green	M.2 Card2	The M.2 PCIe module on M.2 PCIe slot 2 (J52) is powered properly and its transmitter is ready to transmit

Table continues on the next page...

Table 27. FRWY-LS1046A LEDs (continued)

Reference designator	LED color	LED name	Description (when LED is ON)
D509	Green	4_GRN_LED	Four stacked LEDs to indicate: • Power status • System readyness • PROG_SFP fuse programming power enable

1. It is placed on the bottom side of PCB next to J46 connector.

2.18 System reset

The figure below shows the reset diagram for the FRWY-LS1046A.

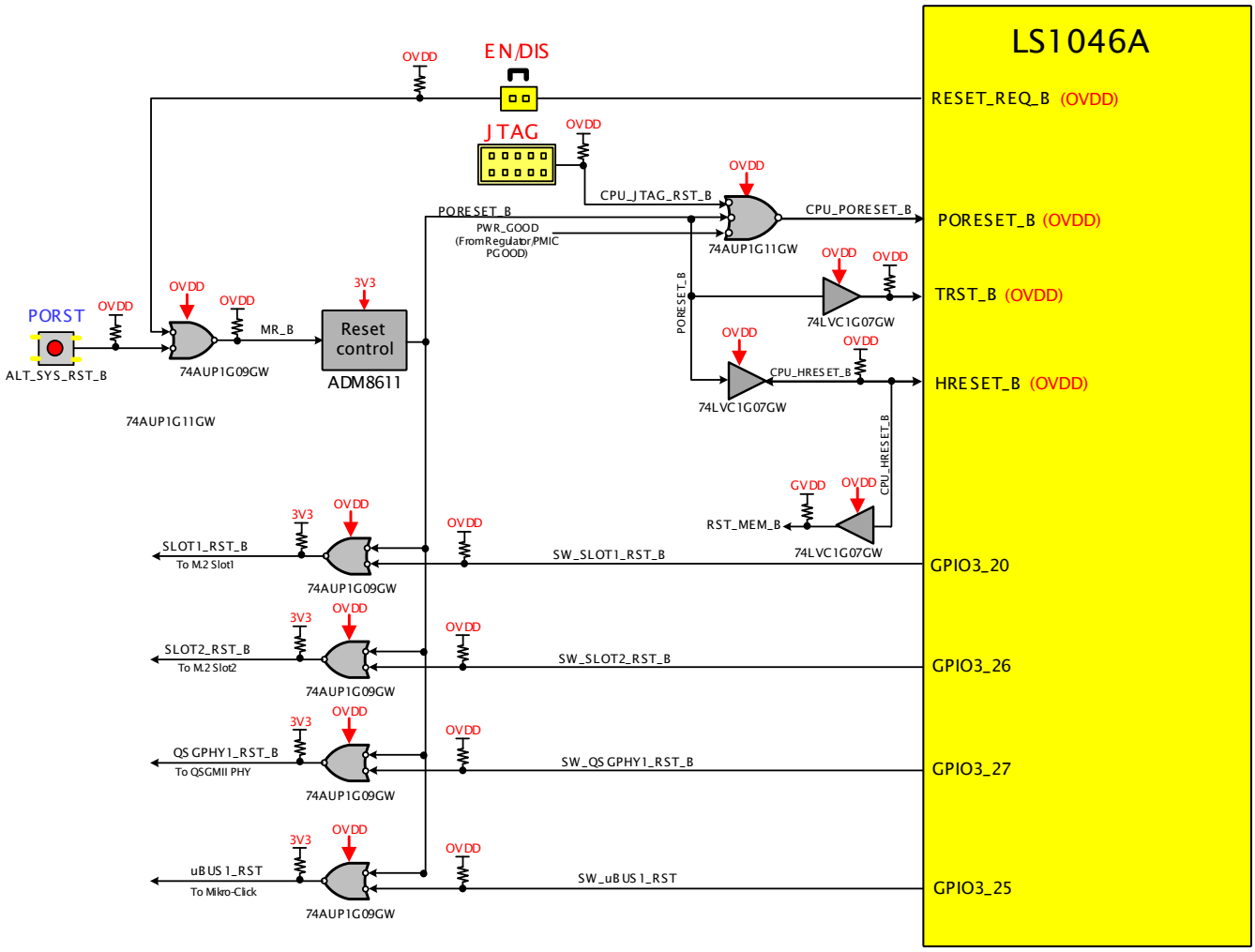

Figure 25. FRWY-LS1046A reset diagram

System reset can be triggered from various sources, as described in the table below.

Table 28. Reset sources

Reset source	Reset reason	Actions taken
Power ON / power failure	Initialization after a power cycle	All the onboard devices are reset after a power cycle. PLL and clock circuitry initialize to default configuration.
SW6	Reset switch is pressed	All devices are reset
RESET_REQ_B[1]	Reset request from processor	All devices are reset
CPU JTAG header (J15)	Reset JTAG debugger	PORESET is asserted to the processor

1. RESET_REQ_B only works when a jumper is placed on header J14.

Appendix A
Revision History

The table below summarizes the revisions to this document.

Table 29. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 0	04/2019		Initial public release

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