PRELIMINARY

1/4 DUTY LCD DRIVER

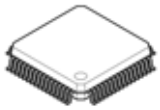
■ GENERAL DESCRIPTION

The NJU6433B is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 50-segment drives up to 200 segments.

The NJU6433B is useful for the digital tuning system or others segment type display driver.

■ PACKAGE OUTLINE



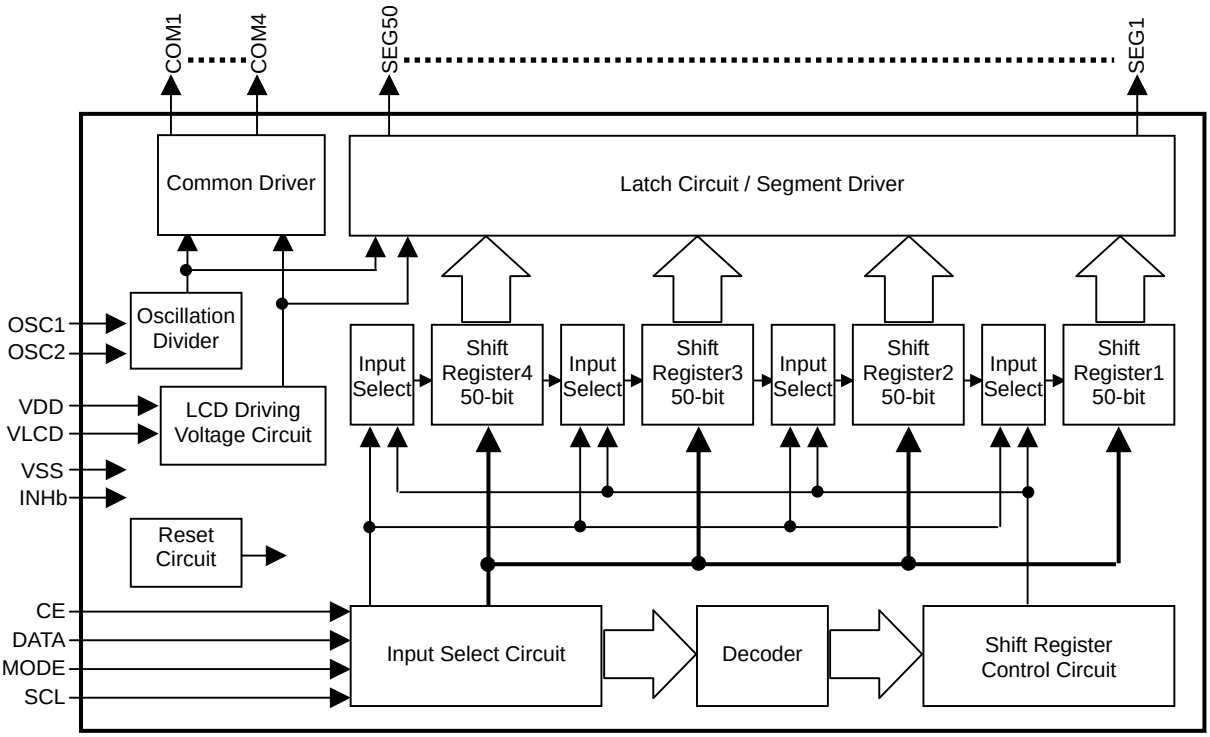
NJU6433BFH1

NJU6433BC

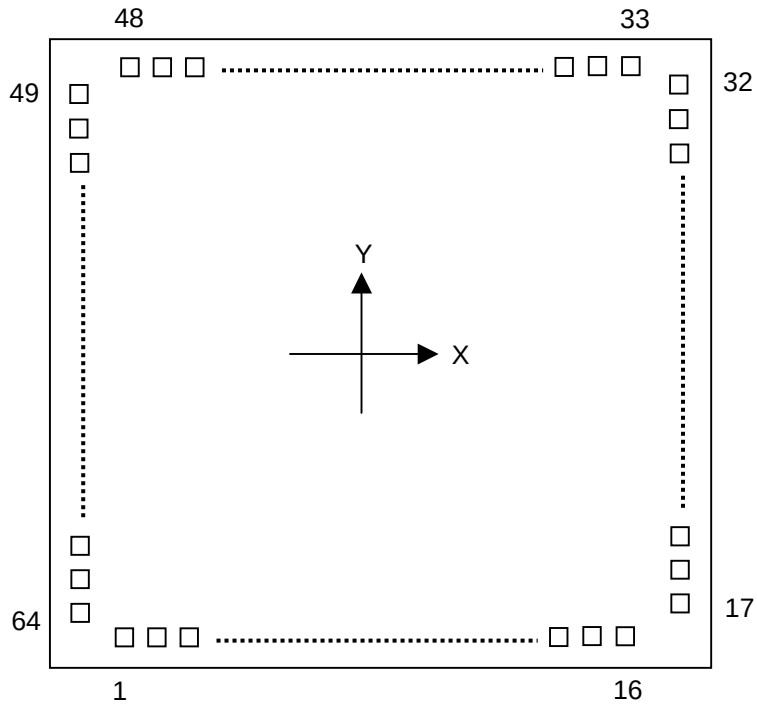
■ FEATURES

- 50 Segment Drivers
- Duty Ratio 1/4 (Up to 200-Segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip (External Resistance Required)
- Display Off Function (INHb Terminal)
- Operating Voltage 2.4 to 5.5V
- LCD Driving Voltage 6.5V Max.
- Package Outline Chip, QFP64-H1
- C-MOS Technology

■ BLOCK DIAGRAM



■ PAD LOCATION



Chip Center : X=0μm, Y=0μm
Chip Size : X=3.20 mm, Y=3.20 mm
Chip Thickness : 400 μm
PAD Size : X=99.2 μm, Y=99.2 μm
PAD Pitch : 171.2 μm

■ PAD COORDINATES

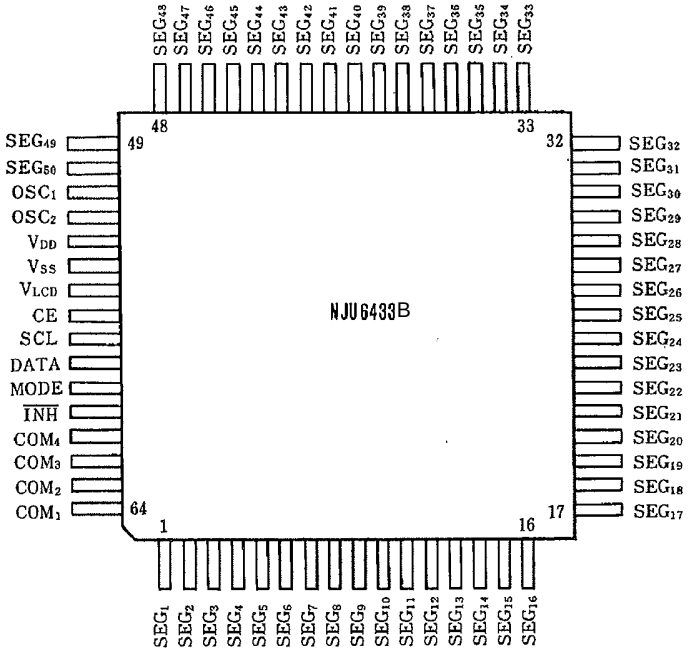
Chip Size 3.20 x 3.20 mm(Chip Center X=0μm, Y=0μm)

PAD No.	Terminal	X= μm	Y= μm
1	SEG_1	-1279	-1437
2	SEG_2	-1107	-1437
3	SEG_3	-936	-1437
4	SEG_4	-765	-1437
5	SEG_5	-594	-1437
6	SEG_6	-423	-1437
7	SEG_7	-251	-1437
8	SEG_8	-80	-1437
9	SEG_9	91	-1437
10	SEG_{10}	262	-1437
11	SEG_{11}	433	-1437
12	SEG_{12}	605	-1437
13	SEG_{13}	776	-1437
14	SEG_{14}	947	-1437
15	SEG_{15}	1118	-1437
16	SEG_{16}	1289	-1437
17	SEG_{17}	1437	-1288
18	SEG_{18}	1437	-1117
19	SEG_{19}	1437	-946
20	SEG_{20}	1437	-775
21	SEG_{21}	1437	-603
22	SEG_{22}	1437	-432
23	SEG_{23}	1437	-261
24	SEG_{24}	1437	-90

PAD No.	Terminal	X= μm	Y= μm
25	SEG_{25}	1437	81
26	SEG_{26}	1437	253
27	SEG_{27}	1437	424
28	SEG_{28}	1437	595
29	SEG_{29}	1437	766
30	SEG_{30}	1437	937
31	SEG_{31}	1437	1109
32	SEG_{32}	1437	1280
33	SEG_{33}	1280	1437
34	SEG_{34}	1109	1437
35	SEG_{35}	937	1437
36	SEG_{36}	766	1437
37	SEG_{37}	595	1437
38	SEG_{38}	424	1437
39	SEG_{39}	253	1437
40	SEG_{40}	81	1437
41	SEG_{41}	-90	1437
42	SEG_{42}	-261	1437
43	SEG_{43}	-432	1437
44	SEG_{44}	-603	1437
45	SEG_{45}	-775	1437
46	SEG_{46}	-946	1437
47	SEG_{47}	-1117	1437
48	SEG_{48}	-1288	1437

PAD No.	Terminal	X= μm	Y= μm
49	SEG_{49}	-1437	1280
50	SEG_{50}	-1437	1109
51	OSC_1	-1437	937
52	OSC_2	-1437	766
53	V_{DD}	-1437	595
54	V_{SS}	-1437	424
55	V_{LCD}	-1437	253
56	CE	-1437	81
57	SCL	-1437	-90
58	DATA	-1437	-261
59	MODE	-1437	-432
60	INHX	-1437	-603
61	COM_4	-1437	-775
62	COM_3	-1437	-946
63	COM_2	-1437	-1117
64	COM_1	-1437	-1288

■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION
1~50	SEG_1~SEG_{50}	LCD Segment Output Terminals
61~64	COM_4~COM_1	LCD Common Output Terminals
51 52	OSC_1 OSC_2	Oscillation Terminals : External resistance is connected to these terminals.
53	V_{DD}	Power Supply (+5V)
54	V_{SS}	Power Supply (0V)
55	V_{LCD}	Power Supply for LCD Driving The relation : $1.3V_{DD} \geq \lvert V_{DD} - V_{LCD} \rvert$, $V_{SS} \geq V_{LCD}$ must be maintained.
56	CE	Chip Enable Signal Input Terminal : "H" : LCD display data and mode setting data input "L" : Disable Fall Edge : LCD display data latch
57	SCL	Serial Data Transmission Clock Input Terminal : LCD display and Mode setting data are input synchronized SCL clock signal rise edge.
58	DATA	Serial Data Input Terminal Data input timing : SCL clock rise edge
59	MODE	Data or Mode Select Terminal "H" : Data input mode "L" : LCD display data input mode (Refer the mode setting table for mode setting contents)
60	INHb	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-On "L" : Display-Off

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

The oscillation circuit operates by connecting external resistance (capacitance is incorporated). This circuit provides the clock signal to both common and segment drivers.

(1-2) Divider Circuit

This circuit divides the oscillating signal to generate the common and segment timing.

(1-3) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-4) Latch Circuit and Segment Driver

When the CE signal falling, the display data is latched, and the data controls the segment signal of display-on/off.

(1-5) Common Driver

The Common driver generates driving waveform to common terminal.

(1-6) Reset Circuit

The Reset circuit is type of detectable voltage. It resets internal circuit when the power turns on.

(2) Mode Setting

The mode setting is composed of 4-bit, and selects the shift register that writes the display data by writing data in the mode setting register. (Refer to "(4) Data Input Timing" for details.)

When the data (1,1,1,1) is input, “0” (All Display-off) is written in all shift registers.

The mode setting register is selected by CE="H" and MODE="H". The data is latched at the rising edge of the SCL, and selected at falling edge of the CE.

Table 1. Mode Setting Table

Mode	Data	Description
1	(MSB) 1,0,0,0 (LSB)	Shift register 1 is selected.
2	0,1,0,0	Shift register 2 is selected.
3	1,1,0,0	Shift register 3 is selected.
4	0,0,1,0	Shift register 4 is selected.
5	1,0,1,0	All Shift register (1~4) is selected, and data is written continuously.
F	1,1,1,1	All shift register is “0”.

(3) Correspondence of the transfer data and output terminal

The display data is written by CE="H" and MODE="L". The data is latched at the rising edge of the SCL, and written at falling edge of the CE.

The correspondence of the data and the output terminals is as follows.

Output Terminal	COM_1	COM_2	COM_3	COM_4
SEG_1	D1	D2	D3	D4
SEG_2	D5	D6	D7	D8
SEG_3	D9	D10	D11	D12
SEG_4	D13	D14	D15	D16
SEG_5	D17	D18	D19	D20
SEG_6	D21	D22	D23	D24
SEG_7	D25	D26	D27	D28
SEG_8	D29	D30	D31	D32
SEG_9	D33	D34	D35	D36
SEG_{10}	D37	D38	D39	D40
SEG_{11}	D41	D42	D43	D44
SEG_{12}	D45	D46	D47	D48
SEG_{13}	D49	D50	D51	D52
SEG_{14}	D53	D54	D55	D56
SEG_{15}	D57	D58	D59	D60
SEG_{16}	D61	D62	D63	D64
SEG_{17}	D65	D66	D67	D68
SEG_{18}	D69	D70	D71	D72
SEG_{19}	D73	D74	D75	D76
SEG_{20}	D77	D78	D79	D80
SEG_{21}	D81	D82	D83	D84
SEG_{22}	D85	D86	D87	D88
SEG_{23}	D89	D90	D91	D92
SEG_{24}	D93	D94	D95	D96
SEG_{25}	D97	D98	D99	D100

Output Terminal	COM_1	COM_2	COM_3	COM_4
SEG_{26}	D101	D102	D103	D104
SEG_{27}	D105	D106	D107	D108
SEG_{28}	D109	D110	D111	D112
SEG_{29}	D113	D114	D115	D116
SEG_{30}	D117	D118	D119	D120
SEG_{31}	D121	D122	D123	D124
SEG_{32}	D125	D126	D127	D128
SEG_{33}	D129	D130	D131	D132
SEG_{34}	D133	D134	D135	D136
SEG_{35}	D137	D138	D139	D140
SEG_{36}	D141	D142	D143	D144
SEG_{37}	D145	D146	D147	D148
SEG_{38}	D149	D150	D151	D152
SEG_{39}	D153	D154	D155	D156
SEG_{40}	D157	D158	D159	D160
SEG_{41}	D161	D162	D163	D164
SEG_{42}	D165	D166	D167	D168
SEG_{43}	D169	D170	D171	D172
SEG_{44}	D173	D174	D175	D176
SEG_{45}	D177	D178	D179	D180
SEG_{46}	D181	D182	D183	D184
SEG_{47}	D185	D186	D187	D188
SEG_{48}	D189	D190	D191	D192
SEG_{49}	D193	D194	D195	D196
SEG_{50}	D197	D198	D199	D200

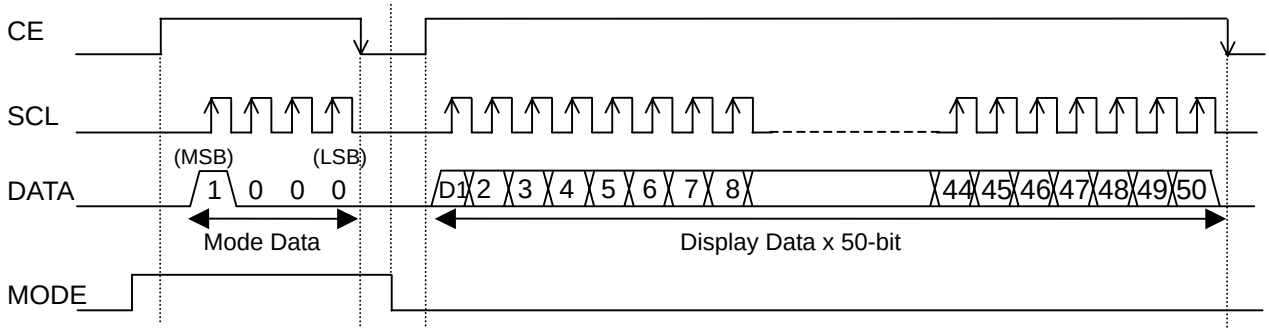
Correspondence of the transfer data and Segment Status

Transfer Data	Segment Status
”H”	ON
”L”	OFF

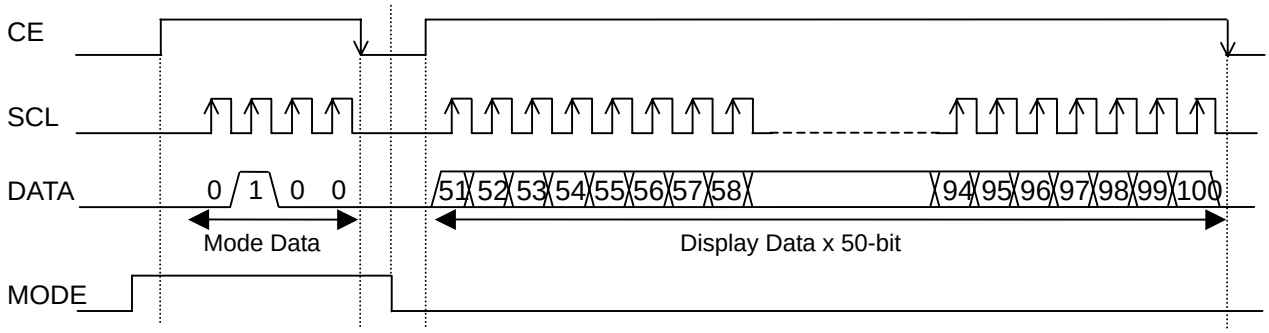
(4) Data Input Timing

The format of data is as follows. The mode data is input by 4-bit of MSB first, and after the shift register is selected, the display data is written

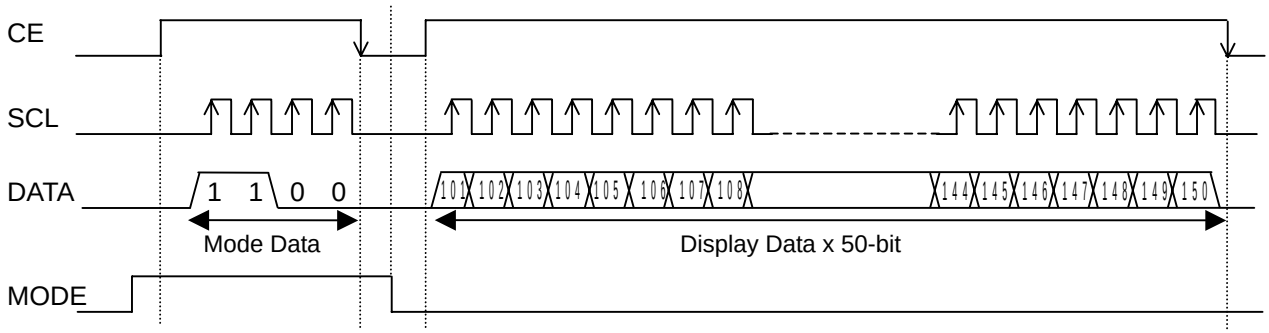
- Mode 1 : Shift Register 1 (D1~D50)



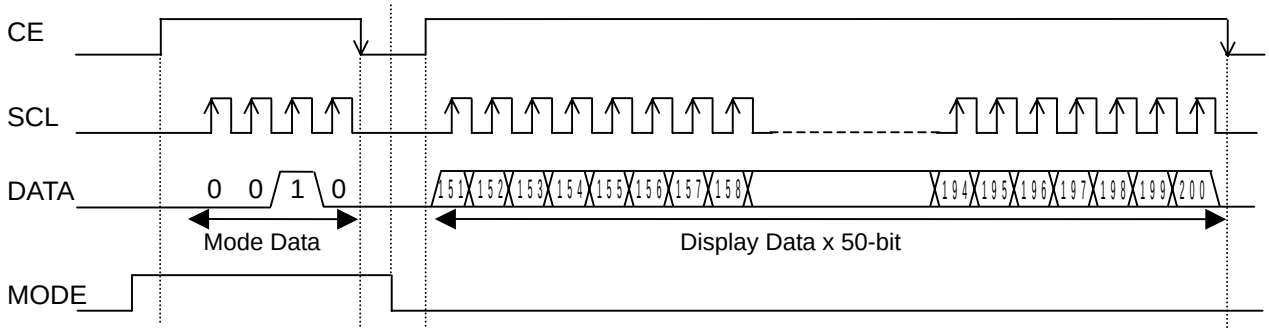
- Mode 2 : Shift Register 2 (D51~D100)



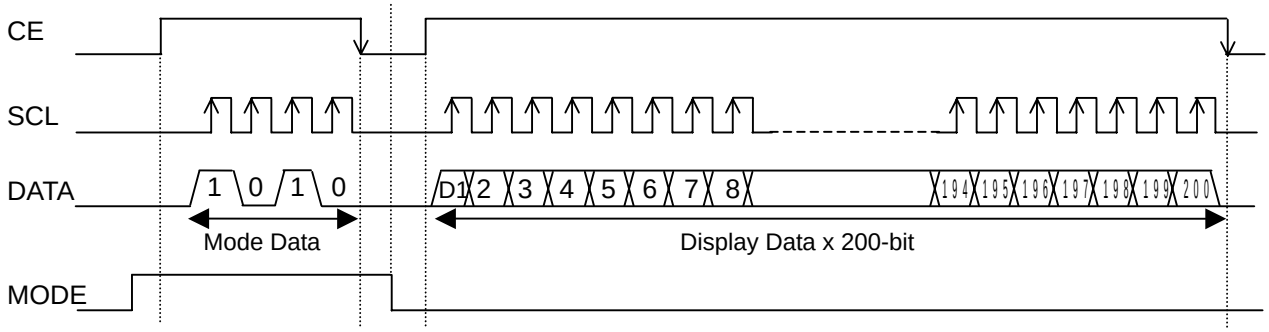
- Mode 3 : Shift Register 3 (D101~D150)



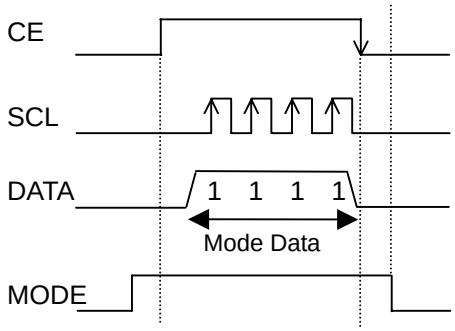
- Mode 4 : Shift Register 4 (D151~D200)



- Mode 5 : Shift Register 1~4 (D1~D200)



- Mode F : Shift Register 1~4 all “0”



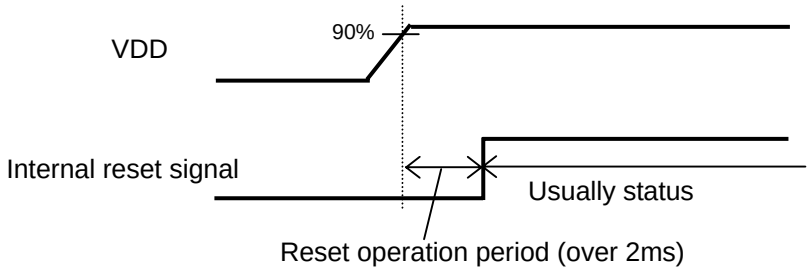
Note 1) All of display data should be transmitted within 30ms to keep the display quality, because huge display data D1 to D200 are transmitted at 4 times totally.
Note 2) Data is latched at the rising edge of the SCL.
Note 3) Mode data and display data are executed at the falling edge of the CE.
Note 4) In case of less than 4-bit data, the mode data remains the LSB side of the previous mode data.
Note 5) In case of over 4-bit data, the mode data is valid the previous 4-bit of the falling edge of the CE.
Note 6) In case of less than 50-bit data, the display data remains the last part of the previous display data.
Note 7) In case of over 50-bit data, the display data is valid the previous 50-bit of the falling edge of the CE.

(5) Initialization by Power On Reset

The **NJU6433B** incorporates the reset circuit of the detectable voltage type, and when the power supply is turned on, it automatically initializes it (reset). When the VDD becomes 90% of the working voltage, the reset signal is generated internally. Reset is completed after 2ms, and it becomes usually status. The serial data is able to transmit after completed reset.

(5-1) Status of Power On Reset

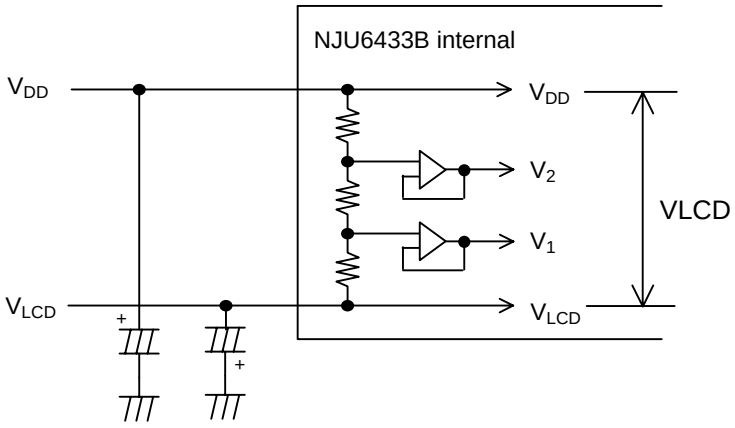
1. Mode setting release (nonselective status)
2. Shift register : all “0”
3. Latch circuit : all “0”



(6) LCD Panel Drive

(6-1) LCD driving volyage generation circuit

The LCD driving voltage generation circuit generates LCD driving bias voltages V1 and V2 from input voltage VDD-VLCD. It is generated by the bleeder resistance in IC, and after impedance is converted by the voltage follower, it is supplied to the LCD driving circuit. The VDD and VLCD terminal requires external capacitors for bias voltage stabilization for display quality as shown in below.



■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Operating Voltage (1)	V_{DDmax}	V_{DD} Terminal, Ta=25°C	-0.3~+7.0	V
Operating Voltage (2)	V_{LCD}		V_{DD}-6.5~V_{SS}	V
Input Voltage (1)	$V_{1(1)}$	CE, SCL, DATA, MODE, INHb Terminals Ta=25°C	-0.3~+7.0	V
Input Voltage (2)	$V_{1(2)}$	OSC_1, OSC_2 Terminals	-0.3~V_{DD}+0.3	V
Output Voltage	V_0	OSC_1, OSC_2 Terminals	-0.3~V_{DD}+0.3	V
Output Current (1)	$I_{O(1)}$	SEG_1~SEG_{50} Terminals	100	uA
Output Current (2)	$I_{O(2)}$	COM_1~COM_4 Terminals	1.0	mA
Power Dissipation	P_{Dmax}	Ta=85°C	300	mW
Operating Temperature	T_{opr}		-30~+85	°C
Storage Temperature	T_{stg}		-40~+125	°C

Note 1) All voltage values are specified as V_{SS} = 0V.

Note 2) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 3) The relation $V_{DD} > V_{SS} \geq V_{LCD}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the LSI.

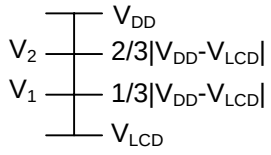
■ ELECTRICAL CHARACTERISTICS

- DC Characteristics

(V_{DD}=5V±10%, V_{LCD}=V_{DD}-6.5V, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	V_{DD}	V_{DD} Terminal		2.4	5.0	5.5	V	
Operating Voltage (2)	V_{LCD}	V_{LCD} Terminal		V_{SS}		V_{DD}-6.5	V	
"H" Input Voltage	V_{IH}	CE, SCL, DATA, MODE, INHb		0.7V_{DD}		V_{DD}	V	
"L" Input Voltage	V_{IL}			V_{SS}		0.3V_{DD}	V	
"H" Input Current	V_{IH}	CE,SCL, DATA,MODE, INHb	V_I =V_{DD}			5	uA	
"L" Input Current	V_{IL}		V_I =V_{SS}			5	uA	
"H" Output Voltage (1)	$V_{OH(1)}$	SEG_1~SEG_{50}	I_O=-10uA	V_{DD}-1.0			V	
"L" Output Voltage (1)	$V_{OL(1)}$		I_O=+10uA			V_{LCD}+1.0	V	
Middle Level Voltage 1/3(1)	$V_{MS1/3}$	SEG_1~SEG_{50}	I_O=±10uA	V_1-1.0	V_1	V_1+1.0	V	1
Middle Level Voltage 2/3(1)	$V_{MS2/3}$		I_O=±10uA	V_2-1.0	V_2	V_2+1.0	V	
"H" Output Voltage (2)	$V_{OH(2)}$	COM_1~COM_4	I_O=-100uA	V_{DD}-0.6			V	
"L" Output Voltage (2)	$V_{OL(2)}$		I_O=+100uA			V_{LCD}+0.6	V	
Middle Level Voltage 1/3(2)	$V_{MC1/3}$	COM_1~COM_4	I_O=±100uA	V_1-0.6	V_1	V_1+0.6	V	1
Middle Level Voltage 2/3(2)	$V_{MC2/3}$		I_O=±100uA	V_2-0.6	V_2	V_2+0.6	V	
Oscillating Frequency Range	f_{RNG}	OSC_1, OSC_2 Terminals		25		200	kHz	
Oscillating Frequency	f_{OSC}	OSC_1, OSC_2 Terminals R=140kΩ, V_{DD}=5V		115	130	145	kHz	
Operating Current (1)	I_{SS}	V_{SS} Terminal, V_{DD}=5V			50	80	uA	
Operating Current (2)	I_{LCD}	V_{LCD} Terminal, V_{DD}=5V, V_{LCD}=V_{DD}-6.5V			15	25	uA	
Hysteresis Voltage	V_H	CE, SCL, DATA, MODE, INHb V_{DD}=5V		0.3			V	

Note 1) V_1=1/3|V_{DD}-V_{LCD}|, V_2=2/3|V_{DD}-V_{LCD}|

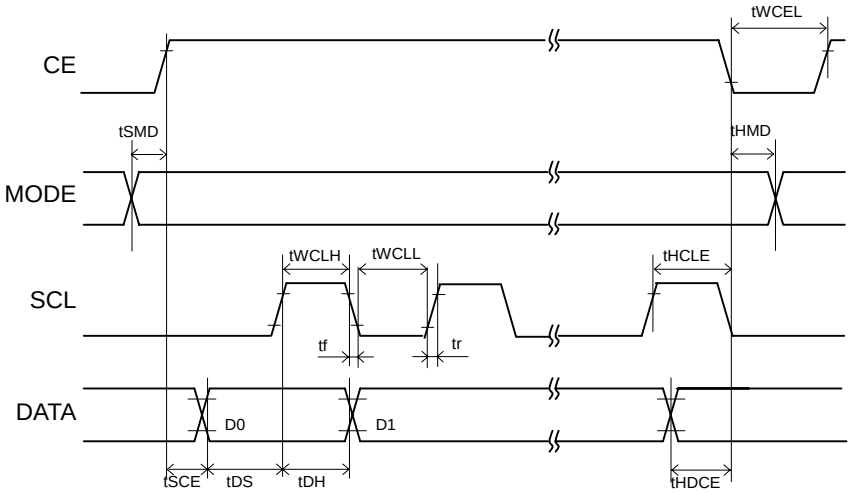


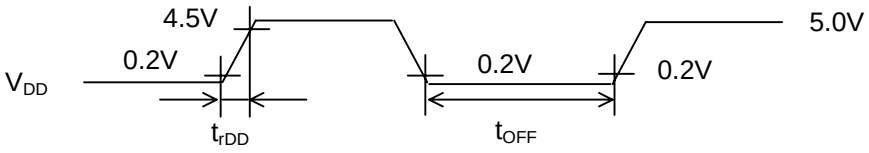
- AC Characteristics

(V_{DD}=5V±10%, Ta=25°C)

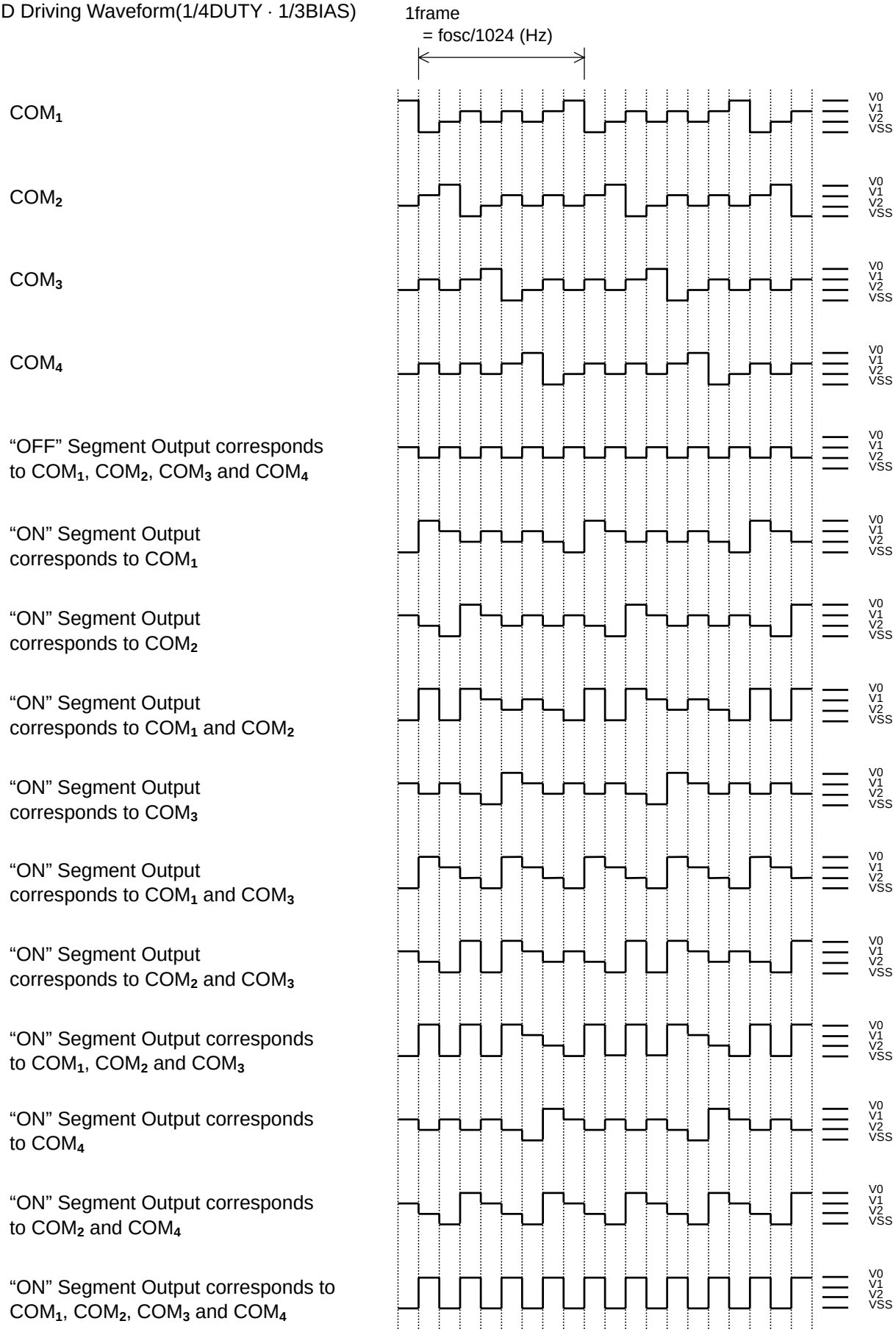
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL	0.25			us
"H" Clock Pulse Width	t_{WCLH}	SCL	0.25			us
DATA Set-up Time	t_{DS}	SCL, DATA	0.25			us
DATA Hold Time	t_{DH}	SCL, DATA	0.25			us
CE Set-up Time	t_{SCE}	CE, DATA	1.0			us
CE Hold Time (1)	t_{HDCE}	CE, DATA	1.0			us
CE Hold Time (2)	t_{HCLE}	CE, SCL	1.25			us
MODE Set-up Time	t_{SMD}	MODE, CE	0.25			us
MODE Hold Time	t_{HMD}	MODE, CE	0.25			us
"L" Chip Enable Pulse Width	t_{WCEL}	CE	4.0			us
Power Supply Rise Time	t_{rDD}	V_{DD}	0.1		10	ms
Power Supply OFF Time	t_{OFF}	V_{DD}	1			ms

- Input Timing Characteristics



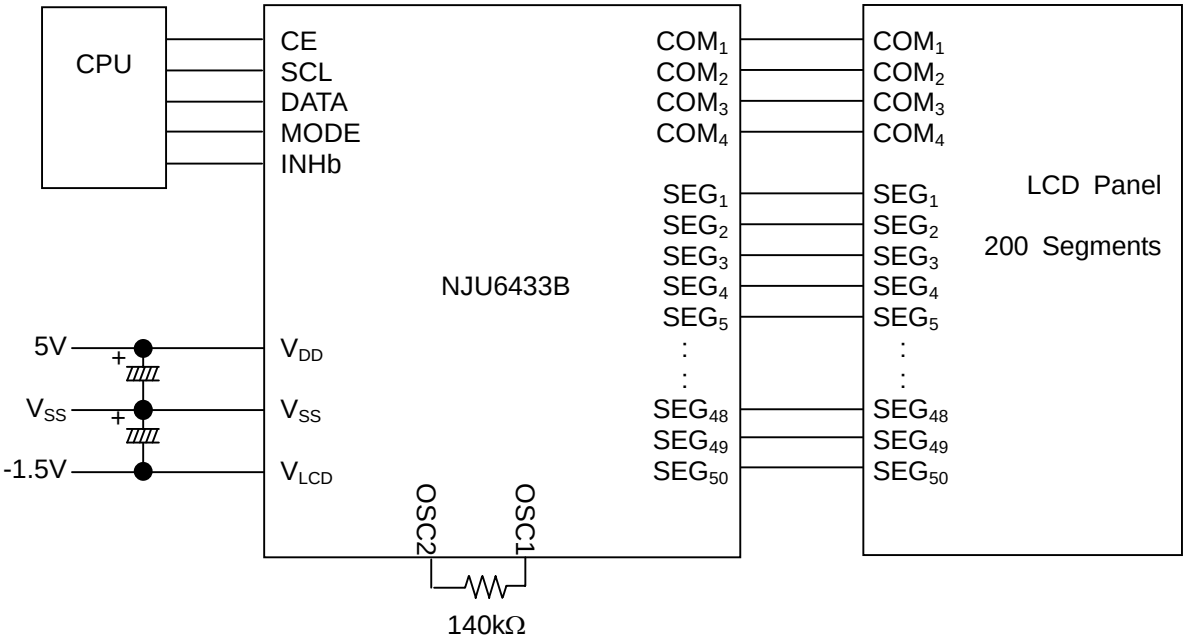


- LCD Driving Waveform(1/4DUTY · 1/3BIAS)

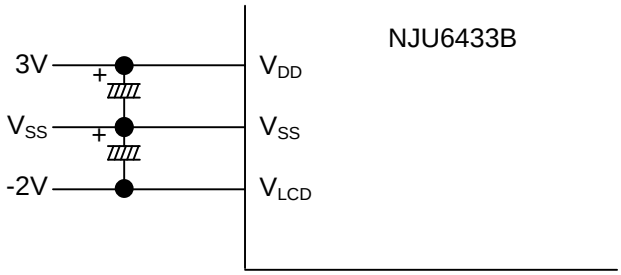


■ APPLICATION CIRCUIT

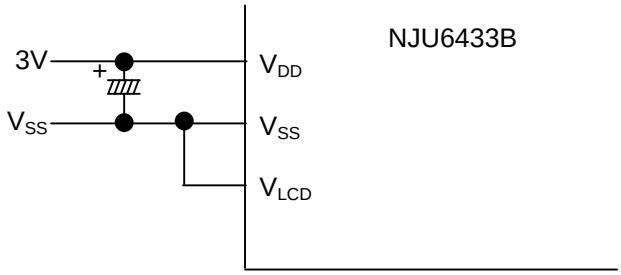
Example) VDD=5V, VLCD=6.5V



Example) VDD=3V, VLCD=5V



Example) VDD=3V, VLCD=3V



[CAUTION]
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