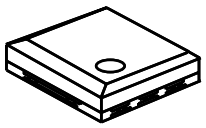
X SPDT SWITCH GaAs MMIC

■ GENERAL DESCRIPTION

The NJG1642HE3 is a GaAs X (Cross) SPDT switch MMIC. This is suitable for the application of selecting one circuit with two ports such as balanced type circuit from among two circuits with two ports. This switch features low insertion loss, high isolation, and wide frequency coverage from 50MHz to 3GHz at low control voltage of 1.85 V. The ultra-small and ultra-thin USB12 package is adopted.

■ PACKAGE OUTLINE

NJG1642HE3

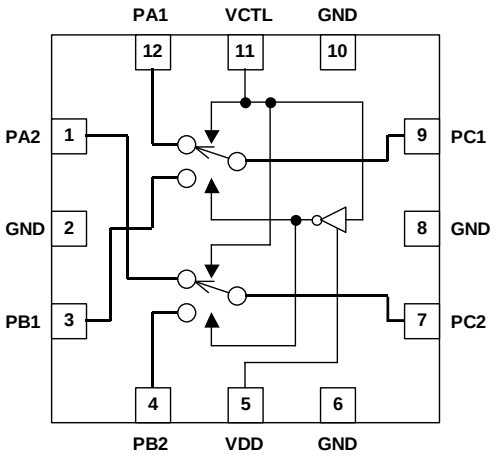


■ FEATURES

● Low voltage operation	V_{DD}=+2.0~+5.0V
● Low voltage Logic control	V_{CTL}(H)=+1.7~V_{DD}
● Low insertion loss	0.3dB typ. @f=1.0GHz, P_{IN}=0dBm, each switch, V_{DD}=2.7V
	0.4dB typ. @f=2.0GHz, P_{IN}=0dBm, each switch, V_{DD}=2.7V
	0.55dB typ. @f=3.0GHz, P_{IN}=0dBm, each switch, V_{DD}=2.7V
● High isolation	28dB typ. @f=2.0GHz, PC1-PC2 P_{IN}=0dBm, V_{DD}=2.7V
	27dB typ. @f=1.0GHz, P_{IN}=0dBm, V_{DD}=2.7V PC1-PA1, PC2-PA2, PC1-PB1, PC2-PB2
	21dB typ. @f=2.0GHz, P_{IN}=0dBm, V_{DD}=2.7V PC1-PA1, PC2-PA2, PC1-PB1, PC2-PB2
● Operating current consumption	16uA typ. @f=1.0GHz, P_{IN}=0dBm, V_{DD}=2.7V
● Control current consumption	8uA typ. @f=1.0GHz, P_{IN}=0dBm, V_{DD}=2.7V
● Ultra-small & ultra-thin package	USB12-E3 (Package size: 2.35x2.35x0.75mm)

■ PIN CONFIGURATION

USB12Type (Top View)



Pin connection
1. PA2
2. GND
3. PB1
4. PB2
5. VDD
6. GND
7. PC2
8. GND
9. PC1
10. GND
11. VCTL
12. PA1

■ TRUTH TABLE

"H"=VCTL(H), "L"=VCTL(L)

ON PATH	VCTL
PC1-PA1,PC2-PA2	H
PC1-PB1,PC2-PB2	L

X SPDT Switch : Switch that output port of two SPDT switches crosses internally.

NOTE: Please note that any information on this catalog will be subject to change.

■ ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C, Z_s=Z_l=50Ω)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	P_{IN}	V_{DD} =2.7V, VCTL=0V/1.85V PC1,PC2,PA1,PA2,PB1,PB2	28	dBm
Supply Voltage	V_{DD}	VDD terminal	5.0	V
Control Voltage	V_{CTL}	VCTL terminal	5.0	V
Power Dissipation	P_D		250	mW
Operating Temp.	T_{opr}		-40~+85	°C
Storage Temp.	T_{stg}		-55~+150	°C

■ ELECTRICAL CHARACTERISTICS 1

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, VCTL(L)=0V, VCTL(H)=1.85V)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Current	I_{DD}	P_{IN}=0dBm	-	16	30	uA
Supply Voltage	V_{DD}		2.0	2.7	5.0	V
Control Voltage (LOW)	V_{CTL}(L)		0	-	0.4	V
Control Voltage (HIGH)	V_{CTL}(H)		1.7	1.85	V_{DD}	V
Control Current	I_{CTL}	f=1.0GHz, P_{IN}=0dBm	-	8	15	uA
Insertion Loss 1	LOSS1	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 ON f=1.0GHz, P_{IN}=0dBm	-	0.3	0.55	dB
Insertion Loss 2	LOSS2	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 ON f=2.0GHz, P_{IN}=0dBm	-	0.4	0.65	dB
Insertion Loss 3	LOSS3	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 ON f=3.0GHz, P_{IN}=0dBm	-	0.55	0.9	dB
Isolation 1	ISL1	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 OFF f=1.0GHz, P_{IN}=0dBm	24	27	-	dB
Isolation 2	ISL2	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 OFF f=2.0GHz, P_{IN}=0dBm	18	21	-	dB
Isolation 3	ISL3	PC1-PA1, PC2-PA2 PC1-PB1, PC2-PB2 OFF f=3.0GHz, P_{IN}=0dBm	15	17	-	dB
Isolation 4	ISL4	PA1, PA2, PB1, PB2 port 50Ω terminated, PC1-PC2 port f=2.0GHz, P_{IN}=0dBm	24	28	-	dB

■ ELECTRICAL CHARACTERISTICS 2

(General conditions: T_a=+25°C, Z_s=Z_l=50Ω, V_{DD}=2.7V, VCTL(L)=0V, VCTL(H)=1.85V)

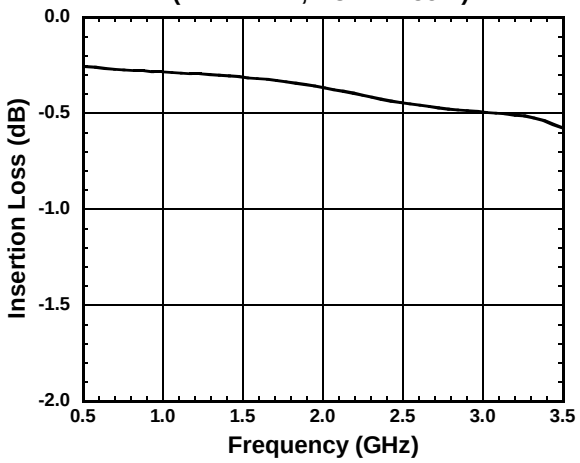
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input power at 0.2dB Compression Point	$P_{-0.2dB}$	f=2.0GHz	20	24	-	dBm
VSWR	$VSWR_i$	on-state ports, f=0.9GHz	-	1.2	1.4	
Switching time	T_{SW}	f=0.1~3 GHz	-	1.5	5.0	μs

■ TERMINAL INFORMATION

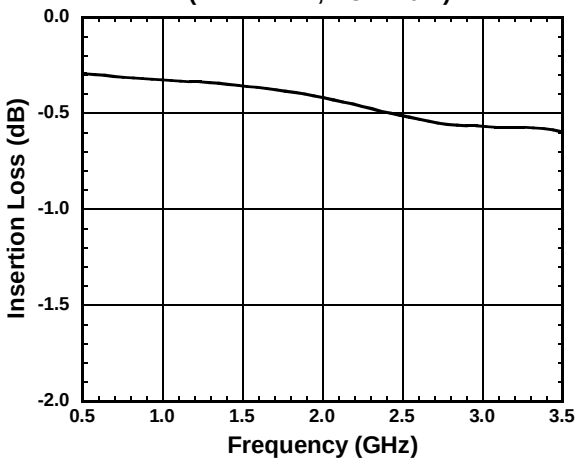
No.	SYMBOL	DESCRIPTION
1	PA2	RF port. This port is connected with PC2 port by controlling 11pin-VCTL(H) (+1.7~V_{DD}). In order to block the DC bias voltage of internal circuit, an external capacitor is required.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	PB1	RF port. This port is connected with PC1 port by controlling 11pin-VCTL(L) (0~+0.4V). In order to block the DC bias voltage of internal circuit, an external capacitor is required.
4	PB2	RF port. This port is connected with PC2 port by controlling 11pin-VCTL(L) (0~+0.4V). In order to block the DC bias voltage of internal circuit, an external capac is required.
5	VDD	Positive voltage supply terminal. The positive voltage (+2.0~+5.0V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
6	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
7	PC2	Common RF port PC2. In order to block the DC bias voltage of internal circuit, an external capacitor is required.
8	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
9	PC1	Common RF port PC1. In order to block the DC bias voltage of internal circuit, an external capacitor is required.
10	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
11	VCTL	Control signal input terminal. This terminal is set to High-Level (+1.7V~V_{DD}) or Low-Level (0~+0.4V).
12	PA1	RF port. This port is connected with PC1 port by controlling 11pin-VCTL(H) (+1.7~V_{DD}). In order to block the DC bias voltage of internal circuit, an external capacitor is required.

■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

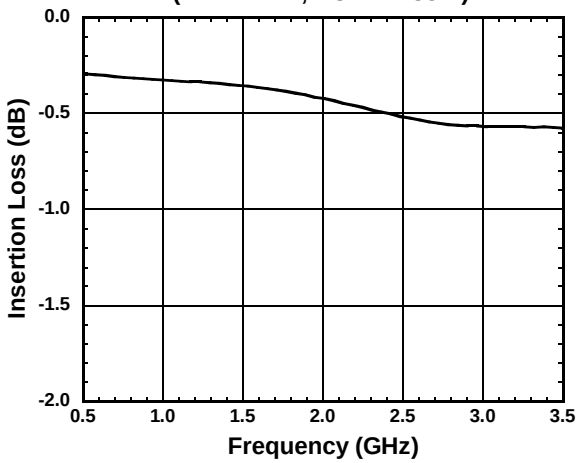
PC1-PA1 Insetion Loss vs. Frequency
(VDD=2.7V, VCTL=1.85V)



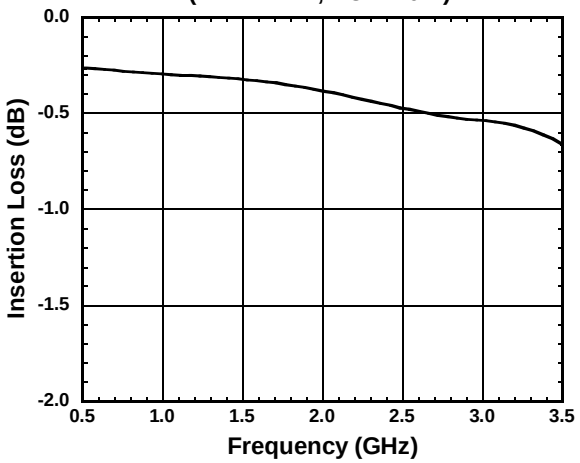
PC1-PB1 Insetion Loss vs. Frequency
(VDD=2.7V, VCTL=0V)



PC2-PA2 Insetion Loss vs. Frequency
(VDD=2.7V, VCTL=1.85V)



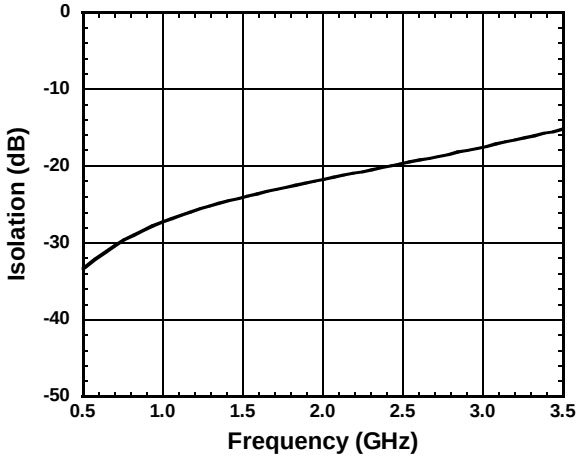
PC2-PA2 Insetion Loss vs. Frequency
(VDD=2.7V, VCTL=0V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

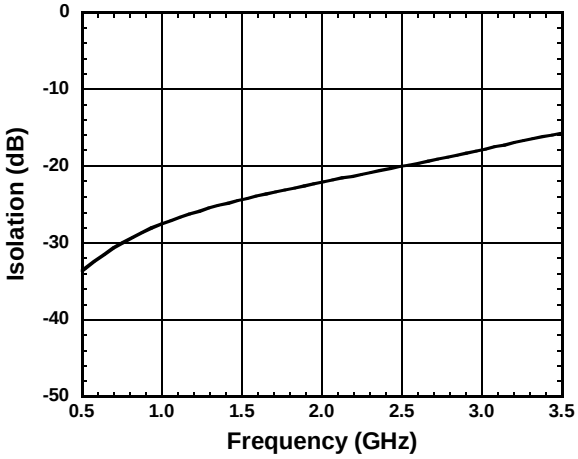
PC1-PA1 Isolation vs. Frequency

(VDD=2.7V, VCTL=0V)



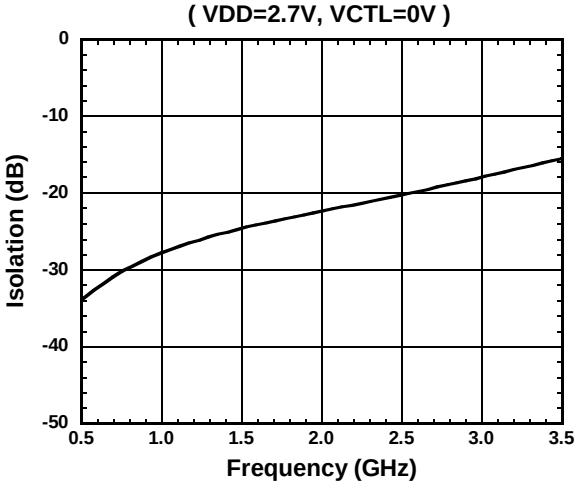
PC1-PB1 Isolation vs. Frequency

(VDD=2.7V, VCTL=1.85V)



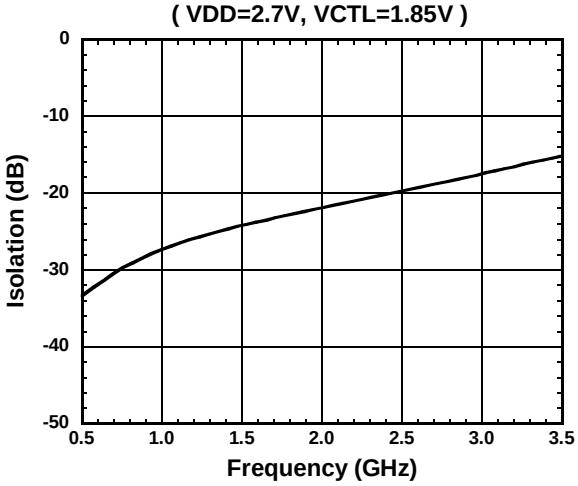
PC2-PA2 Isolation vs. Frequency

(VDD=2.7V, VCTL=0V)



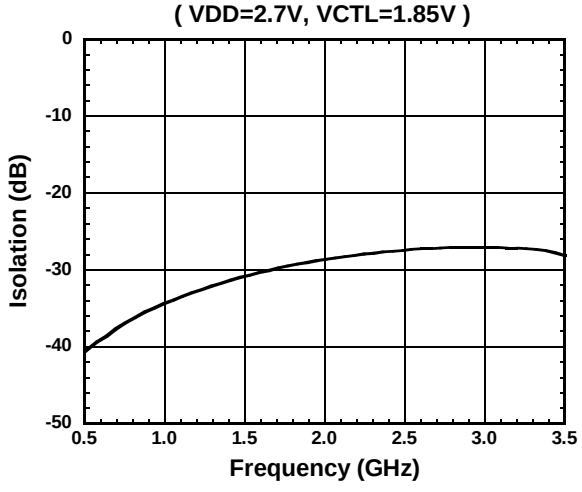
PC2-PB2 Isolation vs. Frequency

(VDD=2.7V, VCTL=1.85V)



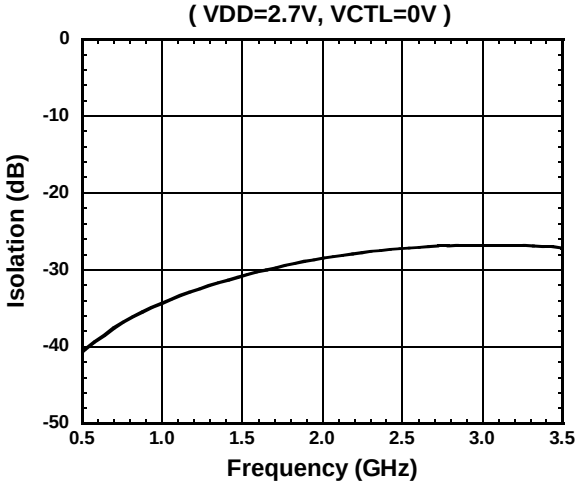
PC1-PC2 Isolation vs. Frequency

(VDD=2.7V, VCTL=1.85V)



PC1-PC2 Isolation vs. Frequency

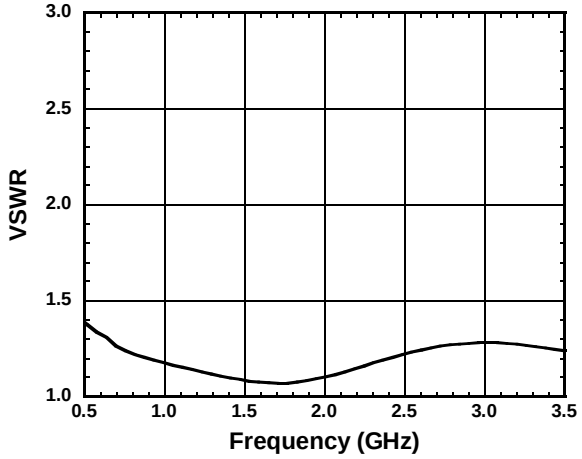
(VDD=2.7V, VCTL=0V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

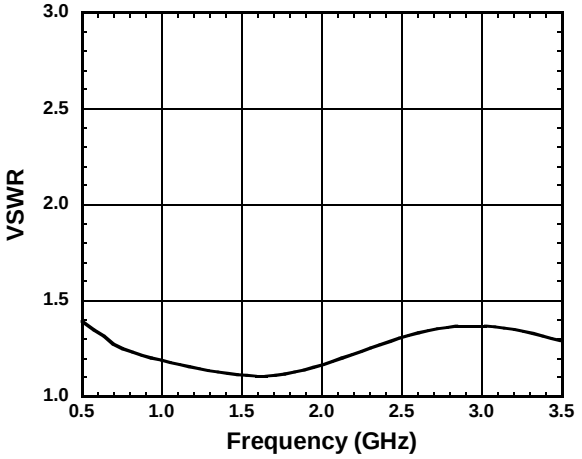
PA1 VSWR vs. Frequency

(VDD=2.7V, VCTL=1.85V)



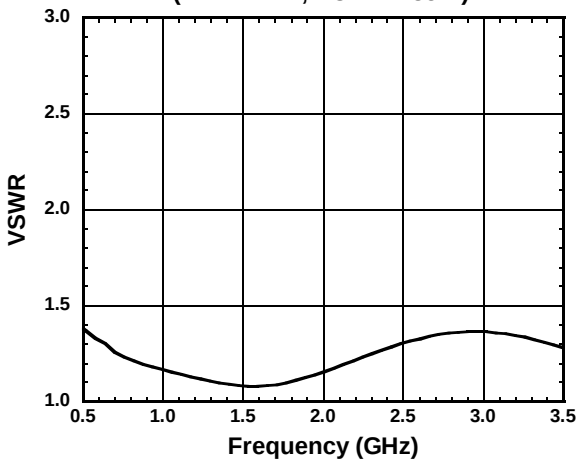
PB1 VSWR vs. Frequency

(VDD=2.7V, VCTL=0V)



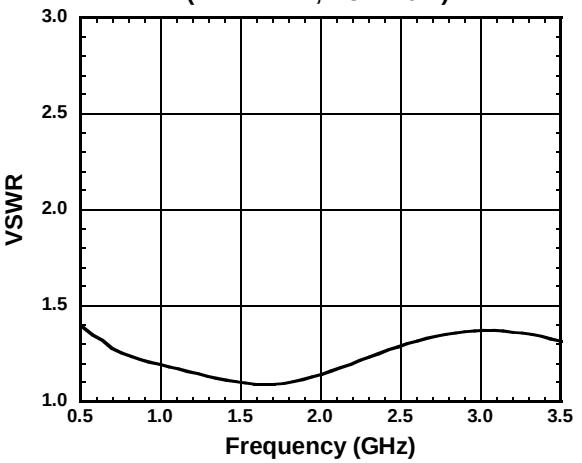
PA2 VSWR vs. Frequency

(VDD=2.7V, VCTL=1.85V)

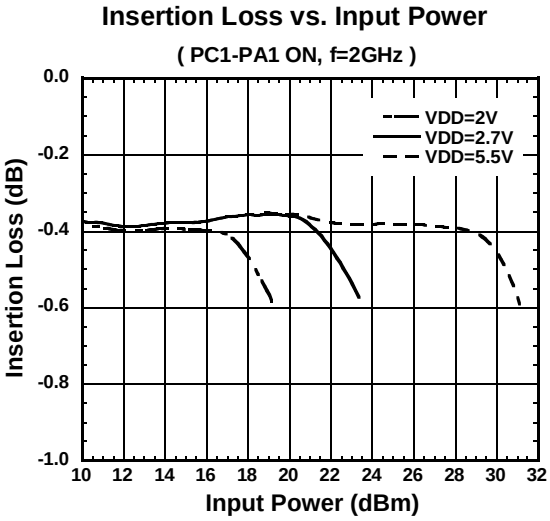


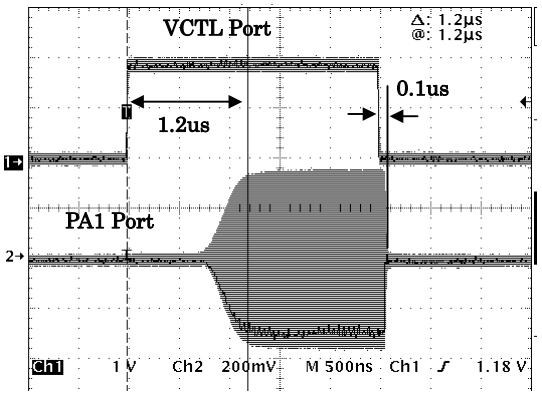
PB2 VSWR vs. Frequency

(VDD=2.7V, VCTL=0V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

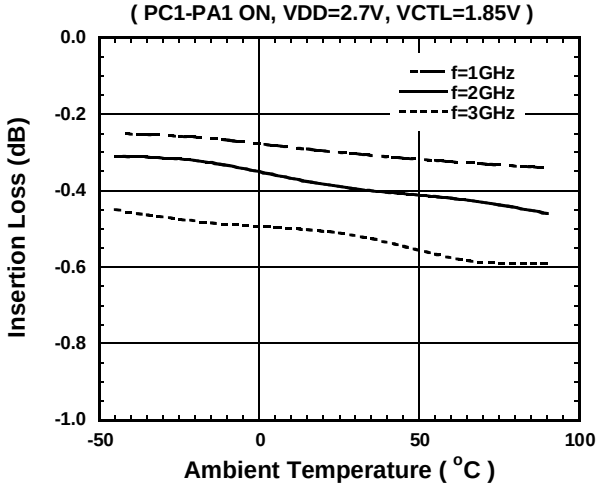




■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

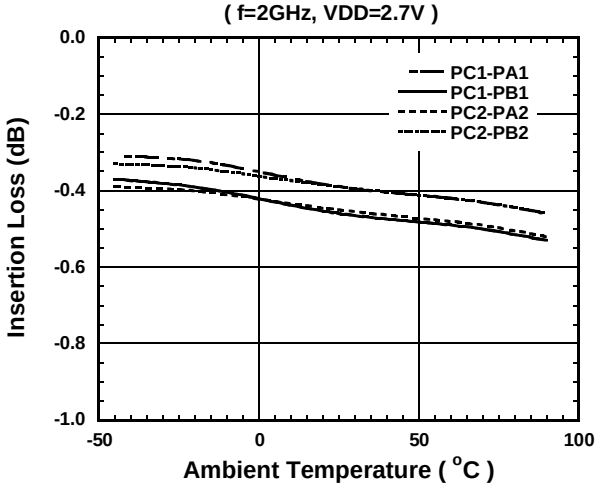
Insertion Loss vs. Ambient Temperature

(PC1-PA1 ON, VDD=2.7V, VCTL=1.85V)



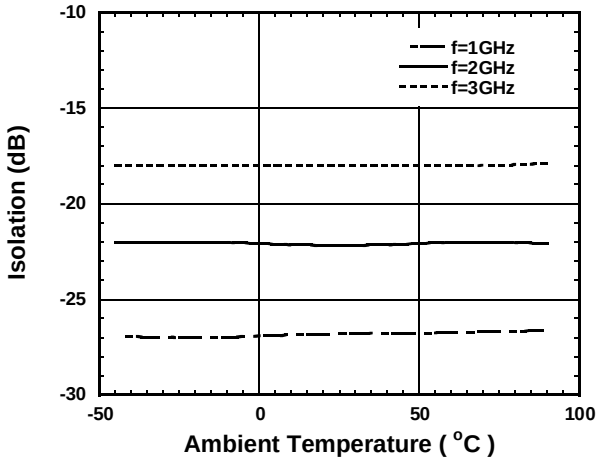
Insertion Loss vs. Ambient Temperature

(f=2GHz, VDD=2.7V)



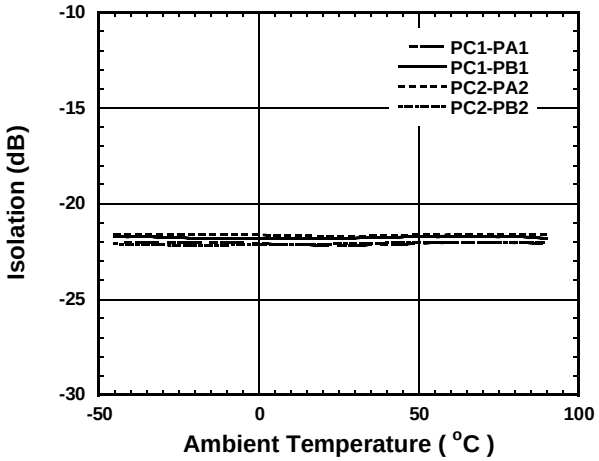
Isolation vs. Ambient Temperature

(PC1-PA1 ON, VDD=2.7V, VCTL=0V)



Isolation vs. Ambient Temperature

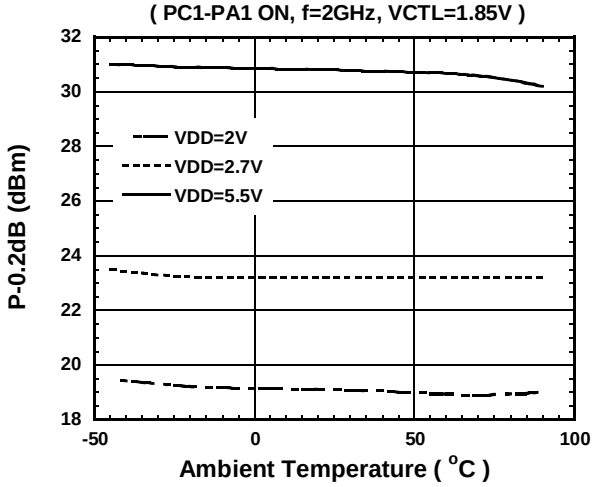
(f=2GHz, VDD=2.7V)



■ **ELECTRICAL CHARACTERISTICS** (With Application circuit, Loss of external circuit are excluded)

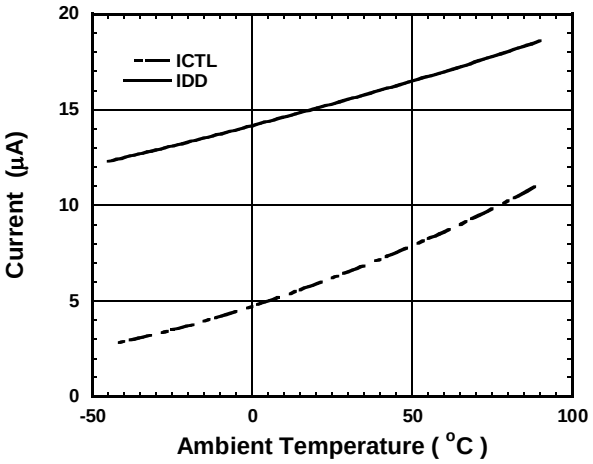
P-0.2dB vs. Ambient Temperature

(PC1-PA1 ON, f=2GHz, VCTL=1.85V)



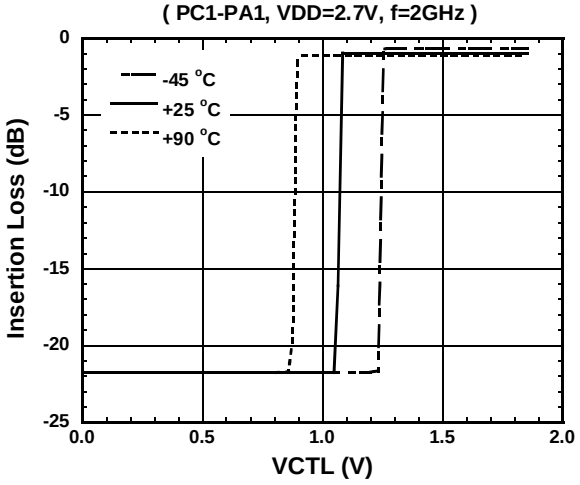
Current vs. Ambient Temperature

(VDD=2.7V, VCTL=1.85V)

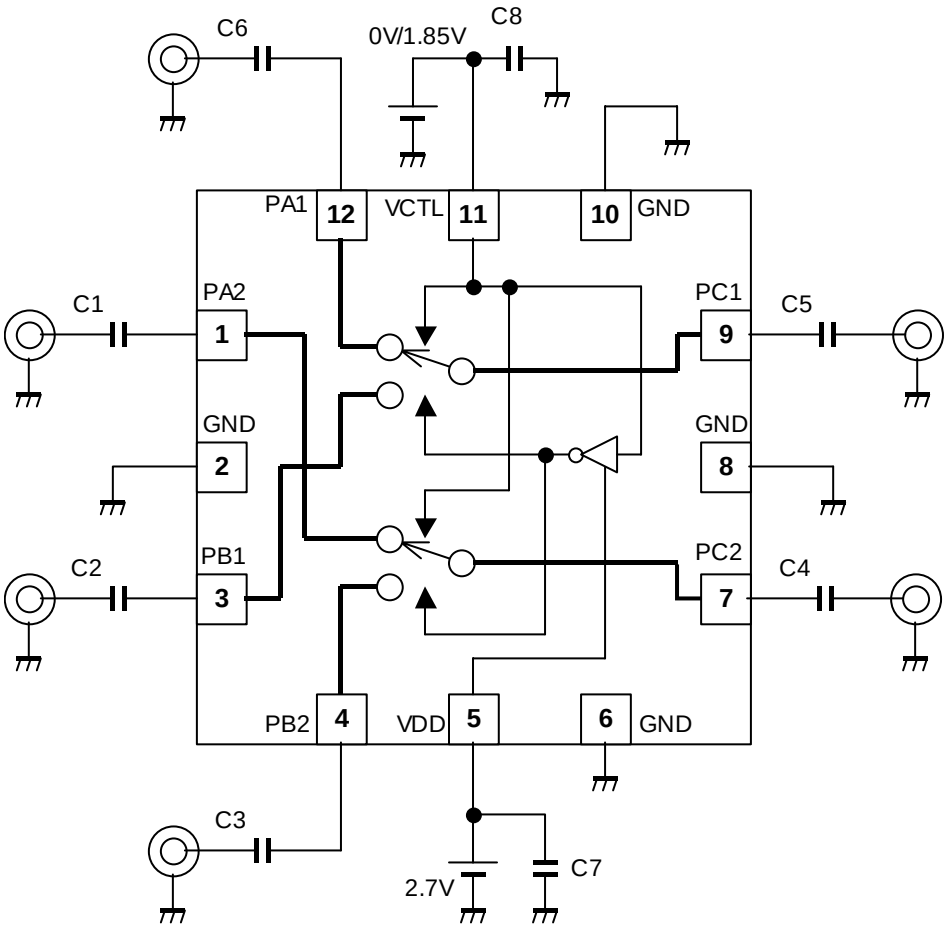


Insertion Loss vs. VCTL

(PC1-PA1, VDD=2.7V, f=2GHz)



■ **APPLICATION CIRCUIT**



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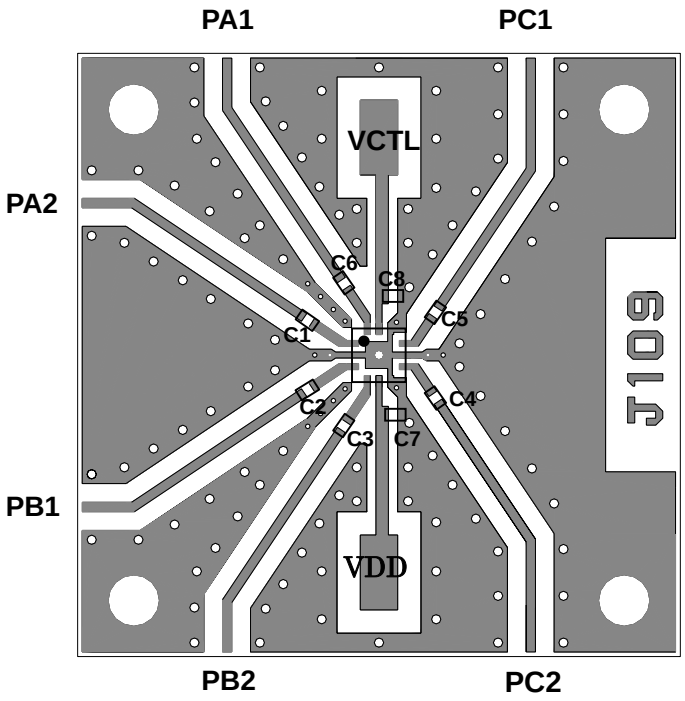
■ **PARTS LIST**

No.	Parts list 1	Parts list 2	Parts list 3
	f=0.05~0.1GHz	f=0.1~0.5GHz	f=0.5~3.0GHz
C1~C6	0.01uF	1000pF	56pF
C7	1000pF	1000pF	1000pF
C8	10pF	10pF	10pF

■ TEST PCB LAYOUT

(TOP VIEW)



Circuit losses including losses of capacitors and connectors

freq (GHz)	Loss (dB)
1.0	0.37
2.0	0.54
3.0	0.70

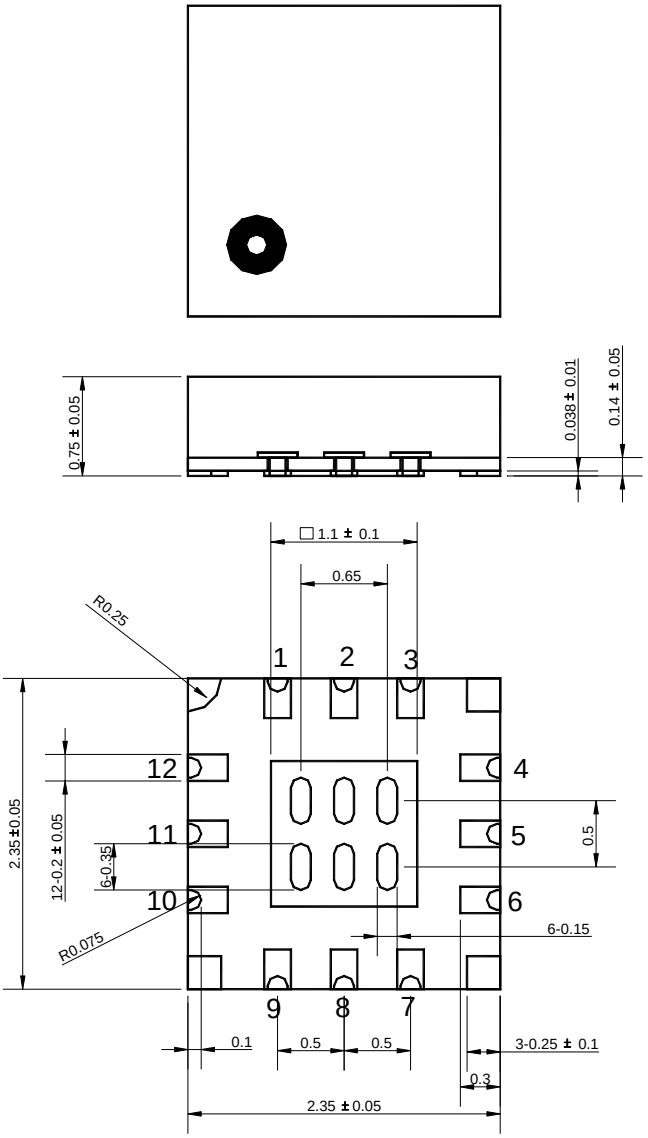
PRECAUTIONS

[1] The DC blocking capacitors have to be placed at RF terminal of PC1, PC2, PA1, PA2, PB1, PB2.

[2] To reduce stripline influence on RF characteristics, please locate bypass capacitors (C7, C8) close to each terminal within 3mm.

[3] To avoid degradation of isolation or high power characteristics, please layout ground pattern right under the IC.

■ **PACKAGE OUTLINE**(USB12-E3)



Unit :mm

Terminal Finish :Au Plating(Cu/Ni/Au)
Substrate Material :FR5
Mold Material :Epoxy Resin
Mass (typ.) :9mg

CAUTIONS ON USING THIS PRODUCT

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

This product may be damaged with electric static discharge (ESD) or spike voltage.
Please handle with care to avoid these damages.

- The product specifications and descriptions listed in this catalog are subject to change without prior notice.
- New Japan Radio has no responsibilities on any violation of the right of the patent by the third party who contains the information and drawing in this catalog.
- This product is not designed for the system requiring high reliability, such as space or air system, submarine cable system, nuclear power plant control system or medical instrument for life keeping.
  If you are planning to use in the system above, please ask for our sales representatives.
- The technology or freights of this device may be controlled by the regulation on the Foreign Export and the Foreign Export Control Law.