

## Features

- 3GPP release 14 compliant
- LTE CAT M1 – 23 dBm (nominal)
- LTE NB1 – 23 dBm (nominal) (dual module only)
- 16 MByte of flash
- GPS/GLONASS (optional)
- Dimension: 11.1x11.4x1.4 mm (typ), 1.5mm(max)
- Package: LGA
- Antenna configurations: external
- SIM configuration: external; integrated SIM capable for MNO/MVNO (optional)
- 3GPP Rel. 14 eDRX and PSM modes
- Power Consumption: enables up to 10 year battery life
  - Hibernation current: 1.5  $\mu$ A(avg)
  - eDRX current: <45  $\mu$ A (avg) @ 8 Hyperframes
  - PSM current: dormant window configurable
- Moisture control: MSL4
- Operating temperature range: -40°C to 85°C
- OTA firmware upgrade
- Regulatory certificate: FCC/IC, ETSI, TELEC
- Global Certification: PTCRB, GCF
- Carrier Certifications: AT&T, Vodafone, DT, Telefonica, Softbank, KDDI, KT, Truphone, TMO, Telstra, SKT, LG U+, and USCC
- OMA Lightweight M2M (LWM2M)
- Control via AT commands according to 3GPP TS27.005, 27.007 and customized AT commands
- IPv4/IPv6 stack with TCP and UDP protocol
- SSL/TLS

## Benefits

- 4G LTE technology capability
- Dedicated LTE half-duplex operation (HD-FDD) for CatM1
- Cellular transceiver designed to meet 3GPP Rel-14 specifications
- LTE universal modem supports (low-band and mid-band):
  - Low-band B5/B8/B12/B13/B17/B18/B19/B20/B26/B28
  - Mid-band B1/B2/B3/B4/B25
- Optimized for Class 3 LTE output power (+23 dBm)

## Applications

- Wearables
- Smart Meter
- Medical/Healthcare
- Asset Tracking

## GPS/GLONASS:

- Supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a powerful and cost efficient manner
- GNSS receiver shares certain hardware resources with the modem. Enables GNSS measurement slots to be efficiently scheduled based on the modem link state. Allows GNSS positioning for asset management applications where infrequent position updates are required
- Can support either single LTE+GNSS or dedicated LTE and GNSS antennas

**LBAD0XX1SC**

**LTE CAT M1&NB1  
Module**



## RoHS Compliance

This component is compliant with RoHS directive. This component was always RoHS compliant from the first date of manufacture.

## Revision History

Revision	Date	Author	Change Description
1.0	03/30/2019	RF PD	New Certified Module Release
1.1	04/22/2020	RF PD	Fixed Dimensions of tape on page 18 and Storage period condition to 72 hours on page 21.
1.2	08/25/2020	N1 SE	Updated GLONASS to 1.3Acronyms, Updated a size table to 2.2 Footprint, Table 2.2 Pinouts (Pin43,45,46,94,to Port1 20~22,74 to Internal use only, Pin64,66 to pull up) ,Added 3.RF Specification , Added 4.4 Digital I/O Pin's specifications, Added 4.5 Analog I/O Pin's specifications, Added 5 Power Sequence, Added 6 UART Interface ,Updated comment "Please refer to" Reference Circuit_Type1SC"for Reference Circuit, Update ASSEMBLY INFORMATION
1.3	09/28/2020	N1 SE	Delete VoLTE from Features (Will be added after certified), And Internal change
1.4	11/04/2020	N1 SE	Updated 3 RF Specification , 4 Environmental Specification, 5 Power sequence, Table2.2 Pinouts, 8 Reference circuit
1.5	02/22/2021	PF PD	Merge Cat M1 only and dual mode into one document.
1.6	05/07/2021	RF PD	Updated the reference circuit with a better resolution version and pin description for pin 56, PMU_VBACKUP pin. Update NB-IoT current value. Remove reference schematics, since there is a separate reference schematics file, no need to duplicate. Updated 1.3 Acronyms.
1.7	06/03/2021	RF PD	Updated table 2.1. Added the missing a2 value.
1.8	03/13/2023	W2 SE	Updated 10.1 Dimensions of Tape Updated 3GPP rel-13 to rel-14 Updated Carrier Certifications
1.9	11/27/2023	N1 SE	Updated 2.1 Dimensions (added e4) Updated 13 Ordering Information (Murata Ordering Part Number of EVK)

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# 1 Introduction

## 1.1 Scope

This product is designed to meet 3GPP Rel-14 specifications

- Host Interface : UART
- Reference Clock : Reference clock embedded
- Size : 11.1 x 11.4 x 1.5 mm (max)
- Weight : 0.45g (typ)
- RoHS : This component can meet with RoHS compliance
- MSL :Level 4
- \*This product is moisture sensitive. Please check the detail in 14.1 Storage Condition section.

## 1.2 Block Diagram

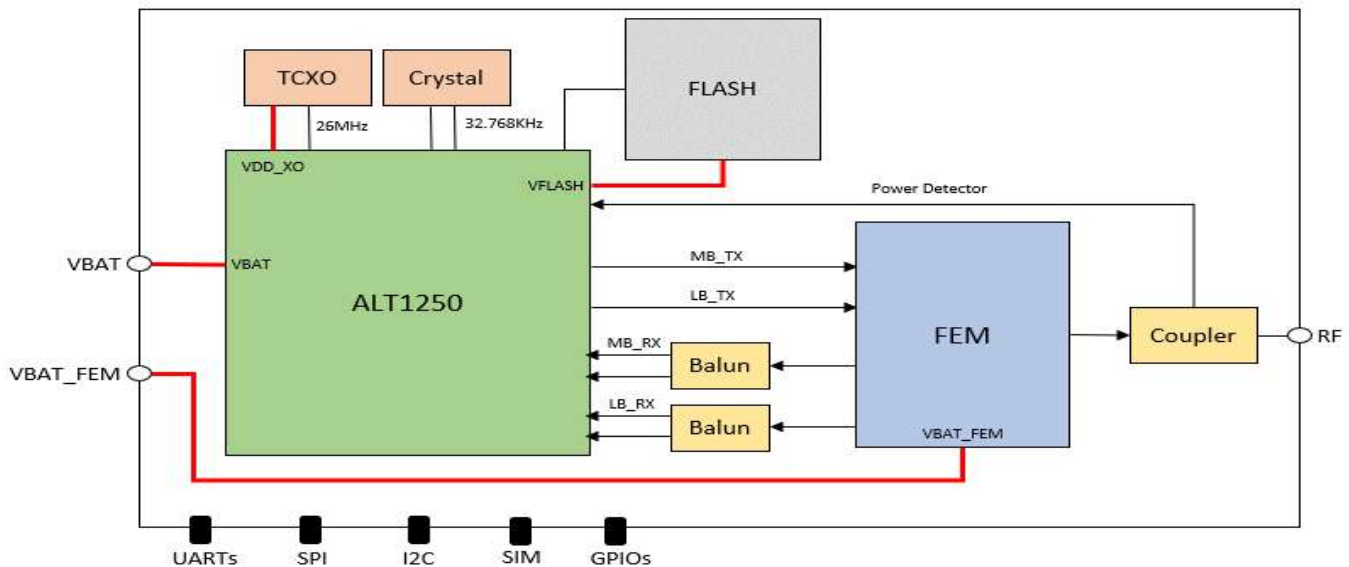


Figure 1.1 Block Diagram

## 1.3 Acronyms

- LTE Long Term Evolution
- UART Universal Asynchronous Receiver Transmitter
- eUICC Embedded Universal Integrated Circuit Card
- LGA Land Grid Array
- BB Baseband
- RFIC Radio Frequency Integrated Circuit
- GPS Global Positioning System
- LB Low Band (699 MHz to 960 MHz frequency range)
- MB Mid Band (1710 MHz to 2170 MHz frequency range)
- PSM Power Save Mode
- eDRX Extended Discontinuous Reception
- GLONASS Global Navigation Satellite System

## 1.4 References

[1] Altair Semiconductor, AL1250 – Datasheet 1.24, August 2020

## 2 Mechanical Specification

### 2.1 Dimension

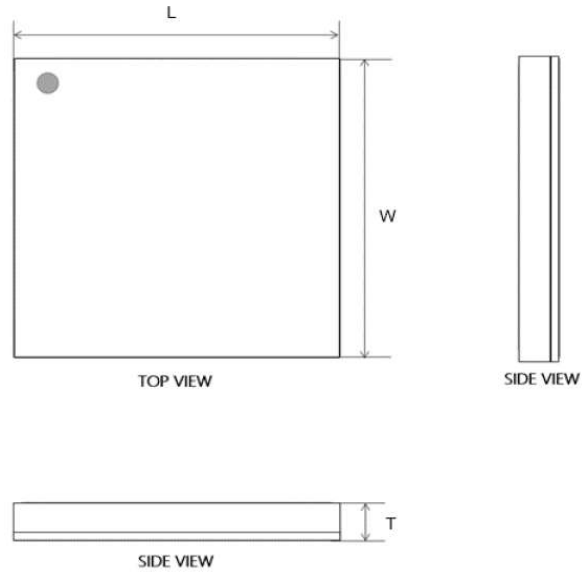


Figure 2.1 Module Top and Side View

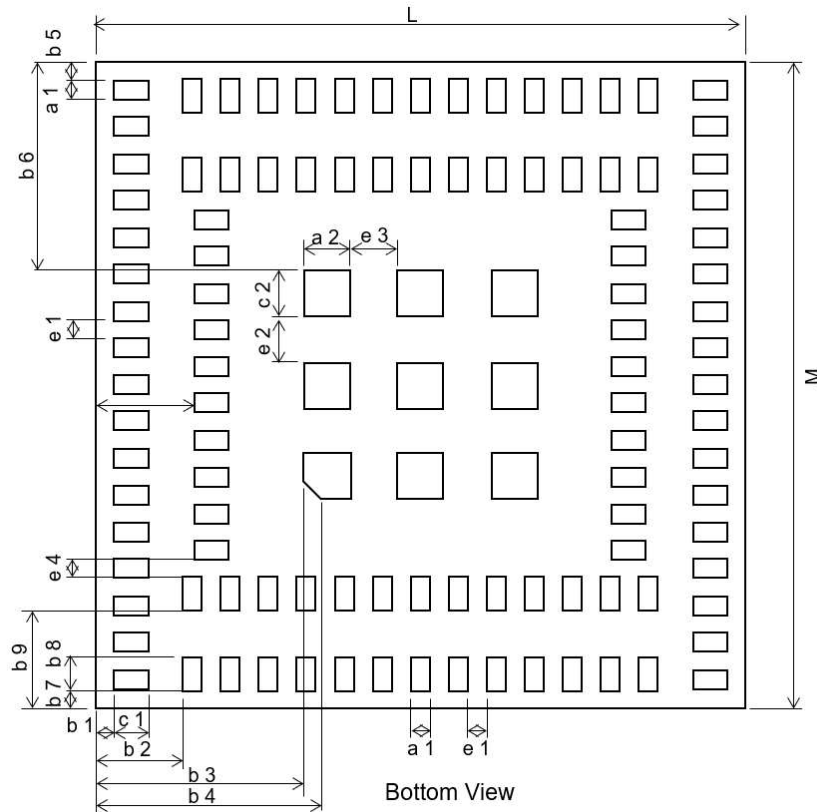


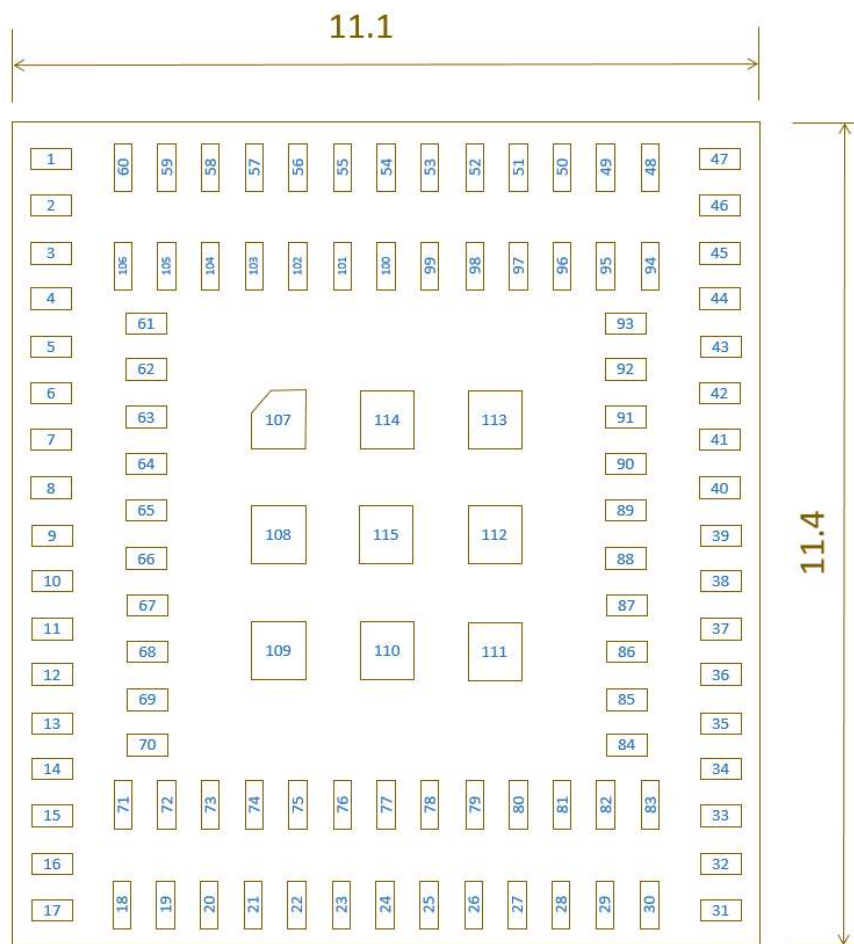
Figure 2.2 Module Footprint Bottom View

**Table 2.1 Dimension**

Mark	Dimension	Mark	Dimension	Mark	Dimension
<b>L</b>	11.10 ± 0.20	<b>W</b>	11.4 ± 0.20	<b>T</b>	1.50 max
<b>a1</b>	0.30 ± 0.10	<b>a2</b>	0.80 ± 0.10	<b>b1</b>	0.30 ± 0.20
<b>b2</b>	1.50 ± 0.20	<b>b3</b>	3.55 ± 0.20	<b>b4</b>	3.85 ± 0.20
<b>b5</b>	0.35 ± 0.20	<b>b6</b>	3.70 ± 0.20	<b>b7</b>	0.30 ± 0.20
<b>b8</b>	0.60 ± 0.10	<b>b9</b>	1.70 ± 0.20	<b>b10</b>	1.70 ± 0.20
<b>c1</b>	0.60 ± 0.10	<b>c2</b>	0.80 ± 0.10	<b>e1</b>	0.35 ± 0.10
<b>e2</b>	0.80 ± 0.10	<b>e3</b>	0.80 ± 0.10	<b>e4</b>	0.325 ± 0.20

unit [mm]

## 2.2 Pin Configuration



**Figure 2.3 Pinout Diagram Top View**



Table 2.2 Pinouts

1SC Pin#	Module Pin Name	ALT1250 Pin No	ALT1250 IC Symbol Pin Name	Type	Direction	Reset Value	IO Domain / Supply	Description
1	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
2	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
3	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
4	EJ_TRST	J5	EJ_TRST/GPIO20	Digital	I	PD	VDDIO	JTAG Test Reset - require external pull down(10kOhm)
5	PMU_AT_IN	R3	PMU_AT_IN	Analog	I		PMU_VRTC	Anti-tamper input; short to GND if not used
6	PMU_WAKEUP	P2	PMU_WAKEUP	Analog	I		PMU_VRTC	Wakeup active high; Device Wake-Up (HI)
7	VDD_RF	L1	PMU_VO_RF	Power	O			MIPI RFFE IO (antenna tuning)
8	VSIM	R1	PMU_VO_SIM	Power	O			SIM LDO output
9	VDD_AUX	T2	PMU_VO_AUX_LDO	Power	O			SC2 LDO output
10	NC			N/A	N/A	N/A	N/A	Reserved (No Connection)
11	SIMIO	M10	SC IO/GPIO14	Digital	I/O	PD	VDDIO	SIM Data 1.8V
12	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
13	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
14	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
15	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
16	VBAT_FEM			Power	I			Input from battery to FEM
17	VBAT_FEM			Power	I			Input from battery to FEM
18	VBAT_FEM			Power	I			Input from battery to FEM
19	GND							
20	UART2_RX	H14	UART2_RX	Digital	I	PU	VDDIO	Only use for internal test
21	UART2_CTS	G15	UART2_CTS	Digital	I	PD	VDDIO	Only use for internal test
22	UART2_TX	G13	UART2_TX	Digital	O	PU	VDDIO	Only use for internal test
23	GND							
24	RF_GNSS_COMMON_ANT			RF	O			GPS/GLONASS receiver output, GNSS is not default support,
25	RF_GNSS_ANT			RF	I			GPS/GLONASS receiver input, GNSS is not default support,
26	GND							
27	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
28	GND							
29	RF_RXTX			RF				CAT-M1 RF in/out signal
30	GND							
31	GPIO53	N13	GPIO53	Digital	O	PU	VDDIO	TX Indicator
32	GPIO50	P10	GPIO50	Digital	O	PD	VDDIO	Device Reset Status (HI)
33	GPIO5	H12	GPIO5	Digital	O	PD	VDDIO	External DCDC Control
34	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
35	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
36	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
37	GPIO2		GPIO2	Digital	O	PD	VDDIO	GPS/GLONASS coexistence indicator GNSS is not default support,
38	GND							
39	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)

1SC Pin#	Module Pin Name	ALT1250 Pin No	ALT1250 IC Symbol Pin Name	Type	Direction	Reset Value	IO Domain / Supply	Description
40	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
41	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
42	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
43	UART1_RTS	P12	UART1_RTS	Digital	O	PU	VDDIO	Port 1: UART RTS
44	GPIO36	R13	GPIO36	Digital	O	PU	VDDIO	External LNA GPS/GLONASS GNSS is not default support,
45	UART1_RX	T12	UART1_RX	Digital	I	PU	VDDIO	Port 1: UART RX
46	UART1_TX	U13	UART1_TX	Digital	O	PU	VDDIO	Port 1: UART TX
47	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
48	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
49	VDDIO	AA7 Y6	PMU_VDDIO PMU_VO_IO	Power	O			IO Reference
50	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
51	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
52	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
53	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
54	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
55	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
56	PMU_VBACKUP	W7	PMU_VBACKUP	Power	I			Connect to backup battery or VBAT
57	PMU_VRTC	W5	PMU_VRTC	Power	O			Use for PMU_SHUTDOWN and PMU_POWERBUTTON pull source
58	VBAT	U3	PMU_VBAT_LDO	Power	I			Voltage from Battery
59	VBAT	V2	PMU_VBAT_DCDC_V2	Power	I			Voltage from Battery
60	VBAT	W1	PMU_VBAT_DCDC_W1	Power	I			Voltage from Battery
61	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
62	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
63	PMU_AT_OUT	N3	PMU_AT_OUT	Analog	O		PMU_VRTC	Anti-tamper output; connect to PMU_AT_IN or NC if not used
64	PMU_SHUTDOWN	M2	PMU_SHUTDOWN	Analog	I	PU	PMU_VRTC	"Shutdown active low , Pull up with 620kΩ on to PMU_VRTC
65	PMU_EXT_ALARM	L3	PMU_EXT_ALARM/	Analog	O		VDDIO	Debug monitoring only
66	PMU_POWER_BUTTON	K2	PMU_POWER_BUTTON	Analog	I	PU	PMU_VRTC	Power button active low Pull up with 620kΩ onto PMU_VRTC
67	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
68	SIMRST	M8	SC_RST/GPIO13	Digital	O	PD	VDDIO	SIM Reset 1.8V
69	SIMCLK	L9	SC_CLK/GPIO15	Digital	O	PD	VDDIO	SIM Clock 1.8V
70	SIM_DETECT	J11	SC_DET	Digital	I	PD	VDDIO	SIM Detection 1.8V
71	SC_SWP	J9	SC_SWP	Digital	O	PD	VDDIO	Host Wake-Up (HI)
72	UART0_RTS	K8	UART0_RTS	Digital	O	PU	VDDIO	• Default is UART0 Request to Send • Data host interface; UART RTS

1SC Pin#	Module Pin Name	ALT1250 Pin No	ALT1250 IC Symbol Pin Name	Type	Direction	Reset Value	IO Domain / Supply	Description
73	UART0_TX	K10	UART0_TX	Digital	O	PU	VDDIO	<ul style="list-style-type: none"> <li>• Default is UART0 Transmit Data</li> <li>• Data host interface; UART TX</li> </ul>
74	UART2_RTS	K6	UART2_RTS	Digital	O	PU	VDDIO	Only use for internal test
75	UART0_RX	G11	UART0_RX	Digital	I	PU	VDDIO	<ul style="list-style-type: none"> <li>• Default is UART0 Clear to Send</li> <li>• Data host interface; UART RX</li> </ul>
76	UART0_CTS	G9	UART0_CTS	Digital	I	PU	VDDIO	<ul style="list-style-type: none"> <li>• Default is UART0 Clear to Send</li> <li>• Data host interface; UART CTS</li> </ul>
77	RFFE_SCLK	H6	RFFE_SCLK	Digital	O	PD	VDDIO	MIPI RFFE Clock (antenna tuning)
78	RFFE_SDATA	H8	RFFE_SDATA	Digital	I/O	PD	VDDIO	MIPI RFFE data (antenna tuning)
79	GND							
80	GND							
81	GND							
82	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
83	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
84	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
85	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
86	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
87	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
88	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
89	GND							
90	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
91	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
92	GND							
93	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
94	UART1_CTS	V12	UART1_CTS	Digital	I	PU	VDDIO	Port1 : UART CTS
95	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
96	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
97	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
98	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
99	GND							
100	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
101	GND							
102	PMU_VCAP	V6	PMU_VCAP	Analog	O		VBAT	Connecting external capacitor as backup for VBAT or NC if not used
103	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
104	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
105	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
106	NC		N/A	N/A	N/A	N/A	N/A	Reserved (No Connection)
107-115	GND							

## 3 RF Specification

### 3.1 Tx Output Power

The module is compliant to the 3GPP spec for release 14 and rated at a Class 3 device (23 dBm) for CATM1 and NB1.

### 3.2 Rx Sensitivity

Table 3.1 Rx Sensitivity

Items		Contents			
		Min	Typ.	Max	Unit
Frequency Range	LB	699	-	960	MHz
	MB	1710	-	2170	MHz
Rx Sensitivity	MCS5, BER<5% All OneSKU bands	-	-103	-	dBm

### 3.3 Power Consumption for CAT M1

Table 3.2 Power Consumption for CAT M1

Mode	Current (TYP)	Condition
Tx Power @23dBm	400mA	CAT M1
Rx	90mA	RRC connected monitoring consecutive sub frames
PSM	1.5uA	Hibernation period when module is asleep
eDRX	45uA	eDRX, 8HF, 81.92s, PTW=1, excluding SIM

### 3.4 Power Consumption for NB1 ( for dual mode only)

Table 3.3 Power Consumption for NB1

Mode	Current (TYP)	Condition
Tx Power @23dBm	800mA	Single Tone (3.75kHz)
Rx	90mA	RRC connected monitoring consecutive sub frames
PSM	1.5uA	Hibernation period when module is asleep
eDRX	45uA	eDRX, 8HF, 81.92s, PTW=1, excluding SIM

## 4 Environmental Specification

### 4.1 Absolute Maximum Rating

Table 4.1 Absolute Maximum Rating

Parameters		Min	Typ	Max	Unit
Storage Temperature		-40	-	+85	degC
Supply Voltage	VBAT	-0.3	-	4.35	V
	PMU_VBACKUP	-0.3	-	4.35	V
	PMU_VCAP	-0.3	-	4.35	V
	VBAT_FEM	-0.5	-	5.2	V

### 4.2 Recommended Operating Condition

Table 4.2 Recommended Operating Condition

Parameters		Min	Typ	Max	Unit
Operating Temperature		-40	25	+85	degC
Supply Voltage	VBAT	2.2	-	4.35	V
	PMU_VBACKUP	2.2	-	4.35	V
	PMU_VCAP	2.2	-	4.35	V
	VBAT_FEM	2.85	-	4.5	V

### 4.3 Interface Voltage specifications

Table 4.3 Interface Voltage Condition

Parameters	Min	Typ	Max	Unit
VDDIO	1.7	1.8	1.9	V

For VDDIO, the total current from all IOs combined, and supplied by PMU\_VDDIO, should not exceed 50mA.

### 4.4 Digital I/O Pin's specifications

Table 4.4 Digital IO Pin's Specifications

Parameters		Min	typ	Max	Unit
Input Voltage	High-level	0.7*VDDIO	-	VDDIO	V
	Low-level	VSS	-	0.3*VDDIO	V
Output Voltage	High-level	0.8*VDDIO	-	-	V
	Low-level	-	-	0.2*VDDIO	V
IO Drive Strength		2	-	12	mA

(\*)The total current from all IOs combined should not exceed 50mA

Table 4.5 Digital IO Absolute Maximum Rating

	Min	typ	Max	Unit
All digital 1.8V IOs	-0.2	-	VDDIO + 0.2	V

## 4.5 Analog I/O Pin's specifications

Table 4.6 Analog IO Pin's specifications

Parameters		Min	typ	Max	Unit
PMU_WAKEUP	Low-level	-	-	0.3	V
	High-level	1.2	-	-	V
PMU_POWER_BUTTON	Low-level	-	-	0.3	V
	High-level	1	-	-	V
PMU_SHUTDOWN	Low-level	-	-	0.3	V
	High-level	1.3	-	-	V

Table 4.7 Analog IO Absolute Maximum Rating

	Min	typ	Max	Unit
All Analog 1.8V IOs	-0.2	-	VDDIO + 0.2	V

# 5 POWER SEQUENCE

## 5.1 Power Sequence for power up

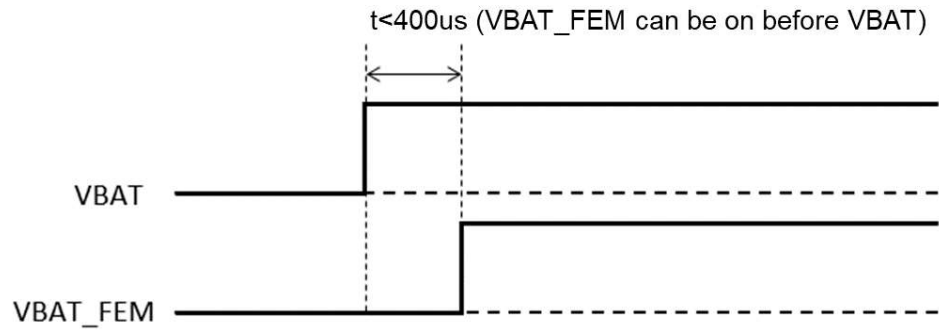


Figure 5.1 Power Sequence Diagram – Power Up

## 5.2 Power Sequence for power down

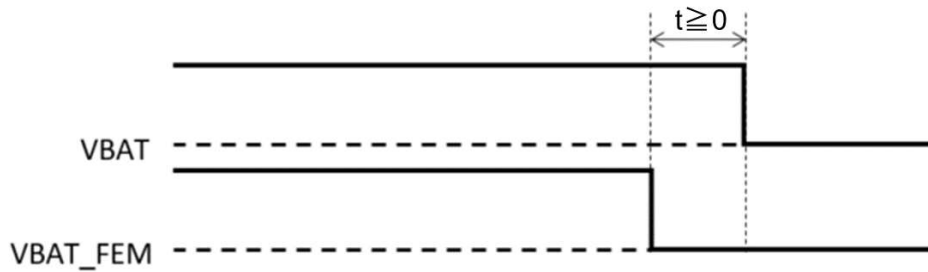


Figure 5.2 Power Sequence Diagram – Power Up

## 5.3 Power Sequence for reset

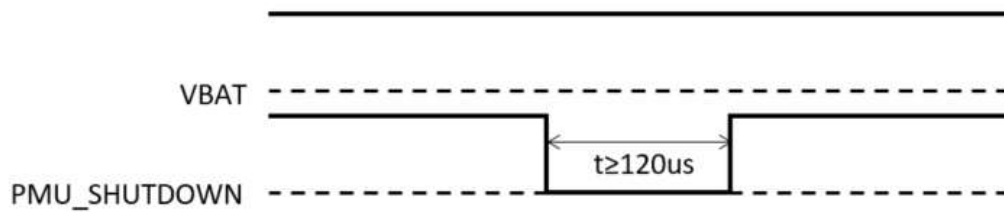


Figure 5.3 Power Sequence Diagram – Power Up

## 6 UART Interface

Table 6.1 UART Interface

Parameters	Setting
Serial wires	Tx and Rx
Baud rate	115200 bps
Data bit	8bit
Start bit	1bit
Stop bit	1bit
Flow control	None
Parity bit	None
Transmission Order	LSB first

## 7 Host PCB Landing Pattern (Top View)

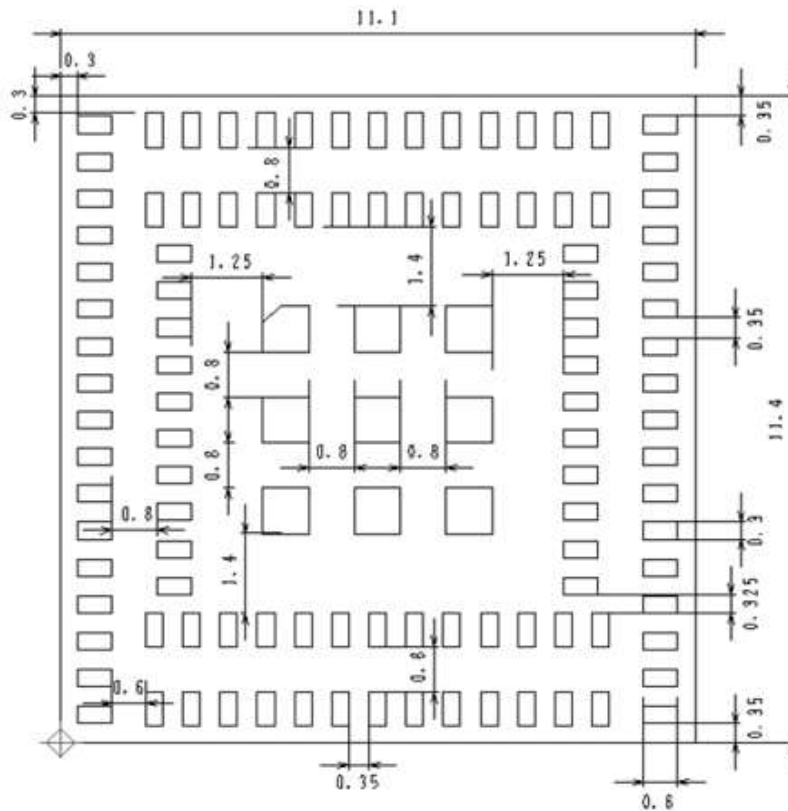


Figure 7.1 Recommended PCB Landing Pattern



## 8 Reference Circuit

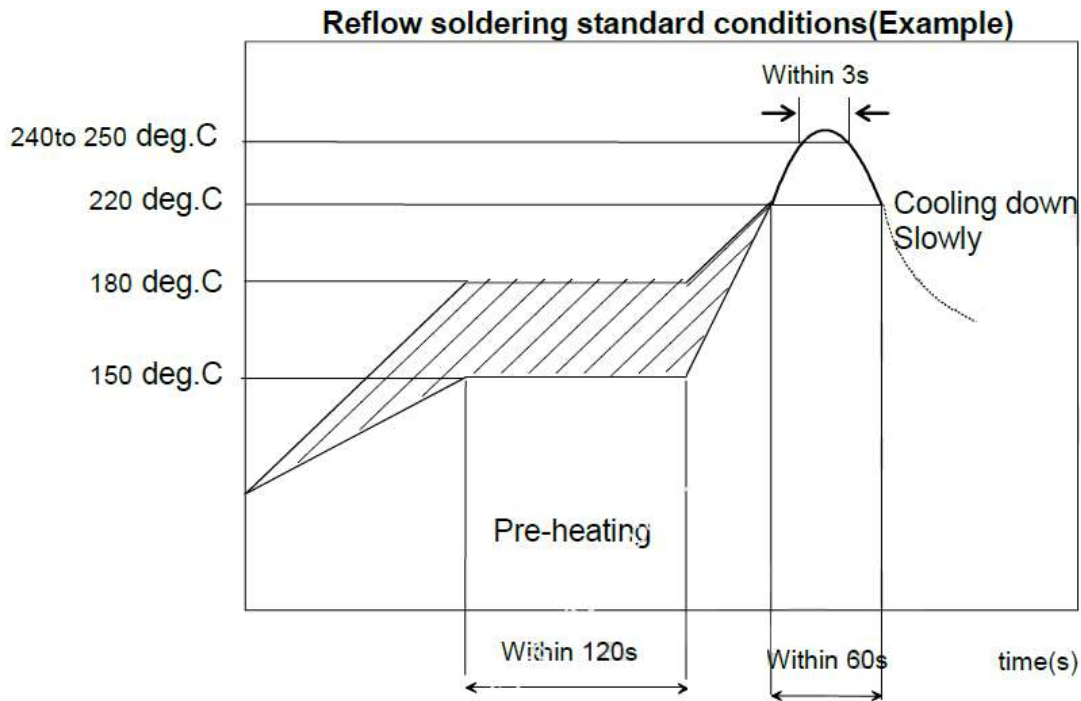
Please refer to "Reference Circuit\_Type1SC"

## 9 Assembly Information

Refer to Figure 9.1 for recommended soldering conditions.

Soldering must be done by this method to prevent products from damage. Set up the highest temperature of reflow within 260 °C. If considering other soldering conditions, you must contact Murata before proceeding.

Reflow soldering standard conditions



**Figure 9.1 Reflow Profile**

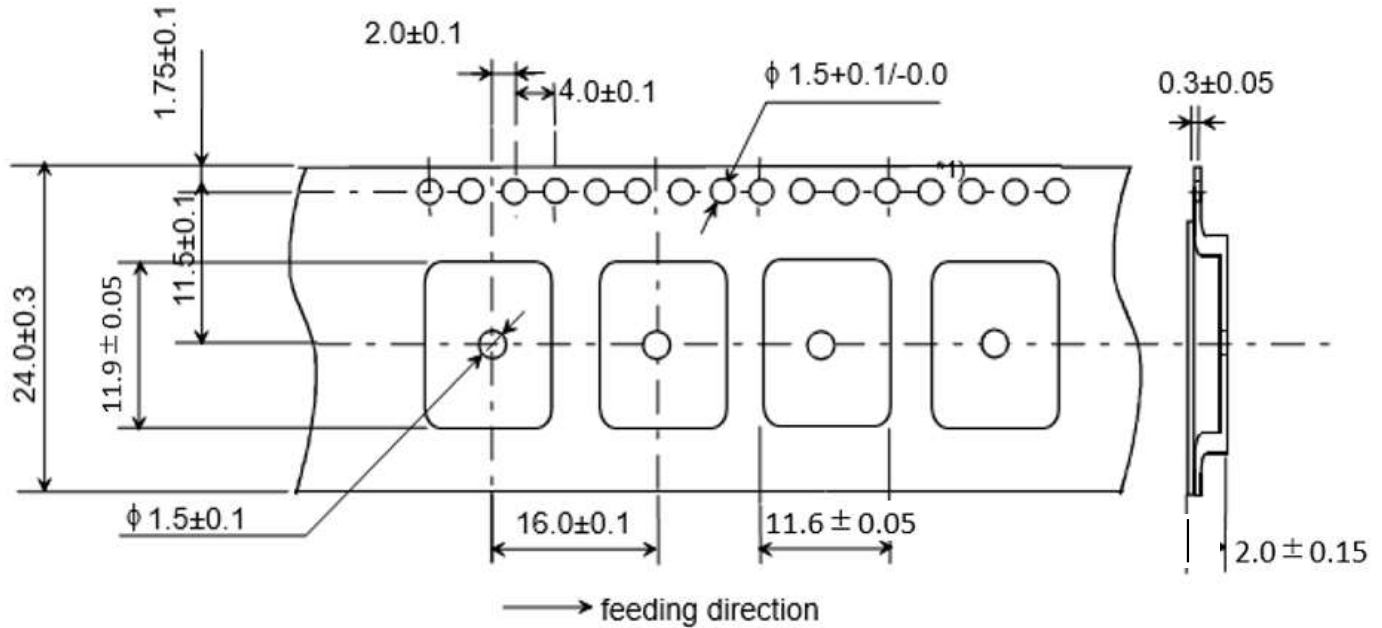
Please don't use the reflow method more than twice.

Use rosin type flux or a weakly active flux with a chlorine content of 0.2 wt % or less.

Since this Product is Moisture Sensitive, any cleaning with liquid is NOT permitted.

# 10 Packaging and Marking Information

## 10.1 Dimensions of Tape (Plastic tape)



- 1) The corner and ridge radiuses (R) of inside cavity are 0.3mm max.
- 2) Cumulative tolerance of 10 pitches of the sprocket hole is  $\pm 0.2$ mm
- 3) Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

Figure 10.1 Tape Dimensions (Unit: mm)

## 10.2 Dimensions of Reel

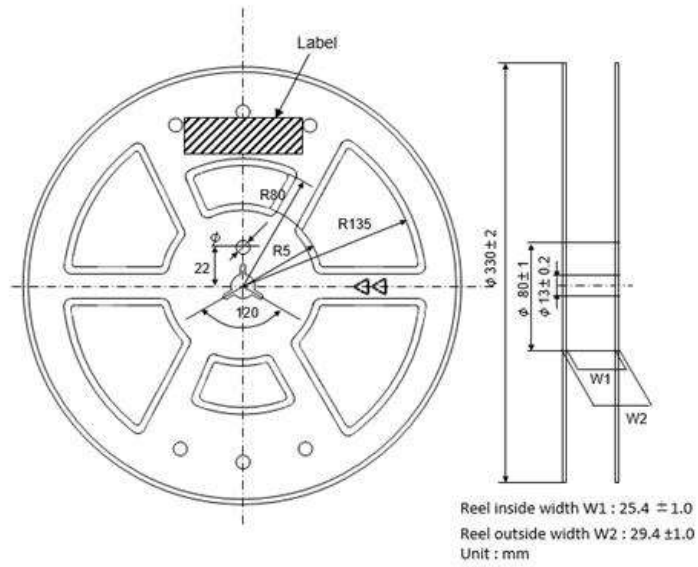


Figure 10.2 Reel Dimensions (Unit: mm)

## 10.3 Taping Diagrams

[1] Feeding Hole : As specified in (1)

[2] Hole for chip : As specified in (1)

[3] Cover tape : 62μm in thickness

[4] Base tape : As specified in (1)

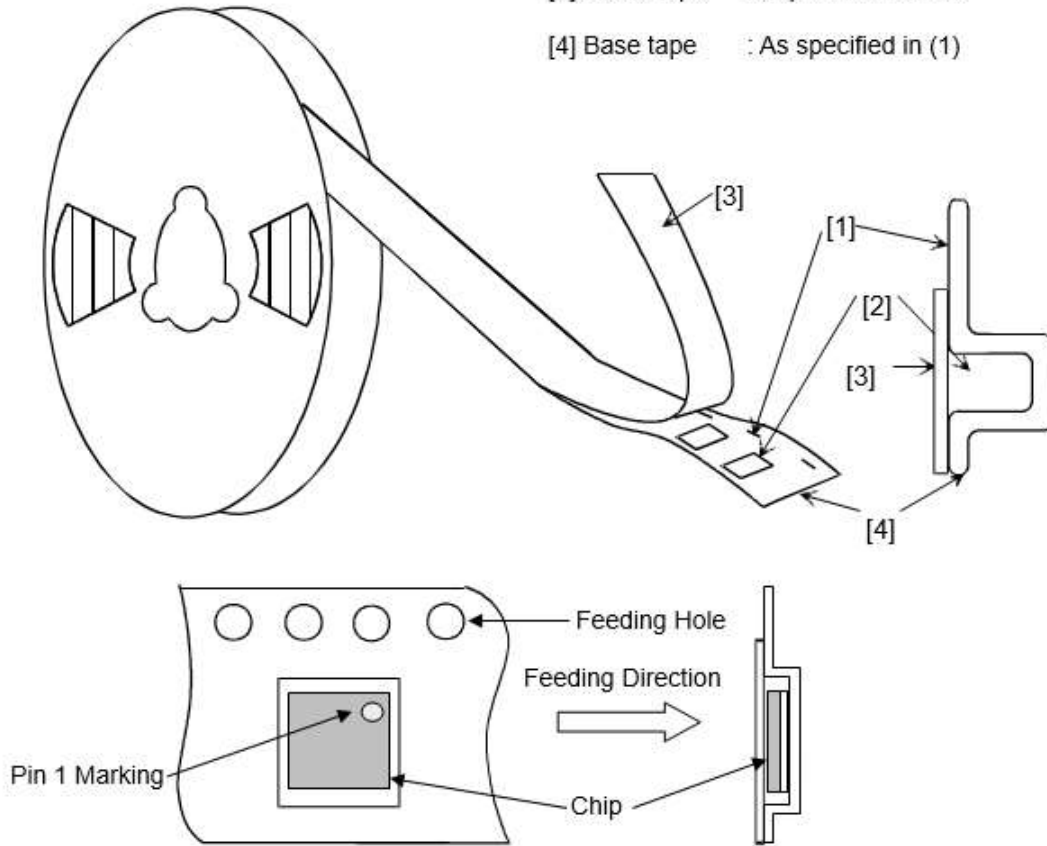


Figure 10.3 Tape Diagram

## 10.4 Module Marking Information

Figures below show the module marking. Dimensions are nominal, not absolute.

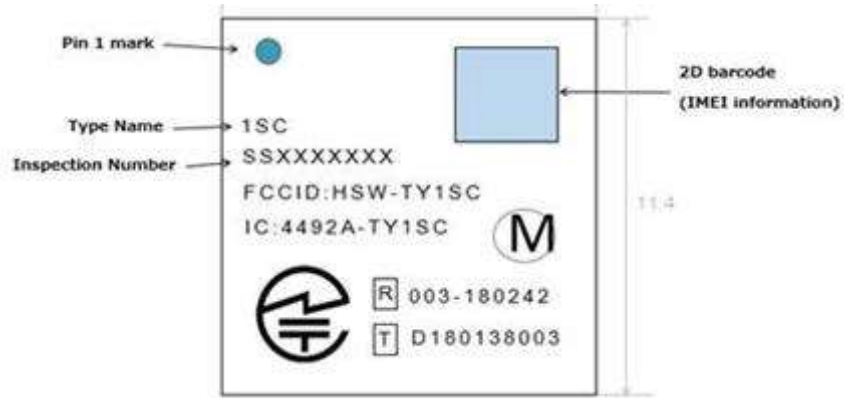


Figure 10.4 Type 1SC Module Marking Diagram

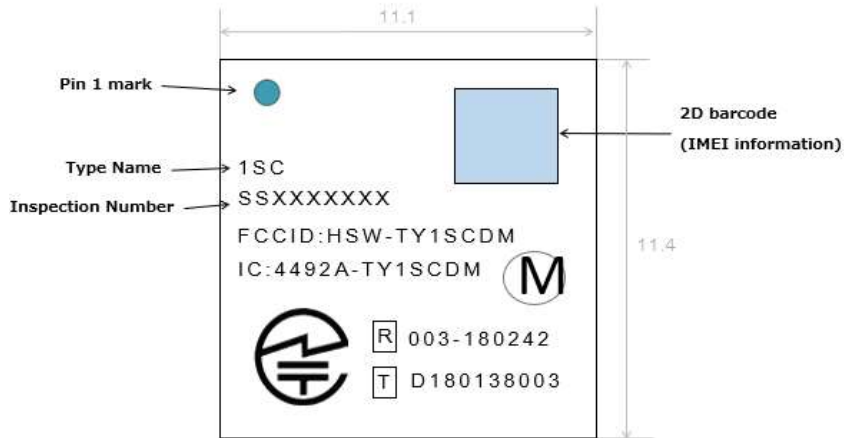


Figure 10.5 Type 1SC DM Module Marking Diagram

## 10.5 Moisture Sensitivity Level

The module is rated to MSL 4 (72 hours). Please observe this rating with the utmost importance. For storage condition detail, please refer to 14.1 Storage Conditions.

# 11 Regulatory Information

The table below shows the regulatory compliance status of the Type 1SC module.

**Table 11.1 Regulatory Standards Conformance for 1SC single mode**

<b>Regulatory Body</b>	<b>Country</b>	<b>Certificate ID for Cat M1 only</b>	<b>Certificate ID for Cat M1/NB1</b>
FCC	US	HSW-TY1SC	HSW-TY1SCDM
IC	Canada	4492A-TY1SC	4492A-TY1SCDM
ETSI	EU	Compliant	Compliant
TELEC	Japan	003-180242	003-180242
RCM/ACMA	Australia, New Zealand	1102MUR_LBAD0_S0 42-1	1102MUR_LBAD0_S 042-1
RRA/KC	Korea	R-C-VPY-Type1SC	R-C-VPY-Type1SC
NCC	Taiwan	CCAM20NB0010T3	CCAM20NB0010T3
GCF	Global	Compliant	Compliant
PTCRB	Global	Compliant	Compliant

For the details; Please refer to Type1SC Hardware Design Guidelines.

## 12 RoHS Information

The Type 1SC module conforms to RoHS requirements.

## 13 Ordering Information

Product	Model Name	Murata Ordering Part Number	Standard Order Increment
Module Sample	Type 1SC	LBAD0XX1SC-314TEMP	1000 pcs
Development Kit	Type 1SC DK	LBAD0XX1SC-DM-EVK-B	1 pcs

## 14 Notice

### 14.1 Storage Conditions

Please use this product within 6 months after receipt.

- The product shall be stored in original package under with an ambient temperature from 5 to 35°C, and humidity from 20% to 70%RH. (Packing materials, in particular, may become deformed if the temperature exceeds 40°C.)
- If the product is not used for more than 6 months after receipt, confirm the solderability before use.
- Store the product in non-corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>2</sub>, NO<sub>x</sub>, etc.).
- Avoid mechanical shock, such as dropping or puncturing the product, to preserve integrity of the packing materials.
- After the package is opened, store it at <30°C / <60%RH and use the product within **72** hours.
- If the color of the indicator in the packing changes, bake the product before soldering.

**Baking condition:** 125 +5/-0 °C, 24hours, 1 time

Bake the product on a heat-resistant tray because other materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

### 14.2 Handling Conditions

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle products with care to avoid cracks or damages on the terminals, causing unwarranted changes in the product characteristics. Do not touch products with bare hands to avoid degrading solder ability or damage caused by static electrical charge.

### 14.3 Standard PCB Design (Land Pattern and Dimensions)

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is in accordance with Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC

terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. If using non-standard lands, contact Murata beforehand.

## 14.4 Notice for Chip Placer

When positioning products on the PCB, be aware that mechanical chucking may damage products. When placing products on the PCB, a worn-out chucking locating claw or a suction nozzle can cause undue stress and uneven force, resulting in damaged products. To prevent products from damage, be sure to follow the specifications for the maintenance of the chip placer in use.

## 14.5 Operational Environment Conditions

Products are designed to work under normal environmental conditions (ambient temperature, humidity and pressure) as stated above. However, if products are used under the following circumstances, they may be damaged, resulting in leakage of electricity and abnormal temperatures.

- In an atmosphere containing corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>x</sub>, NO<sub>x</sub>, etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty environment.
- Direct sunlight.
- Excessive moisture.
- Excessive humidity where water condenses.
- Extreme cold, such as in freezing temperatures.

If products could be exposed to those conditions described above, consult with Murata before actual use.

Static electricity may degrade or destroy products. Avoid static electricity or excessive voltage while assembling and measuring.

## 14.6 Input Power Capacity

Avoid exceeding the input power capacity as specified in this document.

If operating conditions may exceed parameters as stated in this document, inform Murata before use.