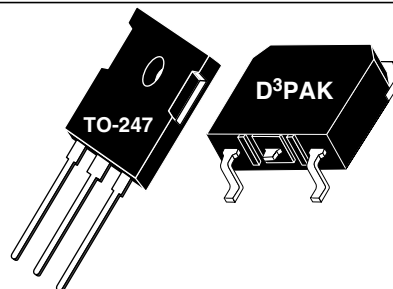
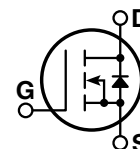


POWER MOS 7[®] MOSFET

Power MOS 7[®] is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7[®] by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7[®] combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT5014BLL-SLL(G)	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	35	Amps
I_{DM}	Pulsed Drain Current ^①	140	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	403	Watts
	Linear Derating Factor	3.22	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	35	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	500			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 17.5A$)			0.140	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 500V, V_{GS} = 0V$)			100	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 400V, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			500	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT5014 BLL - SLL(G)

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		3261		pF
C_{oss}	Output Capacitance			704		
C_{rss}	Reverse Transfer Capacitance			50		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 250V$ $I_D = 35A @ 25^\circ C$		72		nC
Q_{gs}	Gate-Source Charge			20		
Q_{gd}	Gate-Drain ("Miller") Charge			36		
$t_{d(on)}$	Turn-on Delay Time	RESISTIVE SWITCHING $V_{GS} = 15V$ $V_{DD} = 250V$ $I_D = 35A @ 25^\circ C$ $R_G = 1.6\Omega$		11		ns
t_r	Rise Time			6		
$t_{d(off)}$	Turn-off Delay Time			23		
t_f	Fall Time			3		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C $V_{DD} = 333V, V_{GS} = 15V$ $I_D = 35A, R_G = 5\Omega$		325		μJ
E_{off}	Turn-off Switching Energy			249		
E_{on}	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C $V_{DD} = 333V, V_{GS} = 15V$ $I_D = 35A, R_G = 5\Omega$		545		
E_{off}	Turn-off Switching Energy			288		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			35	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			140	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -35A$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -35A, di_S/dt = 100A/\mu s$)		510		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -35A, di_S/dt = 100A/\mu s$)		10		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			8	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.31	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_J = +25^\circ C$, $L = 2.12mH$, $R_G = 25\Omega$, Peak $I_L = 35A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -35A$ $di/dt \leq 700A/\mu s$ $V_R \leq 500V$ $T_J \leq 150^\circ C$

⑥ E_{on} includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

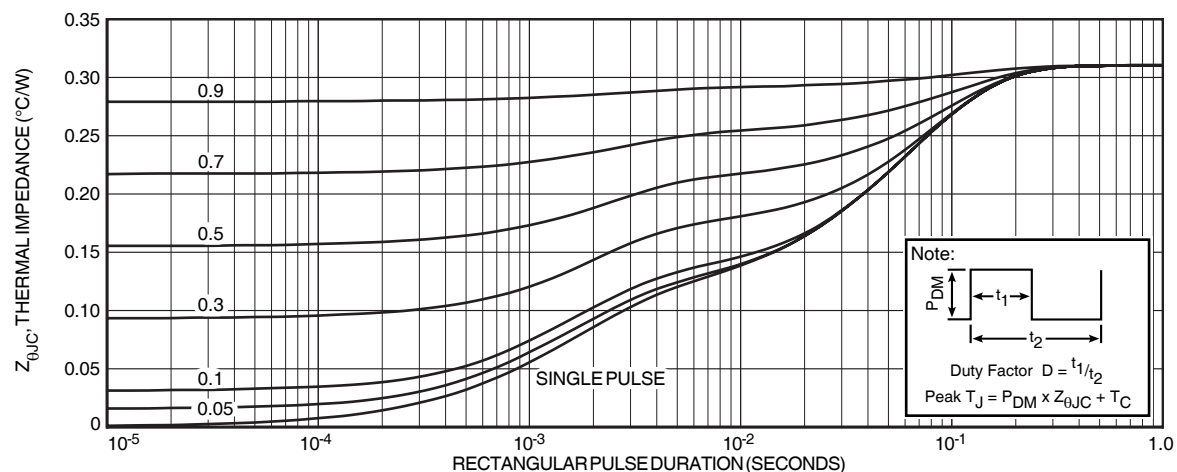


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Typical Performance Curves

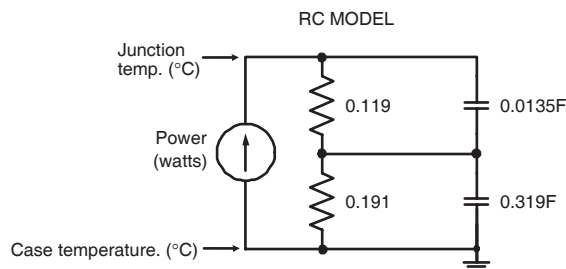


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

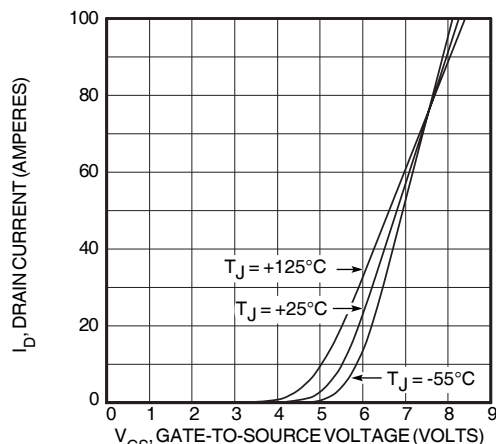


FIGURE 4, TRANSFER CHARACTERISTICS

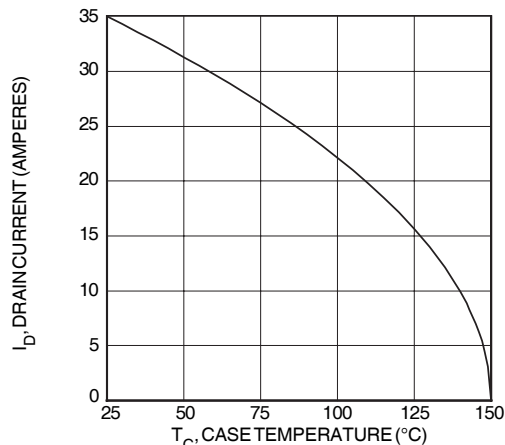


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

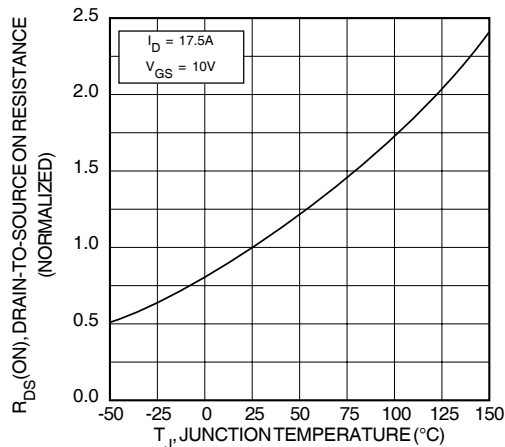


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

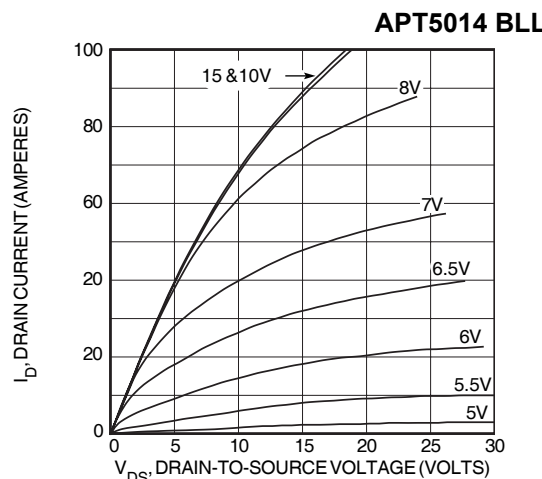


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

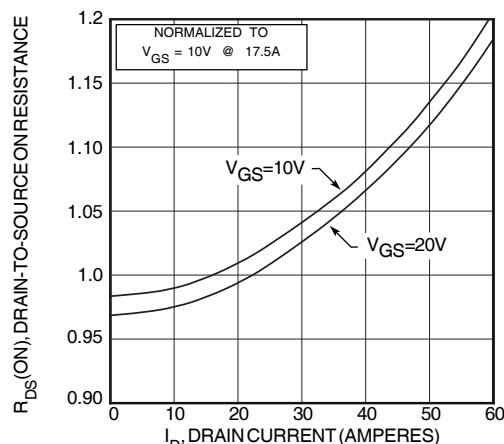


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

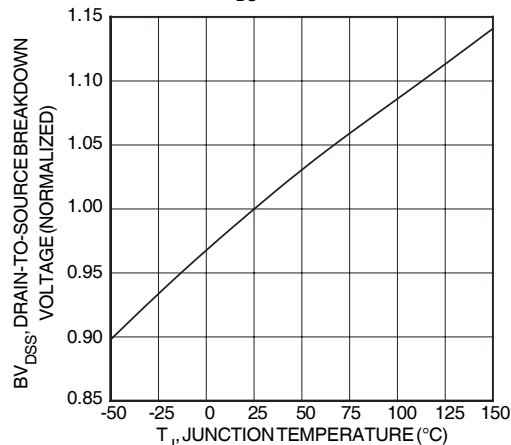


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

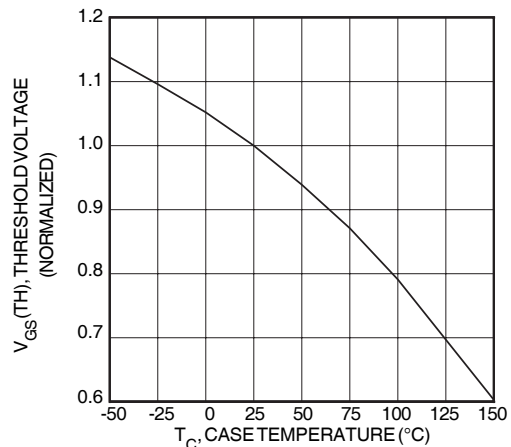


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

Typical Performance Curves

APT5014 BLL - SLL(G)

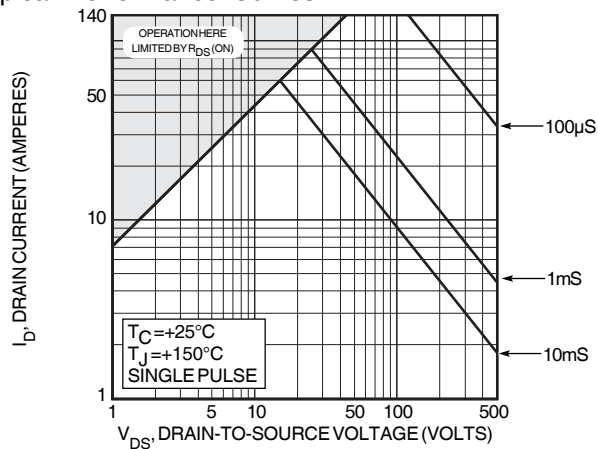


FIGURE 10, MAXIMUM SAFE OPERATING AREA

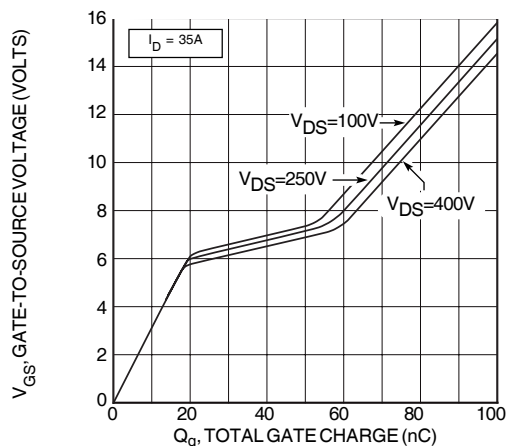


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

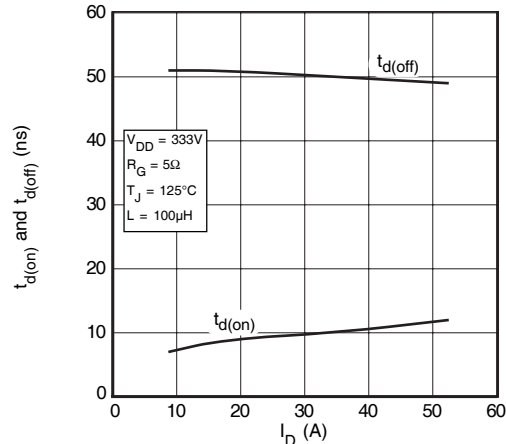


FIGURE 14, DELAY TIMES vs CURRENT

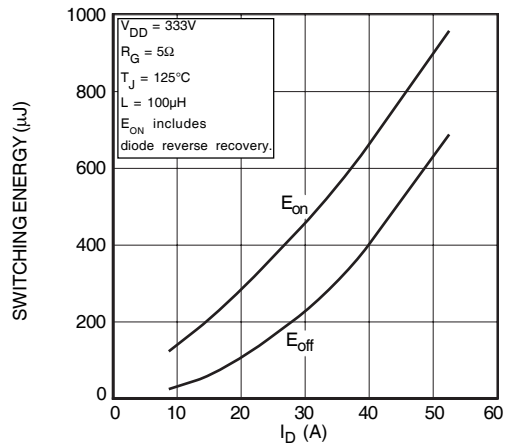


FIGURE 16, SWITCHING ENERGY vs CURRENT

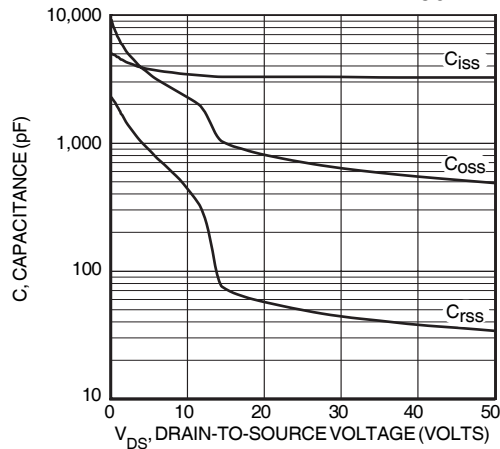


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

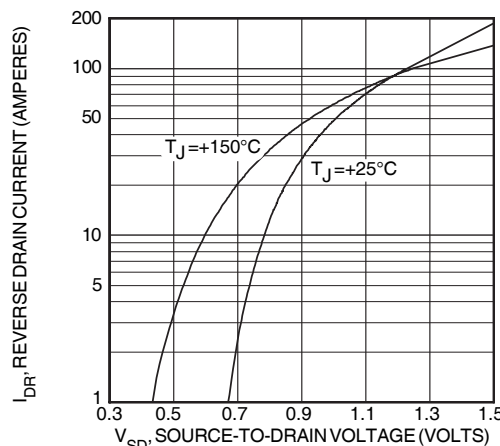


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

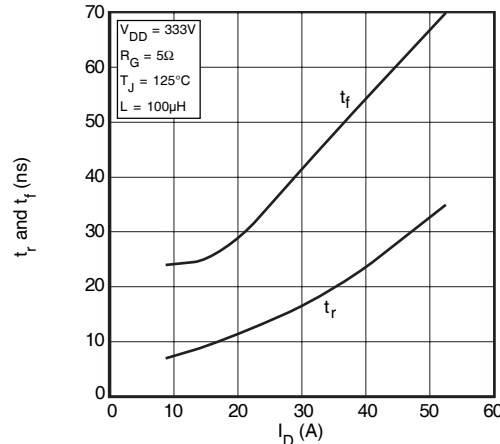


FIGURE 15, RISE AND FALL TIMES vs CURRENT

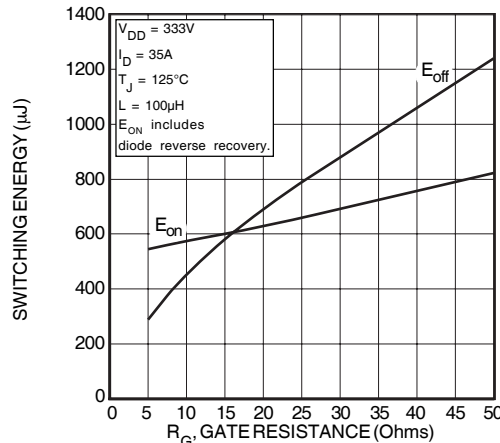


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

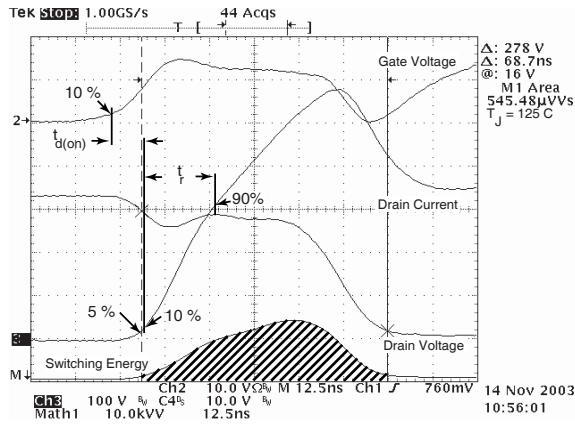


Figure 18, Turn-on Switching Waveforms and Definitions

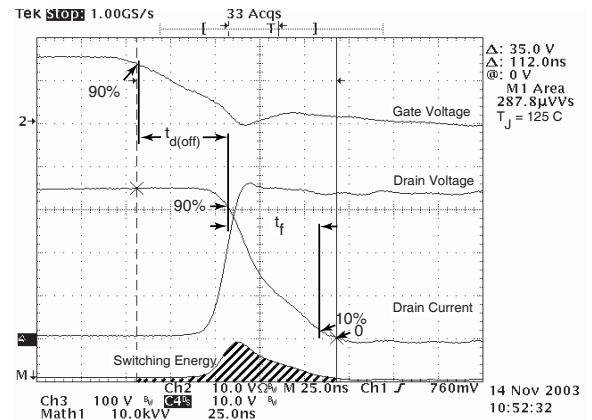


Figure 19, Turn-off Switching Waveforms and Definitions

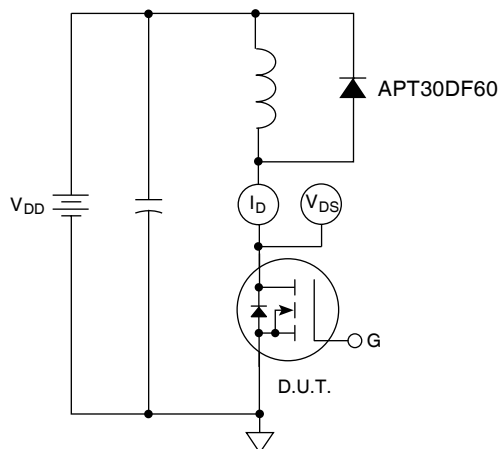
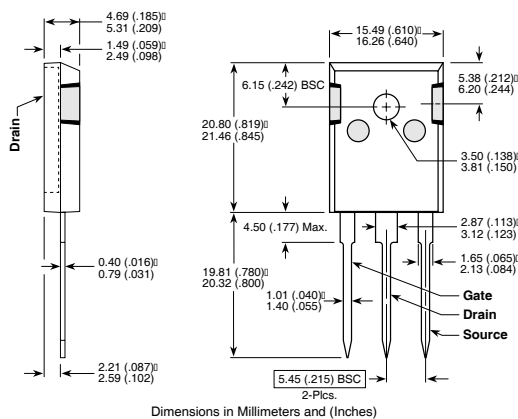


Figure 20, Inductive Switching Test Circuit

TO-247 Package Outline

e1 SAC: Tin, Silver, Copper



D³PAK Package Outline

e3 100% Sn Plated

