USB3250

Hi-Speed USB Device Transceiver with UTMI Interface

PRODUCT FEATURES

Data Brief

- USB-IF "Hi-Speed" certified to USB 2.0 electrical specification
- Interface compliant with the UTMI specification (60MHz 8-bit unidirectional interface or 30MHz 16-bit bidirectional interface)
- Supports 480Mbps High Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45Ω and 1.5kΩ termination resistors reduce external component count
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 12MHz crystal
- Robust and low power digital clock and data recovery circuit
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- Draws 72mA (185mW) maximum current consumption in HS mode - ideal for bus powered functions
- On-die decoupling capacitance and isolation for immunity to digital switching noise
- Available in a 56-pin QFN package
- Full industrial operating temperature range from -40°C to +85°C (ambient)

Applications

The Universal Serial Bus (USB) is the preferred interface to connect Hi-Speed PC peripherals.

- Digital Still and Video Cameras
- MP3 Players
- External Hard Drives
- Scanners
- Entertainment Devices
- Printers
- Test and Measurement Systems
- POS Terminals
- Set Top Boxes

PRODUCT PREVIEW

Ordering Information:

USB3250-ABZJ for 56 pin, QFN lead-free RoHS compliant package, 8 x 8 x 0.85mm

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

PRODUCT PREVIEW

General Description

The USB3250 provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The IC is available in a 56 pin QFN.

The USB3250 is a USB 2.0 physical layer transceiver (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY can be configured for either an 8-bit unidirectional or a 16-bit bidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports 480Mbps transfer rate, while remaining backward compatible with USB 1.1 legacy protocol at 12Mbps.

All required termination for the USB 2.0 Transceiver is internal. Internal 5.25V short circuit protection of DP and DM lines is provided for USB compliance.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

Block Diagram

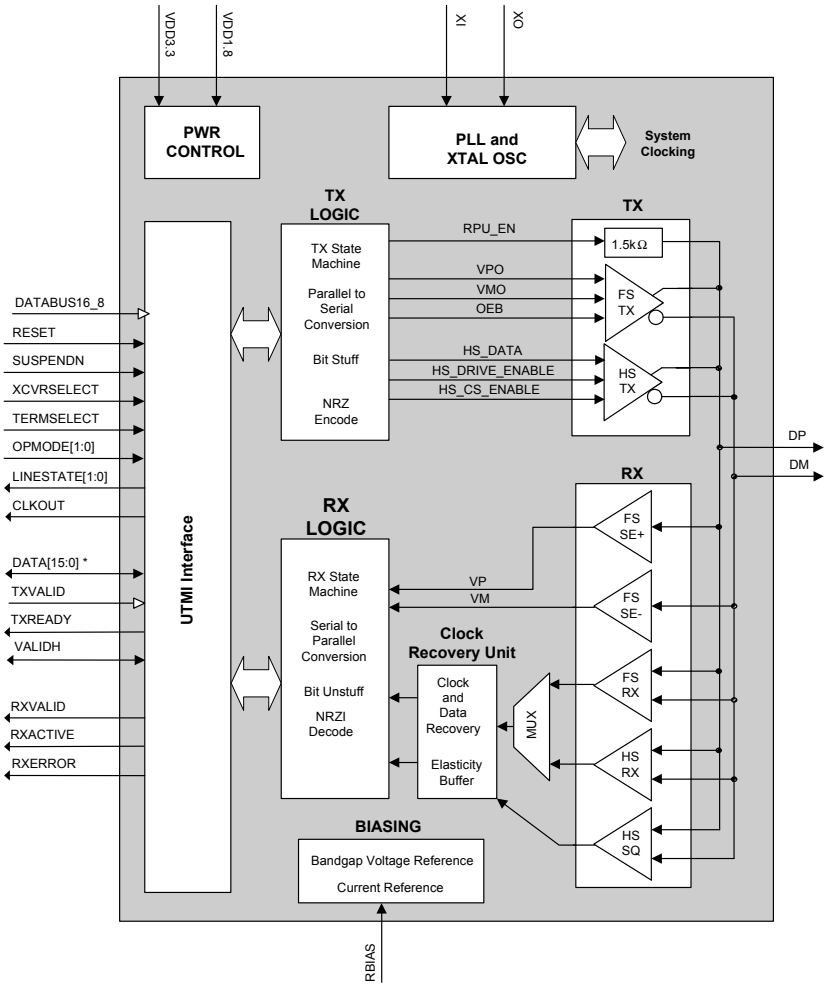


Figure 1 USB3250 Functional Block Diagram

Pin Configuration

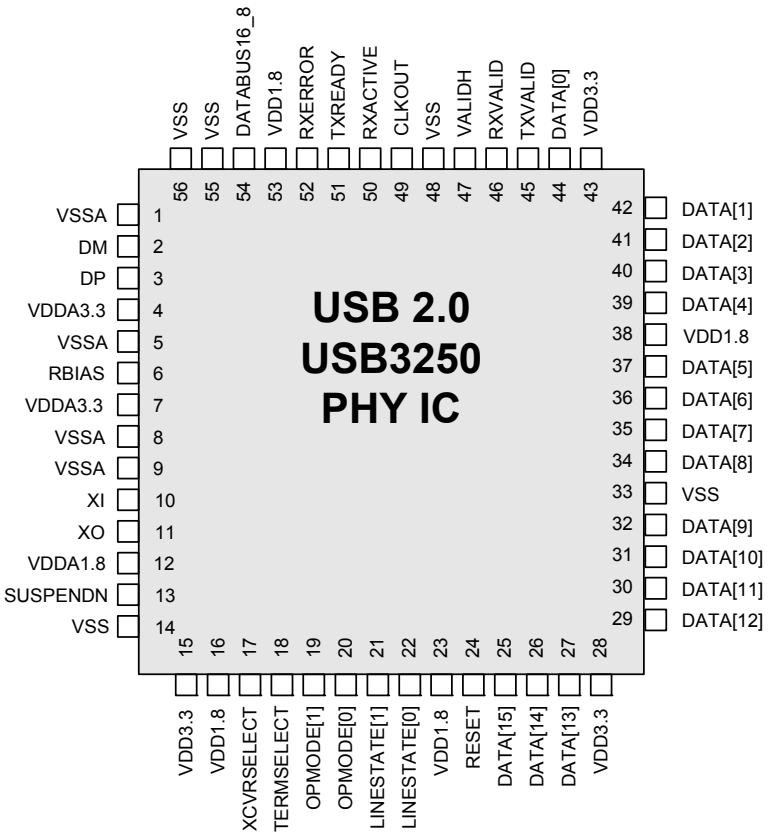


Figure 2 56-Pin USB3250 Pin Configuration (Top View)

Pin Description Tables

Table 1 System Interface Pins

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RESET	Input	High	**Reset.** Reset all state machines. After coming out of reset, must wait 5 rising edges of clock before asserting TXValid for transmit. Assertion of Reset: May be asynchronous to CLKOUT. De-assertion of Reset: Must be synchronous to CLKOUT unless RESET is asserted longer than two periods of CLKOUT.
XCVRSELECT	Input	N/A	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: HS transceiver enabled 1: FS transceiver enabled.
TERMSELECT	Input	N/A	**Termination Select.** This signal selects between the FS and HS terminations: 0: HS termination enabled 1: FS termination enabled
SUSPENDN	Input	Low	**Suspend.** Places the transceiver in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, TERMSELECT must always be in FS mode to ensure that the 1.5k Ω pull-up on DP remains powered. 0: Transceiver circuitry drawing suspend current 1: Transceiver circuitry drawing normal current
CLKOUT	Output	Rising Edge	**System Clock.** This output is used for clocking receive and transmit parallel data at 60MHz (8-bit mode) or 30MHz (16-bit mode). When in 8-bit mode, this specification refers to CLKOUT as CLK60. When in 16-bit mode, CLKOUT is referred to as CLK30.
OPMODE[1:0]	Input	N/A	**Operational Mode.** These signals select between the various operational modes: [1] [0] Description 0 0 0: Normal Operation 0 1 1: Non-driving (all terminations removed) 1 0 2: Disable bit stuffing and NRZI encoding 1 1 3: Reserved
LINESTATE[1:0]	Output	N/A	**Line State.** These signals reflect the current state of the USB data bus in FS mode, with [0] reflecting the state of DP and [1] reflecting the state of DM. When the device is suspended or resuming from a suspended state, the signals are combinatorial. Otherwise, the signals are synchronized to CLKOUT. [1] [0] Description 0 0 0: SE0 0 1 1: J State 1 0 2: K State 1 1 3: SE1
DATABUS16_8	Input	N/A	**Databus Select.** Selects between 8-bit and 16-bit data transfers. 0: 8-bit data path enabled. VALIDH is undefined. CLKOUT = 60MHz. 1: 16-bit data path enabled. CLKOUT = 30MHz.

Table 2 Data Interface Pins

<table>
<tr><th>NAME</th><th>DIRECTION</th><th>ACTIVE LEVEL</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="11">DATA[15:0]</td><td rowspan="11">Bidir</td><td rowspan="11">N/A</td><td colspan="4">DATA BUS. 16-BIT BIDIRECTIONAL MODE.</td></tr>
<tr><td>TXVALID</td><td>RXVALID</td><td>VALIDH</td><td>DATA[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>X</td><td>Not used</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DATA[7:0] output is valid for receive
VALIDH is an output</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DATA[15:0] output is valid for receive
VALIDH is an output</td></tr>
<tr><td>1</td><td>X</td><td>0</td><td>DATA[7:0] input is valid for transmit
VALIDH is an input</td></tr>
<tr><td>1</td><td>X</td><td>1</td><td>DATA[15:0] input is valid for transmit
VALIDH is an input</td></tr>
<tr><td colspan="4">DATA BUS. 8-BIT UNIDIRECTIONAL MODE.</td></tr>
<tr><td>TXVALID</td><td>RXVALID</td><td colspan="2">DATA[15:0]</td></tr>
<tr><td>0</td><td>0</td><td colspan="2">Not used</td></tr>
<tr><td>0</td><td>1</td><td colspan="2">DATA[15:8] output is valid for receive</td></tr>
<tr><td>1</td><td>X</td><td colspan="2">DATA[7:0] input is valid for transmit</td></tr>
<tr><td>TXVALID</td><td>Input</td><td>High</td><td colspan="4">Transmit Valid. Indicates that the TXDATA bus is valid for transmit. The assertion of TXVALID initiates the transmission of SYNC on the USB bus. The negation of TXVALID initiates EOP on the USB.

Control inputs (OPMODE[1:0], TERMSELECT,XCVRSELECT) must not be changed on the de-assertion or assertion of TXVALID. The PHY must be in a quiescent state when these inputs are changed.</td></tr>
<tr><td>TXREADY</td><td>Output</td><td>High</td><td colspan="4">Transmit Data Ready. If TXVALID is asserted, the SIE must always have data available for clocking into the TX Holding Register on the rising edge of CLKOUT. TXREADY is an acknowledgement to the SIE that the transceiver has clocked the data from the bus and is ready for the next transfer on the bus. If TXVALID is negated, TXREADY can be ignored by the SIE.</td></tr>
<tr><td>VALIDH</td><td>Bidir</td><td>N/A</td><td colspan="4">Transmit/Receive High Data Bit Valid (used in 16-bit mode only). When TXVALID = 1, the 16-bit data bus direction is changed to inputs, and VALIDH is an input. If VALIDH is asserted, DATA[15:0] is valid for transmission. If deasserted, only DATA[7:0] is valid for transmission. The DATA bus is driven by the SIE.

When TXVALID = 0 and RXVALID = 1, the 16-bit data bus direction is changed to outputs, and VALIDH is an output. If VALIDH is asserted, the DATA[15:0] outputs are valid for receive. If deasserted, only DATA[7:0] is valid for receive. The DATA bus is read by the SIE.</td></tr>
<tr><td>RXVALID</td><td>Output</td><td>High</td><td colspan="4">Receive Data Valid. Indicates that the RXDATA bus has received valid data. The Receive Data Holding Register is full and ready to be unloaded. The SIE is expected to latch the RXDATA bus on the rising edge of CLKOUT.</td></tr>
</table>

Table 2 Data Interface Pins (continued)

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RXACTIVE	Output	High	**Receive Active.** Indicates that the receive state machine has detected Start of Packet and is active.
RXERROR	Output	High	**Receive Error.** 0: Indicates no error. 1: Indicates a receive error has been detected. This output is clocked with the same timing as the RXDATA lines and can occur at anytime during a transfer.

Table 3 USB I/O Pins

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
DP	I/O	N/A	**USB Positive Data Pin**.
DM	I/O	N/A	**USB Negative Data Pin**.

Table 4 Biasing and Clock Oscillator Pins

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
RBIAS	Input	N/A	**External 1% bias resistor**. Requires a 12KΩ resistor to ground. Used for setting HS transmit current level and on-chip termination impedance.
XI/XO	Input	N/A	**External crystal**. 12MHz crystal connected from XI to XO.

Table 5 Power and Ground Pins

NAME	DIRECTION	ACTIVE LEVEL	DESCRIPTION
VDD3.3	N/A	N/A	**3.3V Digital Supply**. Powers digital pads. See Note 2.1
VDD1.8	N/A	N/A	**1.8V Digital Supply**. Powers digital core.
VSS	N/A	N/A	**Digital Ground**. See Note 2.2
VDDA3.3	N/A	N/A	**3.3V Analog Supply**. Powers analog I/O and 3.3V analog circuitry.
VDDA1.8	N/A	N/A	**1.8V Analog Supply**. Powers 1.8V analog circuitry. See Note 2.1
VSSA	N/A	N/A	**Analog Ground**. See Note 2.2

Note 2.1 A Ferrite Bead (with DC resistance <.5 Ohms) is recommended for filtering between both the VDD3.3 and VDDA3.3 supplies and the VDD1.8 and VDDA1.8 Supplies.

Note 2.2 All VSS and VSSA are bonded to the exposed pad under the IC in the package. The exposed pad must be connected to solid GND plane on printed circuit board.

Application Diagram

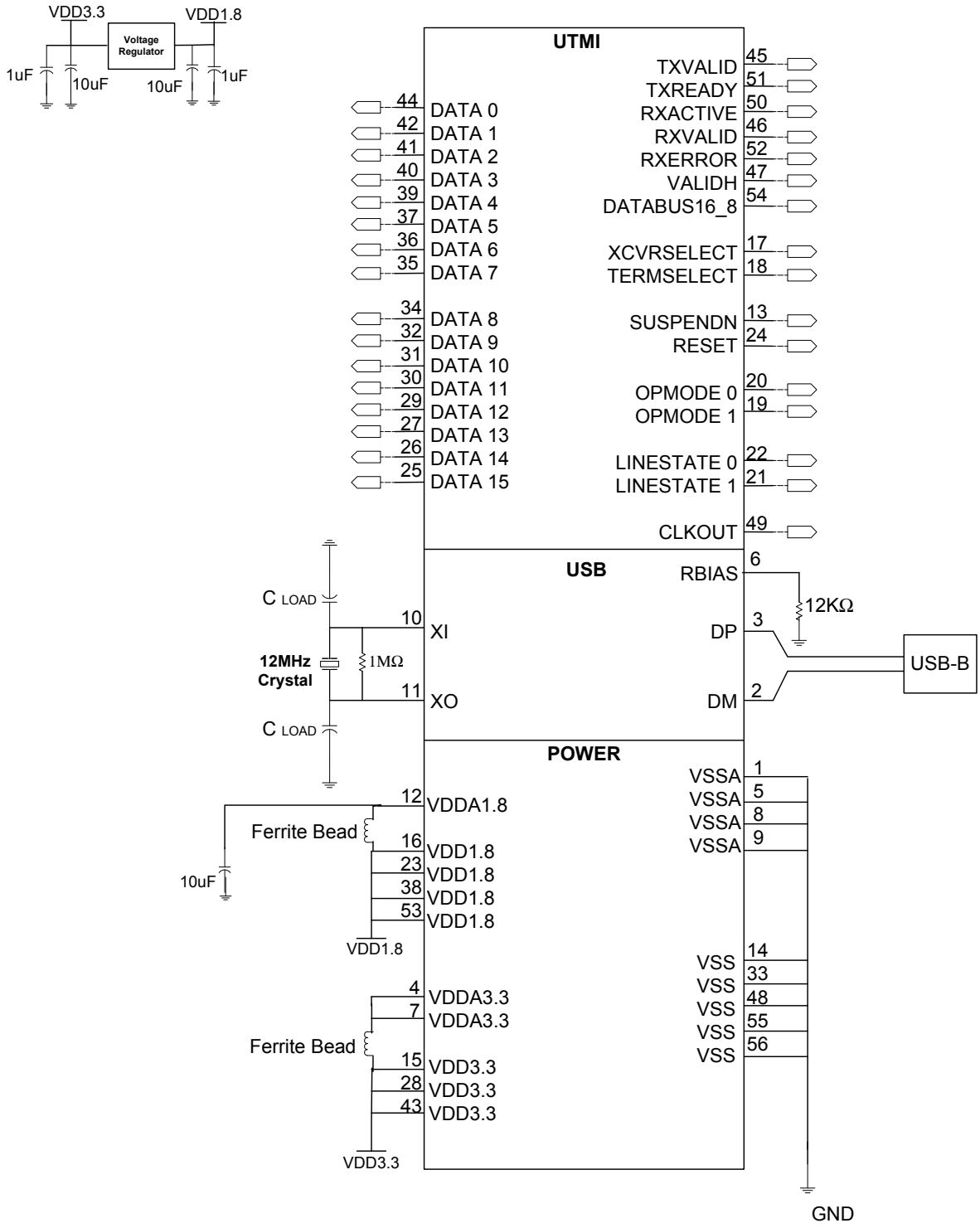
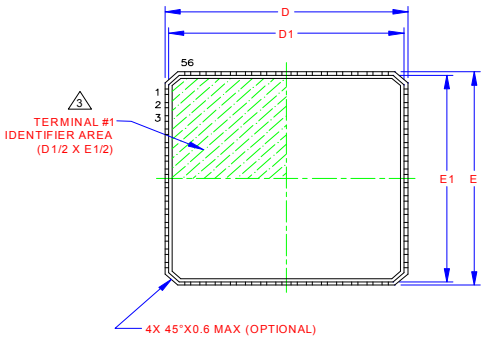
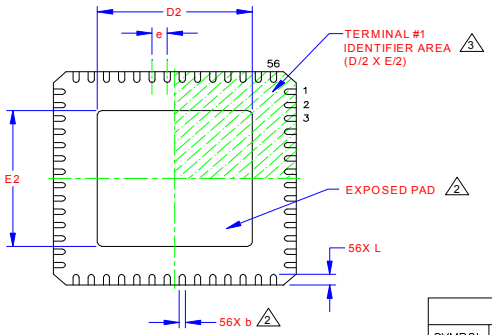


Figure 3 Application Diagram for 56-pin QFN Package

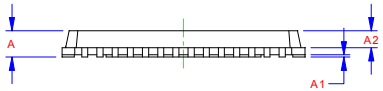
Package Outline



TOP VIEW



BOTTOM VIEW

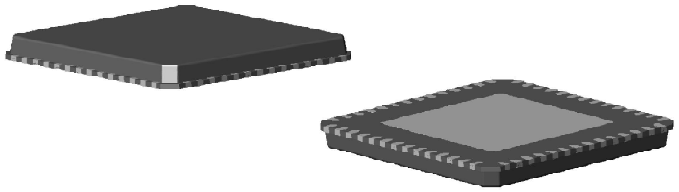


SIDE VIEW

REVISION HISTORY			
REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	2/07/04	S.K.ILIEV
B	REMOVE "PRELIMINARY" NOTE	10/7/04	S.K.ILIEV
C	L(MAX) FROM 0.55 TO 0.50. ADDED D2/E2 VARIATIONS TABLE	7/2/05	S.K.ILIEV

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	–	1.00	–	OVERALL PKG HEIGHT
A1	0	0.02	0.05	–	STANDOFF
A2	–	–	0.90	–	MOLD THICKNESS
D/E	7.85	8.00	8.15	–	"X"/"Y" BODY SIZE
D1/E1	7.55	–	7.95	–	"X"/"Y" MOLD SIZE
D2/E2	SEE VARIATIONS			–	"X"/"Y" EXPOSED PAD SIZE
L	0.30	–	0.50	–	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			–	TERMINAL PITCH

D2 / E2 VARIATIONS				
MIN	NOM	MAX	NOTE	CATALOG PART
4.15	4.30	4.45	–	USB3250, USB3500 & EMC2700



3-D VIEWS

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL X.X ±0.1, X.XX ±0.05, X.XXX ±0.025 ANGULAR ±1°
DIM AND TOL PER ASME Y14.5M - 1994
MATERIAL -
FINISH -
PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

	NAME	DATE
DRAWN	S.K.ILIEV	2/06/04
CHECKED	S.K.ILIEV	2/07/04
APPROVED	S.K.ILIEV	2/07/04

80 ARKAY DRIVE
HAUPPAUGE, NY 11788
USA

SMSC SUCCESS BY DESIGN

TITLE: PACKAGE OUTLINE
56 TERMINAL QFN, 8x8mm BODY, 0.5mm PITCH

DWG NUMBER: MO-56-QFN-8x8 REV: C

SCALE: 1:1 STD COMPLIANCE: JEDEC: MO-220 SHEET: 1 OF 1