KSZ8463MLI Evaluation Kit User Guide

Preliminary Revision 0.6 / September 26, 2011

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Introduction

The KSZ8463MLI Evaluation Kit provides network designers the opportunity of exploring the functionality and features of Micrel's KSZ8463 IEEE 1588 Precision Time Protocol (PTP) Enabled Switch product. The KSZ8463MLI device is a highly integrated 2-port 10/100Base-T/TX/FX managed Ethernet switch with MII interface connectivity to a Host on Port 3. It is an ideal solution in industrial applications where real time clock synchronization using Ethernet connectivity across a network is desired.

This KSZ8463MLI Evaluation Kit User Guide provides the information necessary to set up and use the KSZ8463MLI evaluation platform.

1 Tour of the Kit Contents

The KSZ8463MLI Evaluation Kit consists of three main elements; the Evaluation H/W Kit, the Evaluation S/W Kit, and this document you are reading. A description of the entire Evaluation Kit is broken out below.

(1) KSZ8463MLI Evaluation Kit User Guide

(2) KSZ8463MLI Evaluation H/W Kit
- 8463 Eval Board
- 8463 Eval Board User Guide
- 8463 Eval Board Schematics
- 8463 SPI Cable Assembly
- 8463 Interrupt Wire Assembly
- SOC Board
- SOC Board User Guide
- SOC Board Schematics
- 8463 IBIS File

(3) KSZ8463MLI Evaluation S/W Kit
- F/W that goes on SOC Board
- ptp_cli Linux Utility
- ptp Linux/windows Utility
- PTP Utilities User Guide
- PTP Development Guide

2 Setting up the KSZ8463MLI Evaluation Platform

During set up of the evaluation platform, please have ready and nearby the KSZ8463 Eval Board User Guide, the KSZ8463 Schematics, the SOC Eval Board User Guide, and the SOC Eval Board Schematics. This will make it easier to locate key components requiring configuration and/or modification.

2.1 Basic Hardware Setup

There are several configurations that can be set up for verifying the general functionality of all components. The first example setup consists of two pairs of KSZ8463/SOC boards connected together with one pair acting as the Grandmaster and the other pair as the Slave. The second example setup

consists of two pairs of KSZ8463/SOC boards and one external Grandmaster clock source. These example setups are shown in Figures 1 and 2.

Note that every setup requires a connection to a computer for communication with the boards. There are two ways to connect. Each SOC board has a serial port. A connection between the serial port on the board and the computer can be created. For those computers that do not have a serial port, a USB to serial port conversion product can be used to allow interfacing USB on the computer to the serial port on the SOC board. This method is shown is Figure 1. In addition, you can access the boards via Ethernet. In this case, an IEEE 1588 enabled switch can be introduced into the system to allow communication across the Ethernet cable. This method is advantageous in situations where multiple slaves are attached and hence communication to all SOC devices can occur over one link to the computer. A communication program of the user's choice can be used to facilitate the communication. This method is shown in Figure 2.

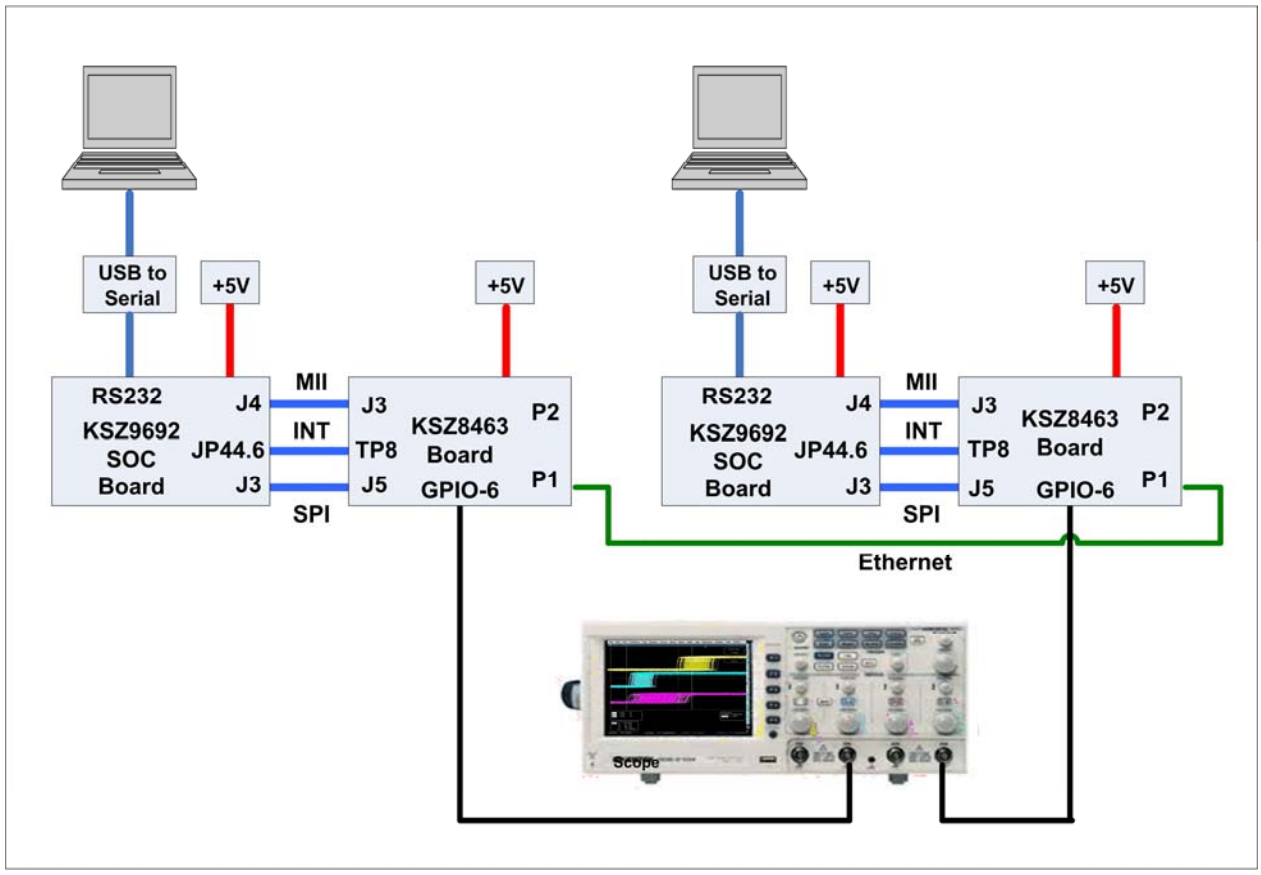

Figure 1 Basic Setup #1

Refer to the KSZ8463MLI/RLI Eval Board User Guide and the KSZ8463MLI/RLI Eval Board Schematics for details of the locations and usage of the various connectors, interfaces, and signal pins shown in Figures 1 and 2.

The +5V power can be supplied to each board via a common power supply or separate power supply modules dedicated to each board. You should allot around 1 amp per each board.

The MII interface is used to connect Port 3 of the KSZ8463 device to the SOC board. The network data is transferred across the MII interface. The MII interface is located on connector J3 on the KSZ8463 Eval

Board and on J4 on the SOC board. These two connectors are mating connectors and used to connect the two boards together.

The SPI interface is used by the processor on the SOC Board to communicate with the KSZ8463 device to read and write registers.

The Interrupt signal from the KSZ8463 device must be made available to the processor on the SOC board. The Figures indicate this connection.

Figure 3 is a photograph showing the actual connections of the two boards. Figure 4 shows more connection details on the SOC board.

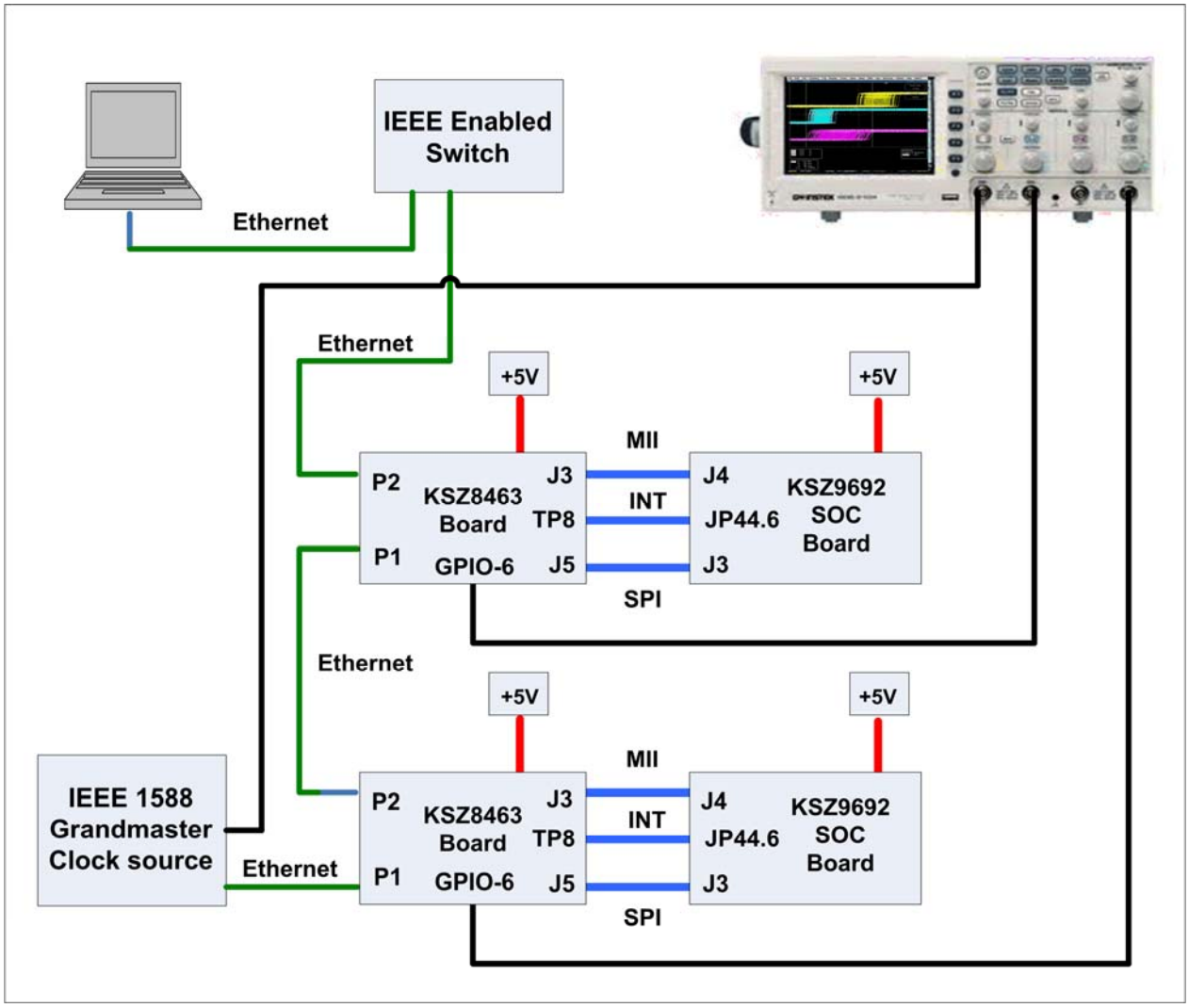

Figure 2 Basic Setup #2

About Setup #1

Setup #1 uses the onboard crystal on one of the KSZ8463 Eval Boards as the Grandmaster clock. This offers a convenient way to investigate PTP behavior without the use of a more expensive GPS based Grandmaster clock source. Each SOC board is connected to a separate computer using the RS232 interface. The onboard firmware is set up to configure the KSZ8463's GPIO-6 pin as a 1 pulse per second

signal (PPS). In this set up, the oscilloscope is used to monitor the two “1 PPS” signals; one which is the Grandmaster clock and the other which is generated by the slave. The oscilloscope can show the jitter and difference between the Grandmaster clock and the clock created by the slave.

About Setup #2

Setup #2 uses a GPS Based Network Time Server/PTP Grandmaster Clock Unit to generate the reference clock for the system. A precision time signal is received via GPS and is used as the Grandmaster clock in the PTP protocol. This is the clock information that is distributed to all the network nodes in the Evaluation Kit. Only one computer is used. This computer uses the Ethernet network to communicate inband to all the boards attached on the local PTP network. The onboard firmware that is preloaded on the SOC board is set up to configure the KSZ8463’s GPIO-6 pin as a 1 pulse per second signal (PPS). In this set up, the oscilloscope is used up to monitor the Grandmaster clock and the two “1 PPS” signals which are generated from the Grandmaster clock. The oscilloscope can show the jitter and difference between the Grandmaster clock and the clocks created by the slaves.

Suggested Power Up Sequence

After all the pieces are connected, it is suggested that the 8463 Eval Board be powered up first followed by the SOC Board and then the computer. This is generally the order of power up that should be followed every time the system is powered up.

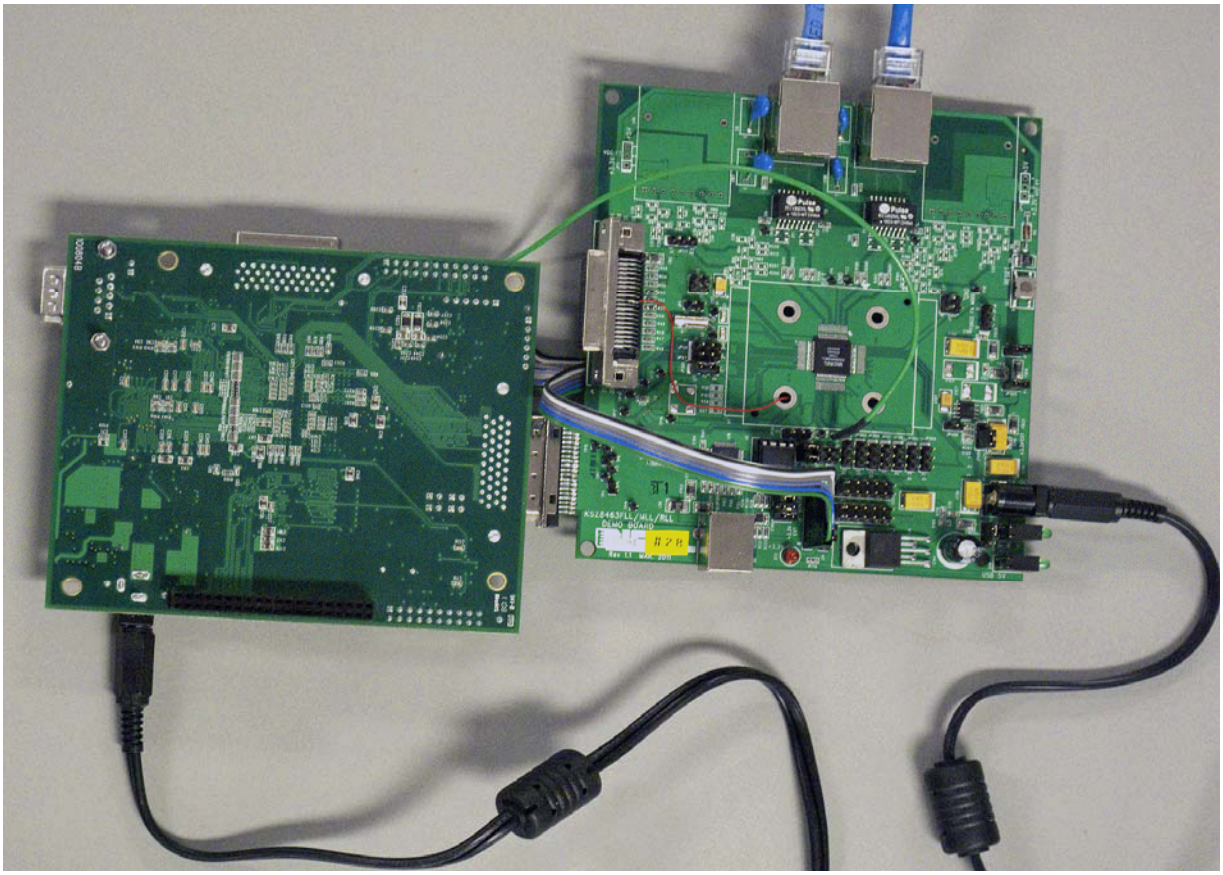

Figure 3 KSZ8463MLI/RLI Eval Board & SOC Board

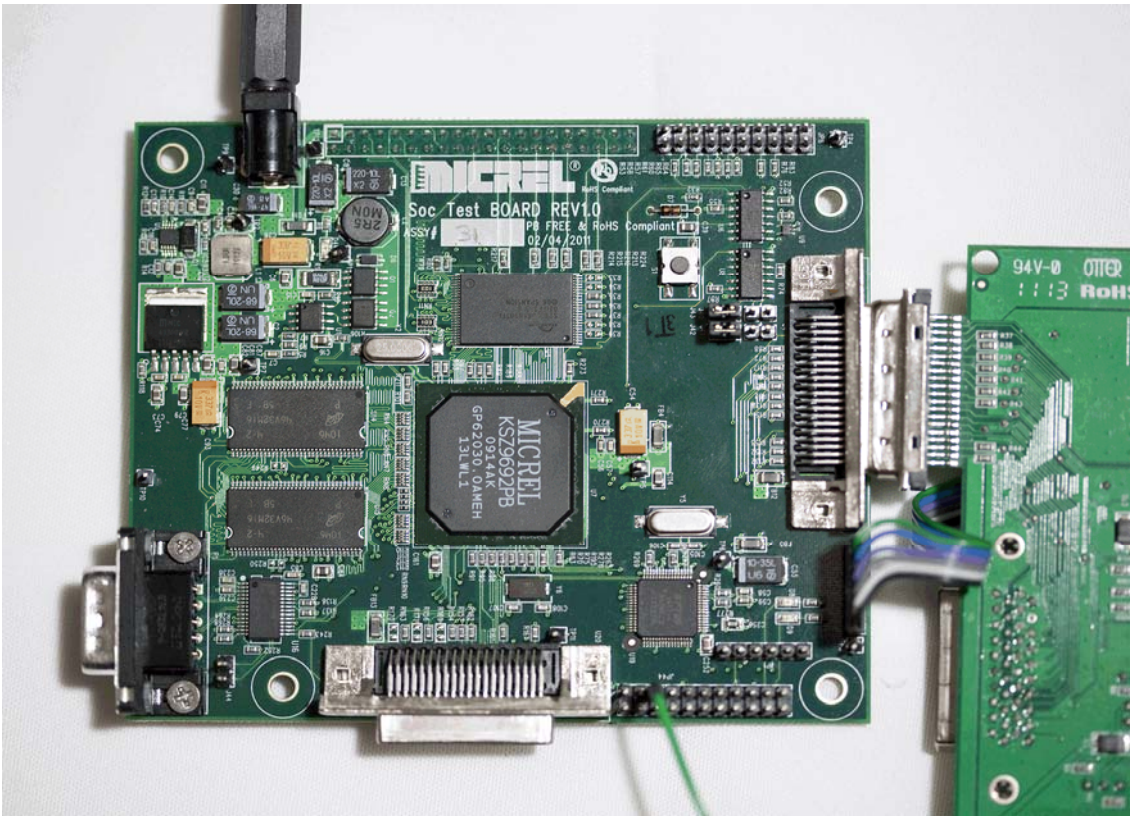

Figure 4 SOC Board Connections

2.2 Setting up the Software and Firmware

The SOC board comes loaded with a Linux 2.6 environment with a Micrel 1588 PTP Stack. This is the engine that drives the PTP protocol across a network utilizing Micrel KSZ84xx based devices. In order to talk to this environment, the computer must be set up with a communication program of the users choice. In order to successfully communicate with the firmware on the SOC board, the communication program should be set up for 115,200 BAUD rate and 8 bits, no parity, and 1 stop bit (8N1).

When the SOC Board and the PC are communicating, you should see activity as indicated in Figure 4 with some final communication ending with the Linux OS prompt being displayed in the command line window as shown in Figure 5.

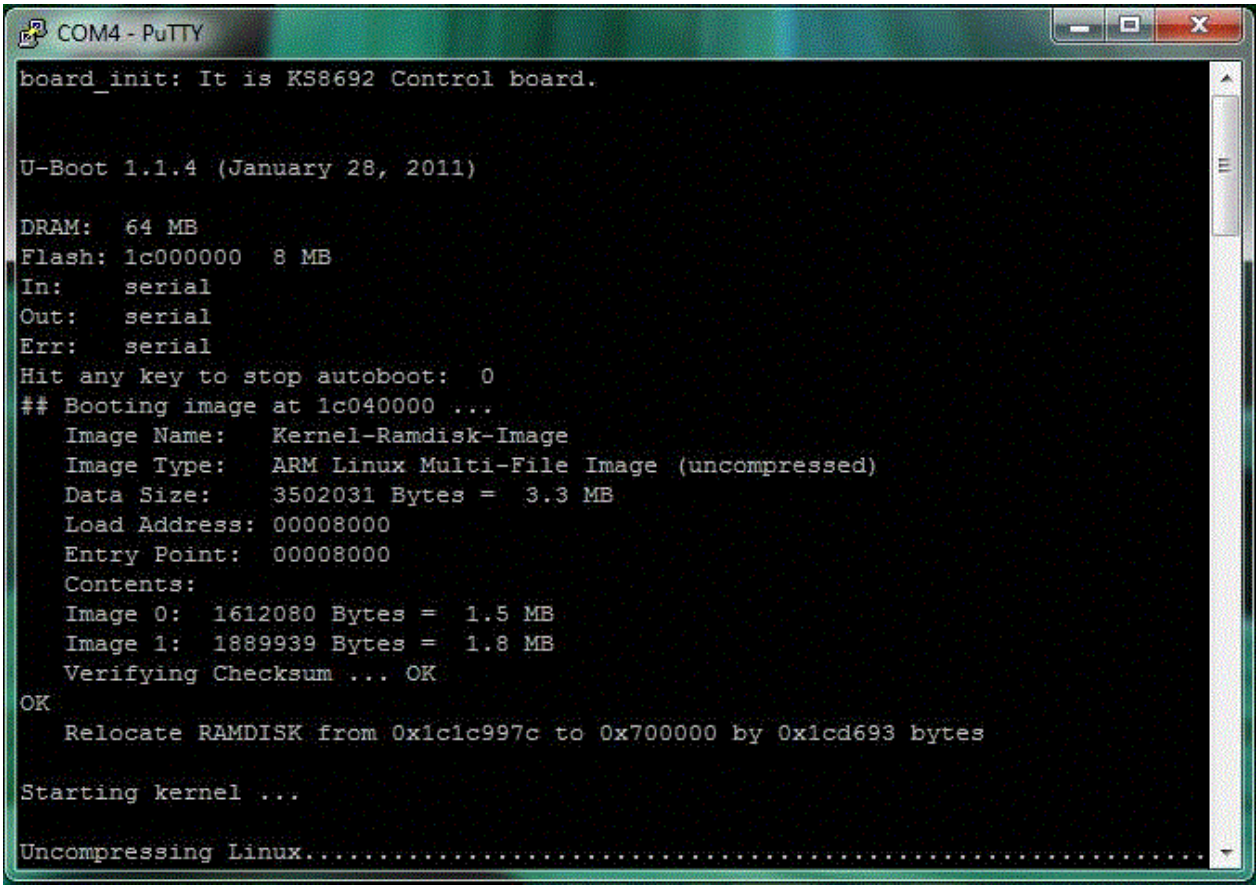

Figure 5 Startup of Communication Activity

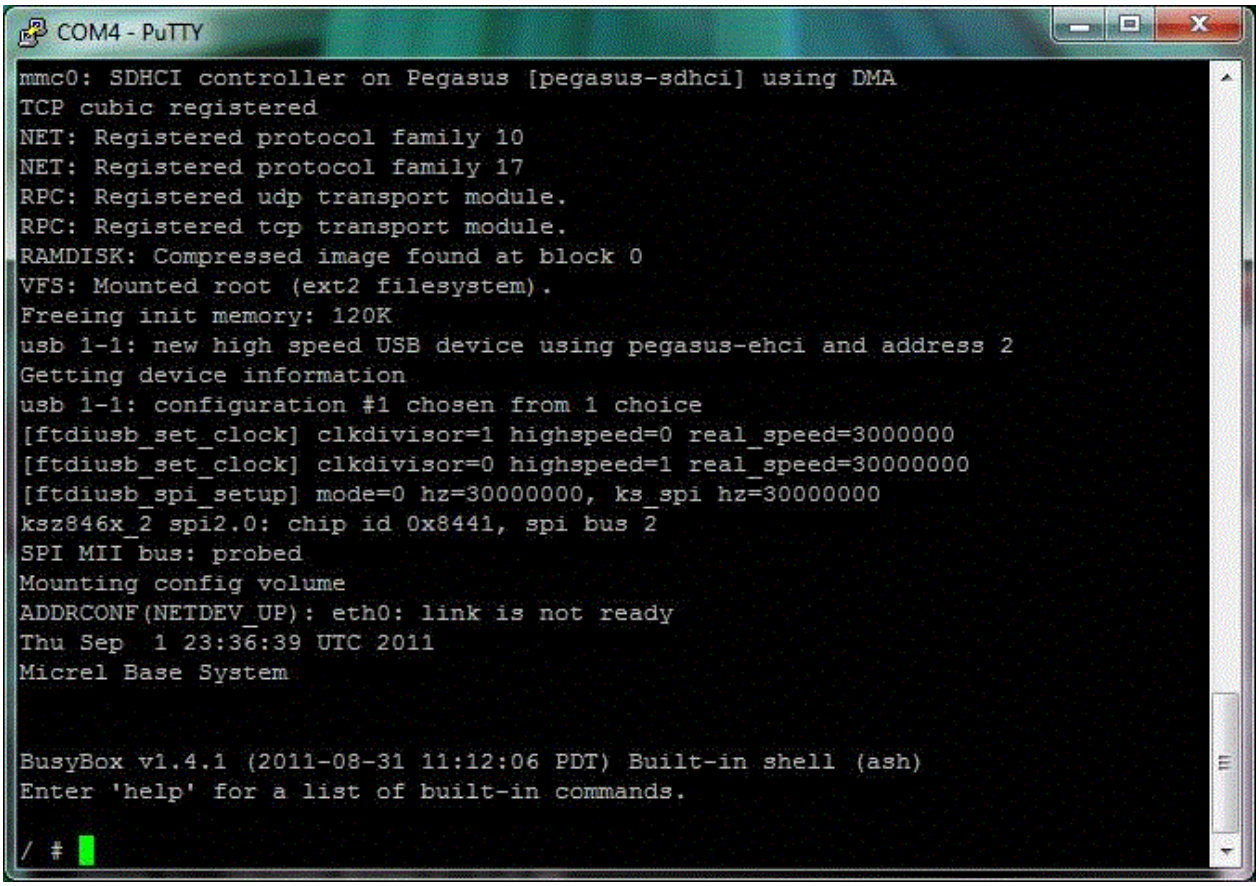

Figure 6 Linux Prompt - Communication OK

Each SOC board is shipped with a unique IP address so multiple SOC boards can be configured in a single PTP network and communication can occur between the PC and any specific board. The IP address is stored in the onboard f/w as a parameter. Each IP address will take on the form xxxxxx10.32.2.sn where “sn” is the serial number of the SOC board. In systems where the network is not used to communicate between the PC and the SOC board, you must connect the USB Serial port to the specific SOC board that you want to communicate with.

There are two utilities which are supplied with the Evaluation Kit. One is called ptp_cli and the other is called ptp.exe. These utilities allow the user to interact and explore the functionality of the KSZ84xx PTP environment.

2.2.1 ptp_cli Utility

The ptp_cli utility runs in the Linux environment and comes shipped installed on the SOC board. This is a command line utility that can be used to control the PTP hardware. This utility can read and write all registers within the KSZ8463 device. As such, it can also be used to set up GPIO pins to generate user defined waveforms with respect to the PTP clock. Refer to the Micrel PTP Utilities User guide for detailed information.

2.2.2 ptp Utility

The ptp utility can be compiled to run in either the Linux environment or the Windows environment. The SOC board that is shipped with the Evaluation Kit, has it already installed in the onboard Linux environment. A version has been compiled to run in the Windows environment. It is called ptp.exe and is available for those customers requiring that usage.

The ptp utility provides a mechanism for sending PTP messages for testing and development of the PTP platform. Refer to the Micrel PTP Utilities User guide for detailed information.

3 Using the KSZ8463MLI Evaluation Platform

The Evaluation Kit is intended to provide a platform that enables designers to investigate and evaluate the capabilities of the KSZ8463 device. It is not intended to be a complete development system to be used for an entire product design effort.

While much work and development can be accomplished by using the basic setup shown in Figure 1, the setup described in Figure 2 offers a more realistic and robust environment in which to work. There are other setups and topologies that can be evaluated and is limited only by the imagination of the user. This section offers a few suggestions of activities that can be undertaken with the use of this Evaluation Kit.

Investigation of Various PTP Topology Parameters

- Point to Point topology
- End to End Topology
- One Step PTP operation
- Two Step PTP operation
- Multiple masters
- Best of Master algorithm

GPIO/Input-Timestamp/Output Triggering

- Creation of register settings to generate custom waveforms on the GPIO outputs
- Creation of register setting to intercept and recognize waveforms at the GPIO inputs

PTP Protocol Execution Under Varying NetworkTraffic Patterns

- Introducing the desired network traffic into the switch

4 Frequently Asked Questions and Help

Hopefully you will find the answers to your questions here before needing to contact Micrel for assistance.

4.1 Frequently Asked Questions

Q1. How many KSZ8463 Evaluation Boards can I put into the system to test out the PTP environment?

A1. The software currently has a limitation of 64 nodes for the Master to keep track of. Any value over that may cause issues depending on the nature of the traffic.

Q2. If the system hangs and stops functioning, what is the best recovery procedure to follow?

A2. There is a reset switch on both boards. Reset the boards to attempt recovery.

Q3. How should the oscilloscope be set up to properly monitor the 1 PPS signals from the KSZ8463 Evaluation boards and the Grandmaster or Master source?

A3. Typically, the 1 PPS signal from the Grandmaster or Master node is used as the trigger on channel one of the oscilloscope. Channel 2 is connected to the 1 PPS signal on one of the other KSZ8463 Evaluation boards. The 1 PPS signal is generated on the GPIO6 signal pin. If the oscilloscope has a persistence feature, it can be used to view accumulating past occurrences of the signal on channel two with respect to the 1 PPS signal on channel 1. Depending on the oscilloscope used, there is other statistical analysis that can be performed on the signals. Figure 6 illustrates an oscilloscope signal capture.

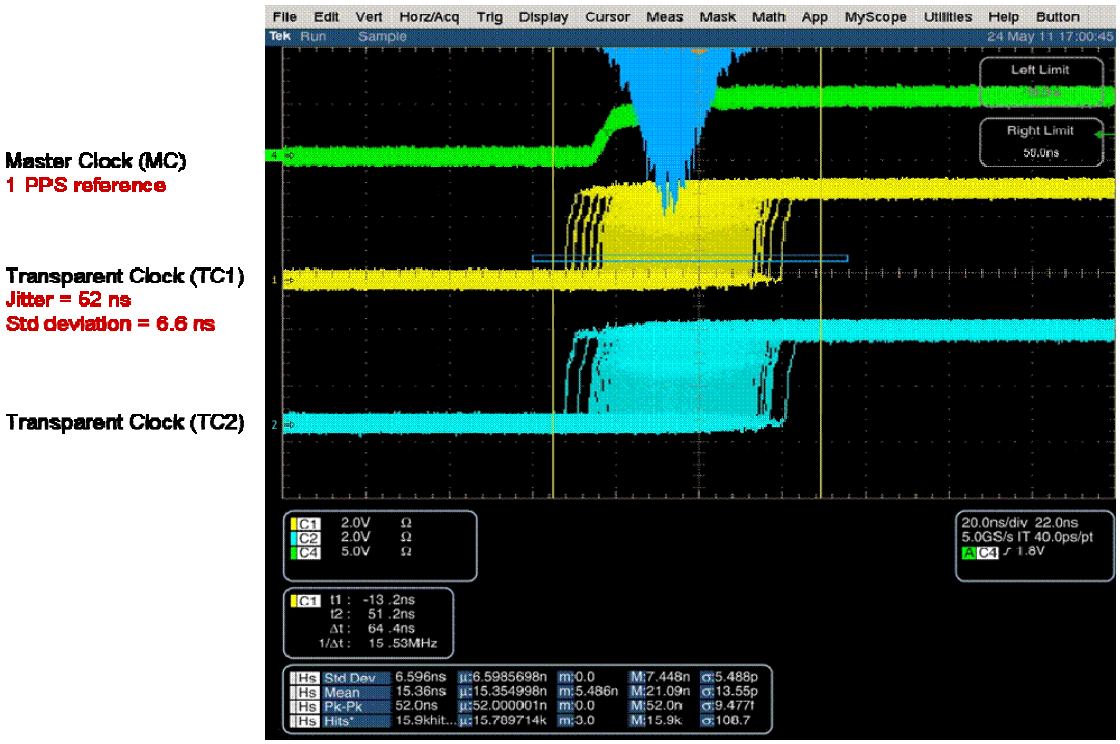

Figure 7 Sample 1 PPS Oscilloscope Capture

Q4. How do I update the onboard SOC firmware to the latest revision available from Micrel?

A4. There are two sections of the onboard firmware; the U-Boot section which rarely gets modified and the regular code area which gets updated periodically as needed. Micrel has a document available which goes over the details of updating either section.

4.2 Help!

For assistance, contact your Micrel representative at the following location.

http://www.micrel.com/help_Info.jsp

5 Reference Material

KSZ8463MLI/RLI Datasheet (Contact Micrel for latest Datasheet)
IEEE 802.3 Specification
RMII Specification by RMII Consortium
IEEE 1588 Specification

6 Revision History

Revision	Date	Summary of Changes
0.1	08/09/11	- Initial Release
0.2	08/09/11	- Updated Fig. 1 & 2.
0.3	09/07/11	- Added Figure 4, 5, and 6. - Updated many areas with better text
0.4	09/12/11	- Added Figure 4 for SOC Board Connections - Updated FAQ area.
0.5	09/23/11	- Changed part number from MLL to MLI - Embedded word “Preliminary into header/footer”.
0.6	09/26/11	- Added cable and wire assembly to 8463 board items. - Cleaned up page breaks. - Re-did TOC, TOC for Figures.

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