KSZ8081RNA/KSZ8081RND

10Base-T/100Base-TX PHY with RMII Support

Data Sheet Rev. 1.0

General Description

The KSZ8081RNA is a single-supply 10Base-T/100Base-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8081RNA is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering 1.8/2.5/3.3V digital I/O interface support.

The KSZ8081RNA offers the Reduced Media Independent Interface (RMII) for direct connection to RMII-compliant MACs in Ethernet processors and switches.

As the power-up default, the KSZ8081RNA uses a 25MHz crystal to generate all required clocks, including the 50MHz RMII reference clock output for the MAC. The KSZ8081RND is the version that takes in the 50MHz RMII reference clock as the power-up default.

To facilitate system bring-up and debugging in production testing and in product deployment, parametric NAND tree support enables fault detection between KSZ8081RNA I/Os and the board. Micrel's LinkMD® TDR-based cable diagnostics identify faulty copper cabling.

The KSZ8081RNA and KSZ8081RND are available in 24-pin, lead-free QFN packages (see "Ordering Information").

Data sheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Single-chip 10Base-T/100Base-TX IEEE 802.3 compliant Ethernet transceiver
- RMII v1.2 Interface support with a 50MHz reference clock output to MAC, and an option to input a 50MHz reference clock
- RMII back-to-back mode support for a 100Mbps copper repeater
- MDC/MDIO management interface for PHY register configuration
- Programmable interrupt output
- LED outputs for link and activity status indication
- On-chip termination resistors for the differential pairs
- Baseline wander correction
- HP Auto MDI/MDI-X to reliably detect and correct straight-through and crossover cable connections with disable and enable option
- Auto-negotiation to automatically select the highest link-up speed (10/100Mbps) and duplex (half/full)
- Power-down and power-saving modes
- LinkMD TDR-based cable diagnostics to identify faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and the board

Functional Diagram
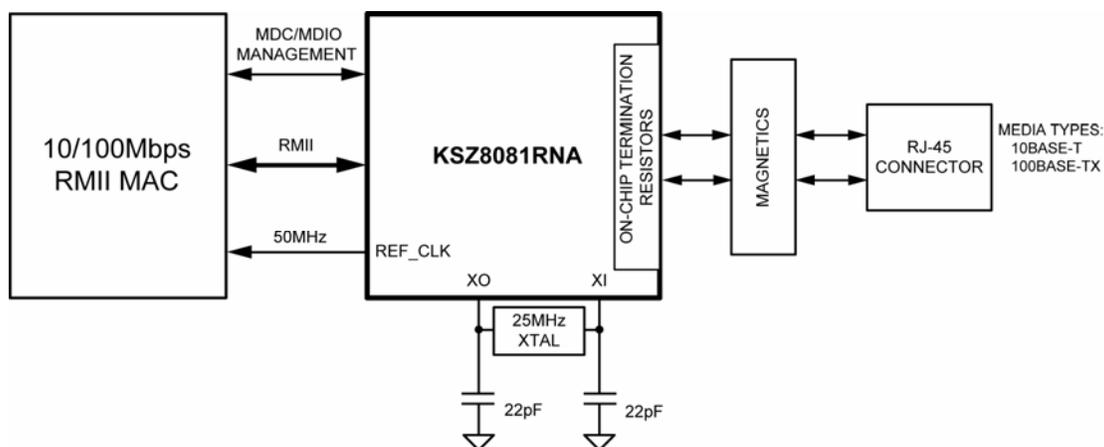
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Features (Continued)

- Loopback modes for diagnostics
- Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V
- Built-in 1.2V regulator for core
- Available in 24-pin (4mm x 4mm) QFN package

Applications

- Game console
- IP phone
- IP set-top box
- IP TV
- LOM
- Printer

Ordering Information

Part Number	Temperature Range	Package	Lead Finish	Wire Bonding	Description
KSZ8081RNACA	0°C to 70°C	24-Pin QFN	Pb-Free	Gold	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Commercial Temperature, Gold Wire Bonding
KSZ8081RNACC[1]	0°C to 70°C	24-Pin QFN	Pb-Free	Copper	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Commercial Temperature, Copper Wire Bonding
KSZ8081RNAIA[1]	−40°C to 85°C	24-Pin QFN	Pb-Free	Gold	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Industrial Temperature, Gold Wire Bonding
KSZ8081RNAIC[1]	−40°C to 85°C	24-Pin QFN	Pb-Free	Copper	RMII with 25MHz crystal/clock input and 50MHz RMII REF_CLK output (power-up default), Industrial Temperature, Copper Wire Bonding
KSZ8081RNDCA	0°C to 70°C	24-Pin QFN	Pb-Free	Gold	RMII with 50MHz clock input (power-up default), Commercial Temperature, Gold Wire Bonding
KSZ8081RNDCC[1]	0°C to 70°C	24-Pin QFN	Pb-Free	Copper	RMII with 50MHz clock input (power-up default), Commercial Temperature, Copper Wire Bonding
KSZ8081RNA-EVAL	0°C to 70°C	24-Pin QFN	Pb-Free		KSZ8081RNA Evaluation Board (Mounted with KSZ8081RNA device in commercial temperature)
KSZ8081RND-EVAL	0°C to 70°C	24-Pin QFN	Pb-Free		KSZ8081RND Evaluation Board (Mounted with KSZ8081RND device in commercial temperature)

Note:

1.   Contact factory for lead time.

Revision History

Revision	Date	Summary of Changes
1.0	11/05/12	Data sheet created

Contents

List of Figures

List of Tables

Pin Configuration

24-Pin (4mm x 4mm) QFN

Pin Description

Pin Number	Pin Name	Type[1]	Pin Function
1	VDD_1.2	P	1.2V core V_{DD} (power supplied by KSZ8081RNA/KSZ8081RND)
			Decouple with 2.2µF and 0.1µF capacitors to ground.
2	VDDA_3.3	P	3.3V analog V_{DD}
3	RXM	I/O	Physical receive or transmit signal (− differential)
4	RXP	I/O	Physical receive or transmit signal (+ differential)
5	TXM	I/O	Physical transmit or receive signal (− differential)
6	TXP	I/O	Physical transmit or receive signal (+ differential)
7	XO	O	Crystal feedback for 25MHz crystal
			This pin is a no connect if an oscillator or external clock source is used.
8	XI	I	RMII – 25MHz Mode: 25MHz ±50ppm Crystal / Oscillator / External Clock Input
			RMII – 50MHz Mode: 50MHz ±50ppm Oscillator / External Clock Input
			For unmanaged mode (power-up default setting),
			KSZ8081RNA takes in the 25MHz crystal/clock on this pin.
			KSZ8081RND takes in the 50MHz clock/on this pin.
			After power-up, both the KSZ8081RNA and KSZ8081RND can be programmed to either the 25MHz mode or 50MHz mode using PHY register 1Fh bit [7].
			See also REF_CLK (pin 16).
9	REXT	I	Set PHY transmit output current
			Connect a 6.49kΩ resistor to ground on this pin.
10	MDIO	Ipu/Opu	Management Interface (MII) Data I/O
			This pin has a weak pull-up, is open-drain, and requires an external 1.0kΩ pull-up resistor.
11	MDC	Ipu	Management Interface (MII) Clock input
			This clock pin is synchronous to the MDIO data pin.
12	RXD1	Ipd/O	RMII Receive Data Output[1][2]
13	RXD0	Ipu/O	RMII Receive Data Output[0][2]
14	VDDIO	P	3.3V, 2.5V, or 1.8V digital VDD
15	CRS_DV / PHYAD[1:0]	Ipd/O	RMII Mode: Carrier Sense/Receive Data Valid output /
			Config Mode: The pull-up/pull-down value is latched as PHYAD[1:0] at the de-assertion of reset.
			See the "Strapping Options" section for details.
16	REF_CLK	Ipd/O	RMII – 25MHz Mode: This pin provides the 50MHz RMII reference clock output to the MAC.
			RMII – 50MHz Mode: This pin is a no connect.
			For unmanaged mode (power-up default setting),
			KSZ8081RNA is in RMII – 25MHz mode and outputs the 50MHz RMII reference clock on this pin.
			KSZ8081RND is in RMII – 50MHz mode and does not use this pin.
			After power-up, both KSZ8081RNA and KSZ8081RND can be programmed to either 25MHz mode or 50MHz mode using PHY register 1Fh bit [7].
			See also XI (pin 8).
17	RXER	Ipd/O	RMII Receive Error output

Pin Number	Pin Name	Type[1]	Pin Function
18	INTRP	Ipu/Opu	Interrupt output: Programmable interrupt output This pin has a weak pull-up, is open drain, and requires an external 1.0kΩ pull-up resistor.
19	TXEN	I	RMII Transmit Enable input
20	TXD0	I	RMII Transmit Data Input[0][3]
21	TXD1	I/O	RMII Transmit Data Input[1][3] NAND Tree mode: NAND Tree output pin
22	GND	Gnd	Ground
23	LED0 / ANEN_SPEED	Ipu/O	LED output: Programmable LED0 output Config mode: Latched as auto-negotiation enable (register 0h, bit [12]) and Speed (register 0h, bit [13]) at the de-assertion of reset. See the "Strapping Options" section for details. The LED0 pin is programmable using register 1Fh bits [5:4], and is defined as follows. **LED mode = [00]** | Link/Activity	Pin State	LED Definition
---	---	---
No link	High	OFF
Link	Low	ON
Activity	Toggle	Blinking | **LED mode = [01]** | Link	Pin State	LED Definition
---	---	---
No link	High	OFF
Link	Low	ON	 **LED mode = [10], [11]** Reserved
24	RST#	Ipu	Chip reset (active low)
PADDLE	GND	Gnd	Ground

Notes:

1. P = Power supply.

    Gnd = Ground.

    I = Input.

    O = Output.

    I/O = Bi-directional.

    Ipu = Input with internal pull-up (see "Electrical Characteristics" for value).

    Ipu/O = Input with internal pull-up (see "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

    Ipd/O = Input with internal pull-down (see "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

    Ipu/Opu = Input with internal pull-up (see "Electrical Characteristics" for value) and output with internal pull-up (see "Electrical Characteristics" for value).

2. RMII RX Mode: The RXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent by the PHY to the MAC.

3. RMII TX Mode: The TXD[1:0] bits are synchronous with the 50MHz RMII Reference Clock. For each clock period in which TXEN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options

Pin Number	Pin Name	Type[1]	Pin Function
15	PHYAD[1:0]	Ipd/O	The PHY Address is latched at the de-assertion of reset and is configurable to either one of the following two values: Pull-up = PHY Address is set to 00011b (0x3h) Pull-down (default) = PHY Address is set to 00000b (0x0h) PHY Address bits [4:2] are set to 000 by default.
23	ANEN_SPEED	Ipu/O	Auto-Negotiation Enable and SPEED mode Pull-up (default) = Enable Auto-Negotiation and set 100Mbps Speed Pull-down = Disable Auto-Negotiation and set 10Mbps Speed At the de-assertion of reset, this pin value is latched into register 0h bit [12] for Auto-negotiation enable/disable, register 0h bit [13] for the Speed select, and register 4h (Auto-Negotiation Advertisement) for the Speed capability support.

Note:

1. Ipu/O = Input with internal pull-up (see "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

    Ipd/O = Input with internal pull-down (see "Electrical Characteristics" for value) during power-up/reset; output pin otherwise.

The PHYAD[1:0] strap-in pin is latched at the de-assertion of reset. In some systems, the RMII MAC receive input pins may drive high/low during power-up or reset, and consequently cause the PHYAD[1:0] strap-in pin, a shared pin with the RMII CRS_DV signal, to be latched to the unintended high/low state. In this case an external pull-up (4.7kΩ) or pull-down (1.0kΩ) should be added on the PHYAD[1:0] strap-in pin to ensure that the intended value is strapped-in correctly.

Functional Description: 10Base-T/100Base-TX Transceiver

The KSZ8081RNA is an integrated single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3 Specification, and reduces board cost and simplifies board layout by using on-chip termination resistors for the two differential pairs and by integrating the regulator to supply the 1.2V core.

On the copper media side, the KSZ8081RNA supports 10Base-T and 100Base-TX for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable, and HP Auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

On the MAC processor side, the KSZ8081RNA offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches

The MII management bus option gives the MAC processor complete access to the KSZ8081RNA control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

As the power-up default, the KSZ8081RNA uses a 25MHz crystal to generate all required clocks, including the 50MHz RMII reference clock output for the MAC. The KSZ8081RND version uses the 50MHz RMII reference clock as the power-up default.

The KSZ8081RNA is used to refer to both KSZ8081RNA and KSZ8081RND versions in this data sheet.

100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B encoding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding and followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 6.49kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

100Base-TX Receive

The 100Base-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion is a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal to NRZ format. This signal is sent through the de-scrambler, then the 4B/5B decoder. Finally, the NRZ serial data is converted to MII format and provided as the input data to the MAC.

Scrambler/De-Scrambler (100Base-TX Only)

The scrambler spreads the power spectrum of the transmitted signal to reduce electromagnetic interference (EMI) and baseline wander. The de-scrambler recovers the scrambled signal.

10Base-T Transmit

The 10Base-T drivers are incorporated with the 100Base-TX drivers to allow for transmission using the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output 10Base-T signals with a typical amplitude of 2.5V peak. The 10Base-T signals have harmonic contents that are at least 27dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

10Base-T Receive

On the receive side, input buffer and level detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV, or with short pulse widths, to prevent noise at the RXP and RXM inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8081RNA/RND decodes a data frame. The receive clock is kept active during idle periods between data receptions.

PLL Clock Synthesizer

The KSZ8081RNA/RND in RMII – 25MHz Clock mode generates all internal clocks and all external clocks for system timing from an external 25MHz crystal, oscillator, or reference clock. For the KSZ8081RNA/RND in RMII – 50MHz clock mode, these clocks are generated from an external 50MHz oscillator or system clock.

Auto-Negotiation

The KSZ8081RNA/RND conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest priority.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8081RNA/RND link partner is forced to bypass auto-negotiation, then the KSZ8081RNA/RND sets its operating mode by observing the signal at its receiver. This is known as parallel detection, which allows the KSZ8081RNA/RND to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

Auto-negotiation is enabled by either hardware pin strapping (ANEN_SPEED, pin 23) or software (register 0h, bit [12]).

By default, auto-negotiation is enabled after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled by register 0h, bit [12]. If auto-negotiation is disabled, the speed is set by register 0h, bit [13], and the duplex is set by register 0h, bit [8].

The auto-negotiation link-up process is shown in Figure 1.
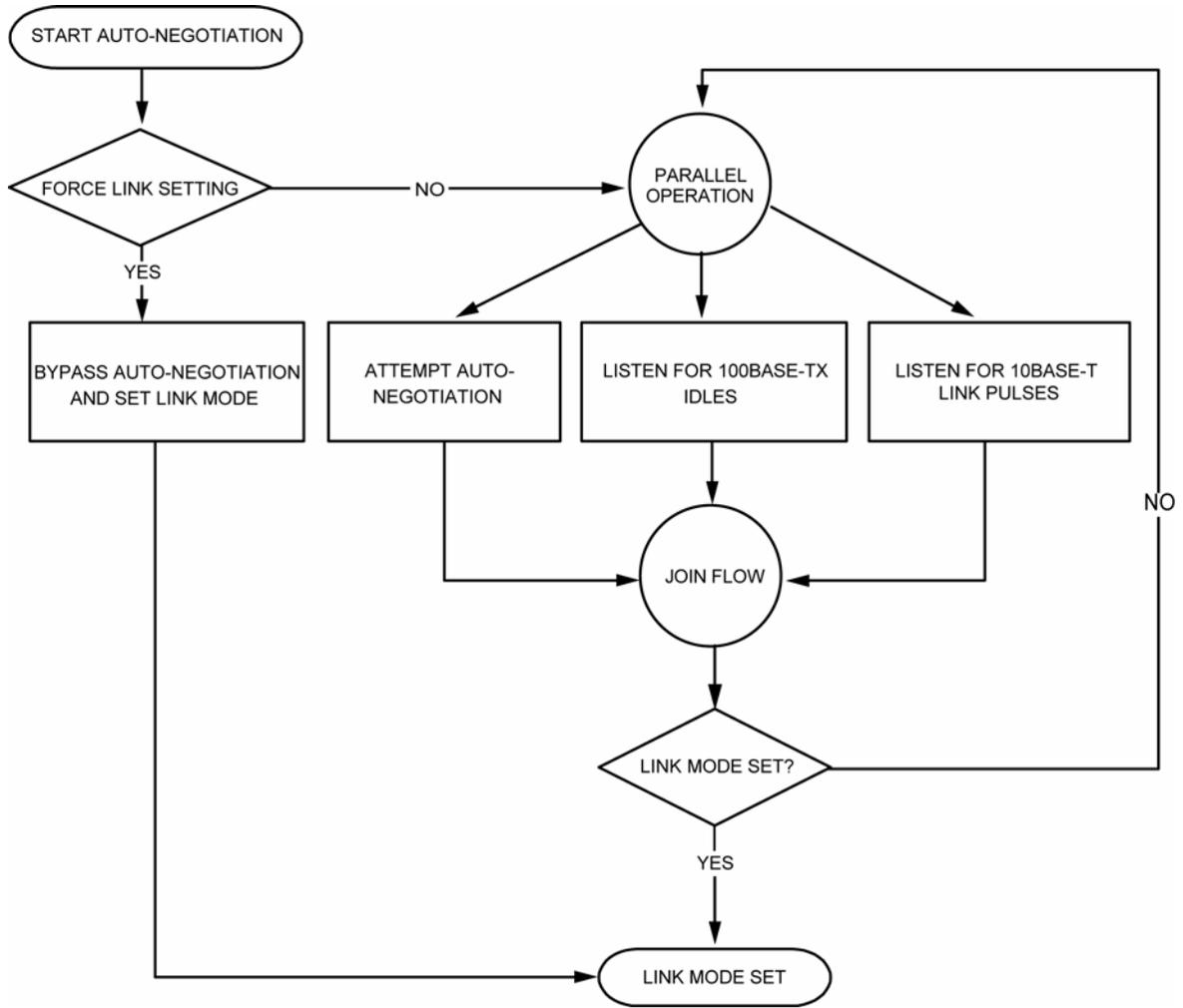
**Figure 1. Auto-Negotiation Flow Chart**

RMII Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Pin count is 8 pins (3 pins for data transmission, 4 pins for data reception, and 1 pin for the 50MHz reference clock).
- 10Mbps and 100Mbps data rates are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each 2 bits wide, a dibit.

RMII Signal Definition

Table 1 describes the RMII signals. Refer to RMII Specification v1.2 for detailed information.

RMII Signal Name	Direction (with respect to PHY, KSZ8081RNA/RND signal)	Direction (with respect to MAC)	Description
REF_CLK	Output (25MHz clock mode) / <no connect> (50MHz clock mode)	Input/ Input or <no connect>	Synchronous 50MHz reference clock for receive, transmit, and control interface
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data[1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data[1:0]
RXER	Output	Input, or (not required)	Receive Error

Table 1. RMII Signal Definition

Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for TXEN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

For RMII – 25MHz Clock Mode, the KSZ8081RNA/RND generates and outputs the 50MHz RMII REF_CLK to the MAC at REF_CLK (pin 16).

For RMII – 50MHz Clock Mode, the KSZ8081RNA/RND takes in the 50MHz RMII REF_CLK from the MAC or system board at XI (pin 8) and leaves the REF_CLK (pin 16) as no connect.

Transmit Enable (TXEN)

TXEN indicates that the MAC is presenting dibits on TXD[1:0] for transmission. It is asserted synchronously with the first dibit of the preamble and remains asserted while all dibits to be transmitted are presented on the RMII. It is negated before the first REF_CLK following the final dibit of a frame.

TXEN transitions synchronously with respect to REF_CLK.

Transmit Data[1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TXEN is asserted, the PHY accepts TXD[1:0] for transmission.

TXD[1:0] is 00 to indicate idle when TXEN is de-asserted. The PHY ignores values other than 00 on TXD[1:0] while TXEN is de-asserted.

Carrier Sense / Receive Data Valid (CRS_DV)

The PHY asserts CRS_DV when the receive medium is non-idle. It is asserted asynchronously when a carrier is detected. This happens when squelch is passed in 10Mbps mode, and when two non-contiguous 0s in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRS_DV.

While carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered dibit of the frame through the final recovered dibit. It is negated before the first REF_CLK that follows the final dibit. The data on RXD[1:0] is considered valid after CRS_DV is asserted. However, because the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is 00 until receive signals are properly decoded.

Receive Data[1:0] (RXD[1:0])

RXD[1:0] transitions synchronously with respect to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY.

RXD[1:0] is 00 to indicate idle when CRS_DV is de-asserted. The MAC ignores values other than 00 on RXD[1:0] while CRS_DV is de-asserted.

Receive Error (RXER)

RXER is asserted for one or more REF_CLK periods to indicate that a symbol error (for example, a coding error that a PHY can detect that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame being transferred from the PHY.

RXER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RXER has no effect on the MAC.

Collision Detection (COL)

The MAC regenerates the COL signal of the MII from TXEN and CRS_DV.

RMII Signal Diagram – 25/50MHz Clock Mode

The KSZ8081RNA/RND RMII pin connections to the MAC for 25MHz clock mode are shown in Figure 2. The connections for 50MHz clock mode are shown in Figure 3 .

RMII – 25MHz Clock Mode

The KSZ8081RNA is configured to RMII – 25MHz clock mode after it is powered up or hardware reset with the following:

- A 25MHz crystal connected to XI, XO (pins 8, 7), or an external 25MHz clock source (oscillator) connected to XI

The KSZ8081RND can optionally be configured to RMII – 25MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- A 25MHz crystal connected to XI, XO (pins 8, 7), or an external 25MHz clock source (oscillator) connected to XI
- Register 1Fh, bit [7] programmed to '1' to select RMII – 25MHz clock mode
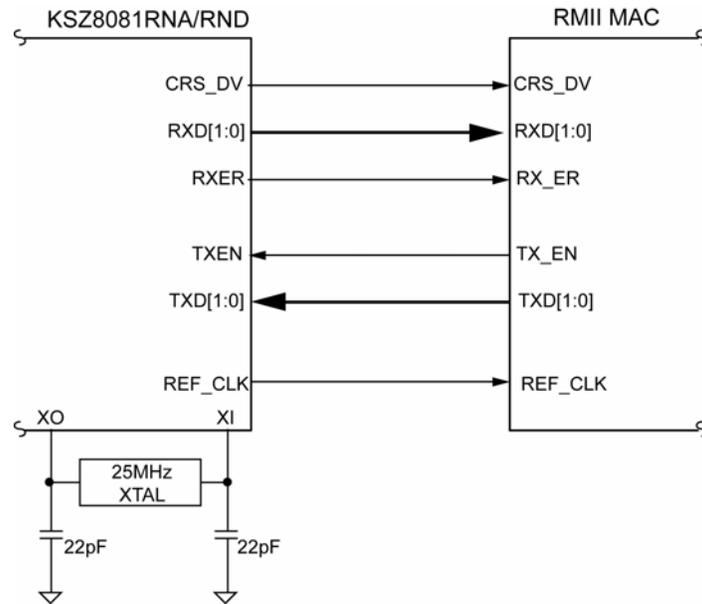
Figure 2. KSZ8081RNA/RND RMII Interface (RMII – 25MHz Clock Mode)

RMII – 50MHz Clock Mode

The KSZ8081RND is configured to RMII – 50MHz clock mode after it is powered up or hardware reset with the following:

- An external 50MHz clock source (oscillator) connected to XI (pin 8)

The KSZ8081RNA can optionally be configured to RMII – 50MHz clock mode after it is powered up or hardware reset and software programmed with the following:

- An external 50MHz clock source (oscillator) connected to XI (pin 8)
- Register 1Fh, bit [7] programmed to '1' to select RMII – 50MHz clock mode
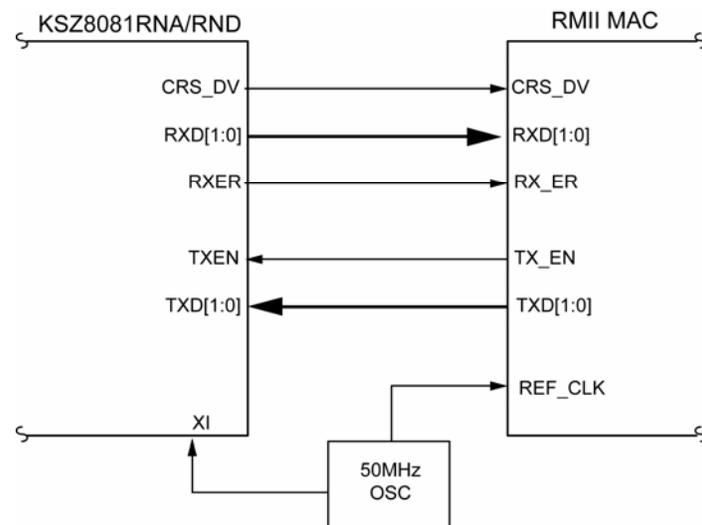
Figure 3. KSZ8081RNA/RND RMII Interface (RMII – 50MHz Clock Mode)

Back-to-Back Mode – 100Mbps Copper Repeater

Two KSZ8081RNA/RND devices can be connected back-to-back to form a managed 100Base-TX copper repeater.
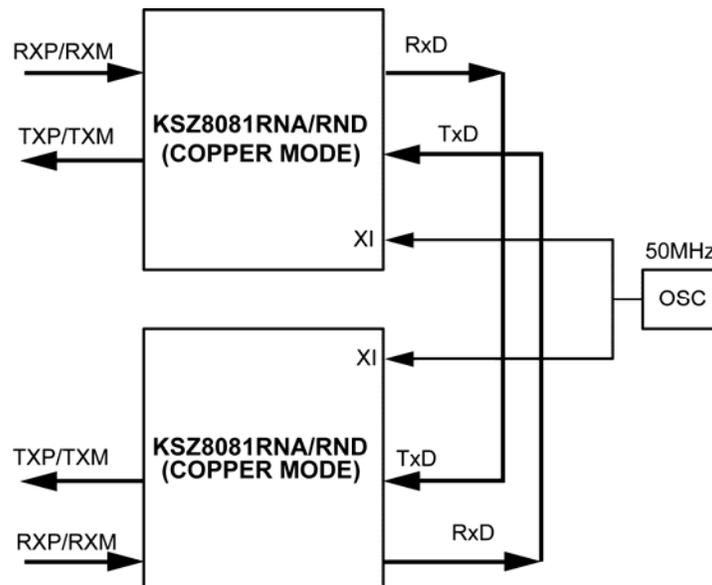
Figure 4. KSZ8081RNA/RND and KSZ8081RNA/RND RMII Back-to-Back Copper Repeater

RMII Back-to-Back Mode

In RMII back-to-back mode, a KSZ8081RNA/RND interfaces with another KSZ8081RNA/RND to provide a 100Mbps copper repeater solution.

The KSZ8081RNA/RND devices are configured to RMII back-to-back mode after power-up or reset, and software programming, with the following:

- A common 50MHz reference clock connected to XI (pin 8)
- Register 1Fh, bit [7] programmed to '1' to select RMII – 50MHz clock mode for KSZ8081RNA
  (KSZ8081RND is set to RMII – 50MHz clock mode as the default after power up or hardware reset)
- Register 16h, bits [6] and [1] programmed to '1' and '1', respectively, to enable RMII back-to-back mode.
- RMII signals connected as shown in Table 2

KSZ8081RNA/RND (100Base-TX copper) [Device 1]			KSZ8081RNA/RND (100Base-TX copper) [Device 2]		
Pin Name	Pin Number	Pin Type	Pin Name	Pin Number	Pin Type
CRS_DV	15	Output	TXEN	19	Input
RXD1	12	Output	TXD1	21	Input
RXD0	13	Output	TXD0	20	Input
TXEN	19	Input	CRS_DV	15	Output
TXD1	21	Input	RXD1	12	Output
TXD0	20	Input	RXD0	13	Output

Table 2. RMII Signal Connection for RMII Back-to-Back Mode (100Base-TX Copper Repeater)

MII Management (MIIM) Interface

The KSZ8081RNA/RND supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows an upper-layer device, such as a MAC processor, to monitor and control the state of the KSZ8081RNA/RND. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).

- A specific protocol that operates across the physical connection mentioned earlier, which allows the external controller to communicate with one or more PHY devices.

- A set of 16-bit MDIO registers. Registers [0:8] are standard registers, and their functions are defined in the IEEE 802.3 Specification. The additional registers are provided for expanded functionality. See the "Register Map" section for details.

The KSZ8081RNA/RND supports only two unique PHY addresses. The PHYAD[1:0] strapping pin is used to select either 0h or 3h as the unique PHY address for the KSZ8081RNA/RND device.

PHY address 0h is defined as the broadcast PHY address according to the IEEE 802.3 Specification, and can be used to read/write to a single PHY device, or write to multiple PHY devices simultaneously. For the KSZ8081RNA/RND, PHY address 0h defaults to the broadcast PHY address after power-up, but PHY address 0h can be disabled as the broadcast PHY address using software to assign it as a unique PHY address.

For applications that require two KSZ8081RNA/RND PHYs to share the same MDIO interface with one PHY set to address 0h and the other PHY set to address 3h, use PHY address 0h (defaults to broadcast after power-up) to set both PHYs' register 16h, bit [9] to '1' to assign PHY address 0h as a unique (non-broadcast) PHY address.

Table 3 shows the MII management frame format for the KSZ8081RNA/RND.

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	000AA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	000AA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Table 3. MII Management Frame Format for the KSZ8081RNA/RND

Interrupt (INTRP)

INTRP (pin 18) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8081RNA/RND PHY register. Bits [15:8] of register 1Bh are the interrupt control bits to enable and disable the conditions for asserting the INTRP signal. Bits [7:0] of register 1Bh are the interrupt status bits to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit [9] of register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII management bus option gives the MAC processor complete access to the KSZ8081RNA/RND control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the need to decide whether to use a straight cable or a crossover cable between the KSZ8081RNA/RND and its link partner. This feature allows the KSZ8081RNA/RND to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner and assigns transmit and receive pairs to the KSZ8081RNA/RND accordingly.

HP Auto MDI/MDI-X is enabled by default. It is disabled by writing a '1' to register 1Fh, bit [13]. MDI and MDI-X mode is selected by register 1Fh, bit [14] if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

Table 4 shows how the IEEE 802.3 Standard defines MDI and MDI-X.

MDI		MDI-X	
RJ-45 Pin	Signal	RJ-45 Pin	Signal
1	TX+	1	RX+
2	TX−	2	RX−
3	RX+	3	TX+
6	RX−	6	TX−

Table 4. MDI/MDI-X Pin Definition

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 5 shows a typical straight cable connection between a NIC card (MDI device) and a switch or hub (MDI-X device).
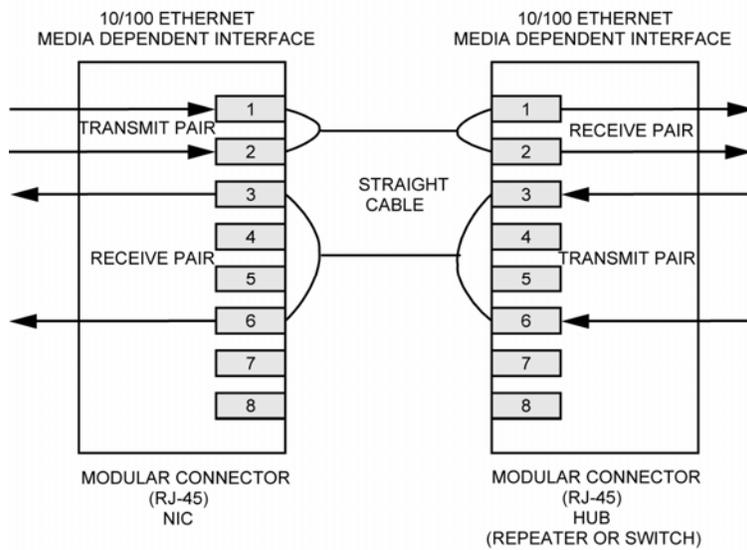

Figure 5. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Figure 6 shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).
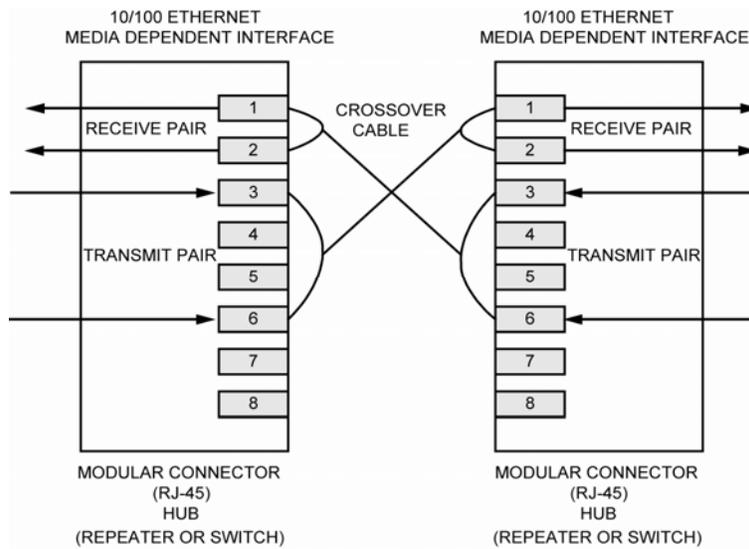
Figure 6. Typical Crossover Cable Connection

Loopback Mode

The KSZ8081RNA/RND supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

Local (Digital) Loopback

This loopback mode checks the RMII transmit and receive data paths between the KSZ8081RNA/RND and the external MAC, and is supported for both speeds (10/100Mbps) at full-duplex.

The loopback data path is shown in Figure 7.

1. The RMII MAC transmits frames to the KSZ8081RNA/RND.
2. Frames are wrapped around inside the KSZ8081RNA/RND.
3. The KSZ8081RNA/RND transmits frames back to the RMII MAC.
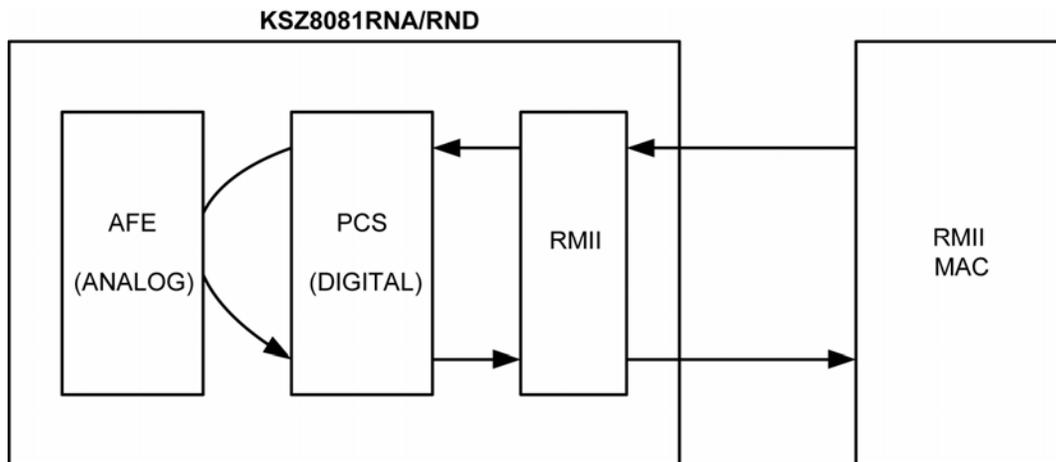
Figure 7. Local (Digital) Loopback

The following programming action and register settings are used for local loopback mode.

For 10/100Mbps loopback,

> Set register 0h,
>
> - Bit [14] = 1   // Enable local loopback mode
> - Bit [13] = 0/1   // Select 10Mbps/100Mbps speed
> - Bit [12] = 0   // Disable auto-negotiation
> - Bit [8] = 1   // Select full-duplex mode

Remote (Analog) Loopback

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the KSZ8081RNA/RND and its link partner, and is supported for 100Base-TX full-duplex mode only.

The loopback data path is shown in Figure 8.

1. The Fast Ethernet (100Base-TX) PHY link partner transmits frames to the KSZ8081RNA/RND.
2. Frames are wrapped around inside the KSZ8081RNA/RND.
3. The KSZ8081RNA/RND transmits frames back to the Fast Ethernet (100Base-TX) PHY link partner.
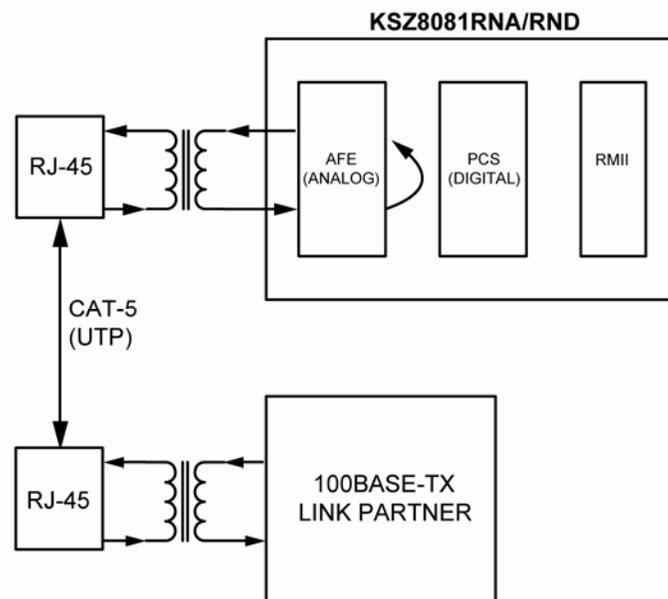
Figure 8. Remote (Analog) Loopback

The following programming steps and register settings are used for remote loopback mode.

1. Set Register 0h,
   - Bits [13] = 1   // Select 100Mbps speed
   - Bit [12] = 0   // Disable auto-negotiation
   - Bit [8] = 1   // Select full-duplex mode

   Or just auto-negotiate and link up at 100Base-TX full-duplex mode with the link partner.

2. Set Register 1Fh,
   - Bit [2] = 1   // Enable remote loopback mode

LinkMD® Cable Diagnostic

The LinkMD function uses time-domain reflectometry (TDR) to analyze the cabling plant for common cabling problems. These include open circuits, short circuits, and impedance mismatches.

LinkMD works by sending a pulse of known amplitude and duration down the MDI or MDI-X pair, then analyzing the shape of the reflected signal to determine the type of fault. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing register 1Dh, the LinkMD Control/Status register, in conjunction with register 1Fh, the PHY Control 2 register. The latter register is used to disable Auto MDI/MDI-X and to select either MDI or MDI-X as the cable differential pair for testing.

NAND Tree Support

The KSZ8081RNA/RND provides parametric NAND tree support for fault detection between chip I/Os and board. The NAND tree is a chain of nested NAND gates in which each KSZ8081RNA/RND digital I/O (NAND tree input) pin is an input to one NAND gate along the chain. At the end of the chain, the TXD1 pin provides the output for the nested NAND gates.

The NAND tree test process includes:

- Enabling NAND tree mode
- Pulling all NAND tree input pins high
- Driving each NAND tree input pin low, sequentially, according to the NAND tree pin order
- Checking the NAND tree output to make sure there is a toggle high-to-low or low-to-high for each NAND tree input driven low

Table 5 lists the NAND tree pin order.

Pin Number	Pin Name	NAND Tree Description
10	MDIO	Input
11	MDC	Input
12	RXD1	Input
13	RXD0	Input
15	CRS_DV	Input
16	REF_CLK	Input
18	INTRP	Input
19	TXEN	Input
23	LED0	Input
20	TXD0	Input
21	TXD1	Output

Table 5. NAND Tree Test Pin Order for KSZ8081RNA/RND

NAND Tree I/O Testing

Use the following procedure to check for faults on the KSZ8081RNA/RND digital I/O pin connections to the board:

1. Enable NAND tree mode by setting register 16h, bit [5] to '1'.
2. Use board logic to drive all KSZ8081RNA/RND NAND tree input pins high.
3. Use board logic to drive each NAND tree input pin, in KSZ8081RNA/RND tree pin order, as follows:
   a. Toggle the first pin (MDIO) from high to low, and verify that the TDX1 pin switches from high to low to indicate that the first pin is connected properly.
   b. Leave the first pin (MDIO) low.

     c.   Toggle the second pin (MDC) from high to low, and verify that the TXD1 pin switches from low to high to indicate that the second pin is connected properly.

     d.   Leave the first pin (MDIO) and the second pin (MDC) low.

     e.   Toggle the third pin from high to low, and verify that the TXD1 pin switches from high to low to indicate that the third pin is connected properly.

     f.   Continue with this sequence until all KSZ8081RNA/RND NAND tree input pins have been toggled.

Each KSZ8081RNA/RND NAND tree input pin must cause the TXD1 output pin to toggle high-to-low or low-to-high to indicate a good connection. If the TXD1 pin fails to toggle when the KSZ8081RNA/RND input pin toggles from high to low, the input pin has a fault.

Power Management

The KSZ8081RNA/RND incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

Power-Saving Mode

Power-saving mode is used to reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a '1' to register 1Fh, bit [10], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In this mode, the KSZ8081RNA/RND shuts down all transceiver blocks except the transmitter, energy detect, and PLL circuits.

By default, power-saving mode is disabled after power-up.

Energy-Detect Power-Down Mode

Energy-detect power-down (EDPD) mode is used to further reduce transceiver power consumption when the cable is unplugged. It is enabled by writing a '0' to register 18h, bit [11], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

EDPD mode works with the PLL off (set by writing a '1' to register 10h, bit [4] to automatically turn the PLL off in EDPD mode) to turn off all KSZ8081RNA/RND transceiver blocks except the transmitter and energy-detect circuits.

Power can be reduced further by extending the time interval between transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure two link partners in the same low power state and with auto MDI/MDI-X disabled can wake up when the cable is connected between them.

By default, energy-detect power-down mode is disabled after power-up.

Power-Down Mode

Power-down mode is used to power down the KSZ8081RNA/RND device when it is not in use after power-up. It is enabled by writing a '1' to register 0h, bit [11].

In this mode, the KSZ8081RNA/RND disables all internal functions except the MII management interface. The KSZ8081RNA/RND exits (disables) power-down mode after register 0h, bit [11] is set back to '0'.

Slow-Oscillator Mode

Slow-oscillator mode is used to disconnect the input reference crystal/clock on XI (pin 8) and select the on-chip slow oscillator when the KSZ8081RNA/RND device is not in use after power-up. It is enabled by writing a '1' to register 11h, bit [5].

Slow-oscillator mode works in conjunction with power-down mode to put the KSZ8081RNA/RND device in the lowest power state, with all internal functions disabled except the MII management interface. To properly exit this mode and return to normal PHY operation, use the following programming sequence:

1.   Disable slow-oscillator mode by writing a '0' to register 11h, bit [5].

2.   Disable power-down mode by writing a '0' to register 0h, bit [11].

3.   Initiate software reset by writing a '1' to register 0h, bit [15].

Reference Circuit for Power and Ground Connections

The KSZ8081RNA/RND is a single 3.3V supply device with a built-in regulator to supply the 1.2V core. The power and ground connections are shown in Figure 9 and Table 6 for 3.3V VDDIO.
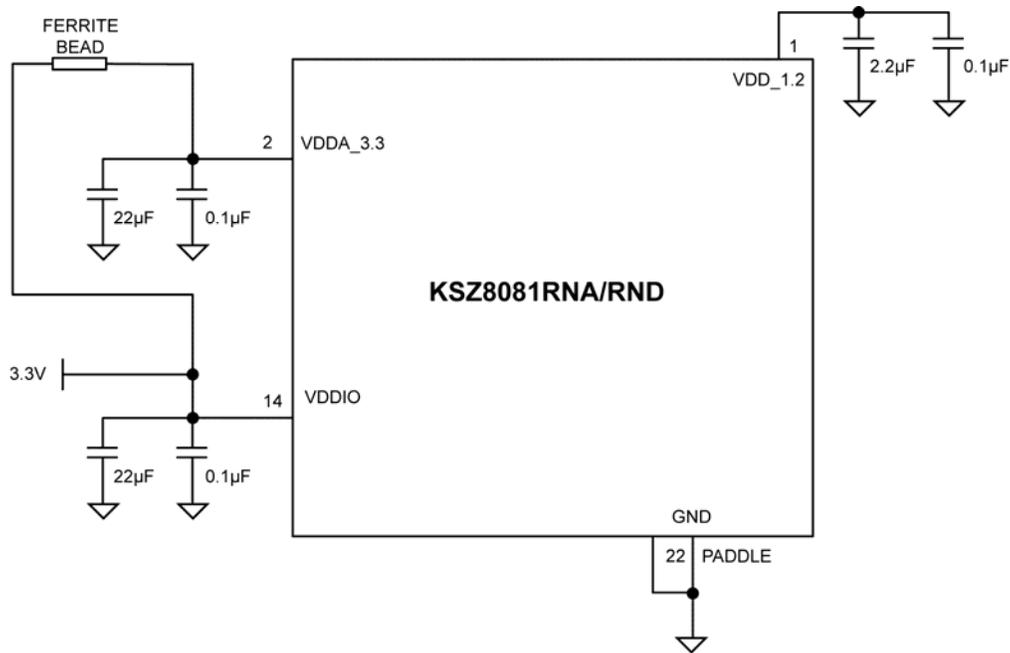

Figure 9. KSZ8081RNA/RND Power and Ground Connections

Power Pin	Pin Number	Description
VDD_1.2	1	Decouple with 2.2µF and 0.1µF capacitors to ground.
VDDA_3.3	2	Connect to board's 3.3V supply through a ferrite bead.
		Decouple with 22µF and 0.1µF capacitors to ground.
VDDIO	14	Connect to board's 3.3V supply for 3.3V VDDIO.
		Decouple with 22µF and 0.1µF capacitors to ground.

Table 6. KSZ8081RNA/RND Power Pin Description

Typical Current/Power Consumption

Table 7 through Table 9 show typical values for current consumption by the transceiver (VDDA_3.3) and digital I/O (VDDIO) power pins and typical values for power consumption by the KSZ8081RNA/RND device for the indicated nominal operating voltage combinations. These current and power consumption values include the transmit driver current and on-chip regulator current for the 1.2V core.

Transceiver (3.3V), Digital I/Os (3.3V)

Condition	3.3V Transceiver (VDDA_3.3)	3.3V Digital I/Os (VDDIO)	Total Chip Power
	mA	mA	mW
100Base-TX Link-up (no traffic)	34	12	152
100Base-TX Full-duplex @ 100% utilization	34	13	155
10Base-T Link-up (no traffic)	14	11	82.5
10Base-T Full-duplex @ 100% utilization	30	11	135
Power-saving mode (Reg. 1Fh, bit [10] = 1)	14	10	79.2
EDPD mode (Reg. 18h, bit [11] = 0)	10	10	66.0
EDPD mode (Reg. 18h, bit [11] = 0) and PLL off (Reg. 10h, bit [4] = 1)	3.77	1.54	17.5
Software power-down mode (Reg. 0h, bit [11] =1)	2.59	1.51	13.5
Software power-down mode (Reg. 0h, bit [11] =1) and slow-oscillator mode (Reg. 11h, bit [5] =1)	1.36	0.45	5.97

Table 7. Typical Current/Power Consumption (VDDA_3.3 = 3.3V, VDDIO = 3.3V)

Transceiver (3.3V), Digital I/Os (2.5V)

Condition	3.3V Transceiver (VDDA_3.3)	2.5V Digital I/Os (VDDIO)	Total Chip Power
	mA	mA	mW
100Base-TX Link-up (no traffic)	34	12	142
100Base-TX Full-duplex @ 100% utilization	34	13	145
10Base-T Link-up (no traffic)	15	11	77.0
10Base-T Full-duplex @ 100% utilization	27	11	117
Power-saving mode (Reg. 1Fh, bit [10] = 1)	15	10	74.5
EDPD mode (Reg. 18h, bit [11] = 0)	11	10	61.3
EDPD mode (Reg. 18h, bit [11] = 0) and PLL off (Reg. 10h, bit [4] = 1)	3.55	1.35	15.1
Software power-down mode (Reg. 0h, bit [11] =1)	2.29	1.34	10.9
Software power-down mode (Reg. 0h, bit [11] =1) and slow-oscillator mode (Reg. 11h, bit [5] =1)	1.15	0.29	4.52

Table 8. Typical Current/Power Consumption (VDDA_3.3 = 3.3V, VDDIO = 2.5V)

Transceiver (3.3V), Digital I/Os (1.8V)

Condition	3.3V Transceiver (VDDA_3.3)	1.8V Digital I/Os (VDDIO)	Total Chip Power
	mA	mA	mW
100Base-TX Link-up (no traffic)	34	11	132
100Base-TX Full-duplex @ 100% utilization	34	12	134
10Base-T Link-up (no traffic)	15	10	67.5
10Base-T Full-duplex @ 100% utilization	27	10	107
Power-saving mode (Reg. 1Fh, bit [10] = 1)	15	9.0	65.7
EDPD mode (Reg. 18h, bit [11] = 0)	11	9.0	52.5
EDPD mode (Reg. 18h, bit [11] = 0) and PLL off (Reg. 10h, bit [4] = 1)	4.05	1.21	15.5
Software power-down mode (Reg. 0h, bit [11] =1)	2.79	1.21	11.4
Software power-down mode (Reg. 0h, bit [11] =1) and slow-oscillator mode (Reg. 11h, bit [5] =1)	1.65	0.19	5.79

Table 9. Typical Current/Power Consumption (VDDA_3.3 = 3.3V, VDDIO = 1.8V)

Register Map

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h	Reserved
10h	Digital Reserved Control
11h	AFE Control 1
12h – 14h	Reserved
15h	RXER Counter
16h	Operation Mode Strap Override
17h	Operation Mode Strap Status
18h	Expanded Control
19h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch	Reserved
1Dh	LinkMD Control/Status
1Eh	PHY Control 1
1Fh	PHY Control 2

Register Description

Address	Name	Description	Mode[1]	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loopback	1 = Loopback mode 0 = Normal operation	RW	0
0.13	Speed Select	1 = 100Mbps 0 = 10Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Set by the ANEN_SPEED strapping pin. See the "Strapping Options" section for details.
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, the auto-negotiation result overrides the settings in registers 0.13 and 0.8.	RW	Set by the ANEN_SPEED strapping pin. See the "Strapping Options" section for details.
0.11	Power-Down	1 = Power-down mode 0 = Normal operation If software reset (register 0.15) is used to exit power-down mode (register 0.11 = 1), two software reset writes (register 0.15 = 1) are required. The first write clears power-down mode; the second write resets the chip and re-latches the pin strapping pin values.	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII 0 = Normal operation	RW	0
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation. This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	1
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:0	Reserved	Reserved	RO	000_0000
Register 1h – Basic Status				
1.15	100Base-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100Base-TX Full-Duplex	1 = Capable of 100Mbps full-duplex 0 = Not capable of 100Mbps full-duplex	RO	1
1.13	100Base-TX Half-Duplex	1 = Capable of 100Mbps half-duplex 0 = Not capable of 100Mbps half-duplex	RO	1
1.12	10Base-T Full-Duplex	1 = Capable of 10Mbps full-duplex 0 = Not capable of 10Mbps full-duplex	RO	1
1.11	10Base-T Half-Duplex	1 = Capable of 10Mbps half-duplex 0 = Not capable of 10Mbps half-duplex	RO	1
1.10:7	Reserved	Reserved	RO	000_0

Address	Name	Description	Mode[1]	Default
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Can perform auto-negotiation 0 = Cannot perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capability registers	RO	1
Register 2h – PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex).	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). KENDIN Communication's OUI is 0010A1 (hex).	RO	0001_01
3.9:4	Model Number	Six-bit manufacturer's model number	RO	01_0110
3.3:0	Revision Number	Four-bit manufacturer's revision number	RO	Indicates silicon revision
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability	RW	0
4.14	Reserved	Reserved	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	Reserved	RO	0
4.11:10	Pause	[00] = No pause [10] = Asymmetric pause [01] = Symmetric pause [11] = Asymmetric and symmetric pause	RW	00
4.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RW	Set by the ANEN_SPEED strapping pin. See the "Strapping Options" section for details.

Address	Name	Description	Mode[1]	Default
4.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RW	Set by the ANEN_SPEED strapping pin. See the "Strapping Options" section for details.
4.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RW	1
4.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved	Reserved	RO	0
5.11:10	Pause	[00] = No pause [10] = Asymmetric pause [01] = Symmetric pause [11] = Asymmetric and symmetric pause	RO	00
5.9	100Base-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100Base-TX Full-Duplex	1 = 100Mbps full-duplex capable 0 = No 100Mbps full-duplex capability	RO	0
5.7	100Base-TX Half-Duplex	1 = 100Mbps half-duplex capable 0 = No 100Mbps half-duplex capability	RO	0
5.6	10Base-T Full-Duplex	1 = 10Mbps full-duplex capable 0 = No 10Mbps full-duplex capability	RO	0
5.5	10Base-T Half-Duplex	1 = 10Mbps half-duplex capable 0 = No 10Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved	Reserved	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0

Address	Name	Description	Mode[1]	Default
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next pages will follow 0 = Last page	RW	0
7.14	Reserved	Reserved	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic 1 0 = Logic 0	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional next pages will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Can act on the information 0 = Cannot act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic 0 0 = Previous value of transmitted link code word equal to logic 1	RO	0
8.10:0	Message Field	11-bit wide field to encode 2048 messages	RO	000_0000_0000
Register 10h – Digital Reserved Control				
10.15:5	Reserved	Reserved	RW	0000_0000_000
10.4	PLL Off	1 = Turn PLL off automatically in EDPD mode 0 = Keep PLL on in EDPD mode. See also register 18h, bit [11] for EDPD mode	RW	0
10.3:0	Reserved	Reserved	RW	0000
Register 11h – AFE Control 1				
11.15:6	Reserved	Reserved	RW	0000_0000_00

Address	Name	Description	Mode[1]	Default
11.5	Slow-Oscillator Mode Enable	Slow-oscillator mode is used to disconnect the input reference crystal/clock on the XI pin and select the on-chip slow oscillator when the KSZ8081RNA/RND device is not in use after power-up. 1 = Enable 0 = Disable This bit automatically sets software power-down to the analog side when enabled.	RW	0
11.4:0	Reserved	Reserved	RW	0_0000
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for symbol error frames	RO/SC	0000h
Register 16h – Operation Mode Strap Override				
16.15:11	Reserved	Reserved	RW	0000_0
16.10	Reserved	Reserved	RO	0
16.9	B-CAST_OFF Override	1 = Override strap-in for B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RW	0
16.8:7	Reserved	Reserved	RW	0_0
16.6	RMII B-to-B Override	1 = Override strap-in for RMII back-to-back mode (also set bit 1 of this register to '1')	RW	0
16.5	NAND Tree Override	1 = Override strap-in for NAND tree mode	RW	0
16.4:2	Reserved	Reserved	RW	0_00
16.1	RMII Override	1 = Override strap-in for RMII mode	RW	1
16.0	Reserved	Reserved	RW	0
Register 17h – Operation Mode Strap Status				
17.15:13	PHYAD[2:0] Strap-In Status	[000] = Strap to PHY Address 0 [011] = Strap to PHY Address 3 The KSZ8081RNA/RND supports only PHY addresses 0h and 3h.	RO	
17.12:2	Reserved	Reserved	RO	
17.1	RMII Strap-In Status	1 = Strap to RMII mode	RO	
17.0	Reserved	Reserved	RO	
Register 18h – Expanded Control				
18.15:12	Reserved	Reserved	RW	0000
18.11	EDPD Disabled	Energy-detect power-down mode 1 = Disable 0 = Enable See also register 10h, bit [4] for PLL off.	RW	1
18.10:0	Reserved	Reserved	RW	000_0000_0000
Register 1Bh – Interrupt Control/Status				
1B.15	Jabber Interrupt Enable	1 = Enable jabber interrupt 0 = Disable jabber interrupt	RW	0

Address	Name	Description	Mode[1]	Default
1B.14	Receive Error Interrupt Enable	1 = Enable receive error interrupt 0 = Disable receive error interrupt	RW	0
1B.13	Page Received Interrupt Enable	1 = Enable page received interrupt 0 = Disable page received interrupt	RW	0
1B.12	Parallel Detect Fault Interrupt Enable	1 = Enable parallel detect fault interrupt 0 = Disable parallel detect fault interrupt	RW	0
1B.11	Link Partner Acknowledge Interrupt Enable	1 = Enable link partner acknowledge interrupt 0 = Disable link partner acknowledge interrupt	RW	0
1B.10	Link-Down Interrupt Enable	1= Enable link-down interrupt 0 = Disable link-down interrupt	RW	0
1B.9	Remote Fault Interrupt Enable	1 = Enable remote fault interrupt 0 = Disable remote fault interrupt	RW	0
1B.8	Link-Up Interrupt Enable	1 = Enable link-up interrupt 0 = Disable link-up interrupt	RW	0
1B.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occur	RO/SC	0
1B.6	Receive Error Interrupt	1 = Receive error occurred 0 = Receive error did not occur	RO/SC	0
1B.5	Page Receive Interrupt	1 = Page receive occurred 0 = Page receive did not occur	RO/SC	0
1B.4	Parallel Detect Fault Interrupt	1 = Parallel detect fault occurred 0 = Parallel detect fault did not occur	RO/SC	0
1B.3	Link Partner Acknowledge Interrupt	1 = Link partner acknowledge occurred 0 = Link partner acknowledge did not occur	RO/SC	0
1B.2	Link-Down Interrupt	1 = Link-down occurred 0 = Link-down did not occur	RO/SC	0
1B.1	Remote Fault Interrupt	1 = Remote fault occurred 0 = Remote fault did not occur	RO/SC	0
1B.0	Link-Up Interrupt	1 = Link-up occurred 0 = Link-up did not occur	RO/SC	0
Register 1Dh – LinkMD Control/Status				
1D.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0

Address	Name	Description	Mode[1]	Default
1D.14:13	Cable Diagnostic Test Result	[00] = Normal condition [01] = Open condition has been detected in cable [10] = Short condition has been detected in cable [11] = Cable diagnostic test has failed	RO	00
1D.12	Short Cable Indicator	1 = Short cable (<10 meter) has been detected by LinkMD	RO	0
1D.11:9	Reserved	Reserved	RW	000
1D.8:0	Cable Fault Counter	Distance to fault	RO	0_0000_0000
Register 1Eh – PHY Control 1				
1E.15:10	Reserved	Reserved	RO	0000_00
1E.9	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1E.8	Link Status	1 = Link is up 0 = Link is down	RO	0
1E.7	Polarity Status	1 = Polarity is reversed 0 = Polarity is not reversed	RO	
1E.6	Reserved	Reserved	RO	0
1E.5	MDI/MDI-X State	1 = MDI-X 0 = MDI	RO	
1E.4	Energy Detect	1 = Signal present on receive differential pair 0 = No signal detected on receive differential pair	RO	0
1E.3	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RW	0
1E.2:0	Operation Mode Indication	[000] = Still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = Reserved [100] = Reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = Reserved	RO	000
Register 1Fh – PHY Control 2				
1F.15	HP_MDIX	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	RW	1

Address	Name	Description	Mode[1]	Default
1F.14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 1 = MDI-X mode Transmit on RXP,RXM (pins 4, 3) and Receive on TXP,TXM (pins 6, 5) 0 = MDI mode Transmit on TXP,TXM (pins 6, 5) and Receive on RXP,RXM (pins 4, 3)	RW	0
1F.13	Pair Swap Disable	1 = Disable Auto MDI/MDI-X 0 = Enable Auto MDI/MDI-X	RW	0
1F.12	Reserved	Reserved	RW	0
1F.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allows the transmitter to send a pattern even if there is no link.	RW	0
1F.10	Power Saving	1 = Enable power saving 0 = Disable power saving	RW	0
1F.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1F.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1F.7	RMII Reference Clock Select	1 = For KSZ8081RNA, clock input to XI (pin 8) is 50MHz for RMII – 50MHz clock mode. For KSZ8081RND, clock input to XI (pin 8) is 25MHz for RMII – 25MHz clock code. 0 = For KSZ8081RNA, clock input to XI (pin 8) is 25MHz for RMII – 25MHz clock code. For KSZ8081RND, clock input to XI (pin 8) is 50MHz for RMII – 50MHz clock mode.	RW	0
1F.6	Reserved	Reserved	RW	0
1F.5:4	LED Mode	[00] = LED0: Link/Activity [01] = LED0: Link [10], [11] = Reserved	RW	00
1F.3	Disable Transmitter	1 = Disable transmitter 0 = Enable transmitter	RW	0
1F.2	Remote Loopback	1 = Remote (analog) loopback is enabled 0 = Normal mode	RW	0
1F.1	Reserved	Reserved	RW	0
1F.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note:

1.   RW = Read/Write.
     RO = Read only.
     SC = Self-cleared.
     LH = Latch high.
     LL = Latch low.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN})

　　($V_{DD\_1.2}$) .... −0.5V to +1.8V

　　($V_{DDIO,}$ $V_{DDA\_3.3}$) .... −0.5V to +5.0V

Input Voltage (all inputs) .... −0.5V to +5.0V

Output Voltage (all outputs) .... −0.5V to +5.0V

Lead Temperature (soldering, 10sec.) .... 260°C

Storage Temperature (T_s) .... −55°C to +150°C

Operating Ratings[2]

Supply Voltage

　　($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) .... +3.135V to +3.465V

　　($V_{DDIO\_2.5}$) .... +2.375V to +2.625V

　　($V_{DDIO\_1.8}$) .... +1.710V to +1.890V

Ambient Temperature

　　(T_A, Commercial) .... 0°C to +70°C

　　(T_A, Industrial) .... −40°C to +85°C

Maximum Junction Temperature (T_J max.) .... 125°C

Thermal Resistance (θ_{JA}) .... 49.22°C/W

Thermal Resistance (θ_{JC}) .... 25.65°C/W

Electrical Characteristics[3]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current (V_{DDIO}, $V_{DDA\_3.3}$ = 3.3V)[4]						
$I_{DD1\_3.3V}$	10Base-T	Full-duplex traffic @ 100% utilization		41		mA
$I_{DD2\_3.3V}$	100Base-TX	Full-duplex traffic @ 100% utilization		47		mA
$I_{DD3\_3.3V}$	EDPD Mode	Ethernet cable disconnected (reg. 18h.11 = 0)		20		mA
$I_{DD4\_3.3V}$	Power-Down Mode	Software power-down (reg. 0h.11 = 1)		4		mA
CMOS Level Inputs						
V_{IH}	Input High Voltage	V_{DDIO} = 3.3V	2.0			V
		V_{DDIO} = 2.5V	1.8			V
		V_{DDIO} = 1.8V	1.3			V
V_{IL}	Input Low Voltage	V_{DDIO} = 3.3V			0.8	V
		V_{DDIO} = 2.5V			0.7	V
		V_{DDIO} = 1.8V			0.5	V
$|I_{IN}|$	Input Current	V_{IN} = GND ~ VDDIO			10	µA
CMOS Level Outputs						
V_{OH}	Output High Voltage	V_{DDIO} = 3.3V	2.4			V
		V_{DDIO} = 2.5V	2.0			V
		V_{DDIO} = 1.8V	1.5			V
V_{OL}	Output Low Voltage	V_{DDIO} = 3.3V			0.4	V
		V_{DDIO} = 2.5V			0.4	V
		V_{DDIO} = 1.8V			0.3	V
$|I_{oz}|$	Output Tri-State Leakage				10	µA
LED Output						
I_{LED}	Output Drive Current	LED0 pin		8		mA

Notes:

1. Exceeding the absolute maximum rating can damage the device. Stresses greater than the absolute maximum rating can cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

2. The device is not guaranteed to function outside its operating rating.

3. T_A = 25°C. Specification is for packaged product only.

4. Current consumption is for the single 3.3V supply KSZ8081RNA/RND device only, and includes the transmit driver current and the 1.2V supply voltage ($V_{DD\_1.2}$) that are supplied by the KSZ8081RNA/RND.

| Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
All Pull-Up/Pull-Down Pins (including Strapping Pins)						
pu	Internal Pull-Up Resistance	V_{DDIO} = 3.3V	30	45	73	kΩ
		V_{DDIO} = 2.5V	39	61	102	kΩ
		V_{DDIO} = 1.8V	48	99	178	kΩ
pd	Internal Pull-Down Resistance	V_{DDIO} = 3.3V	26	43	79	kΩ
		V_{DDIO} = 2.5V	34	59	113	kΩ
		V_{DDIO} = 1.8V	53	99	200	kΩ
100Base-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output			2	%
t_r, t_f	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.25	ns
	Overshoot				5	%
	Output Jitter	Peak-to-peak		0.7		ns
10Base-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2		2.8	V
	Jitter Added	Peak-to-peak			3.5	ns
t_r, t_f	Rise/Fall Time			25		ns
10Base-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
Transmitter – Drive Setting						
V_{SET}	Reference Voltage of I_{SET}	R(I_{SET}) = 6.49kΩ		0.65		V
REF_CLK Output						
	50MHz RMII Clock Output Jitter	Peak-to-peak (Applies only to RMII – 25MHz clock mode)		300		ps
100Mbps Mode – Industrial Applications Parameters						
t_{llr}	Link Loss Reaction (Indication) Time	Link loss detected at receive differential inputs to PHY signal indication time for each of the following: 1. For LED mode 01, Link LED output changes from low (link-up) to high (link-down). 2. INTRP pin asserts for link-down status change.		4.4		µs

Timing Diagrams

RMII Timing
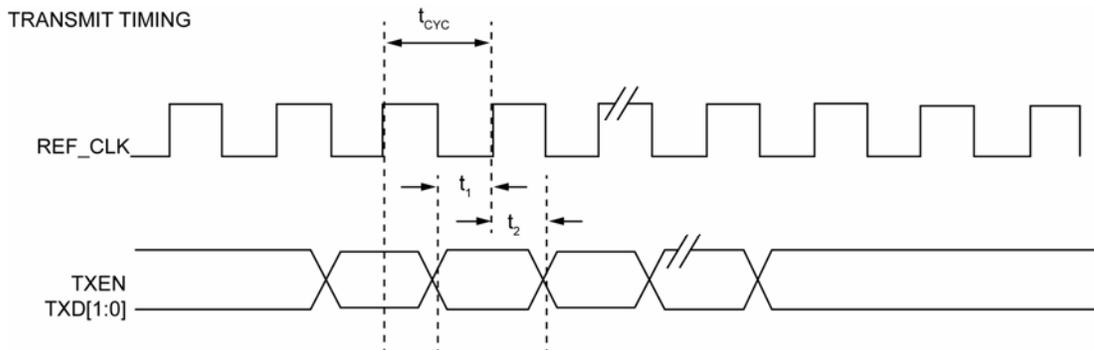
Figure 10. RMII Timing – Data Received from RMII
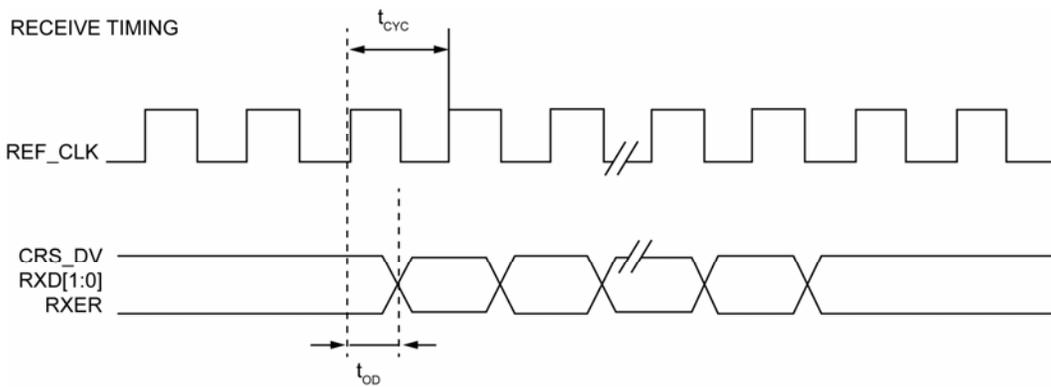
Figure 11. RMII Timing – Data Input to RMII

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_{CYC}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{OD}	Output delay	7	10	13	ns

Table 10. RMII Timing Parameters – KSZ8081RNA/RND (25MHz input to XI pin, 50MHz output from REF_CLK pin)

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_{CYC}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{OD}	Output delay	8	11	13	ns

Table 11. RMII Timing Parameters – KSZ8081RNA/RND (50MHz input to XI pin)

Auto-Negotiation Timing

AUTO-NEGOTIATION
FAST LINK PULSE (FLP) TIMING
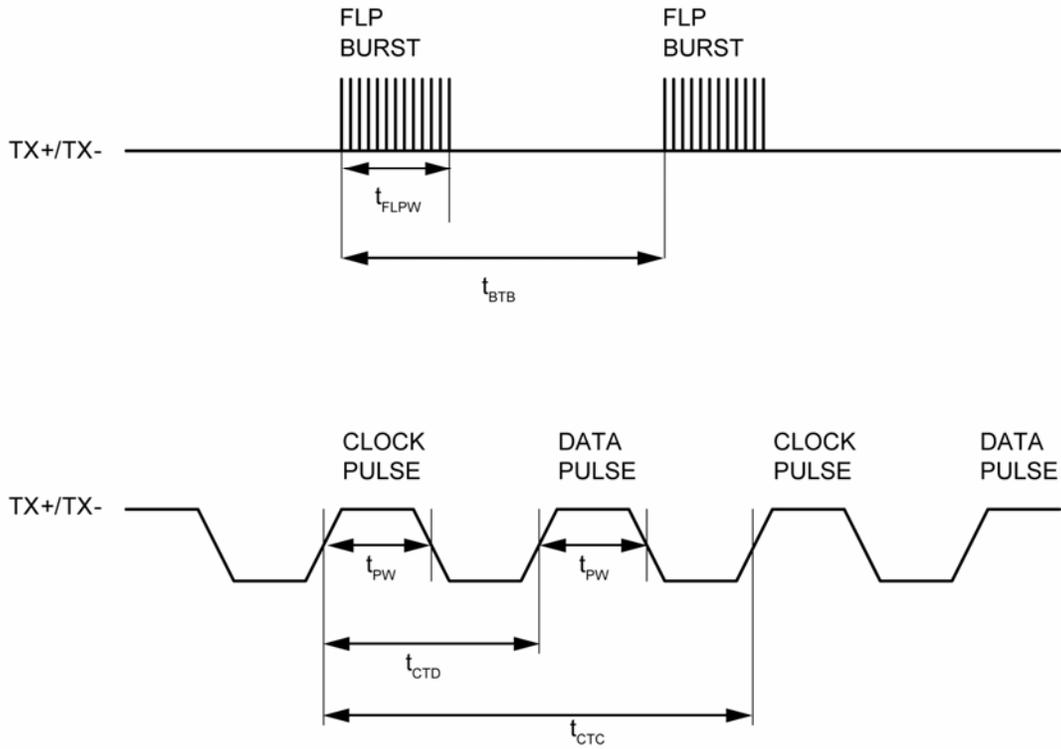
Figure 12. Auto-Negotiation Fast Link Pulse (FLP) Timing

Timing Parameter	Description	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per FLP burst	17		33	

Table 12. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

MDC/MDIO Timing
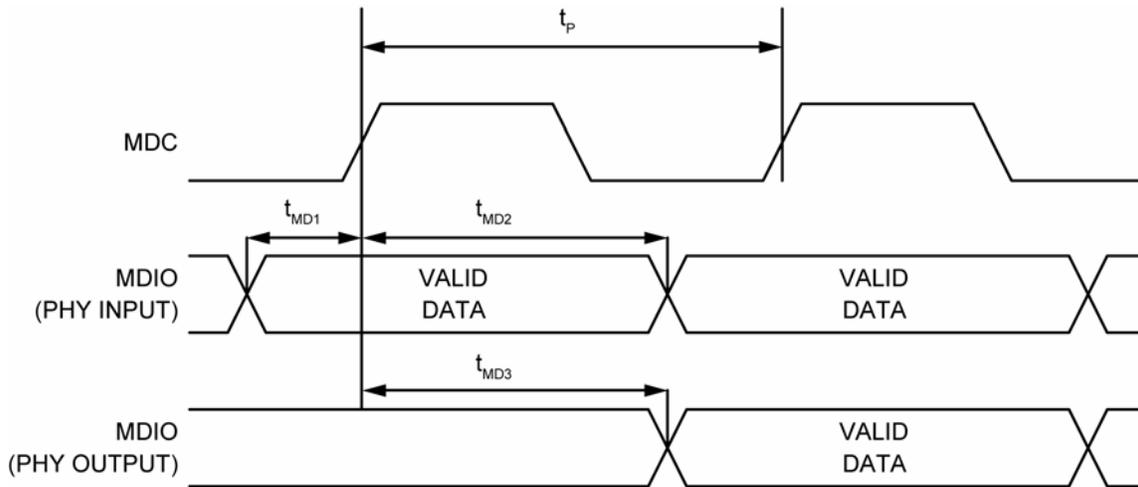
Figure 13. MDC/MDIO Timing

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	MDC period		400		ns
t_{MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC	5			ns

Table 13. MDC/MDIO Timing Parameters

Power-Up/Reset Timing

The KSZ8081RNA/RND reset timing requirement is summarized in Figure 14 and Table 14.
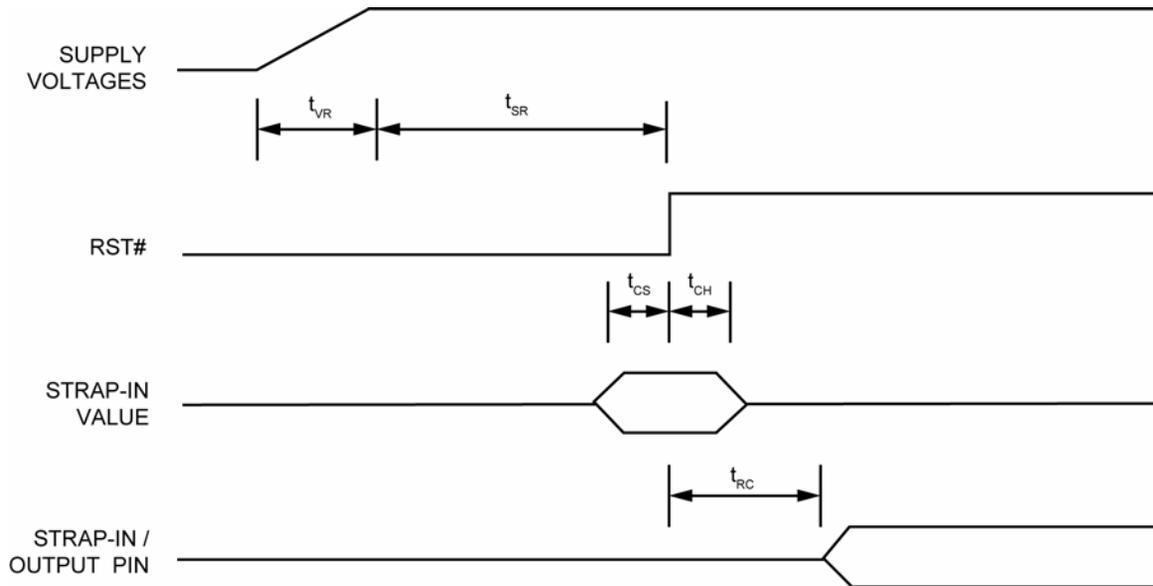
Figure 14. Power-Up/Reset Timing

Parameter	Description	Min.	Max.	Units
t_{VR}	Supply voltage (V_{DDIO}, $V_{DDA\_3.3}$) rise time	300		µs
t_{SR}	Stable supply voltage (V_{DDIO}, $V_{DDA\_3.3}$) to reset high	10		ms
t_{CS}	Configuration setup time	5		ns
t_{CH}	Configuration hold time	5		ns
t_{RC}	Reset to strap-in pin output	6		ns

Table 14. Power-Up/Reset Timing Parameters

The supply voltage (V_{DDIO} and $V_{DDA\_3.3}$) power-up waveform should be monotonic. The 300µs minimum rise time is from 10% to 90%.

For warm reset, the reset (RST#) pin should be asserted low for a minimum of 500µs. The strap-in pin values are read and updated at the de-assertion of reset.

After the de-assertion of reset, wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) interface.

Reset Circuit

Figure 15 shows a reset circuit recommended for powering up the KSZ8081RNA/RND if reset is triggered by the power supply.
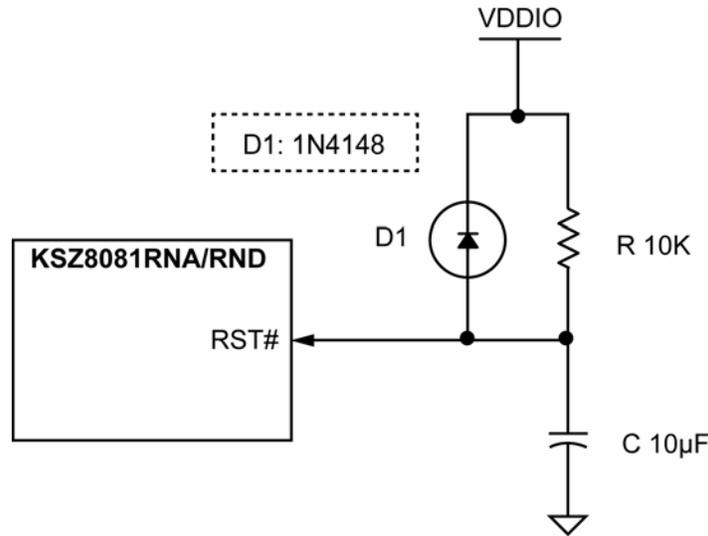
Figure 15. Recommended Reset Circuit

Figure 16 shows a reset circuit recommended for applications where reset is driven by another device (for example, the CPU or an FPGA). At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the KSZ8081RNA/RND device. The RST_OUT_n from the CPU/FPGA provides the warm reset after power-up.
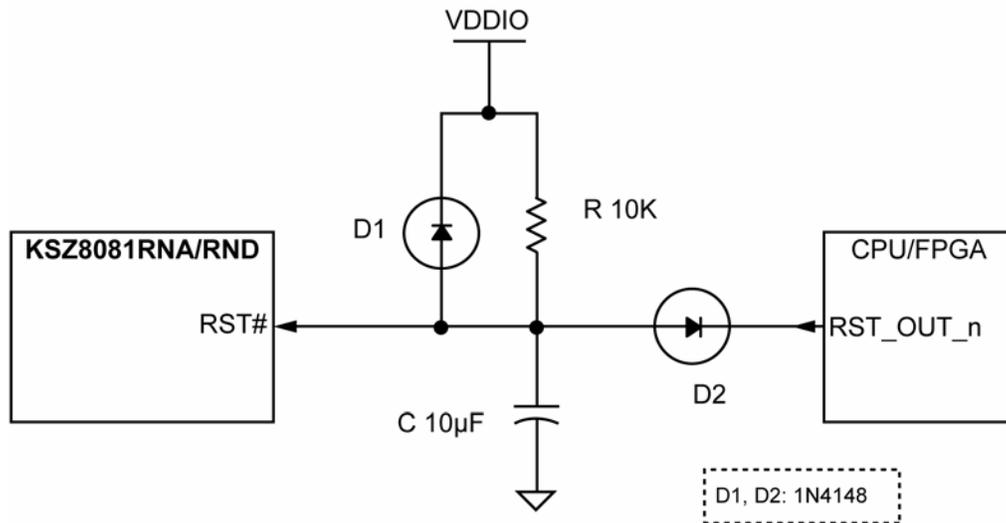
Figure 16. Recommended Reset Circuit for Interfacing with CPU/FPGA Reset Output

Reference Circuits – LED Strap-In Pins

The pull-up, float, and pull-down reference circuits for the LED0/ANEN_SPEED strapping pin are shown in Figure 17 for 3.3V and 2.5V VDDIO.
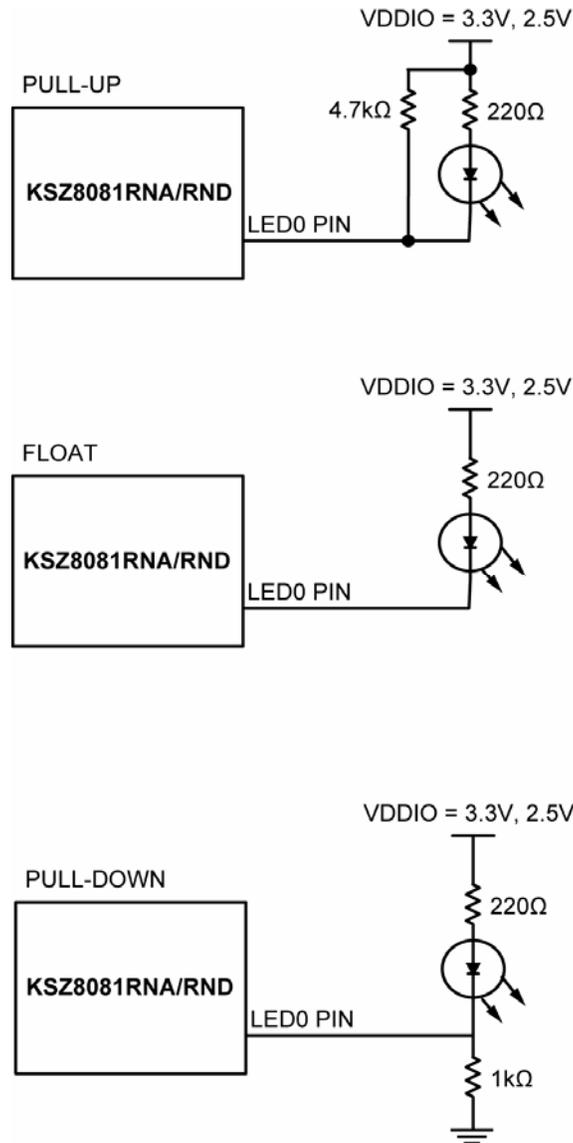
Figure 17. Reference Circuits for LED Strapping Pins

For 1.8V VDDIO, LED indication support is not recommended due to the low voltage. Without the LED indicator, the ANEN_SPEED strapping pin is functional with a 4.7kΩ pull-up to 1.8V VDDIO or float for a value of '1', and with a 1.0kΩ pull-down to ground for a value of '0'.

Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ8081RNA/RND. For the KSZ8081RNA/RND in RMII – 25MHz clock mode, the reference clock is 25 MHz. The reference clock connections to XI (pin 8) and XO (pin 7), and the reference clock selection criteria, are provided in Figure 18 and Table 15.
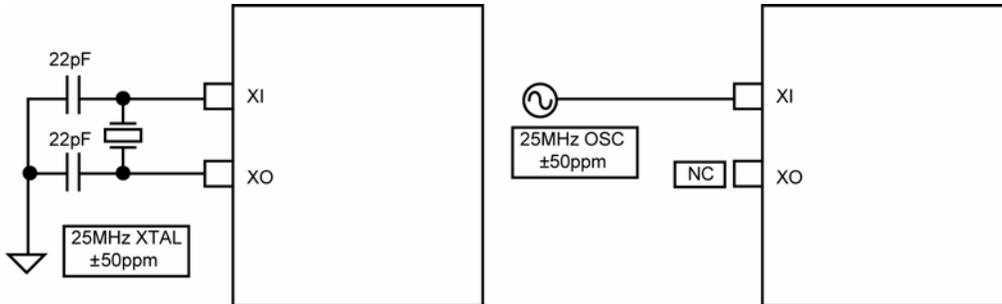

Figure 18. 25MHz Crystal/Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	25	MHz
Frequency tolerance (max.)	±50	ppm

Table 15. 25MHz Crystal / Reference Clock Selection Criteria

For the KSZ8081RNA/RND in RMII – 50MHz clock mode, the reference clock is 50MHz. The reference clock connection to XI (pin 8), and the reference clock selection criteria are provided in Figure 19 and Table 16.
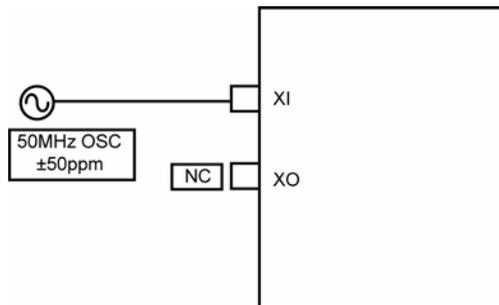

Figure 19. 50MHz Oscillator Reference Clock Connection

Characteristics	Value	Units
Frequency	50	MHz
Frequency tolerance (max)	±50	ppm

Table 16. 50MHz Oscillator / Reference Clock Selection Criteria

Magnetic – Connection and Selection

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements.

The KSZ8081RNA/RND design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the two differential pairs. Therefore, the two transformer center tap pins on the KSZ8081RNA/RND side should not be connected to any power supply source on the board; instead, the center tap pins should be separated from one another and connected through separate 0.1µF common-mode capacitors to ground. Separation is required because the common-mode voltage is different between transmitting and receiving differential pairs.

Figure 20 shows the typical magnetic interface circuit for the KSZ8081RNA/RND.
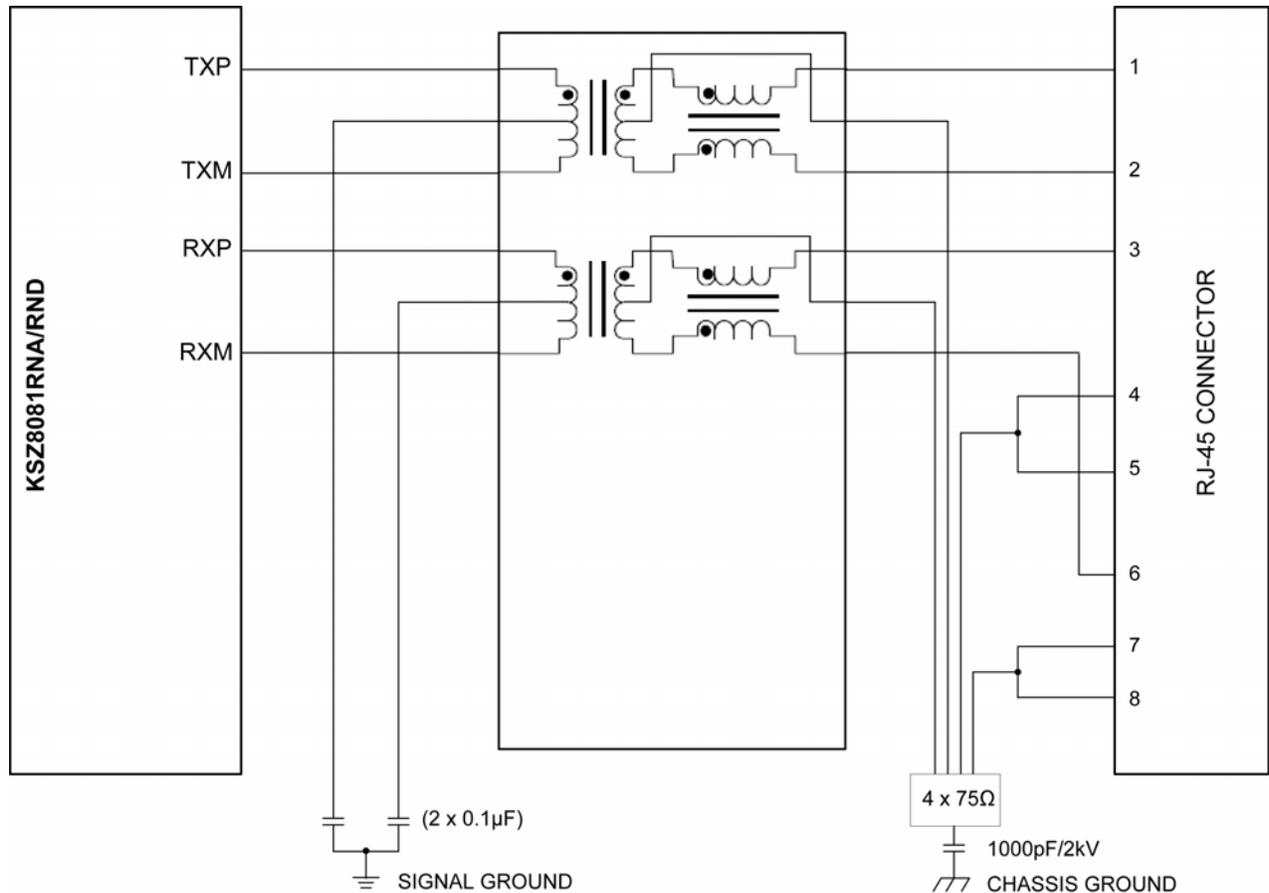
Figure 20. Typical Magnetic Interface Circuit

Table 17 lists recommended magnetic characteristics.

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	
Open-circuit inductance (min.)	350µH	100mV, 100kHz, 8mA
Insertion loss (typ.)	–1.1dB	100kHz to 100MHz
HIPOT (min.)	1500Vrms	

Table 17. Magnetics Selection Criteria

Table 18 is a list of compatible single-port magnetics with separated transformer center tap pins on the PHY chip side that can be used with the KSZ8081RNA/RND.

Manufacturer	Part Number	Temperature Range	Magnetic + RJ-45
Bel Fuse	S558-5999-U7	0°C to 70°C	No
Bel Fuse	SI-46001-F	0°C to 70°C	Yes
Bel Fuse	SI-50170-F	0°C to 70°C	Yes
Delta	LF8505	0°C to 70°C	No
HALO	HFJ11-2450E	0°C to 70°C	Yes
HALO	TG110-E055N5	–40°C to 85°C	No
LANKom	LF-H41S-1	0°C to 70°C	No
Pulse	H1102	0°C to 70°C	No
Pulse	H1260	0°C to 70°C	No
Pulse	HX1188	–40°C to 85°C	No
Pulse	J00-0014	0°C to 70°C	Yes
Pulse	JX0011D21NL	–40°C to 85°C	Yes
TDK	TLA-6T718A	0°C to 70°C	Yes
Transpower	HB726	0°C to 70°C	No
Wurth/Midcom	000-7090-37R-LF1	–40°C to 85°C	No

Table 18. Compatible Single-Port 10/100 Magnetics

Recommended Land Pattern
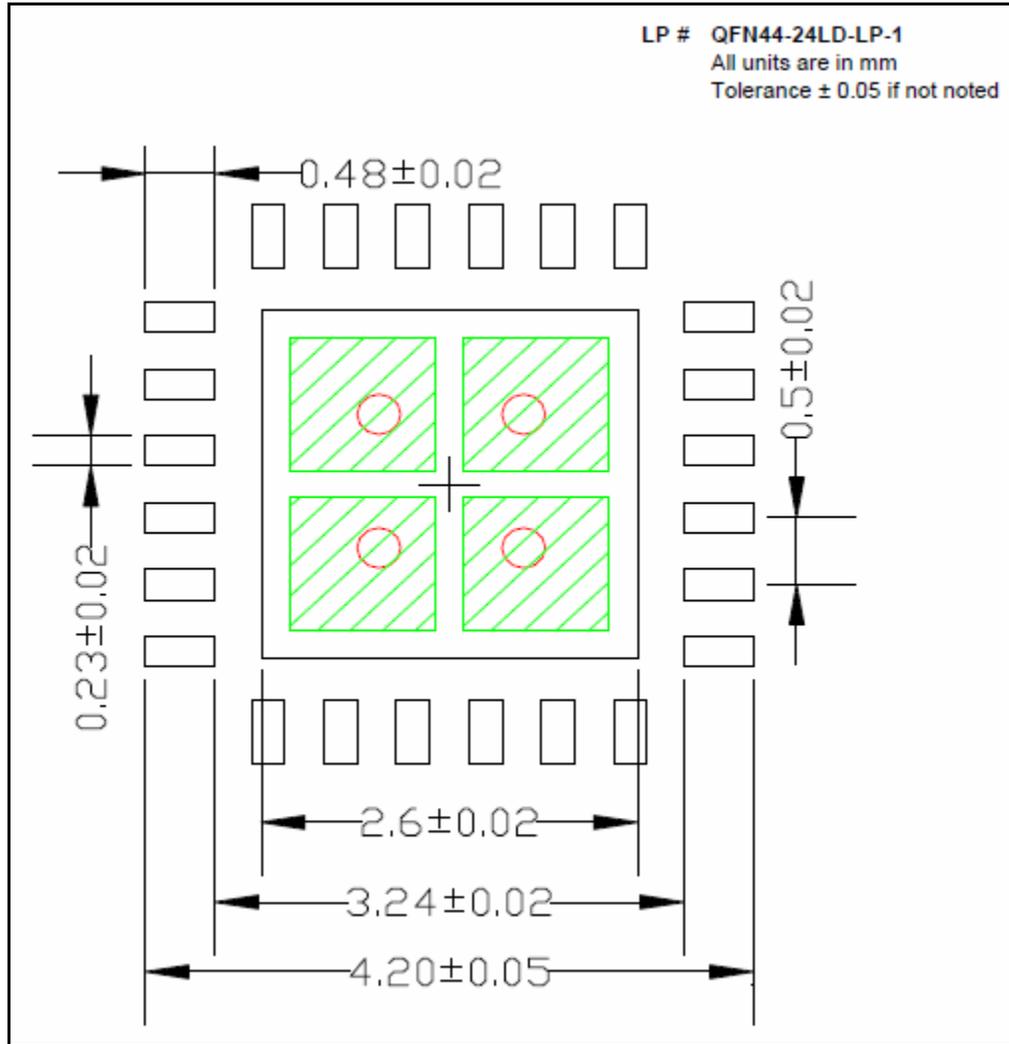
Figure 21. Recommended Land Pattern, 24-Pin (4mm x 4mm) QFN

Red circles indicate thermal vias. They should be 0.350mm in diameter and be connected to the GND plane for maximum thermal performance.

Green rectangles (with shaded area) indicate solder stencil openings on the exposed pad area. They should be 1.00 x 1.00mm in size, 1.20mm pitch.

Package Information[1]

Pin 1 Dot By marking
24
1
2
3
4.00 BSC
4.00 BSC

TOP VIEW

2.50 Exp. DAP
PIN #1 ID
0.40D±0.05
R0.20
2
0.25
2.50 Exp. DAP
0.500 BSC
2.5000 Ref.

BOTTOM VIEW

0.850±0.050
0.05 C
SEATING PLANE
0.203±0.025
0.02
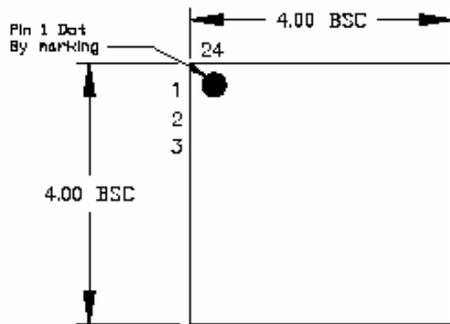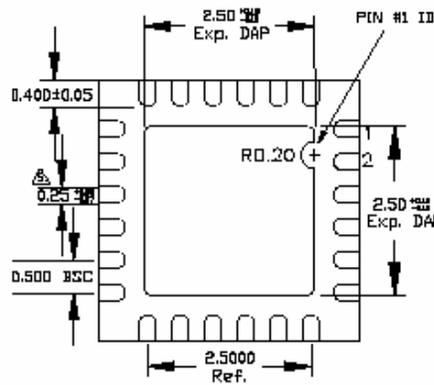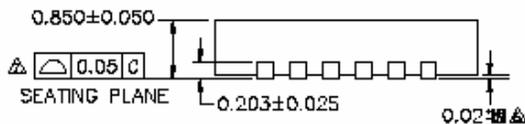
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin (4mm x 4mm) QFN

Note:

1. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com. (Micrel note body)