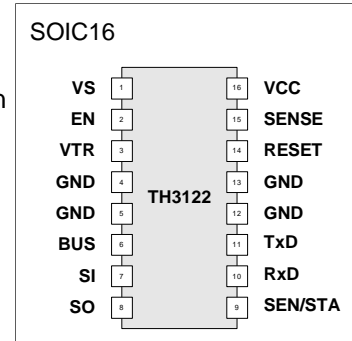


### Features and Benefits

- ❑ K-Bus Transceiver:
  - PNP-open emitter driver with slew rate control and current limitation
  - BUS input voltage -24V ... 30V (independently of  $V_S$ )
  - ISO 9141 and OBDII compliant
  - Possibility of BUS wake up
- ❑ Operating voltage  $V_S = 5.5 \dots 16 \text{ V}$
- ❑ Very low standby current consumption  $< 100 \mu\text{A}$  in normal mode ( $< 50 \mu\text{A}$  in sleep mode)
- ❑ Linear low drop voltage regulator:
  - Output voltage  $5\text{V} \pm 2\%$
  - Output current max. 100mA
  - Output current limitation
- ❑ Overtemperature shutdown
- ❑ Configurable reset time (15ms/100ms) and reset threshold voltage (3.15V / 4.65V)
- ❑ Low voltage detection at  $V_S$
- ❑ Wake-up by K-BUS traffic and start-up capable independent of EN voltage level
- ❑ Universal comparator with an input voltage range  $-24\text{V} \dots 30\text{V}$  and digital output
- ❑ Load dump protected (40V)

### Pin Diagram



### Ordering Information

Part No.	Temperature Code	Package Code
TH3122	K ( -40°C to 125°C )	DF ( SOIC16, 300mil )

### General Description

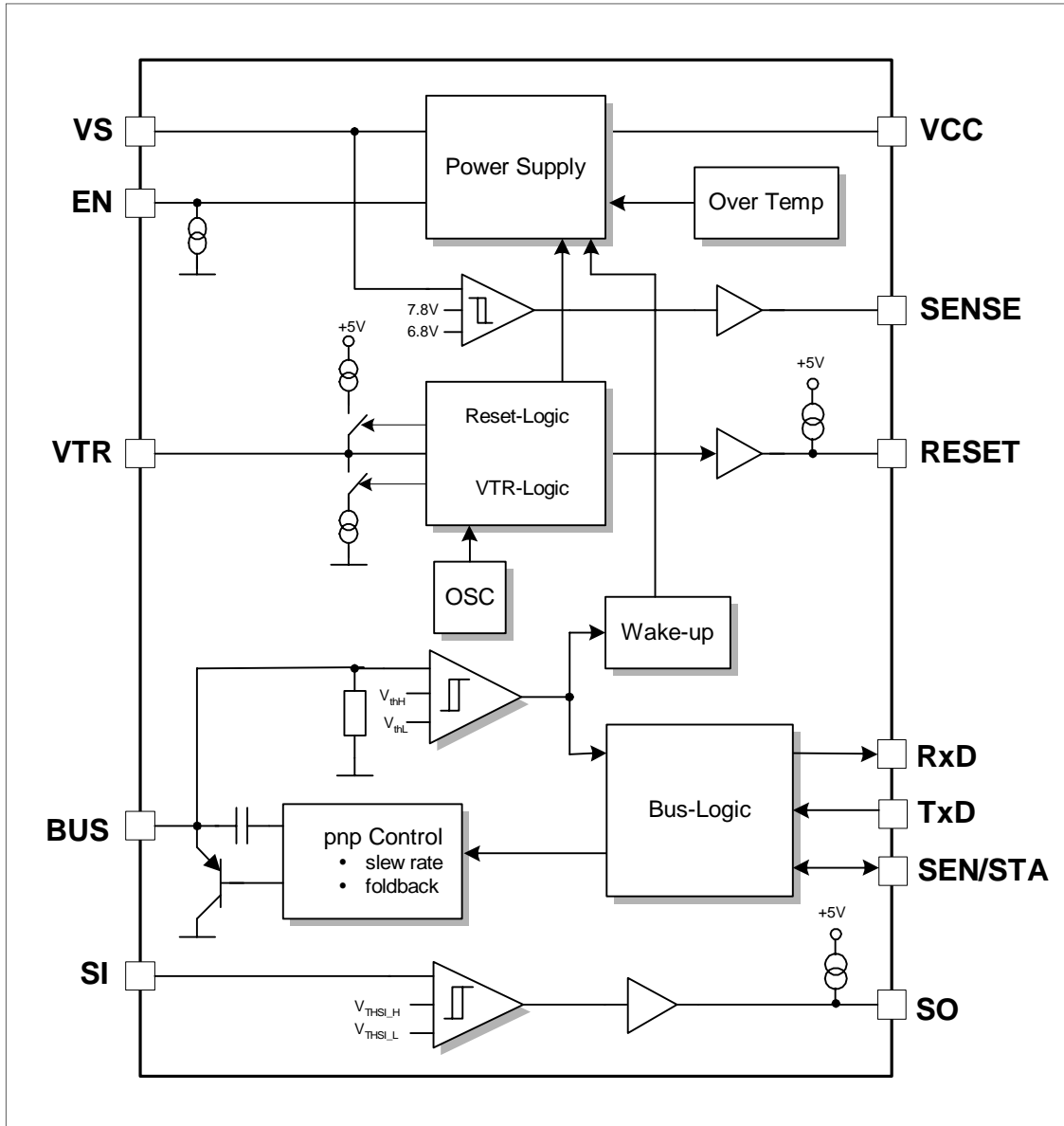
The TH3122 consists of a low drop voltage regulator 5V/100mA and a K-Bus transceiver. The transceiver is suitable for K-Bus systems conform to ISO 9141.

The combination of voltage regulator and bus transceiver in combination with the monitoring

functions make it possible to develop simple, but powerful and cheap nodes in K-Bus systems.

The wide output current area and the configurable reset time and reset voltage works together with many different microcontrollers.

*Functional Diagram*

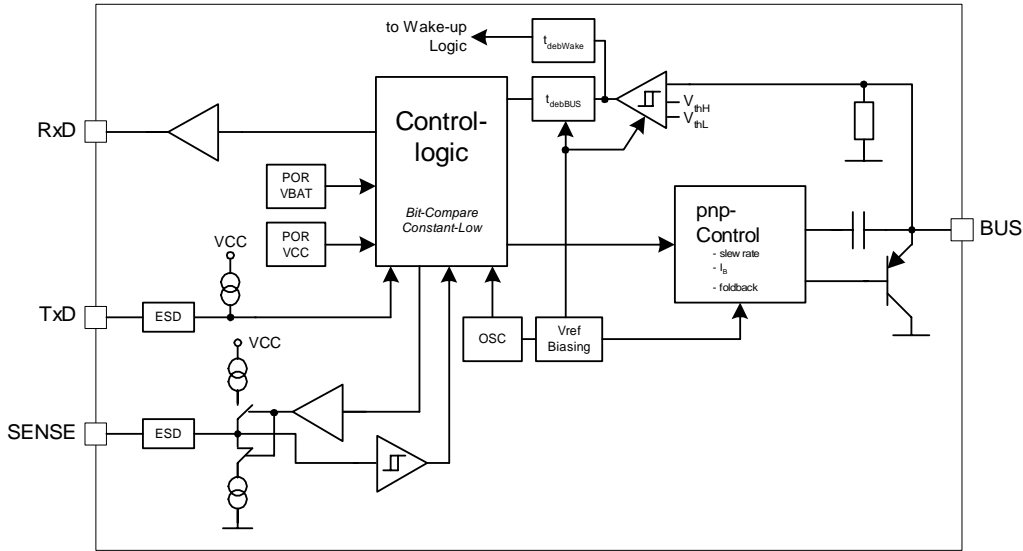


**Figure 1 - Block Diagram**

*Functional Description*

The TH3122 consists of a voltage regulator 5V/100mA and a K-Bus transceiver, which is a bi-directional bus interface device for data transfer between K-Bus and the K-Bus protocol controller.

Also integrated into the transceiver are a voltage and time controlled reset management, power down, wake up function and a universal comparator for extended applications.



**Figure 2 - Block Diagram K-Bus Transceiver**

**K-BUS Interface**

The BUS Interface builds the connection between the serial 5V bus line of the protocol controller and the 12V K-Bus line.

The transceiver consists of a pnp-driver with slew rate control and fold-back characteristic and contains also in the receiver a high voltage comparator followed by a debouncing unit.

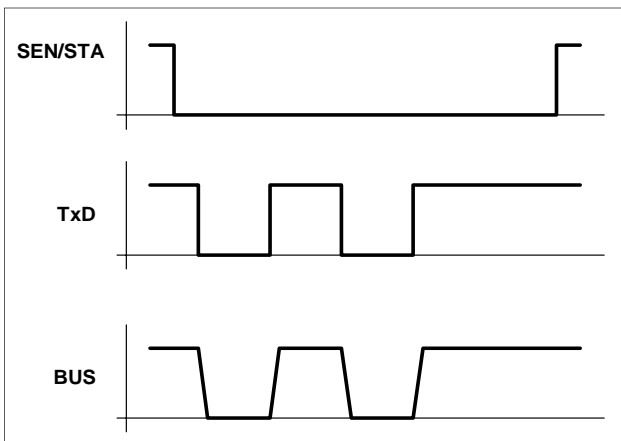
electromagnetic emission of the bus line, the TH3122 has an integrated slew rate control.

**Receive Mode**

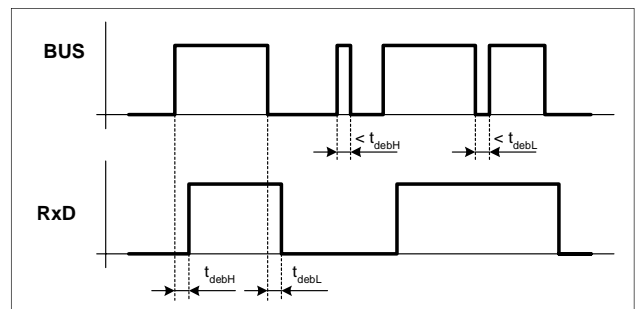
The data at the pin BUS will be transferred to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit.

**Transmit Mode**

During the transmission the data at the pin TxD will be transferred to the pin BUS. To minimize the



**Figure 3 - Transmit Mode Pulse Diagram**

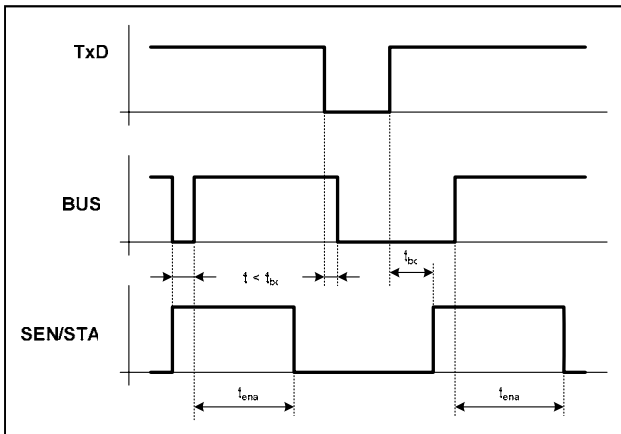


**Figure 4 - Receive Mode Pulse Diagram**

**Bit Compare**

If the signals at the pin TxD and the pin BUS within a specified time  $t_{bc}$  are not identical, the transmission will be interrupted.

If both signals at TxD and BUS are “High” within the time  $t_{ena}$  the transmission will be enabled. The bit-compare-function is active when the pin SEN/STA is open (not overwritten).



**Figure 5 - Bit Compare Pulse Diagram**

**SEN/STA**

The pin SEN/STA is bidirectional. Used as an output the pin indicates whether the transmit-path is enabled or disabled:

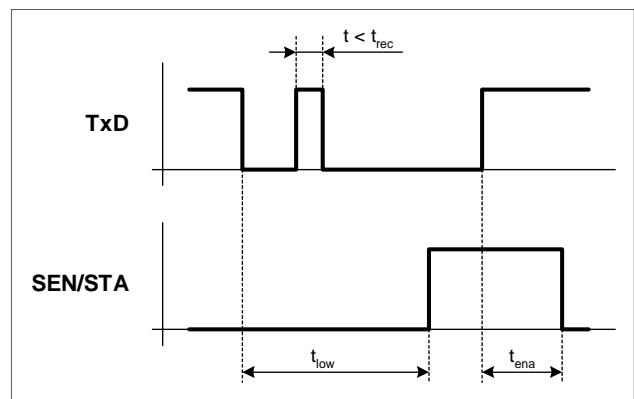
- SEN/STA = "0"  
transmission path is enabled
- SEN/STA = "1"  
transmission path is disabled

Using this pin as an input the transmission path can be overwritten (independent of bit-compare and constant-low function):

- SEN/STA="0"  
forcing the transmission path free
- SEN/STA="1"  
disable the transmission path

**Constant Low Switch Off**

A falling edge at pin TxD (from “1” to “0”) starts the internal constant low timer (SEN/STA open). If the low level “0” is valid for the time  $t_{low}$  the transmission unit of the TH3122 will be disabled. The receive unit is still active. A high level “1” at TxD with a minimum pulse width of  $t_{rec}$  resets the constant low timer. Transmitting is not possible until TxD and BUS is High for the time  $t_{ena}$ .



**Figure 6 - Constant Low Pulse Diagram**

**Linear Regulator and Controlling Functions**

**Regulator**

The TH3122 has an integrated linear regulator with an output voltage of  $5V \pm 2\%$  and an output current of max. 100mA. The regulator is switched on or off with a signal on the EN pin or wakes up with a BUS signal.

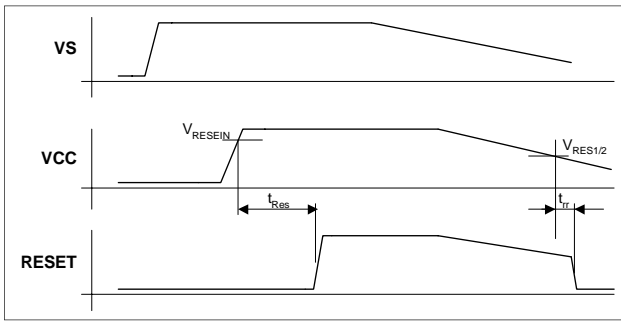
**Initialization**

The initialization is started if the power supply is switched on, or after the temperature limitation has switched off the regulator or in case of BUS traffic (wake up).

If the  $V_{CC}$  voltage level is higher than  $V_{RESEIN}$ , the reset time  $t_{RES}$  is started. This reset time is determined by the

voltage level on the VTR pin (see table VTR Programming). After  $t_{RES}$  a rising edge on the RESET output is generated (see figure 7 - Initialization).

The regulator is active and can only be switched off with a falling edge on EN. The regulator remains with EN=high in active mode and therefore the  $V_{CC}$  voltage is also active.



**Figure 7 - Initialization**

The input EN has an internal pull down resistor. If EN=high, the internal pull down current is switched off to minimize the quiescent current.

**RESET Output**

The RESET output is switched from low to high if  $V_S$  is switched on and  $V_{CC} > V_{RESEIN}$  after the time  $t_{RES}$ .

If the voltage  $V_{CC}$  drops below  $V_{RES1}$  or  $V_{RES2}$  then the RESET output is switched from high to low after the time  $t_{tr}$  has been reached.

The voltage level for  $V_{RES1}$  and  $V_{RES2}$  and the corresponding times  $t_{RES}$  can be programmed via the analogue input VTR.

**Wake up with BUS traffic**

If the regulator is put in standby mode it can be woken up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 45  $\mu$  s will switch on the regulator.

After the BUS has woken up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

**Reset Programming on VTR**

With the VTR pin the reset switches off levels and delay time can be programmed.

The voltage on VCC influences the reset function.

VTR-Mode	$V_{RES}$	$t_{RES}$
VTR = GND	$V_{RES} = V_{RES1} = 3.15V$	100ms
VTR = VCC	$V_{RES} = V_{RES2} = 4.65V$	100ms
VTR with $R \geq 50k \Omega$ to GND	$V_{RES} = V_{RES1} = 3.15V$	15ms
VTR with $R \geq 50k \Omega$ to VCC	$V_{RES} = V_{RES2} = 4.65V$	15ms

**VTR-Programming**

The voltage on VTR input is read out if the voltage at this pin is higher than  $V_{RESEIN}$ . This value defines the reset switch off voltage  $V_{RES}$ . With the next oscillator cycle it switches on the pull up current source if VTR=low or the pull down current source if VTR=high. The sources are active for one oscillator cycle. The level changes during this procedure on VTR, which depends on the external pull up or pull down resistors control the reset time  $t_{RES}$ .

**Temperature Limitation**

If the junction temperature  $150^\circ C < T_j < 170^\circ C$  the over temperature recognition will be active and the regulator voltage and the BUS driver will be switched off. After  $T_j$  falls below  $140^\circ C$  the TH3122 will be initialized, independently of the voltage levels on EN and BUS.

The function of the TH3122 is possible between  $T_{Amax}$  and the switch off temperature, but small parameter differences can appear.

**Low Voltage Detection  $V_S$**

Low voltage on  $V_S$  is monitored on SENSE output.

If  $V_S$  has reached the level of  $V_S = 6.8V$  then the SENSE output generates low level. The normal operating range is  $V_S > 7.8V$  and the SENSE output generates a high level.

**Universal Comparator**

The TH3122 consist of a universal comparator for general use. The positive input of this comparator is connected to the pin SI. The input voltage range of SI is  $0V \dots V_S$ . The input voltage is compared with a fixed reference voltage at high or low level and the comparator output SO drives a 5V digital signal.

*Application Hints*

**Operating during Disturbances**

The absence of  $V_S$ ,  $V_{CC}$  or GND connection or ground shift either alone or in any combination, do not influence or disturb the communication between other bus nodes.

**Undervoltage**

The reset unit secures the correct behavior of the driver during undervoltage. The inputs have pull-up or pull-down characteristics and have therefore defined voltage levels.

With  $4.5V \leq V_{CC} \leq 5.25V$  the bus connection operates within the correct parameters .

If  $V_{RES1} \leq V_{CC} \leq 4.5V$  the TxD signal is transmitted to the bus. The receive mode is also active.

If  $V_{CC} < V_{RES1}$  the bus driver is tristate.

SENSE and SO output the correct signal if  $V_{CC} > V_{RES}$  . The specified values of the input voltages on SO can't guaranteed.

**Regulator Circuitry**

The choice and dimension of the capacitor on VCC is determined by application point of view. Important parameters are the current difference on load changes and the maximum short time voltage drop.

The VCC pin must be connected to a min.  $2\mu F$  capacitor for stable operating of the regulator in the whole operating range.

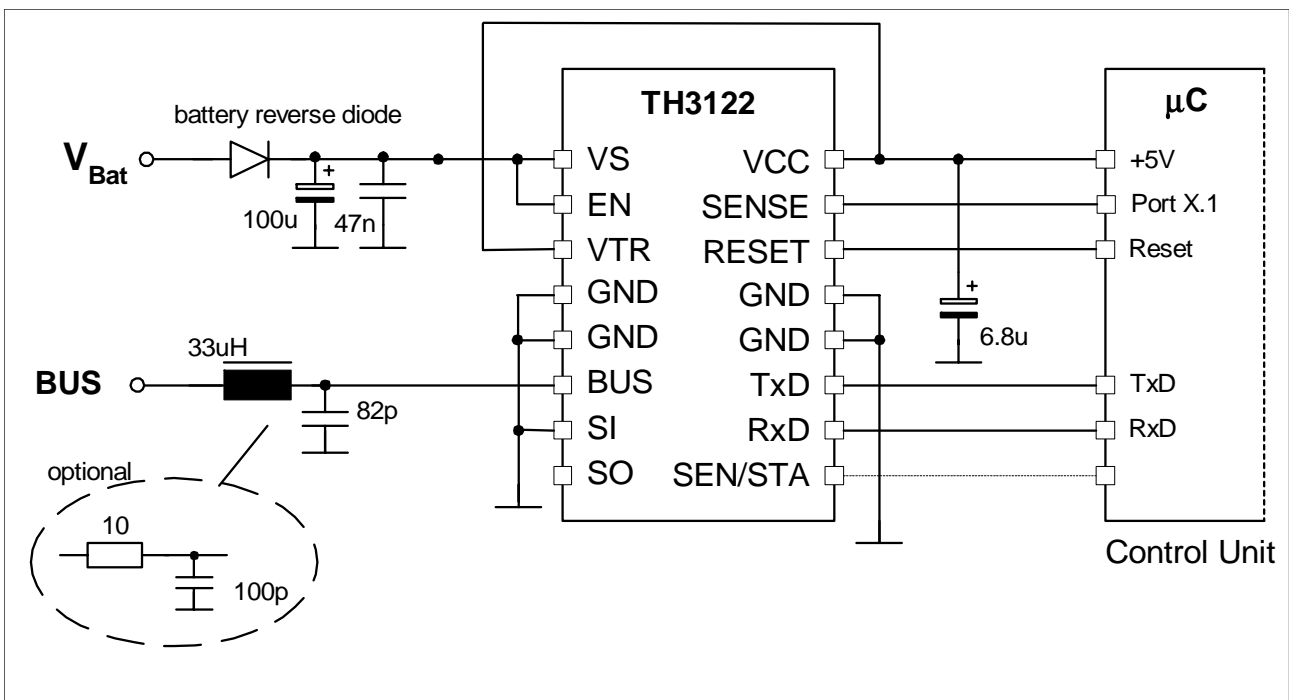
**Short Circuit Proof**

All in- and outputs are short circuit proof to battery and ground. A thermal shut down circuit prevents VCC and BUS from any damage.

**Baud Rate**

The TH3122 has a maximum Baud rate of 9600 Baud ( $C_{BUS} < 25nF$ ,  $R_{PU} > 400\Omega$ ).

**Application Circuitry**



**Figure 8 - Application Circuit**

There should be used an LC-Filter to minimize the influence of EMI on the BUS lines.

### Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding

any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH3122 is only specified within the limits shown in "Operating conditions".

### Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	$V_S$	5.25	16	V
Supply voltage	$V_{CC}$	4.75	5.25	V
Operating ambient temperature	$T_A$	-40	+125	°C
Junction temperature <sup>[1]</sup>	$T_J$		+150	°C

### Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at $V_S$ <sup>[2]</sup>	$V_S$		-1.0	16	V
		$T \leq 1\text{min}$	-	30	
		$T \leq 500\text{ms}$	-	40	
Input voltage at pin BUS <sup>[2]</sup>	$V_{INBUS}$		-24	30	V
		$T \leq 500\text{ms}$	-	40	
Difference $V_S-V_{CC}$	$V_{S-VCC}$		-0.3	40	V
Input voltage at pin EN and SI	$V_{INENSI}$		-0.3	$V_S+0.3$	V
Input voltage at pin VTR, TxD, SEN/STA, SO, RESET, SENSE	$V_{IN}$		-0.3	$V_{CC}+0.3$	V
Input current at pin EN, VTR, SI, SO, SEN/STA, TxD, RxD, RESET, SENSE	$I_{IN}$		-25	25	mA
Input current for short circuit of pin $V_S$ and $V_{CC}$	$I_{Short}$		-500	500	mA
Power dissipation	$P_0$	Internal limited <sup>[3]</sup> <sup>[4]</sup>			mW
Thermal resistance from junction to ambient	$R_{THJA}$			50	K/W
Junction temperature <sup>[4]</sup>	$T_J$			150	°C
Storage temperature	$T_{STG}$		-55	150	°C

<sup>[1]</sup> Junction temperature is defined in IEC 747-1

<sup>[2]</sup> The current and voltage values are valid independent from each other.

<sup>[3]</sup> The maximum power dissipation is defined by the ambient temperature and the thermal resistance. It can be calculated with

$P_0 = (V_S - V_{CC}) \cdot I_{VCC} + P_{BUS}$ .  $P_{BUS}$  is the BUS driver output with normally  $\leq 25\text{mW}$

<sup>[4]</sup> see over temperature protection

### Static Characteristics

( $V_S = 5.25$  to  $16V$ ,  $V_{CC} = 4.75$  to  $5.25V$ ,  $T_A = -40$  to  $+125^\circ C$ , unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Linear Regulator</b>						
Output voltage VCC	$V_{CCn}$	$5.5V \leq V_S \leq 16V$ $T_A = 25^\circ C$	4.95	5.0	5.05	V
	$V_{CCt}$	$5.5V \leq V_S \leq 16V$	4.90	5.0	5.10	V
	$V_{CCh}$	$V_{SUP} > 16V$	4.95	5.0	5.25	V
	$V_{CCl}$	$3.3V < V_S < 5.5V$	$V_S - V_D$		5.1	V
Supply current, „normal mode“	$I_{Snl}$	$V_{EN} = V_S = 12V$ , Pins 8-11, 14-16 open			100	$\mu A$
Supply current, „sleep mode“	$I_{Ssleep}$	$V_{EN} = 0V$ , $V_{CC}$ switched off		35	50	$\mu A$
Drop-out voltage	$V_D$	$V_S \geq 4.0V$ , $I_{VCC} = 25mA$			200	mV
		$V_S \geq 4.0V$ , $I_{VCC} = 100mA$			400	mV
		$V_S \geq 3.3V$ , $I_{VCC} = 20mA$			600	mV
Output current VCC	$I_{VCC}$	$V_S \geq 3.0V$	100			mA
Current limitation VCC	$I_{LVCC}$	$V_S > 0V$			300	mA
Load capacity	$C_{load}$	$ESR \leq 5\Omega$	2			$\mu F$
Power-on-reset threshold “V <sub>CC</sub> on”	$V_{RESEIN}$	referred to $V_{CC}$ , $V_S > 4.6V$	4.5	4.65	4.8	V
Power-on-reset threshold “V <sub>CC</sub> off”	$V_{RES2}$	$V_{TR} = High$ , $V_S > 0V$	4.5	4.65	4.8	V
	$V_{RES1}$	$V_{TR} = Low$ , $V_S > 0V$	3.0	3.15	3.3	
<b>SENSE-Output</b>						
VS - threshold low at SENSE	$V_{SENL}$		6.8			V
VS - threshold high an SENSE	$V_{SENH}$				7.8	V
Hysteresis SENSE	$V_{SENHYS}$		100			mV
Output voltage low	$V_{OL}$	$I_{OUT} = 1mA$			0.8	V
Output voltage high	$V_{OH}$	$I_{OUT} = -1mA$	$V_{CC} - 0.8$			V
<b>Enable-Input EN</b>						
Input voltage low	$V_{ENL}$		-0.3		1.75	V
Input voltage high	$V_{ENH}$		2.5		$V_S + 0.3$	V
Hysteresis	$V_{ENHYS}$		100			mV
Pull-down current EN	$I_{pdEN}$	$V_{EN} > V_{ENH}$	1.8	4.0	7.5	$\mu A$
		$V_{EN} < V_{ENL}$	70	100	130	$\mu A$
<b>Output RESET</b>						
Output voltage low	$V_{OL}$	$I_{OUT} = 1mA$ , $V_{SUP} > 5.5V$			0.8	V
		10 k $\Omega$ RESET to VCC			0.2	V
Pull-up current	$I_{pu}$		-500	-375	-250	$\mu A$



### Static Characteristics (continued)

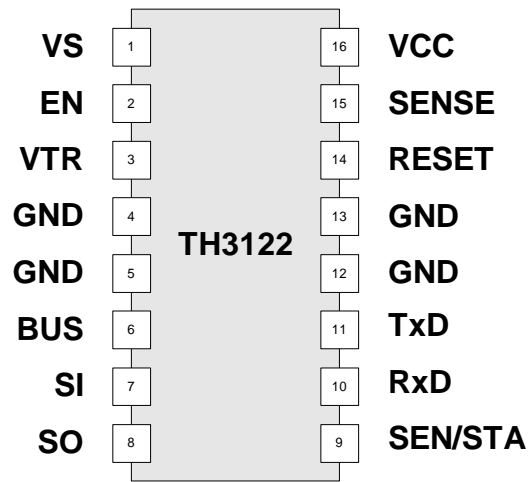
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Comparator SI, SO</b>						
Threshold low SI	$V_{IL}$		1.05	1.16		V
Threshold High SI	$V_{IH}$			1.21	1.4	V
Hysteresis	$V_{HYS}$		30			mV
Output voltage low at SO	$V_{OL}$	$I_{OUT} = 1 \text{ mA}, V_S > 5.5 \text{ V}$			0.8	V
		$10 \text{ k}\Omega \text{ SO to VCC}, V_{CC} > 3.3\text{V}$			0.4	V
Pull-up current at SO	$I_{pu}$		-500	-375	-250	$\mu\text{A}$
<b>Input VTR</b>						
Threshold low	$V_{TRL}$		0.15	0.25		$V_{CC}$
Threshold high	$V_{TRH}$			0.75	0.85	$V_{CC}$
Output current low	$I_{OL}$	$V_{CC} > 3.3 \text{ V}$	160	230	300	$\mu\text{A}$
Output current high	$I_{OH}$		-300	-230	-160	$\mu\text{A}$
<b>K-Bus-Interface</b>						
Power-on-reset threshold	$V_{POR}$	$V_{POR} = V_{RES1}$	3.0	3.15	3.3	V
Pull-up current TxD	$I_{pu}$		-500	-375	-250	$\mu\text{A}$
Pull-down current SEN/STA	$I_{pdSEN}$		250	375	500	$\mu\text{A}$
Pull-up current SEN/STA	$I_{puSEN}$		-500	-375	-250	$\mu\text{A}$
Input voltage low TxD, SEN/STA	$V_{IL}$				0.25	$V_{CC}$
Input voltage high TxD, SEN/STA	$V_{IH}$		0.75			$V_{CC}$
Input voltage low BUS	$V_{IL}$				0.45	$V_S$
Input voltage high BUS	$V_{IH}$		0.55			$V_S$
Hysteresis BUS	$V_{HYS}$			50		mV
Input resistance BUS	$R_{INBUS}$	$0 \leq V_{BUS} \leq 40 \text{ V}$	400	600	1500	k $\Omega$
		$0 \leq V_{BUS} \leq 40 \text{ V}$ $T_A \leq 125 \text{ }^\circ\text{C}$			1300	
		$V_{BUS} = -25\text{V}$ $T_A \leq 125 \text{ }^\circ\text{C}$	60			
Output voltage BUS	$V_{BUS}$	$V_S = 12\text{V}, \text{SENSE} = \text{low}$ $I_{OUT} = 40 \text{ mA}$			1.2	V
		$V_S = 12\text{V}, \text{SENSE} = \text{low}$ $I_{OUT} = 25 \text{ mA}$			1.0	
Current limitation BUS	$I_{LIM}$	$V_{BUS} > 2.5\text{V}$	40		100	mA
Output voltage low RxD	$V_{OL}$	$I_{OUT} = 1 \text{ mA}$			0.8	V
Output voltage high RxD	$V_{OH}$	$I_{OUT} = -1\text{mA}$	$V_{CC}-0.8$			V

### Dynamic Characteristics

( $5.25V \leq V_S \leq 16V$ ,  $4.75V \leq V_{CC} \leq 5.25V$ ,  $-40^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>RESET</b>						
Reset time	$t_{Res}$	$R_{VTR} < 1\text{ k}\Omega$	70	100	140	ms
		$R_{VTR} > 45\text{ k}\Omega$	10	15	20	ms
Reset rising time	$t_{rr}$		3.0	6.5	10	$\mu\text{ s}$
<b>K-Bus-Interface</b>						
Slew rate BUS falling edge	$dV/dT_{fall}$		-2.2	-1.6	-1.0	$V/\mu\text{ s}$
Slew rate BUS rising edge	$dV/dT_{rise}$		1.0	1.6	2.2	
Symmetry of Slew rate BUS	$dV/dT_{sym}$				0.3	$V/\mu\text{ s}$
Debouncing time BUS	$t_{debBUS}$	High pulse or low pulse	1.5	2.8	4.0	$\mu\text{ s}$
Symmetry of debouncing BUS	$t_{debsym}$				0.5	$\mu\text{ s}$
Propagation delay TxD -> RxD	$t_{pd}$				20	$\mu\text{ s}$
Symmetry of propagation delay TxD -> RxD	$t_{pdsym}$				3.5	$\mu\text{ s}$
Bit compare time BUS, SENSE, TxD	$t_{bc}$		35	52	70	$\mu\text{ s}$
Recovery time BUS, TxD	$t_{rec}$		30	50	75	$\mu\text{ s}$
Inhibit time for transmit BUS, TxD	$t_{ena}$		0.92	1.33	1.8	ms
Constant low switch off BUS, TxD	$t_{low}$		3	6	12	ms
Oscillator frequency	$f_{OSC}$		8	12	15	kHz
Debouncing time TxD	$t_{deb}$		0.6	1.0	1.5	$\mu\text{ s}$
Debouncing time EN	$t_{deb}$		200			ns
Wake-up debouncing BUS	$t_{debWake}$		25	45	90	$\mu\text{ s}$
Propagation delay SI -> SO	$t_{pdcomp}$		4		11	$\mu\text{ s}$
Debouncing VS-SENSE	$t_{deb}$		10	17	25	$\mu\text{ s}$

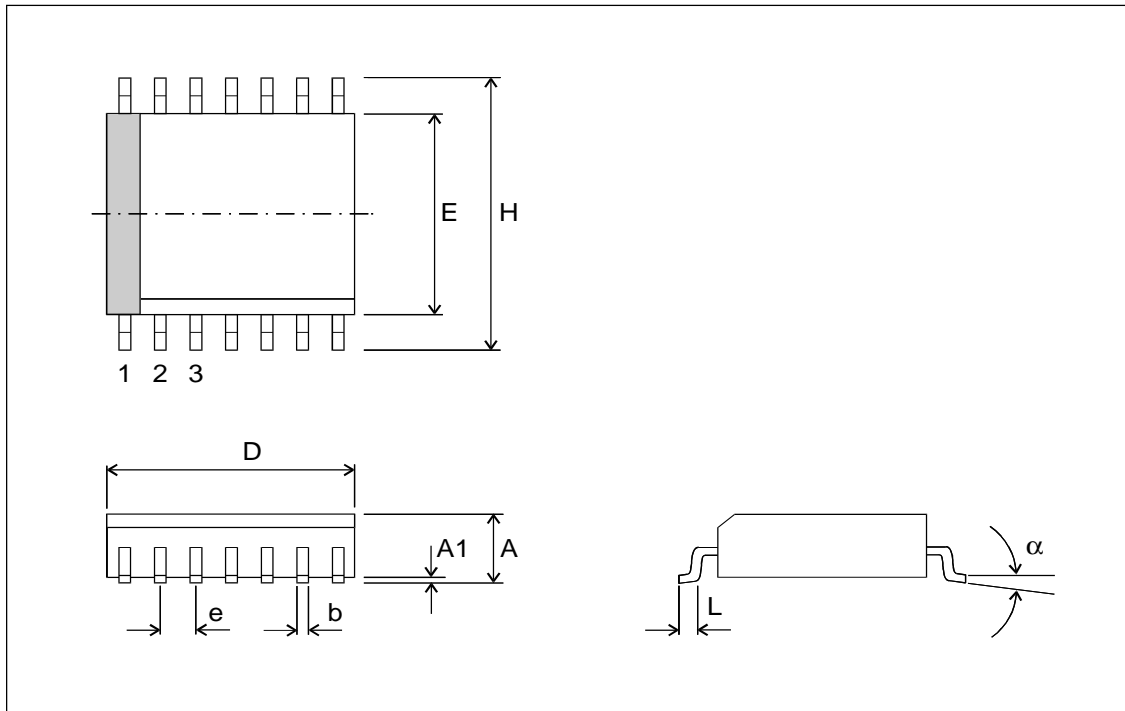
### Pin Description



Pin	Name	I/O	Function
1	VS		Supply voltage
2	EN	I	Enable Input voltage regulator, HV-pull-down-Input, High-active
3	VTR	I	Analogue Input - definition of reset time und Reset voltage level
4	GND		Ground
5	GND		Ground
6	BUS	I/O	Bi-directional bus line
7	SI	I	Comparator Input, HV-Input
8	SO	O	5V-Comparator Output
9	SEN/STA	I/O	Send status
10	RxD	O	Receive Output, 5V-push-pull
11	TxD	I	5V-Transmit Input, pull-up-Input
12	GND		Ground
13	GND		Ground
14	RESET	O	5V-output reset, active low
15	SENSE	O	5V-output of VS-Monitoring
16	VCC	O	Regulator output 5V/100mA

*Mechanical Specifications*

**DF (SOIC16) Package Dimensions**



**Small Outline Integrated Circuit (SOIC), DF (SOIC 16, 300 mil)**

All Dimension in mm, coplanarity < 0.1 mm									
	D	E	H	A	A1	e	b	L	$\alpha$
min	10.1	7.40	10.00	2.35	0.10	1.27	0.33	0.40	0°
max	10.5	7.60	10.65	2.65	0.30		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004"									
min	0.398	0.291	0.394	0.093	0.004	0.050	0.013	0.016	0°
max	0.413	0.299	0.419	0.104	0.012		0.020	0.050	8°

## *Assembly Information*

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

IPC/JEDEC J-STD-020

Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface Mount Devices  
(classification reflow profiles according to table 5-2)

EIA/JEDEC JESD22-A113

Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing  
(reflow profiles according to table 2)

CECC00802

Standard Method For The Specification of Surface Mounting Components (SMDs) of Assessed Quality

EIA/JEDEC JESD22-B106

Resistance to soldering temperature for through-hole mounted devices

EN60749-15

Resistance to soldering temperature for through-hole mounted devices

MIL 883 Method 2003 / EIA/JEDEC JESD22-B102

Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Based on Melexis commitment to environmental responsibility, European legislation (Directive on the Restriction of the Use of Certain Hazardous substances, RoHS) and customer requests, Melexis has installed a roadmap to qualify their package families for lead free processes also.

Various lead free generic qualifications are running, current results on request.

For more information on Melexis lead free statement see quality page at our website:  
<http://www.melexis.com/html/pdf/MLXleadfree-statement.pdf>

## *ESD Precautions*

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

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