

CFP2 LR4 Optical Transceiver with 100 Gigabit Ethernet for up to 10 km Reach

JC2 Series - JC2-10LR4AA2, JC2-10LM4AA2



www.lumentum.com Data Sheet

The Lumentum 100 G CFP2 LR4 optical transceiver is a full duplex, photonic-integrated optical transceiver that provides a high-speed link at a 103.125 or 111.81 Gbps aggregated data rate over up to 10 km of SMF-28. The module complies with the CFP MSA CFP2 Hardware Specification Rev. 1.0, IEEE 802.3-2012 Clause 88, and ITU-T G.959.1-2016-04.

The Lumentum 100 G CFP2 LR4 optical transceiver integrates the transmit and receive path onto one module. On the transmit side, four lanes of serial data streams are recovered, retimed, and passed on to four laser drivers, which control four electricabsorption modulated lasers (EMLs) with 1296, 1300, 1305, and 1309 nm center wavelengths. The optical signals are then multiplexed into a single-mode fiber through an industrystandard LC connector. On the receive side, four lanes of optical data streams are optically demultiplexed by an integrated optical demultiplexer. Each data steam is recovered by a PIN photodetector and transimpedance amplifier, retimed, and passed on to an output driver. This module features a hot-pluggable electrical interface, low power consumption, and MDIO management interface.

Key Features

- · Compliant with 100GBase-LR4 and OTU4
- Supports 103.125 to 111.81 Gbps line rates
- Integrated LAN WDM TOSA/ROSA for up to 10 km reach over SMF-28
- Duplex LC optical receptacle
- Operating temperature range of up to -5 to 70°C
- Low power dissipation <9 W (7 W typical)
- RoHS 6/6 compliant
- Single 3.3 V power supply
- · No external reference clock
- Fast Tx_DIS deassert time (<5 ms) for service disruption recovery
- Compliant with CEI-28G-VSR electrical interface
- Real-time digital diagnostic monitoring (DDM) support

Applications

- Local and wide area networks (LAN and WAN)
- Ethernet switches and router applications
- ITU-T OTU4 OTL4.4 applications

Compliance

- IEEE 802.3-2012 Clause 88 standard
- MDIO IEEE 802.3-2012 Clause 45 standard
- ITU-T G.959.1-2016-04 OTL4.4 standard
- OIF2010.404.08 CEI-28G-VSR standard
- MSA CFP2 Hardware Specification Rev. 1.0
- CFP MSA Management Interface Specification V2.4 (R06b)
- Class 1 laser safety
- Tested in accordance with Telcordia GR-468

Section 1 Functional Description

The Lumentum 100 G CFP2 LR4 Optical Transceiver is a full duplex parallel optical, parallel electric device containing both transmit and receive functions in a single module. The optical signals are multiplexed to a single-mode fiber through an industry-standard LC connector.

The module provides a high-speed link at an aggregated 103.125 to 111.81 Gbps signaling rate. It complies with IEEE 802.3-2012 Clause 88, 100GBase-LR4, and ITU-T G.959.1-2016-04 OTL4.4 (OTU4 striped across four physical lanes) 4I1-9D1F for up to 10 km reach over SMF-28 fiber, and OIF2010.404.08 CEI-28G-VSR electrical specifications. The MDIO management interface complies with IEEE 802.3-2012 Clause 45 standard. The transceiver complies with CFP MSA CFP2 Hardware Specification Rev. 1.0, CFP MSA Management Interface Specification Rev. 2.4, and OIF CEI-28G-VSR standards. Figure 1 shows block diagram.

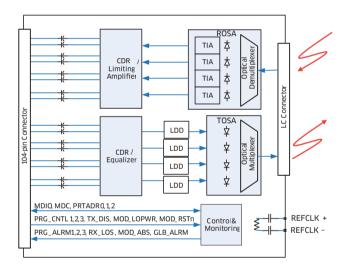


Figure 1. Lumentum CFP2 LR4 Optical Transceiver functional block diagram

Transmitter

The transmitter path converts four lanes of serial NRZ electrical data from 25.78 to 27.95 Gbps line rates to a standard compliant optical signal. Each signal path, or CEI lane, accepts a 100 Ω differential 100 mV peak-to-peak to 900 mV peak-to-peak 25 Gbps CEI electrical signal on TDxn and TDxp pins.

Inside the module, each differential pair of electric signals is input to a CDR (clock-data recovery) chip. The recovered and retimed signals are then passed to a laser driver which transforms the small swing voltage to an output modulation that drives a cooled EML laser. The laser drivers control four EMLs with 1296, 1300, 1305, and 1309 nm center wavelengths, respectively. Closed-loop control of the transmitted laser power and modulation swing

over temperature and voltage variations is provided on each laser. The optical signals from the four lasers are multiplexed together optically. The combined optical signals are coupled to single-mode optical fiber through an industry-standard LC optical connector. The optical signals are engineered to meet the 100 Gigabit Ethernet or OTU4 specifications.

Receiver

The receiver takes incoming combined four lanes of DC-balanced LAN-WDM NRZ optical data from 25.78 to 27.95 Gbps line rates through an industry-standard LC optical connector. The four incoming wavelengths are separated by an optical demultiplexer into four separated channels. Each output is coupled to a PIN photodetector. The electrical currents from each PIN photodetector are converted to a voltage in a high-gain transimpedance amplifier. The electrical output is recovered and retimed by the CDR chip. The four lanes of reshaped electrical signals are output on the RDxp and RDxn pins as a $100\ \Omega$ differential CEI signal.

Low-Speed Signaling

Low-speed signaling is based on low-voltage CMOS (LVCMOS) operating at a nominal voltage of 3.3 V for the control and alarm signals, and at a nominal voltage of 1.2 V for MDIO address, clock, and data signals. All low-speed inputs and outputs are based on CFP MSA CFP2 Hardware Specification Rev. 1.0 and CFP MSA Management Interface Specification Rev. 2.4 RO6b requirements.

Low-Speed Interface Connections	Definition			
MDC/MDIO	Management interface clock and data lines.			
PRTADRO, 1, 2	Input pins. MDIO physical port addresses.			
GLB_ALRMn	Output pin. When asserted low, indicates that the module has detected an alarm condition in any MDIO alarm register.			
PRG_CNTL1, 2, 3	Input pins. Programmable control lines defined in the CFP MSA Management Interface Specification. Pulled up with 4.7 to 10 k Ω resistors to 3.3 V inside the CFP2 module.			
TX_Disable	Input pin. When asserted high or left open, the transmitter output is turned off. When Tx_Disable is asserted low or grounded, the module transmitter is operating normally. Pulled up with 4.7 to 10 k Ω resistors to 3.3 V inside the CFP2 module.			
MOD_LOPWR	Input pin. When asserted high or left open, the CFP2 module is in low-power mode. When asserted low or grounded, the module is operating normally. Pulled up with 4.7 to 10 k Ω resistors to 3.3 V inside the CFP2 module.			
MOD_RSTn	Input pin. When asserted low or grounded, the module is in reset mode. When asserted high or left open, the CFP2 module is operating normally after an initialization process. Pulled down with 4.7 to 10 ${\rm k}\Omega$ resistors to ground inside the CFP2 module.			

Low-Speed Interface Connections	Definition
PRG_ALRM1, 2, 3	Output pins. Programmable alarm lines defined in the CFP MSA Management Interface Specification.
MOD_ABS	Output pin. Asserted high when the CFP2 module is absent and is pulled low when the CFP2 module is inserted.
RX_LOS	Output pin. Asserted high when receiving insufficient optical power for reliable signal reception.

Section 2 Application Schematics

Figure 2 shows an example of an application schematic showing connections from a host IC and host power supply to the Lumentum 100G CFP2 LR4 Optical Transceiver.

CFP2 modules are hot-pluggable and active connections are powered by individual power connection at 3.3 V nominal voltage. Multiple modules can share a single 3.3 V power supply with individual filtering. A possible example of a power-supply filtering circuit that might be used on the host system is a proportional integral (PI) C-L-C filter. To limit wideband noise power, the host system and module shall each meet a maximum of 2% peak-to-peak noise when measured with a 1 MHz low-pass filter. In addition, the host system and the module shall each meet a maximum of 3% peak-to-peak noise when measured with a filter from 1 to 10 MHz.

A module will meet all electrical requirements and remain fully operational in the presence of noise on the 3.3 V power supply. Power supply filtering components should be placed as close to the $V_{\rm cc}$ pins of the host connector as possible for optimal performance.

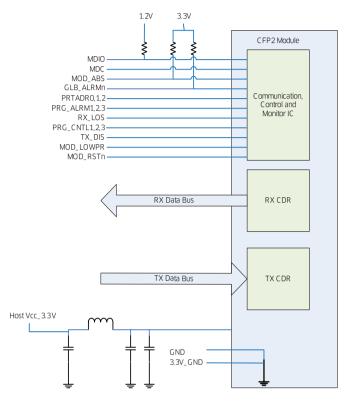


Figure 2. Application schematics for the Lumentum CFP2 optical transceiver

Section 3 **Technical Specifications**

Section 3.1	Pin Function Definitions
Section 3.2	CFP2 Lane Assignment
Section 3.3	Absolute Maximum Ratings
Section 3.4	Low-Speed Electrical Characteristics
Section 3.5	High-Speed Electrical Characteristics
Section 3.6	Timing Requirement of Control and Status I/O
Section 3.7	MDIO Management Interface
Section 3.8	Optical Transmitter Characteristics
Section 3.9	Optical Receiver Characteristics
Section 3.10	Module Startup Setup for Program Control (PRG_CNTLx) Pins
Section 3.11	Regulatory Compliance
Section 3.12	Module Outline
Section 3.13	Connectors

3.1 **Pin Function Definitions**

	Bottom (Nx25G)
1	GND
2	(TX_MCLKn)
3	(TX_MCLKp)
4	GND
5	N.C.
6	N.C.
7	3.3V_GND
8	3.3V_GND
9	3.3V
10	3.3V
11	3.3V
12	3.3V
13	3.3V_GND
14	3.3V_GND
15	VND_IO_A
16	VND_IO_B
17	PRG_CNTL1
18	PRG_CNTL2
19	PRG_CNTL3
20	PRG_ALRM1
21	PRG_ALRM2
22	PRG_ALRM3
23	GND
24	TX_DIS
25	RX_LOS
26	MOD_LOPWR
27	MOD_ABS
28	MOD_RSTn
29	GLB_ALRMn
30	GND
31	MDC
32	MDIO
33	PRTADR0
34	PRTADR1
35	PRTADR2
36	VND_IO_C
37	VND_IO_D
38	VND_IO_E
39	3.3V_GND
40	3.3V GND
41	3.3V
42	3.3V
43	3.3V
44	3.3V
45	3.3V_GND
46	3.3V GND
47	N.C.
48	N.C.
49	GND
50	(RX MCLKn)
51	(RX MCLKII)

	Top (4x25G)
104	GND
103	N.C.
102	N.C.
101	GND
100	TX3n
99	TX3p
98	GND
97	TX2n
96	TX2p
95	GND
94	N.C.
93	N.C.
92	GND
91	N.C.
90	N.C.
89	GND
88	TX1n
87	TX1p
86	GND
85	TX0n
84	TX0p
83	GND
82	N.C.
81	N.C.
80	GND
79	(REFCLKn) (REFCLKp)
78	
77	GND
76	N.C.
75	N.C.
74	GND
73	RX3n
72	RX3p
71	GND
70 69	RX2n
68	RX2p GND
67	N.C.
66	N.C.
65	GND
64	N.C.
63	N.C.
62	GND
61	RX1n
60	RX1p
59	GND
58	RX0n
57	RX0p
56	GND
55	N.C.
54	N.C.
52	GND

Figure 3. CFP2 optical transceiver pin assignments

Table 1.	Pin de	scriptions				
Pin No.	Туре	Name	Description			
1		GND	Module ground			
2	CML	(TX_ MCLKn)	No connect			
3	CML	(TX_ MCLKp)	No connect			
4		GND	Module ground			
5		N.C.	No connect			
6		N.C.	No connect			
7		3.3V_GND	3.3 V ground; tied with module ground			
8		3.3V_GND	3.3 V ground; tied with module ground			
9		3.3 V	3.3 V module supply voltage			
10		3.3 V	3.3 V module supply voltage			
11		3.3 V	3.3 V module supply voltage			
		3.3 V	3.3 V module supply voltage			
		3.3 V_GND	3.3 V ground; tied with module ground			
14		3.3 V_GND	3.3 V ground; tied with module ground			
15		VND_IO_A	Module vendor IO A; do not connect			
16		VND_IO_B	Module vendor IO B; do not connect			
17	LVCMOS ¹	PRG_ CNTL1	Programmable control 1; MSA default: TRXIC_RSTn; "0": reset; "1": enable			
18	LVCMOS ¹	PRG_ CNTL2	Programmable control 2; MSA defaul Hardware interlock LSB; Default "0": ≤ 9 W			
19	LVCMOS ¹	PRG_ CNTL3	Programmable control 3: MSA default: Hardware interlock MSB; Default "1": ≤ 9 W			
20	LVCMOS	PRG_ ALRM1	Programmable alarm 1; MSA default: HIPWR_ON; "1": module power up completed, "0": module not high powered up			
21	LVCMOS	PRG_ ALRM2	Programmable alarm 2; MSA default: MOD_READY, "1": Ready, "0": not Ready			
22	LVCMOS	PRG_ ALRM3	Programmable alarm 3; MSA default: MOD_FAULT, "1": Fault, "0": no Fault			
23		GND	Module ground			
24	LVCMOS ¹	TX_DIS	Transmitter disable for all lanes; "1" or NC: transmitter disabled; "0": transmitter enabled			
25	LVCMOS	RX_LOS	Receiver loss of optical signal; "1": low optical signal, "0": normal condition			
26	LVCMOS ¹	MOD_ LOPWR	Module low power mode; "1" or NC: module in low power mode, "0": power on enabled			
27	GND	MOD_ABS	Module absent; "1" or NC: module absent; "0": module present. Pull up resistor on host.			
28	LVCMOS ²	MOD_RSTn	Module reset; "0": reset the module; "1" or NC: module enabled			
29	LVCMOS	GLB_ ALRMn	Global alarm; "0": alarm in any MDIO alarm register; "1": no alarm condition. Pull up resistor on host.			

Table 1. Pin descriptions (Continued)

Table 1. Pin descriptions (Continued)						
Pin No.	Туре	Name	Description			
30		GND	Module ground			
31	1.2V CMOS	MDC	Management interface clock input			
32	1.2V CMOS	MDIO	Management interface bidirectional data			
33	1.2V CMOS	PRTADR0	MDIO physical port address bit 0			
34	1.2V CMOS	PRTADR1	MDIO physical port address bit 1			
35	1.2V CMOS	PRTADR2	MDIO physical port address bit 2			
36		VND_IO_C	Module vendor IO C; do not connect			
37		VND_IO_D	Module vendor IO D; do not connect			
38		VND_IO_E	Module vendor IO E; do not connect			
39		3.3 V_GND	3.3 V ground; tied with module ground			
40		3.3 V_GND	3.3 V ground; tied with module ground			
41		3.3 V	3.3 V module supply voltage			
42		3.3 V	3.3 V module supply voltage			
43		3.3 V	3.3 V module supply voltage			
44		3.3 V	3.3 V module supply voltage			
45		3.3 V_GND	3.3 V ground; tied with module ground			
46		3.3 V_GND	3.3 V ground; tied with module ground			
47		N.C.	No connect			
48		N.C.	No connect			
49		GND	Module ground			
50	CML	(RX_ MCLKn)	No connect			
51	CML	(RX_ MCLKp)	No connect			
52		GND	Module ground			
53		GND	Module ground			
54		N.C.	No connect			
55		N.C.	No connect			
56		GND	Module ground			
57		RXOP	25 Gbps receiver data; Lane 0			
58		RXOn	25 Gbps receiver data bar; Lane 0			
59		GND	Module ground			
60		RX1p	25 Gbps receiver data; Lane 1			
61		RX1n	25 Gbps receiver data bar; Lane 1			
62		GND	Module ground			
63		N.C.	No connect			
64		N.C.	No connect			
65		GND	Module ground			
66		N.C.	No connect			
67		N.C.	No connect			
68		GND	Module ground			
69		RX2p	25 Gbps receiver data; Lane 2			
70		RX2n	25 Gbps receiver data bar; Lane 2			
71		GND	Module ground			
72		RX3p	25 Gbps receiver data; Lane 3			
73		RX3n	25 Gbps receiver data bar; Lane 3			

Table 1. Pin descriptions (Continued)

Pin No.	Туре	Name	Description	
74	. 7 -	GND	Module ground	
75		N.C.	No connect	
76		N.C.	No connect	
77		GND	Module ground	
78	CML	(REFCLKp)	Module reference clock. No connect.	
79	CML	(REFCLKn)	Module reference clock. No connect.	
80		GND	Module ground	
81		N.C.	No connect	
82		N.C.	No connect	
83		GND	Module ground	
84		TX0p	25 Gbps transmitter data; Lane 0	
85		TX0n	25 Gbps transmitter data bar; Lane 0	
86		GND	Module ground	
87		TX1p	25 Gbps transmitter data; Lane 1	
88		TX1n	25 Gbps transmitter data bar; Lane 1	
89		GND	Module ground	
90		N.C.	No connect	
91		N.C.	No connect	
92		GND	Module ground	
93		N.C.	No connect	
94		N.C.	No connect	
95		GND	Module ground	
96		TX2p	25 Gbps transmitter data; Lane 2	
97		TX2n	25 Gbps transmitter data bar; Lane 2	
98		GND	Module ground	
99		TX3p	25 Gbps transmitter data; Lane 3	
100		TX3n	25 Gbps transmitter data bar; Lane 3	
101		GND	Module ground	
102		N.C.	No connect	
103		N.C.	No connect	
104		GND	Module ground	

^{1.} Pulled up with 4.7 to 10 $k\Omega$ to 3.3 V inside the module.

3.2 CFP2 Lane Assignment

Lane	Center Frequency	Center Wavelength	Wavelength Range
LO	231.4 THz	1295.56 nm	1294.53 to 1296.59 nm
L1	230.6 THz	1300.05 nm	1299.02 to 1301.09 nm
L2	229.8 THz	1304.58 nm	1303.54 to 1305.63 nm
L3	229.0 THz	1309.14 nm	1308.09 to 1310.19 nm

^{2.} Pulled down with 4.7 to 10 $k\Omega$ to GND inside the module.

3.3 Absolute Maximum Ratings

Absolute maximum ratings represent the device's damage threshold. Damage may occur if the device is operated outside the limits stated here. Performance is not guaranteed and reliability is not implied for operation at any condition outside the recommended operating limits.

Parameter	Symbol	Ratings	Unit
Storage temperature	T _{st}	-40 to +85	°C
Operating case temperature	T _{OP}	-5 to +70	°C
Relative humidity	RH	5 to 85 (noncondensing)	%
Static electrical discharge (human body model)	ESD	500	V
Power supply voltages	V _{cc} , max	-0.3 to 3.6	V
Receive input optical power (damage threshold)	P _{dmg}	+ 5.5	dBm

3.4 Low-Speed Electrical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Supply Currents and Voltages						
Voltage	V _{cc}	3.135	3.3	3.465	V	With respect to GND
Supply current	I _{cc}			3.75	А	Per MSA MSA CFP2 Hardware Specification
Power dissipation	P _{wr}		7.0	9.0	W	Rev. 1.0 Table 4-1 Class 3
Power dissipation (low power mode)	P _{lp}			2.0	W	
Inrush current	I_inrush			100	mA/μs	
Turn-off current	I_turnoff	-100			mA/μs	
Low-Speed Control and Sense Signals, 3.3	V LVCMOS					
Outputs low voltage	V _{OL}			0.2	V	Ι _{οΗ} = 100 μΑ
Output high voltage	V _{OH}	V _{cc} -0.2			V	I _{OH} = -100 μA
Input low voltage	V _{IL}	-0.3		0.8	V	
Input high voltage	V _{IH}	2		V _{cc} + 0.3	V	
Input leakage current	I	-10		10	μΑ	
Low-Speed Control and Sense Signals, 1.2	V LVCMOS					
Outputs low voltage	V _{OL}	-0.3		0.2	V	
Output high voltage	V _{OH}	1.0		1.5	V	
Output low current	I _{OL}	4			mA	
Output high current	I _{OH}			-4	mA	
Input low voltage	V _{IL}	-0.3		0.36	V	
Input high voltage	V _{IH}	0.84		1.5	V	
Input leakage current	I _{IN}	-100		100	μΑ	
Input capacitance	С			10	pF	
MDC clock rate		0.1		4	MHz	

3.5 High-Speed Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Transmitter Electrical Input from Host at T	P1a (detailed specificatio	n in CEI-28G-VSR)			
Differential voltage pk-pk			900	mV	
Common mode noise (rms)			17.5	mV	
Differential termination mismatch			10	%	
Transition time		10		ps	20/80%
Common mode voltage		-0.3	2.8	V	
Eye width	EW15	0.46		UI	At 10 ⁻¹⁵ probability
Eye height	EH15	100		mV	At 10 ⁻¹⁵ probability
Receiver Electrical Output to Host at TP4 (a	detailed specification in Cl	EI-28G-VSR)			
Differential voltage pk-pk			900	mV	
Common mode noise (rms)			17.5	mV	
Differential termination mismatch			10	%	
Transition time		9.5		ps	20/80%
Vertical eye closure	VEC		5.5	dB	
Eye width	EW15	0.57		UI	At 10 ⁻¹⁵ probability
Eye height	EH15	228		mV	At 10 ⁻¹⁵ probability

3.6 Timing Requirement of Control and Status I/O

Parameter	Symbol	Min.	Max.	Unit	Notes
Minimum pulse width of control pin signal	t_CNTL	100		μS	
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	
Hardware MOD_LOPWR deassert	t_MOD_LOPWR_ deassert		60	S	Stored in NVR register 8072h
RX_LOS assert time	t_loss_assert		100	μS	From occurrence of loss of signal to assertion of RX_LOS
RX_LOS deassert time	t_loss_deassert		100	μS	From occurrence of return of signal to deassert of RX_LOS
GLB_ALRM assert time	GLB_ALRMn_assert		150	ms	A logic "OR" of associated MDIO alarm and status registers
GLB_ALRM deassert time	GLB_ALRMn_deassert		150	ms	A logic "OR" of associated MDIO alarm and status registers
Management interface clock period	t_prd	250		ns	MDC is 4 MHz rate or less
Host MDIO setup time	t_setup	10		ns	
Host MDIO hold time	t_hold	10		ns	
CFP2 MDIO delay time	t_delay	0	175	ns	
Initialization time from reset	t_initialize		2.5	S	
TX_Disable assert time	t_deassert		100	μS	Transmitter disable, application specific
TX_Disable deassert time ¹	t_assert		5	ms	Time from Tx Disable pin deasserted until CFP2 module enters the Tx-turn-on state Stored in NVR register 8073h

^{1.} The transceiver is stabilized prior to TX_Disable deassert event.

3.7 MDIO Management Interface

The Lumentum 100G CFP2 optical transceiver incorporates an MDIO management interface which is used for serial ID, digital diagnostics, and certain control and status report functions. The CFP2 transceiver supports MDIO pages 8000h NVR 1 Based ID registers, NVR 2 Alarm/Warning threshold registers, and NVR 4 tables, and pages A000h VR 1, and VR 3 tables.

Details of the protocol and interface are explicitly described in IEEE 802.3-2012 Clause 45 and CFP MSA Management Interface Specification V2p4_r06b. Please refer to the specifications for design reference.

3.8 Optical Transmitter Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Signaling rate, each lane		25.78125 ±100 ppm 27.9525 ±20 ppm			GBd	100GBase-LR4
						OTU4
The following specifications are applicable within the op	perating case temp	erature ran	ge			
Side-mode suppression ratio	SMSR	30			dB	
Total launch power				10.5	dD	100GBase-LR4
				10.0	dBm	OTU4
Average launch power, each lane¹	P _{avg}	-4.3		4.5	dDm	100GBase-LR4
		-0.6		4.0	dBm	OTU4
Extinction ratio	ER	4			dB	100GBase-LR4
		4		7		OTU4
Optical modulation amplitude, each lane (OMA) ²	OMA	-1.3		4.5	dBm	100GBase-LR4
Difference in launch power between any two lanes (OMA)				5	dB	100GBase-LR4, OTU4
Transmitter and dispersion penalty, each lane	TDP			2.2	dB	100GBase-LR4
OMA minus TDP, each lane	OMA-TDP	-2.3			dBm	100GBase-LR4
Average launch power of OFF transmitter, each lane				-30	dBm	100GBase-LR4
Optical return loss tolerance				20	dB	
Relative intensity noise	RIN ₂₀ OMA			-130	dB/Hz	100GBase-LR4
Transmitter reflectance ³				-12	dB	
Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			100GBase-LR4	

^{1.} Average launch power, each lane (min) is informative for 100GBase-LR4, not the principal indicator of signal strength.

^{2.} Even if the TDP < 1 dB, the OMA (min) must exceed this value.

^{3.} Transmitter reflectance is defined looking into the transmitter.

3.9 Optical Receiver Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Signaling rate, each lane		25	25.78125 ±100 ppm 27.9525 ±20 ppm		CD.I	100GBase-LR4
		2			GBd	OTU4
The following specifications are applicable within the ope	rating case tem	perature rang	ie			
Average receive power, each lane¹	P _{avg}	-10.6		4.5	dBm	100GBase-LR4
Average receive power, each lane ²	Pavg	-6.9		4	dDm	OTU4 with Tx ER of 4 to 7 dB
		-8.8		2.9	dBm	OTU4 with Tx ER > 7 dB
Receive power, each lane (OMA)				4.5	dBm	100GBase-LR4
Difference in launch power between any two lanes (OMA)				5.5	dB	100GBase-LR4, OTU4
Receiver Sensitivity (OMA), each lane ⁴ at BER= 1x10 ⁻¹²	R _{sen}			-8.6	dBm	100GBase-LR4
Equivalent receiver sensitivity ² at BER=1.8x10 ⁻⁴				-8.4	dD	OTU4 with Tx ER of 4 to 7 dB
				-10.3	dBm	OTU4 with Tx ER > 7 dB
Optical path penalty				1.5	dB	OTU4
Stressed receiver sensitivity (OMA), each lane	SRS			-6.8	dBm	100GBase-LR4, at TP3 for BER= 1x10 ⁻¹²
Stressed receiver sensitivity test conditions						
Vertical eye closure penalty, each lane ³	VECP		1.8		dB	100GBase-LR4
Stressed sys J2 jitter, each lane ³	J2		0.3		UI	100GBase-LR4
Stressed sys J9 jitter, each lane³	J9		0.47		UI	100GBase-LR4
Receiver reflectance				-26	dB	100GBase-LR4, OTU4
LOS assert ⁴	Plos_on			-15	dBm	
LOS hysteresis ⁴		0.5			dB	

^{1.} Minimum average receive power and maximum receiver sensitivity (OMA), each lane, is informative for 100GBase-LR4,

3.10 Module Startup Setup for Program Control (PRG_CNTLx) Pins

MSA default setting of PRG_CNTL1 is TRXIC_RSTn to reset Tx and Rx ICs. CFP2 operation and PRG_CNTL1 Pin State dependencies on hardware pin settings and Soft PRG_CNTL1 shall be as follows.

	PRG_CNTL1 (Hardware pin)	PRG_CNTL1 Pin State (Register A010h.1)	Soft PRG_CNTL1 (Register A010h.10)	CFP2 Operation
А	1=high (Normal)	1	0 (Normal)	Normal
В	1=high (Normal)	1	1 (Reset)	Reset
С	0=low (Reset)	0	0 (Normal)	Reset
D	0=low (Reset)	0	1 (Reset)	Reset

^{2.} For OTU4, 4l1-9D1F defines two sets of specification based on two options of transmitter ER. The minimum average receive power represents an Rx_sensitivity (OMA) of -7.5 dBm at worst case ER over all condition with 10 km fiber link at post GFEC of BER 1x10⁻¹². The maximum receiver sensitivity is informative and representing Rx_sensitivity (OMA) of -9.05 dBm at worst case ER over all condition at pre-GFEC of BER 1.8 x 10⁻⁴.

^{3.} Vertical eye closure penalty, stressed eye J2 jitter, and stressed eye J9 jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

^{4.} LOS function is implemented per modulated input signal.

Hardware pins PRG_CTRL2 and PRG_CTRL3 are used for the hardware interlock function during Initialization State. It is a logic signal CFP module generates internally based upon the comparisons between the module's power class and the host cooling capacity.

Pin No.	Symbol	Description				
17	PRG_CNTL1	Programmable Control 1 MSA Default:TRXIC_RSTn, Tx and Rx ICs reset "0": reset, "1":enabled				
18	PRG_CNTL2	Programmable Control 2 MSA default : Hardware interlock LSB	0	1	0	1
19	PRG_CNTL3	Programmable Control 3 MSA default : Hardware interlock MSB	0	0	1	1
		Power class	1	2	3*	4
		Module power dissipation (W)	≤ 3	≤ 6	≤ 9*	≥ 9

^{*}Lumentum CFP2 module power class/dissipation level

Its purpose is to prevent an otherwise-dangerous high-power condition that may harm either the host or the module itself, due to potential power requirements which the host cannot support. The status of HW_Interlock (CFP2 Module VR1, Address A01D, bit13) is defined as follows:

 $HW_{Interlock} = 0$ if HW_{IL}_{MSB} and $HW_{IL}_{LSB} = 11b$, or $HW_{Interlock} = 0$ if module power \leq Host cooling capacity, or else $HW_{Interlock} = 1$ if module power > Host cooling capacity.

In operation, the module samples the status of the HW_IL_MSB and HW_IL_LSB input pins once during the initialize state. To ensure a reliable sampling, the host shall hold HW_IL_MSB and HW_IL_LSB signal valid until the module exits initialize state. The module stores these values in a variable HW_IL_inputs.

When both the MOD_LOPWR input pin and the soft module low power register bit are deasserted, the module then compares the variable HW_IL_inputs to the power class for which it is designed (defined in the Power Class field of register 8001h). The result of this comparison updates the HW_Interlock status. The module remains in the low-power state if HW_Interlock evaluates to '1' (this does not result in a transition to the fault state). Conversely, if HW_Interlock evaluates to '0', the module may transition to the high-power-up state.

Host capable to manage CFP2 module with power class > 3 are recommended upon MOD_ABS pin deassertion to keep MOD_LOPWR input pin asserted. When MOD_LOPWR state is reached, the host shall interrogate the module via MDIO bus and check whether CFP2 exact power class derived from 807Eh register is matching the host cooling capacity. Only after a positive response from previous check the MOD_LOPWR input pin can be deasserted from the host.

After initialization, the Host is free to reprogram the usage of the PRG_CNTLn input pins and change their values at any time. The pin functions follow PRG_CNTL1, 2, and 3 Function Select settings (A005h, A006h, and A007h).

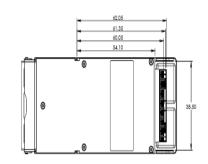
3.11 Regulatory Compliance

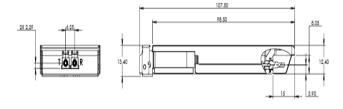
The Lumentum 100G CFP2 optical transceiver is RoHS 6/6 compliant and complies with international electromagnetic compatibility (EMC) and product safety requirements and standards.

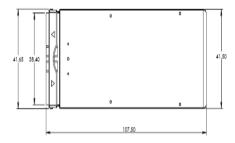
Table 2. Regulatory Compliance

Feature	Test Method	Performance					
Safety							
Product	UL 60950-1	UL recognized component for US and CAN					
	CSA C22.2 No. 60950-1						
	EN 60950-1	TUV certificate					
	IEC 60950-1	CB certificate					
	Flame Class V-0	Passes Needle Flame Test for component flammability verification					
	Low Voltage Directive 2014/35/EU	Certified to harmonized standards listed; Declaration of Conformity issued					
Laser	EN 60825-1, EN 60825-2	TUV certificate					
	IEC 60825-1	CB certificate					
	U.S. 21 CFR 1040.10	FDA/CDRH certified with accession number					
Electromagn	etic Compatibility						
Radiated	EMC Directive 2014/30/EU	Class B digital device with a minimum -6 dB margin to the limit. Final margin may vary					
emissions	FCC rules 47 CFR Part 15	depending on system implementation.					
	CISPR 22, CISPR32	Tested frequency range: 30 MHz to 40 GHz or 5th harmonic (5 times the highest frequency), whichever is less.					
	AS/NZS CISPR22, CISPR32	Requires good system EMI design practice to achieve Class B margins at the system leve					
	EN 55022, EN 55032						
	ICES-003, Issue 6						
	VCCI regulations						
Immunity	EMC Directive 2014/30/EU	Certified to harmonized standards listed; Declaration of Conformity issued					
	CISPR 24						
	EN 55024						
ESD	IEC/EN 61000-4-2	Exceeds requirements. Withstands discharges of ± 8 k V contact, ±15 k V air.					
Radiated	IEC/EN 61000-4-3	Exceeds requirements. Field strength of 10 V/m from 80 MHz to 6 GHz. No effect on					
immunity		transmitter/receiver performance is detectable between these limits.					
Restriction o	f Hazardous Substances (RoHS)						
RoHS	EU Directive 2011/65/EU	Compliant per the Directive 2011/65/EU of the European Parliament and of the 8 June 2011 Council on the restriction of the use of certain hazardous substances in electrical and electronic equipment (recast). A RoHS Certificate of Compliance (C of C) is available upon request. The product may use certain RoHS exemptions.					

3.12 Module Outline







3.13 Connectors

Fiber

The CFP2 module has a duplex LC receptacle connector.

Electrical

The electrical connector is the 104-way, two-row PCB edge connector. Customer connector is Yamaichi CN121P-104-0001 connector or equivalent.

Section 4 Other Related Information

Section 4.1	Packing and Handling Instructions
Section 4.2	Electrostatic Discharge
Section 4.3	Laser Safety
Section 4.4	Electromagnetic Compliance (EMC)

4.1 Package and Handling Instructions

Connector Covers

The Lumentum 100G CFP2 optical transceiver is supplied with an LC duplex receptacle. The connector plug supplied protects the connector during standard manufacturing processes and handling by preventing contamination from dust, aqueous solutions, body oils, or airborne particles.

Note: It is recommended that the connector plug remain on whenever the transceiver optical fiber connector is not inserted. the transceiver optical fiber connector is not inserted.

Recommended Cleaning and Degreasing Chemicals

Lumentum recommends the use of methyl, isopropyl, and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons, such as trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrolldone).

This product is not designed for aqueous wash.

Housing

The Lumentum CFP2 optical transceiver housing is made from zinc.

4.2 Electrostatic Discharge

Handling

Normal electrostatic discharge (ESD) precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and Operation

In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transceiver should meet and exceed common ESD

testing practices and fulfill system ESD requirements.

Typical of optical transceivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike, resulting in a short burst of bit errors. Such an event might require that the application reacquire synchronization at the higher layers (for example, serializer/deserializer chip).

4.3 Laser Safety

The transceiver is certified as a Class 1 laser product per international standard IEC 60825-1:2014 3rd edition and is considered non-hazardous when operated within the limits of this specification.

The transceiver complies with 21 CFR 1040.10 except for deviations pursuant to Laser Notice No. 50.



INVISIBLE LASER RADIATION CLASS 1 LASER PRODUCT per IEC 60825-1:2014 λ = 1294-1310nm, <15mW

Caution

Operating this product in a manner inconsistent with intended usage and specifications may result in hazardous radiation exposure.

Use of controls or adjustments or performance of procedures other than these specified in this product data sheet may result in hazardous radiation exposure.

Tampering with this laser product or operating this product outside the limits of this specification may be considered an 'act of manufacturing' and may require recertification of the modified product.

Viewing the laser output with certain optical instruments, such as eye loupes, magnifiers, microscopes, within a distance of 100 mm may pose an eye hazard.

4.4 EMC (Electromagnetic) Compliance

The transceiver has been tested and found compliant with international electromagnetic compatibility (EMC) standards and regulations and is declared EMC compliant as stated below.

Note: EMC performance depends on the overall system design.

US CAN EU AU/NZ Japan

CAN ICES-3 (B) CE VCI

United States

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- 1. This device may not cause harmful interference
- 2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Caution: Any changes or modifications to the product not expressly approved by Lumentum Operations LLC could void the user's authority to operate this equipment.

Canada

ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

European Union

This product complies with the European Union's Low Voltage Directive 2014/35/EU and EMC Directive 2014/30/EU and is properly CE marked. This declaration is made by Lumentum Operations LLC who is solely responsible for the declared compliance.

Japan

この装置は、クラスB情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。

取扱説明書に従って正しい取り扱いをして下さい。

VCCI-B

Translation: This is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

Ordering Information

For more information on this or other products and their availability, please contact your local Lumentum account manager or Lumentum directly at customer.service@lumentum.com.

Description	Product Code
100 GE, 10 km reach, LR4, commercial temperature range, CFP2 optical transceiver	JC2-10LR4AA2
100 GE and OTU4, 10 km reach, LR4, commercial temperature range, CFP2 optical transceiver	JC2-10LM4AA2



North America Toll Free: 844 810 LITE (5483)

Outside North America Toll Free: 800 000 LITE (5483)

China

Toll Free: 400 120 LITE (5483)

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