Embedded Multi-Media Card

(*e*•MMC™ 5.1)

EMMC16G-TB29-PE90

EMMC32G-TB29-PE90

EMMC32G-TA29-PE90

EMMC64G-TA29-PE90

EMMC128-TA29-PE90

PRELIMINARY

v1.1

Product Features

- Packaged managed NAND flash memory with *e*•MMC™ 5.1 interface
- Backward compatible with all prior *e*•MMC™ specification revisions
- 153-ball JEDEC FBGA RoHS Compliant package
- Operating voltage range:
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V
- Operating Temperature (T_{case}) - 25C to +85C
- Storage Temperature -40C to +85C
- Compliant with e•MMC™ 5.1 JEDEC Standard Number JESD84-B51
- Factory configured with pseudo Single Level Cell (pSLC) mode for enhanced reliability and performance
- Factory configured with reliable write

e•MMC™ Specific Feature Support

- High-speed *e*•MMC™ protocol
- Variable clock frequencies of 0-200MHz
- Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with an optional hardware reset
- Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
- Bus Modes:
  - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
  - Dual data rate mode (DDR-104) : up to 104MB/s @ 52MHz
  - High speed, single data rate mode (HS-200) : up to 200MB/s @ 200MHz
  - High speed, dual data rate mode (HS-400) : up to 400MB/s @ 200MHz
- Supports alternate boot operation mode to provide a simple boot sequence method
  - Supports SLEEP/AWAKE (CMD5)
  - Host initiated explicit sleep mode for power saving
- Enhanced write protection with permanent and partial protection options
- Multiple user data partition with enhanced attribute for increased reliability
- Error free memory access
  - Cyclic Redundancy Code (CRC) for reliable command and data communication
  - Internal error correction code (ECC) for improved data storage integrity
  - Internal enhanced data management algorithm
  - Data protection for sudden power failure during program operations
- Security
  - Secure bad block erase commands
  - Enhanced write protection with permanent and partial protection options
- Power off notification for sleep
- Field firmware update (FFU)
- Production state awareness
- Device health report
- Command queuing

- Enhanced strobe
- Cache flushing report
- Cache barrier
- Background operation control & High Priority Interrupt (HPI)
- RPMB throughput improvement
- Secure write protection
- Pre EOL information
- Optimal size

Product Description

Kingston's e•MMC™ products conform to the JEDEC e•MMC™ 5.1 standard. These devices are an ideal universal storage solution for many commercial and industrial applications. In a single integrated packaged device, e•MMC™ combines triple-level cell (TLC) NAND flash memory with an onboard e•MMC™ controller, providing an industry standard interface to the host system. The integrated e•MMC™ controller directly manages NAND flash media which relieves the host processor of these tasks, including flash media error control, wear-leveling, NAND flash management and performance optimization. Future revision to the JEDEC e•MMC™ standard will always maintain backward compatibility. The industry standard interface to the host processor ensures compatibility across future NAND flash generations as well, easing product sustainment throughout the product life cycle.

Configurations

Kingston's e•MMC™ products support a variety of configurations that allow the e•MMC™ device to be tailored to your specific application needs. The most popular configurations described below are each offered under standard part numbers.

Standard TLC – By default the e•MMC™ device is configured with the NAND flash in a standard TLC mode. This configuration provides reasonable performance and reliability for many applications.

Pseudo Single Level Cell (pSLC) – The TLC NAND flash in the Kingston e•MMC™ device can be configured to further improve device endurance, data retention, reliability and performance over the standard TLC configuration. This is done by converting the NAND TLC cells to a pseudo single level cell (SLC) configuration. In this configuration, along with the performance and reliability gains, the device capacity is reduced by 2/3 of the capacity. This one-time configuration is achieved by setting the e•MMC™ enhanced attribute for the hardware partition.

Kingston e•MMC™ can be ordered preconfigured with the option of *reliable write* or *pSLC* at no additional cost. Standard TLC devices can also be one-time configured in-field by following the procedures outlined in the JEDEC e•MMC™ specification. The JEDEC e•MMC™ specification allows for many additional configurations such as up to 4 additional general purpose (GPn) hardware partitions each with the option to support pSLC and *reliable write*. Additionally, Kingston provides a content loading service that can streamline your product assembly while reducing production costs. For more information, contact your Kingston representative.

Kingston e•MMC™ devices are fully compliant with the JEDEC Standard Specification No. JESD84-B51. This datasheet provides technical specifications for Kingston's family of e•MMC™ devices. Refer to the JEDEC e•MMC™ standard for specific information related to e•MMC™ device function and operation. See: http://www.jedec.org/sites/default/files/docs/JESD84-B51.pdf

e•MMC™ Mode and Controller

TLC mode using PS8229 - Leading edge 3D NAND flash technology in TLC mode rated to 3,000 endurance cycles.
- Strong data protection with LDPC Error control
- Improved data integrity with end-to-end data protection.

pSLC mode using PS8229 - Leading edge 3D NAND flash technology in pSLC mode.
- Strong data protection with LDPC Error control
- Improved data integrity with end-to-end data protection.

Part Numbering

Figure 1 – Part Number Format

EMMC	16G	-	xxxx	-	PZ90
A	B		C		D

Part Number Fields

A: Product Family : **EMMC**

B: Device Capacity : Available capacities of 16GB – 128GB

C: Hardware Revision and Configuration

D: Device Firmware Revision and Configuration

Table 1 - Device Summary

Product Part Number	NAND Density	Package	Operating voltage
EMMC16G-TB29-PE90	16GB	FBGA153	V_{CC}=3.3V, V_{CCQ}=1.8V/3.3V
EMMC32G-TB29-PE90	32GB	FBGA153	V_{CC}=3.3V, V_{CCQ}=1.8V/3.3V
EMMC32G-TA29-PE90	32GB	FBGA153	V_{CC}=3.3V, V_{CCQ}=1.8V/3.3V
EMMC64G-TA29-PE90	64GB	FBGA153	V_{CC}=3.3V, V_{CCQ}=1.8V/3.3V
EMMC128-TA29-PE90	128GB	FBGA153	V_{CC}=3.3V, V_{CCQ}=1.8V/3.3V

Device Performance

Table 2 below provides sequential read and write speeds for all capacities. Performance numbers can vary under different operating conditions. Values are given at HS400 bus mode. Contact your Kingston Representative for performance numbers using other bus modes.

Table 2 - Sequential Read / Write Performance

Product	Transfer Rate (MB/s)	
	Sequential Read	Sequential Write
EMMC16G-TB29-PE90	-	-
EMMC32G-TB29-PE90	-	-
EMMC32G-TA29-PE90	-	-
EMMC64G-TA29-PE90	-	-
EMMC128-TA29-PE90	-	-

Power Consumption

Device current consumption for various device configurations is defined in the power class fields of the EXT_CSD register. Power consumption values are summarized in Table 3 below.

Table 3 - Device Power Consumption

Product	Read (mA)		Write (mA)		Standby (mA)
	VCCQ = 1.8V	VCC=3.3V	VCCQ = 1.8V	VCC = 3.3V	
EMMC16G-TB29-PE90	-	-	-	-	-
EMMC32G-TB29-PE90	-	-	-	-	-
EMMC32G-TA29-PE90	-	-	-	-	-
EMMC64G-TA29-PE90	-	-	-	-	-
EMMC128-TA29-PE90	-	-	-	-	-

Note: Measurement operating conditions were conducted at HS400 bus mode, VCC = 3.3V±5%, VCCQ = 1.8V±5%. Standby current measured at 8-bit bus, VCC = 3.3V±5%, with clock idle.

Device and Partition Capacity

The device NAND flash capacity is divided across two boot partitions (2048 KB each), a Replay Protected Memory Block (RPMB) partition (512 KB), and the main user storage area. Four additional general purpose storage partitions can be created from the user partition. These partitions can be factory preconfigured or configured in-field by following the procedure outlined in section 6.2 of the JEDEC e•MMC™ specification JESD84-B51. A small portion of the NAND storage capacity is used for the storage of the onboard controller firmware and mapping tables. Additionally, several NAND blocks are held in reserve to boost performance and extend the life of the e•MMC™ device. Table 4 identifies the specific capacity of each partition. This information is reported in the device EXT_CSD register. The contents of this register are also listed in the Appendix.

Table 4 - Partition Capacity

Part Number	Partition			
	User	Boot 1	Boot 2	RPMB
EMMC16G-TB29-PE90	-	-	-	-
EMMC32G-TB29-PE90	-	-	-	-
EMMC32G-TA29-PE90	-	-	-	-
EMMC64G-TA29-PE90	-	-	-	-
EMMC128-TA29-PE90	-	-	-	-

Table 5 - e•MMC™ Operating Voltage

Parameter	Symbol	Min	Nom	Max	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.3	3.6	V
Supply voltage (I/O)	V_{CCQ} (1)	2.7	3.3	3.6	V
		1.7	1.8	1.95	V
Supply power-up for 3.3V	t_{PRUH}			35	ms
Supply power-up for 1.8V	t_{PRUL}			25	ms
Note 1：V_{CCQ} (I/O) 3.3 volt range is not supported while operating in HS200 & HS400 modes					

e•MMC™ Bus Modes

Kingston e•MMC™ devices support all bus modes defined in the JEDEC e•MMC™ 5.1 specification. These modes are summarized in Table 6 below.

Table 6 - e•MMC™ Bus Modes

Mode	Data Rate	IO Voltage	Bus Width	CLK Frequency	Maximum Data Bus Throughput
Legacy MMC	Single	3.3V / 1.8V	1, 4, 8	0 – 26 MHz	26 MB/s
High Speed SDR	Single	3.3V / 1.8V	4, 8	0 – 52 MHz	52 MB/s
High Speed DDR	Dual	3.3V / 1.8V	4, 8	0 – 52 MHz	104 MB/s
HS200	Single	1.8V	4, 8	0 – 200 MHz	200 MB/s
HS400	Dual	1.8V	8	0 – 200 MHz	400 MB/s

Signal Description

Table 7 - e•MMC™ Signals

Name	Type	Description
CLK	I	Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
DAT[7:0]	I/O/PP	Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. These bidirectional signals are driven by either the e•MMC™ device or the host controller. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e•MMC™ host controller. The e•MMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7.
CMD	I/O/PP/OD	Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e•MMC™ host controller to the e•MMC™ device and responses are sent from the device to the host.
DS	O	This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status and CMD Response are latched on the positive edge only, and don't care on the negative edge.
RST_n	I	Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
RFU	-	Reserved for future use: These pins are not internally connected. Leave floating
NC	-	Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design. See Kingston's Design Guidelines for further details.
VSF	-	Vendor Specific Function: These pins are not internally connected
Vddi	-	Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor. See Kingston's Design Guidelines for further details.
Vcc	S	Supply voltage for core
Vccq	S	Supply voltage for I/O

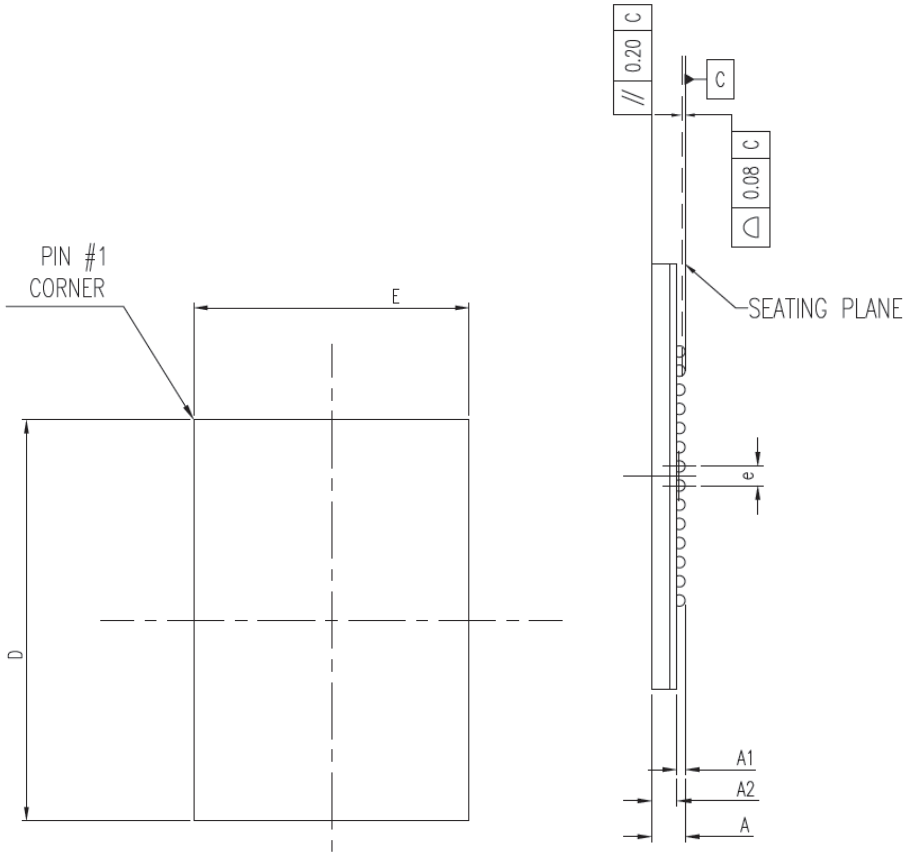
Vss	S	Supply ground for core
Vssq	S	Supply ground for I/O
Note: I=Input; O=Ouput; PP=Push-Pull; OD=Open_Drain; NC=Not Connected(or logical high); S=Power Supply		

Design Guidelines

Design guidelines are outlined in a separate document. Contact your Kingston Representative for more information.

Package Dimensions

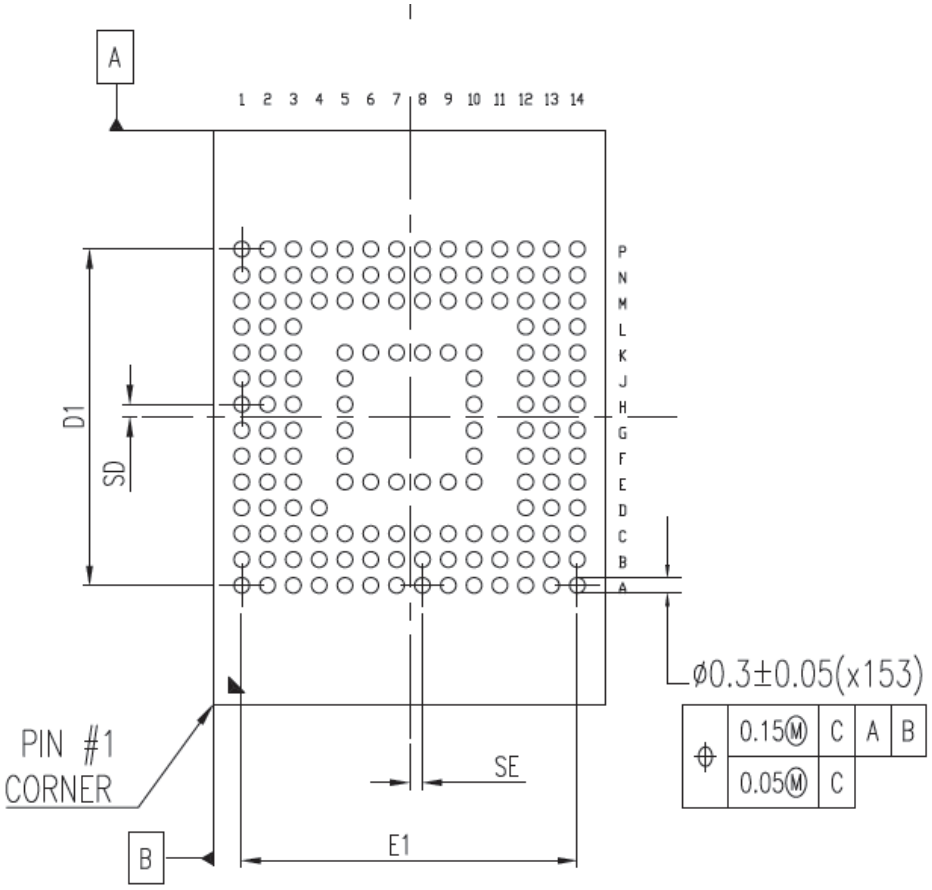
Figure 2 – Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	0.15	---	---	0.006	---	---
A2	---	---	0.57	---	---	0.022
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-276(REF.)/MM					
aaa	0.15					
bbb	0.20					
ddd	0.08					
eee	0.15					
fff	0.05					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
153L	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.

Figure 3 – Ball Pattern Dimensions



N	SE (MM)	SD (MM)	E1(MM)	D1(MM)	JEDEC(REF)
153L	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

Ball Assignment (153 ball)

Table 8 – Ball Assignment, Top View (HS400)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	Vss	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	Vddi	NC	Vssq	NC	Vccq	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	Vcc	Vss	VSF	VSF	VSF		NC	NC	NC	E
F	NC	NC	NC		Vcc					VSF		NC	NC	NC	F
G	NC	NC	RFU		Vss					VSF		NC	NC	NC	G
H	NC	NC	NC		DS					Vss		NC	NC	NC	H
J	NC	NC	NC		Vss					Vcc		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	Vss	Vcc	VSF		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	Vccq	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	Vssq	NC	Vccq	Vssq	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	Vccq	Vssq	Vccq	Vssq	RFU	NC	NC	RFU	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Note: VSF, RFU and NC balls are not electrically connected. RFU balls may be defined with functionality by the Joint Electron Device Engineering Council (JEDEC) in future revisions of the *e*•MMC™ standard. Please refer to Kingston's design guidelines for more info.

Device Marking

Figure 4 - EMMC Package Marking

Kingston Logo
240xxxx-xxx.xxxx：Internal control number
YYWW：Date code (YY– Last 2 digits of year, WW- Work week)
PPPPPPPP： Internal control number
xxxxxxx-xxxx Sales P/N
2xxxxxx : Internal control number
Country：TAIWAN

Card Identification Register (CID)

The Card Identification (CID) register is a 128-bit register that contains device identification information used during the *e*•MMC™ protocol device identification phase. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in *e*•MMC™. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

Extended Card Specific Data Register [EXT_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No.JESD84-B51.