PRELIMINARY DATA SHEET

4G bits DDR4 SDRAM

D5128ACPCPGPH-U (512M words x 8 bits)
D2516ACPCXGPH-U (256M words x 16 bits)

•Specifications

•Density: 4G bits
•Organization
- 32M words × 8 bits × 16 banks
- 32M words × 16 bits × 8 banks

•Package
- 78-ball FBGA
- 96-ball FBGA
- Lead-free

•Power supply (JEDEC standard 1.2V)
- VDD = 1.2V ± 5%
- VPP = 2.375V to 2.75V

•Data rate
- 2400Mbps/2133Mbps/1866Mbps/1600Mbps

•16 or 8 internal banks
- 16 banks (4 banks × 4 bank groups) for ×4/×8 product
- 8 banks (4 banks × 2 bank groups) for ×16 product

•Interface: Pseudo Open Drain (POD)
•Burst Length (BL): 8 and 4 with Burst Chop (BC)
•CAS Latency (CL): 9, 11, 12, 13, 14, 15, 16, 18
•CAS Write Latency (CWL): 9, 10, 11, 12, 14, 16
•Precharge: auto precharge option for each burst access
•Refresh: auto-refresh, self-refresh
•Refresh cycles
Average refresh period
7.8µs at 0°C ≤ TC ≤ +85°C
3.9µs at +85°C < TC ≤ +95°C
•Operating case temperature range
TC = 0°C to +95°C

•Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK_t and CK_c)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Write Cycle Redundancy Code (CRC) is supported.
- Data Bus Inversion (DBI) is supported (x16 only).
- Programmable preamble is supported both of 1tCK and 2tCK mode
- Command Address (CA) Parity (command/address) mode is supported.
- Internal Vref DQ level generation is available.
- Per DRAM Addressability (PDA).
- Fine granularity refresh
2x, 4x mode for smaller tRFC

•Maximum power saving mode for the lowest power consumption with no internal refresh activity (×4/×8 products only)

- Programmable Partial Array Self-Refresh (PASR)
- RESET_n pin for power-up sequence and reset function

Revision History

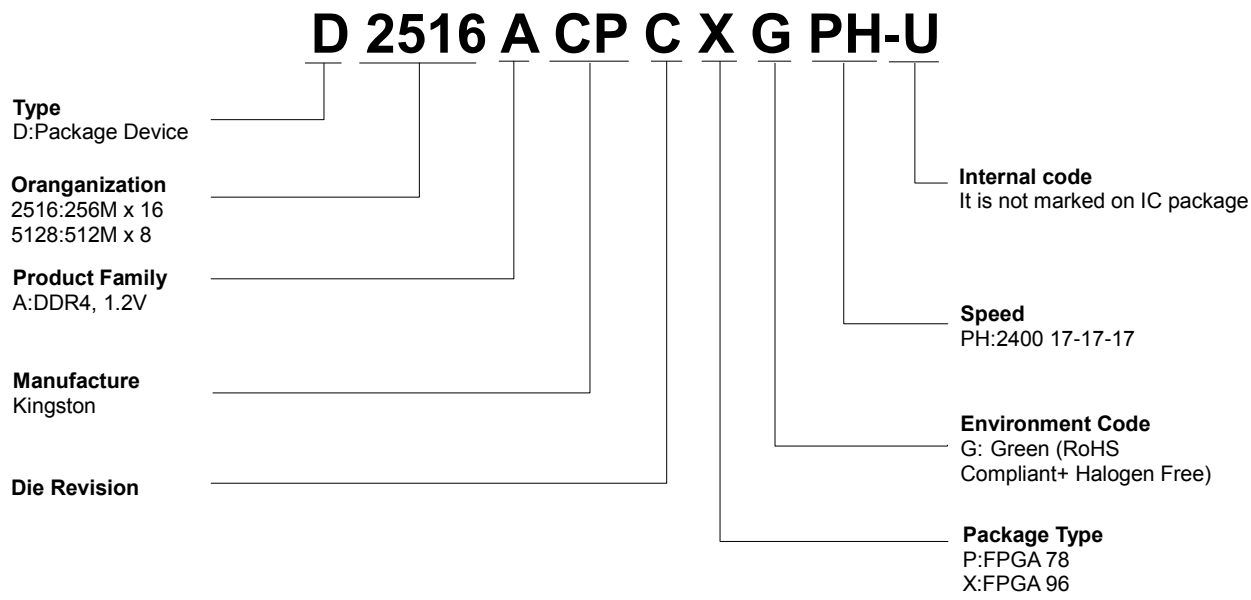
Revision No.	History	Release date	Remark
1.0	Initial release	Oct 2018	
1.1	Second release	Oct 2018	
1.2	Add IDD and IPP values	Jan 2019	
1.3	change 256x16 die revision A to C	Feb 2019	

**Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by without notice. All information discussed herein is provided on an "as is" basis, without warranties of any kind.*

Ordering Information

Part Number	Die revision	Organization (words x bits)	Internal Banks	JEDEC speed bin (CL-tRCD-tRP)	Pakage
D5128ACPCPGPH-U	C	512 x 8	16	DDR4-2400 (17-17-17)	78-ball FBGA
D2516ACPCXGPH-U	C	256M x 16	8	DDR4-2400 (17-17-17)	96-ball FBGA

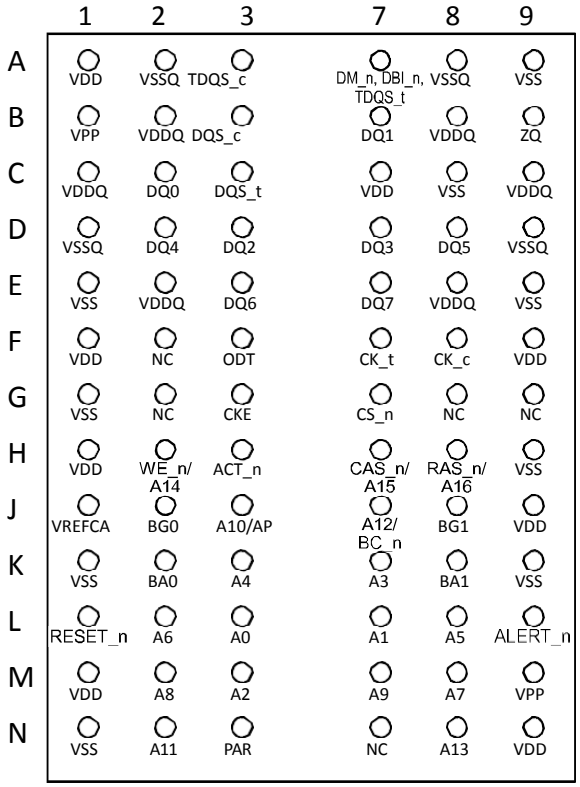
Part Number



Pin Configurations

Pin Configurations (x8 configuration)

78-ball FBGA



Pin name	Function
A0 to A14[*2]	Address inputs A10(AP) : Auto precharge A12(/BC_n) : Burst chop
BA0 to BA1[*2]	Bank select
BG0, BG1[*2]	Bank group input
DQ0 to DQ7	Data input/output
DQS_t, /DQS_c	Differential data strobe
/CS_n[*2]	Chip select
RAS_n/A16[*2] CAS_n/A15[*2] WE_n/A14[*2]	Command input
ACT_n[*2]	Activation command input
CKE[*2]	Clock enable
CK_t, CK_c	Differential clock input
DM_n	Write data mask
DBI_n	Data bus inversion

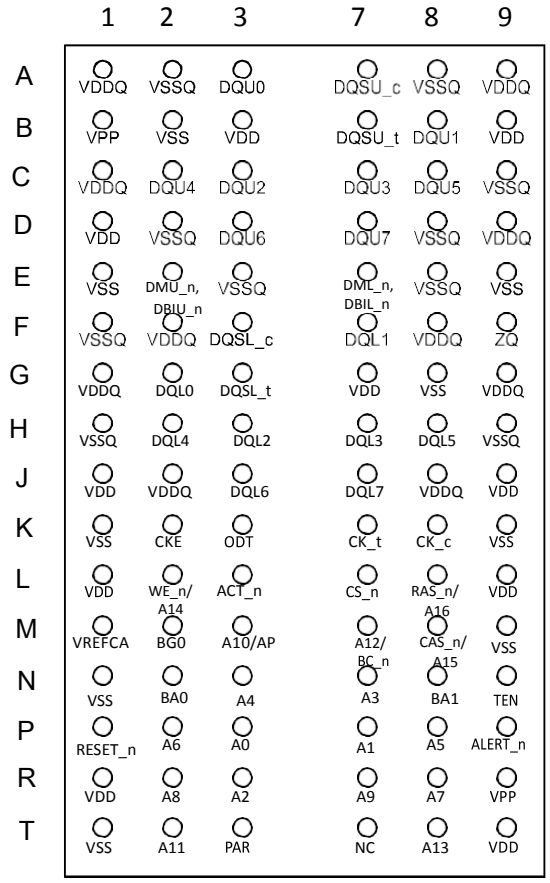
Pin name	Function
ODT[*2]	ODT control
RESET_n[*2]	Active low asynchronous reset
PAR	Command and address parity
ALERT_n	Alert
VDD	Supply voltage for internal circuit
VSS	Ground for internal circuit
VDDQ	Supply voltage for DQ circuit
VSSQ	Ground for DQ circuit
VREFCA	Reference voltage for CA
ZQ	Reference pin for ZQ calibration
NC[*1]	No connection

Notes : 1. Not internally connected with die.

2.Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination

Pin Configurations (x16 configuration)

96-ball FBGA



Pin name	Function
A0 to A14*2	Address inputs A10(AP) : Auto precharge A12(/BC_n) : Burst chop
BA0 to BA1*2	Bank select
BG0	Bank group input
DQU0 to DQU7 DQL0 to DQL7	Data input/output
DQS_t, /DQS_c	Differential data strobe
CS_n*2	Chip select
RAS_n/A16*2 CAS_n/A15*2 WE_n/A14*2	Command input
ACT_n*2	Activation command input
CKE*2	Clock enable
CK_t, CK_c	Differential clock input
DMU_n,DML_n	Write data mask
DBIU_n,DBIL_n	Data bus inversion

Pin name	Function
ODT*2	ODT control
RESET_n*2	Active low asynchronous reset
PAR	Command and address parity
ALERT_n	Alert
TEN	Connectivity test mode enable
VDD	Supply voltage for internal circuit
VSS	Ground for internal circuit
VDDQ	Supply voltage for DQ circuit
VSSQ	Ground for DQ circuit
VREFCA	Reference voltage for CA
ZQ	Reference pin for ZQ calibration
NC*1	No connection

Notes : 1. Not internally connected with die.

2.Input only pins (address, command, CKE, ODT and RESET_n) do not supply termination.

Input/Output Functional Description

Table 1 : Input/Output function description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high through out read and write accesses input buffers, excluding CK_t, CK_c and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/ TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n, CAS_n/A15 and WE_n/A14 will be considered as Row Address A15 and A14
RAS_n, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A15, A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBIU_n/TDQS_t (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_nis sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP,A12/ BC_n, RAS_n, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Setcommands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function onTDQS_t/ TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity withACT_n,RAS_n,CAS_n/A15,WE_n/ A14,BG0-BG1,BA0-BA1,A15-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA

Table 2 : 4Gb Addressing Table

Configuration		512 Mb x8	256 Mb x16
Bank Address	# of Bank Groups	4	2
	BG Address	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1
Row Address		A0~A14	A0~A14
Column Address		A0~A9	A0~A9
Page size		1KB	2KB

CONTENTS

1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

1.1. Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	–0.3 to +1.50	V	1, 3
Power supply voltage for output	VDDQ	–0.3 to +1.50	V	1, 3
DRAM activation power supply	VPP	–0.3 to +3.0	V	4
Input voltage	VIN	–0.3 to +1.50	V	1
Output voltage	VOUT	–0.3 to +1.50	V	1
Storage temperature	Tstg	–55 to +100	°C	1,2

Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than 0.6 × VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Operating case temperature is the case surface temperature on the center/top side of the DRAM.

1.2. Operating Temperature Condition

Table 4: Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1,2,3

Notes: 1. Operating case temperature is the case surface temperature on the center/top side of the DRAM.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply: Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)

1.3. Recommended DC Operating Conditions

Table 5: Recommended DC Operating Conditions (TC = 0°C to +95°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD	1.14	1.2	1.26	V	1, 2, 3
Supply voltage for DQ	VDDQ	1.14	1.2	1.26	V	1, 2, 3
Dram activating power	VPP	2.375	2.5	2.75	V	3
Ground	VSS	0	0	0	V	
Ground for DQ	VSSQ	0	0	0	V	

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. DC bandwidth is limited to 20MHz..

1.4. IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined.
The figure Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD2N, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6N, IDD6E, IDD6A and IDD7) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Note:IDDQ values cannot be directly used to calculate I/O power of the DDR4 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- L and 0: VIN ≤ VIL(AC) max
- H and 1: VIN ≥ VIH(AC) min
- MID-LEVEL: defined as inputs are VREFCA = VDD / 2
- Timings used for IDD, IPP and IDDQ measurement-loop patterns are provided in Table 8.
- Basic IDD, IPP and IDDQ measurement conditions are described in Table 9.

Note:The IDD, IPP and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Detailed IDD, IPP and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting.

  RON = RZQ/7 (34Ω in MR1);
  Qoff = 0B (Output buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40Ω in MR1);
  RTT_WR = RZQ/2 (120Ω in MR2);
  RTT_PARK = Disable;
  TDQS_t feature disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear-down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM_n disabled in MR5
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, L, L, L, L} ; apply BG/BA changes whendirected.
- Define /D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} : = {H, H, H, H, H}; apply BG/BA changes whendirected

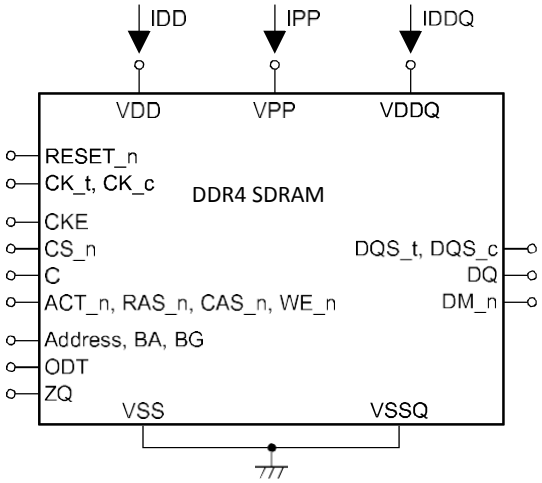


Figure 1: Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

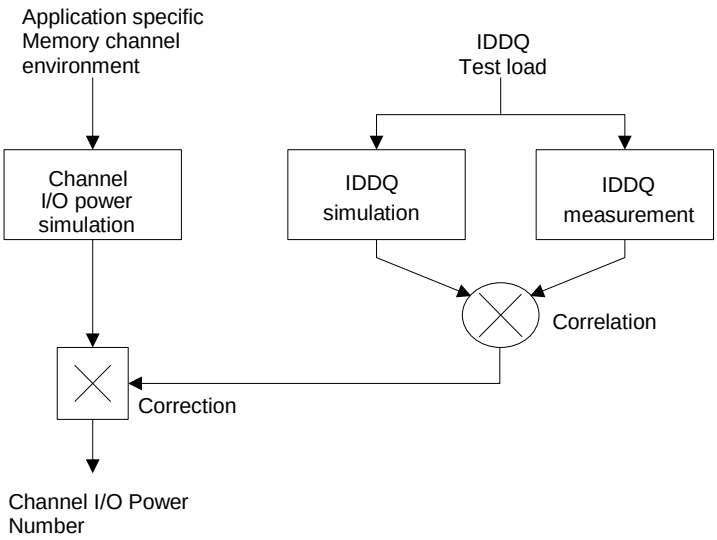


Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

1.4.1. Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 6 : Timings Used for IDD and IDDQ Measurement-Loop Patterns

Parameter		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	
tCK		1.25	1.071	0.938	0.833	ns
CL		11	13	15	17	nCK
CWL		11	12	14	16	nCK
nRCD		11	13	15	17	nCK
nRC		39	45	51	56	nCK
nRAS		28	32	36	39	nCK
nRP		11	13	15	17	nCK
nFAW	x8	20	22	23	26	nCK
	x16	28	28	32	36	nCK
nRRDS	x8	4	4	4	4	nCK
	x16	5	5	6	7	nCK
nRRDL	x8	5	5	6	6	nCK
	x16	6	6	7	8	nCK
tCCD_S		4	4	4	4	nCK
tCCD_L		5	5	6	6	nCK
tWTR_S		2	3	3	3	nCK
tWTR_L		6	7	8	9	nCK
nRFC 4Gb		208	243	278	313	nCK

1.4.2. Basic IDD and IDDQ Measurement Conditions

Table 7: Basic IDD, IPP and IDDQ Measurement Conditions

Parameter	Symbol	Description
Operating one bank active precharge current(AL=0)	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 6; BL: 8[*1]; AL: 0; CS_n: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to Table 8; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 8); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 8
Operating One Bank Active-Precharge Current (AL=CL-1)	IDD0A	AL = CL-1, Other conditions: see IDD0
Operating One Bank Active-Precharge IPP Current	IPP0	Same condition with IDD0
Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 6; BL: 8[*1], [*6]; AL: 0; CS_n: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to Table 9; DM_n: stable at 1; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 9); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 9
Operating One Bank Active-Read-Precharge Current (AL=CL-1)	IDD1A	AL=CL-1, Other conditions : see IDD1
Operating One Bank Active-Read-Precharge IPPCurrent	IPP1	Same condition with IDD1
Precharge standby current (AL=0)	IDD2N	CKE: H; External clock: on; tCK, CL: see Table 6 BL: 8[*1]; AL: 0; CS_n: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 10; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in mode registers[*2]; ODT signal: stable at 0; pattern details: see Table 10
Precharge Standby Current (AL=CL-1)	IDD2NA	Same condition with IDD2N
Precharge Standby IPP Current	IPP2N	AL = CL-1, Other conditions: see IDD2N
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8[*1]; AL: 0; CS_n: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 11; data I/O: VSSQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR[*2]; ODT signal: toggling according to Table 11; pattern details: see Table 11
Precharge standby ODT IDDQ current	IDDQ2NT (Optional)	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
Precharge Standby Current with CAL enabled	IDD2NL	Same definition like for IDD2N, CAL enabled[*3]
Precharge Standby Current with Gear Down mode enabled	IDD2NG	Same definition like for IDD2N, Gear Down mode enabled[*3], [*5]
Precharge Standby Current with DLL disabled	IDD2ND	Same definition like for IDD2N, DLL disabled[*3]
Precharge Standby Current with CA parity enabled	IDD2N_par	Same definition like for IDD2N, CA parity enabled[*3]

Parameter	Symbol	Description
Precharge Power-Down Current	IDD2P	CKE: Low; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Precharge Power-Down IPP Current	IPP2P	Same condition with IDD2P
Precharge Quiet Standby Current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: stable at 0; data I/O: VDDQ; DM_n: stable at 1;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to Table 10; data I/O: VDDQ; DM_n:stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 10
Active Standby Current (AL=CL-1)	IDD3NA	Same condition with IDD3N
Active Standby IPP Current	IPP3N	AL = CL-1, Other conditions: see IDD3N
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; data I/O: VDDQ;; DM_n:stable at 1; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active Power-Down IPP Current	IPP3P	Same condition with IDD3P
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1, *6; AL: 0; CS_n: H between RD; Command, address, Bank group address, bank address Inputs: partially toggling according to Table 13; data I/O: seamless read data burst with different data between one burst and the next one according to Table 13; DM_n: stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 13); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 13
Operating Burst Read Current (AL=CL-1)	IDD4RA	AL = CL-1, Other conditions: see IDD4R
Operating Burst Read Current with Read DBI	IDD4RB	Read DBI enabled*3, Other conditions: see IDD4R
Operating Burst Read IPP Current	IPP4R	Same condition with IDD4R
Operating Burst Read IDDQ Current	IDDQ4R (Optional)	Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
Operating Burst Read IDDQ Current with Read DBI	IDDQ4RB (Optional)	Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current

Parameter	Symbol	Description
Operating Burst Write Current	IDD4W	CKE: H; External clock: on; tCK, CL: see Table 6; BL: 8*1; AL: 0; CS_n: H between WR; command, address, bank group address, bank address inputs: partially toggling according to Table 13; data I/O: seamless write data burst with different data between one burst and the next one according to Table 13;DM_n: stable at 1; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,.. (see Table 13); output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details: see Table 13
Operating Burst Write Current(AL=CL-1)	IDD4WA	AL = CL-1, Other conditions: see IDD4W
Operating Burst Write Current with Write DBI	IDD4WB	Write DBI enabled*3, Other conditions: see IDD4W
Operating Burst Write Current with Write CRC	IDD4WC	Write CRC enabled*3, Other conditions: see IDD4W
Operating Burst Write Current with CA Parity	IDD4W_par	CA Parity enabled*3, Other conditions: see IDD4W
Operating Burst Write IPP Current	IPP4W	Same condition with IDD4W
Burst Refresh Current (1X REF)	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Table 6; BL: 8*1; AL: 0; CS_n: H between REF; Command, address, bank group address, bank address Inputs: partially toggling according to Table 15; data I/O: VDDQ; DM_n: stable at 1; bank activity: REF command every nRFC (Table 14); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 15
Burst Refresh IPP Current (1X REF)	IPP5B	Same condition with IDD5B
Burst Refresh Current (2X REF)	IDD5F2	tRFC=tRFC_x2, Other conditions: see IDD5B
Burst Refresh Write IPP Current (2X REF)	IPP5F2	Same condition with IDD5F2
Burst Refresh Current (4X REF)	IDD5F4	tRFC=tRFC_x4, Other conditions: see IDD5B
Burst Refresh Write IPP Current (4X REF)	IPP5F4	Same condition with IDD5F4
Self Refresh Current: Normal Temperature Range	IDD6N	TC: 0 to 85°C; LP ASR: Normal*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self Refresh IPP Current: Normal Temperature Range	IPP6N	Same condition with IDD6N
Self-Refresh Current: Extended Temperature Range	IDD6E	TC: 0 to 95OC; LP ASR: Extended*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Extended temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self Refresh IPP Current: Extended Temperature Range	IPP6E	Same condition with IDD6E

Parameter	Symbol	Description
Self-Refresh Current: Reduced Temperature Range	IDD6R	TC: 0 to 45°C; LP ASR: Reduced*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: Reduced temperature self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self Refresh IPP Current: Reduced Temperature Range	IPP6R	Same condition with IDD6R
Auto Self Refresh Current	IDD6A	TC: 0 to 95°C; LP ASR: Auto*4; CKE: L; External clock: off; CK_t and CK_c: L; CL: see Table 6; BL: 8*1; AL: 0; CS_n, command, address, bank group address, bank address, data I/O: H; DM_n: stable at 1; bank activity: auto self-refresh operation; Output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Auto Self Refresh IPP Current	IPP6A	Same condition with IDD6A
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 6; BL: 8*1 ; AL: CL-1; CS_n: H between ACT and RDA; Command, address, bank group address, bank address Inputs: partially toggling according to Table 17; data I/O: read data bursts with different data between one burst and the next one according to Table 17; DM_n: stable at 1; bank activity: two times interleaved cycling through banks (0, 1, …7) with different addressing, see Table 17; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 17
Operating Bank Interleave Read IPP Current	IPP7	Same condition with IDD7
Maximum Power Down Current	IDD8	TBD
Maximum Power Down IPP Current	IPP8	Same condition with IDD8

Notes: 1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].

2. MR: Mode Register
   Output buffer enable: set MR1 bit A12 = 0 and MR1 bits [2, 1] = [0,0]; output driver impedance control = RZQ/7
   RTT_Nom enable: set MR1 bits A[10:8] = [0,1,1]: RTT_Nom = RZQ/6
   RTT_WR enable: set MR2 bits A[11:9] = [0,0,1]: RTT_WR = RZQ/2
   RTT_PARK disable: set MR5 bits A[8:6] = [0,0,0]
3. CAL enabled:set MR4 bits A[8:6] = [0,0,1]: 1600MT/s; [0,1,0]: 1866MT/s, 2133MT/s; [0,1,1]: 2400MT/s
   Gear down mode enabled : set MR3 bit A3 = 1: 1/4 Rate
   DLL disabled: set MR1 bit A0 = 0
   CA parity enabled: set MR5 bits A[2:0] = [0,0,1]: 1600MT/s,1866MT/s, 2133MT/s [0,1,0]: 2400MT/s
   Read DBI enabled: set MR5 bit A12 = 1
   Write DBI enabled: set :MR5 bit A11 = 1
4. Low Power Array Self-Refresh (LP ASR) set MR2 bits A[7:6] = [0,0]: Normal; [0,1]: Reduced temperature range; [1,0]: Extended temperature range; [1,1]: Auto self-refresh

Table 8: IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
				repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			.	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x8 only
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	15*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes: 1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 9: IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	D#`, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	**D0=FF, D1=00 D2=00, D3=FF D4=00,**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1instead																
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2instead																
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		8	7*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		9	9*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 0instead																For x8 only
		10	10*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1instead																
		11	11*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		12	12*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3instead																
		13	13*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 1instead																
		14	14*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		15	15*nRC	repeat Sub-Loop 1, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		16	16*nRC	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0instead																

Notes: 1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

Table 10: IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2N_par, IPP2, IDD3N, IDD3NA, and IDD3P Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	0
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 1 instead															
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 3 instead															
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead															
		5	20-23	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 2 instead															
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead															
		7	28-31	repeat Sub-Loop 0, use BG[1:0][2] = 1, BA[1:0] = 0 instead															
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead															
		9	36-39	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 1 instead															
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead															
		11	44-47	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 3 instead															
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead															
		13	52-55	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 2 instead															
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead															
		15	60-63	repeat Sub-Loop 0, use BG[1:0][2] = 3, BA[1:0] = 0 instead															

Notes: 1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 11: IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 1 instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 2 instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 0 instead																For x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes: 1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 12: IDD4R, IDD4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes: 1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command

Table 13: IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00,D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	12-15	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	16-19	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	20-23	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	24-27	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	28-31	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	32-35	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x8 only
		9	36-39	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	40-43	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	44-47	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	48-51	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	52-55	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	56-59	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	60-63	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes: 1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command

Table 14: IDD4WC Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	1	0	1	1	0	0	0	7	F	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	3[2]	3	0	0	0	7	F	0	-
		2	10-14	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 2 instead															
		3	15-19	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
		4	20-24	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
		5	25-29	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
		6	30-34	repeat Sub-Loop 0, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
		7	35-39	repeat Sub-Loop 1, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
		8	40-44	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x8 only
		9	45-49	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
		10	50-54	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
		11	55-59	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
		12	60-64	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
		13	65-69	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
		14	70-74	repeat Sub-Loop 0, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
		15	75-79	repeat Sub-Loop 1, use BG[1:0][2] = 3, BA[1:0] = 0 instead																

Notes: 1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Write Command

Table 15: IDD5B Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	REF	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	-
			3	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4	D#, D#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			5-8	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 1 instead																
			9-12	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 2 instead																
			13-16	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 3 instead																
			17-20	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 1 instead																
			21-24	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 2 instead																
			25-28	repeat pattern 1...4, use BG[1:0][2] = 0, BA[1:0] = 3 instead																
			29-32	repeat pattern 1...4, use BG[1:0][2] = 1, BA[1:0] = 0 instead																
			33-36	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 0 instead																For x8 only
			37-40	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 1 instead																
			41-44	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 2 instead																
			45-48	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 3 instead																
			49-52	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 1 instead																
			53-56	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 2 instead																
			57-60	repeat pattern 1...4, use BG[1:0][2] = 2, BA[1:0] = 3 instead																
			61-64	repeat pattern 1...4, use BG[1:0][2] = 3, BA[1:0] = 0 instead																
		2	65 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

Notes: 1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. DQ signals are VDDQ

Table 16: IDD7 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	1	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	D#	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0]^2 = 0, BA[1:0] = 2 instead																
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 1, BA[1:0] = 3 instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use BG[1:0]^2 = 0, BA[1:0] = 1 instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 1, BA[1:0] = 2 instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]^2 = 0, BA[1:0] = 3 instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 1, BA[1:0] = 0 instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 0 instead																For x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 3, BA[1:0] = 1 instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 2 instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 3, BA[1:0] = 3 instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 1 instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 3, BA[1:0] = 2 instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]^2 = 2, BA[1:0] = 3 instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]^2 = 3, BA[1:0] = 0 instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

Notes: 1. DQS_t, DQS_c are VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

2. Electrical Specifications

2.1 IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

Table 17: IDD and IDDQ Specification

Parameter	Symbol	Data rate (Mbps)	x8(max)	X16(max)	unit	Notes
Operating current (ACT-PRE)	IDD0	2133	75	81	mA	
		2400	79	86		
	IDD0A	2133	75	82	mA	
		2400	80	87		
Operating current (ACT-RD-PRE)	IDD1	2133	78	123	mA	
		2400	93	128		
	IDD1A	2133	91	117	mA	
		2400	96	122		
Precharge standby current	IDD2N	2133	62	62	mA	
		2400	67	67		
	IDD2NA	2133	63	63	mA	
		2400	68	68		
Precharge standby ODT current	IDD2NT	2133	75	81	mA	
		2400	80	86		
Precharge Standby Current with CAL enabled	IDD2NL	2133	54	54	mA	
		2400	59	59		
Precharge Standby Current with Gear Down mode enabled	IDD2NG	2133	60	60	mA	
		2400	65	65		
Precharge Standby Current with DLL disabled	IDD2ND	2133	45	45	mA	
		2400	49	49		
Precharge Standby Current with CA parity enabled	IDD2N_par	2133	77	77	mA	
		2400	82	82		
Precharge Power-Down Current	IDD2P	2133	3	3	mA	
		2400	3	3		
Precharge quiet standby current	IDD2Q	2133	63	64	mA	
		2400	66	67		
Active standby current	IDD3N	2133	75	75	mA	
		2400	78	78		
Active Standby Current (AL=CL-1)	IDD3NA	2133	74	74	mA	
		2400	79	79		
Active power-down current	IDD3P	2133	62	62	mA	
		2400	64	64		
Operating current (Burst read operating)	IDD4R	2133	131	174	mA	
		2400	144	188		
Operating Burst Read Current (AL=CL-1)	IDD4RA	2133	133	178	mA	
		2400	148	197		
Operating Burst Read Current with Read DBI	IDD4RB	2133	131	176	mA	
		2400	144	190		
Operating current (Burst write operating)	IDD4W	2133	141	191	mA	
		2400	157	211		
Operating Burst Write Current(AL=CL-1)	IDD4WA	2133	148	198	mA	
		2400	164	227		
Operating Burst Write Current with Write DBI	IDD4WB	2133	145	189	mA	
		2400	150	199		
Operating Burst Write Current with Write CRC	IDD4WC	2133	142	189	mA	
		2400	147	194		
Operating Burst Write Current with CA Parity	IDD4W_par	2133	163	210	mA	
		2400	168	215		

Parameter	Symbol	Data rate (Mbps)	x8(max)	X16(max)	unit	Notes
Burst refresh current	IDD5B	2133	170	170	mA	
		2400	170	170		
Burst Refresh Current (2X REF)	IDD5F2	2133	179	179	mA	
		2400	179	179		
Burst Refresh Current (4X REF)	IDD5F4	2133	147	147	mA	
		2400	147	147		
All bank interleave read current	IDD7	2133	169	210	mA	
		2400	186	234		
RESET low current	IDD8	2133	30	30	mA	
		2400	30	30		

Table 18: IPP Specification

Symbol	2133		2400		Unit
	x8	x16	x8	x16	
I_{PP0}	4	8	4	8	mA
I_{PP1}	4	8	4	8	mA
I_{PP2N}	3	6	3	6	mA
I_{PP2P}	3	6	3	6	mA
I_{PP3N}	3	6	3	6	mA
I_{PP3P}	3	6	3	6	mA
I_{PP4R}	3	6	3	6	mA
I_{PP4W}	3	6	3	6	mA
I_{PP5B}	22	24	22	24	mA
I_{PP5F2}	23	25	23	25	mA
I_{PP5F4}	17	18	17	18	mA
I_{PP7}	22	33	22	33	mA
I_{PP8}	2	2	2	2	mA

Table 19: IDD6 Specification

Parameter	Symbol	Temperature Range	max	unit	Notes
Self Refresh Current: Normal Temperature Range	IDD6N	0-85°C	6	mA	1
Self-Refresh Current: Extended Temperature Range	IDD6E	0-95°C	8	mA	2
Self-Refresh Current: Reduced Temperature Range	IDD6R	0-45°C	4	mA	3
Auto Self Refresh Current	IDD6A	0-85°C	6	mA	4

Notes: 1. Applicable for MR2 settings A6 = 0 and A7 = 0

2. Applicable for MR2 settings A6 = 0 and A7 =1 . IDD6E is only specified for devices which support the extended temperature range feature C[2:0] are used only for 3DS device
3. Applicable for MR2 settings A6 = 1 and A7 = 0. IDD6R is only specified for devices which support the reduced temperature range feature
4. Applicable for MR2 settings A6 = 1 and A7 = 1. IDD6A is only specified for devices which support the auto self-refresh feature

2.2 Pin Capacitance

Table 20: Silicon pad I/O Capacitance

Parameter	Symbol	DDR4 1600/1866/2133		DDR4 2400		Unit	NOTE
		min	max	min	max		
Input/output capacitance	C_{IO}	0.55	1.4	0.55	1.15	pF	1,2,3
Input/output capacitance delta	C_{DIO}	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
Input/output capacitance delta DQS_t and DQS_c	C_{DDQS}	-	0.05	-	0.05	pF	1,2,3,5
Input capacitance, CK_t and CK_c	C_{CK}	0.2	0.8	0.2	0.7	pF	1,3
Input capacitance delta CK_t and CK_c	C_{DCK}	-	0.05	-	0.05	pF	1,3,4
Input capacitance(CTRL, ADD, CMD pins only)	C_I	0.2	0.8	0.2	0.7	pF	1,3,6
Input capacitance delta(All CTRL pins only)	C_{DI_CTRL}	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
Input capacitance delta(All ADD/CMD pins only)	$C_{DI\_ADD\_CMD}$	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
Input/output capacitance of ALERT	C_{ALERT}	0.5	1.5	0.5	1.5	pF	1,3
Input/output capacitance of ZQ	C_{ZQ}	0.5	2.3	0.5	2.3	pF	1,3,12
Input capacitance of TEN	C_{TEN}	0.2	2.3	0.2	2.3	pF	1,3,13

Notes: 1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBDApplicable for MR2 settings A6 = 0 and A7 =1 . IDD6E is only specified for devices which support the extended temperature range feature C[2:0] are used only for 3DS device

2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_C)
6. CI applies to ODT, CS_n, CKE, A0-A15, BA0-BA1, BG0-BG1, RAS_n, CAS_n/A15, WE_n/A14, ACT_n and PAR
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A15, BA0-BA1, BG0-BG1,RAS_n, CAS_n/A15, WE_n/A14, ACT_n and PAR
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))
12. Maximum external load capacitance on ZQ pin: TBD pF
13. TEN pin is DRAM internally pulled low through a weak pull-down resistor to VSS

Table 21 : DRAM package electrical specifications(x8)

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		min	max		
Z_{IO}	Input/output Zpkg	45	85		1,2,3,4,5,11
T_{dIO}	Input/output Pkg Delay	14	42	ps	1,3,4,5,11
L_{io}	Input/Output Lpkg	-	3.3	nH	11,12
C_{io}	Input/Output Cpkg	-	0.78	pF	11,13
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85		1,2,5,10,11
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	42	ps	1,3,5,10,11
$L_{io\ DQS}$	DQS Lpkg	-	3.3	nH	11,12
$C_{io\ DQS}$	DQS Cpkg	-	0.78	pF	11,13
$DZ_{DIO\ DQS}$	Delta Zpkg DQS_t, DQS_c	-	10		1,2,5,7,10
$D_{TdDIO\ DQS}$	Delta Delay DQS_t, DQS_c	-	5	ps	1,3,5,7,10
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	50	90		1,2,5,9,10,11
$T_{dI\_\ CTRL}$	Input- CTRL pins Pkg Delay	14	42	ps	1,3,5,9,10,11
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	11,12
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	11,13
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90		1,2,5,8,10,11
$Td_{IADD\_\ CMD}$	Input- CMD ADD pins Pkg Delay	14	45	ps	1,3,5,8,10,11
$L_{i\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.6	nH	11,12
$C_{i\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.74	pF	11,13
Z_{CK}	CLK_t & CLK_c Zpkg	50	90		1,2,5,10,11
Td_{CK}	CLK_t & CLK_c Pkg Delay	14	42	ps	1,3,5,10,11
$L_{i\ CLK}$	Input CLK Lpkg	-	3.4	nH	11,12
$C_{i\ CLK}$	Input CLK Cpkg	-	0.7	pF	11,13
DZ_{DCK}	Delta Zpkg CLK_t & CLK_c	-	10		1,2,5,6,10
D_{TdCK}	Delta Delay CLK_t & CLK_c	-	5	ps	1,3,5,6,10
Z_{OZQ}	ZQ Zpkg	40	100		1,2,5,10,11
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	1,3,5,10,11
$Z_{O\ ALERT}$	ALERT Zpkg	40	100		1,2,5,10,11
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	1,3,5,10,11

Notes:
1. This parameter is not subject to production test. It is verified by design and characterization. The package parasitic(L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure TBD
2. Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where

   Zpkg(total per pin) = $\sqrt{Lpkg/Cpkg}$

3. Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where

   Tdpkg(total per pin) = $\sqrt{Lpkg * Cpkg}$
4. Z & Td IO applies to DQ, DM, TDQS_T and TDQS_C
5. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
6. Absolute value of ZCK_t-ZCK_c for impedance(Z) or absolute value of TdCK_t-TdCK_c for delay(Td)
7. Absolute value of ZIO(DQS_t)-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO(DQS_t)-TdIO(DQS_c) for delay(Td)
8. ZI & Td ADD CMD applies to A0-A13, ACT_n BA0-BA1, BG0-BG1, RAS_n, CAS_n/A15, WE_n/A14 and PAR.
9. ZI & Td CTRL applies to ODT, CS_n and CKE
10. This table applies to monolithic X4 and X8 devices
11. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown
12. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
13. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

Table 22 : DRAM package electrical specifications(x16)

Symbol	Parameter	DDR4-1600/1866/2133/2400		Unit	NOTE
		min	max		
Z_{IO}	Input/output Zpkg	45	85		1
T_{dIO}	Input/output Pkg Delay	14	45	ps	1
L_{io}	Input/Output Lpkg	-	3.4	nH	1,2
C_{io}	Input/Output Cpkg	-	0.82	pF	1,3
$Z_{IO\ DQS}$	DQS_t, DQS_c Zpkg	45	85		1
$Td_{IO\ DQS}$	DQS_t, DQS_c Pkg Delay	14	45	ps	1
$L_{io\ DQS}$	DQS Lpkg	-	3.4	nH	1,2
$C_{io\ DQS}$	DQS Cpkg	-	0.82	pF	1,3
$DZ_{DIO\ DQS}$	Delta Zpkg DQSU_t, DQSU_c	-	10		-
	Delta Zpkg DQSL_t, DQSL_c	-	10		
$D_{TdDIO\ DQS}$	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	50	90		1
$T_{dI\_\ CTRL}$	Input- CTRL pins Pkg Delay	14	42	ps	1
$L_{i\ CTRL}$	Input CTRL Lpkg	-	3.4	nH	1,2
$C_{i\ CTRL}$	Input CTRL Cpkg	-	0.7	pF	1,3
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	50	90		1
$Td_{IADD\_\ CMD}$	Input- CMD ADD pins Pkg Delay	14	52	ps	1
$L_{i\ ADD\ CMD}$	Input CMD ADD Lpkg	-	3.9	nH	1,2
$C_{i\ ADD\ CMD}$	Input CMD ADD Cpkg	-	0.86	pF	1,3
Z_{CK}	CLK_t & CLK_c Zpkg	50	90		1
Td_{CK}	CLK_t & CLK_c Pkg Delay	14	42	ps	1
$L_{i\ CLK}$	Input CLK Lpkg	-	3.4	nH	1,2
$C_{i\ CLK}$	Input CLK Cpkg	-	0.7	pF	1,3
DZ_{DCK}	Delta Zpkg CLK_t & CLK_c	-	10		-
D_{TdCK}	Delta Delay CLK_t & CLK_c	-	5	ps	-
Z_{OZQ}	ZQ Zpkg	40	100		
$Td_{O\ ZQ}$	ZQ Delay	20	90	ps	
$Z_{O\ ALERT}$	ALERT Zpkg	40	100		
$Td_{O\ ALERT}$	ALERT Delay	20	55	ps	

Notes: 1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo

2.3 Standard SpeedBins

Table 23: DDR4-1600 Speed Bins

Speed Bin				DDR4-1600K		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75[14](13.50)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75 (13.50)[5,12]	-	ns	12
PRE command period			tRP	13.75 (13.50)[5,12]	-	ns	12
ACT to PRE command period			tRAS	35	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	48.75 (48.50)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				(9),11,12		nCK	13,14
Supported CL Settings with read DBI				(11),13,14		nCK	13
Supported CWL Settings				9,11		nCK	

Table 24: DDR4-1866 Speed Bins

Speed Bin				DDR4-1866M		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92[14] (13.50)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.92 (13.50)[5,12]	-	ns	12
PRE command period			tRP	13.92 (13.50)[5,12]	-	ns	12
ACT to PRE command period			tRAS	34	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.92 (47.50)[5,12]	-	ns	12
	Normal	Read DBI					
CWL=9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11,14
				(Optional)[5,12]			
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL= 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL= 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25		1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25		1,2,3
Supported CL Settings				9,11,12,13,14		nCK	13,14
Supported CL Settings with read DBI				11,13,14 ,15,16		nCK	13
Supported CWL Settings				9,10,11,12		nCK	

Table 25: DDR4-2133 Speed Bins

Speed Bin				DDR4-2133P		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06[14] (13.50)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.06 (13.50)[5,12]	-	ns	12
PRE command period			tRP	14.06 (13.50)[5,12]	-	ns	12
ACT to PRE command period			tRAS	33	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.06 (46.50)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5 (Optional)[5,12]	1.6	ns	1,2,3,4,11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional)[5,12]	<1.5	ns	1,2,3,4,7
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional)[5,12]	<1.25	ns	1,2,3,4,7
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3
Supported CL Settings				(9),(11),12,(13),14,15,16		nCK	13,14
Supported CL Settings with read DBI				(11),(13),14,(15),16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

Table 26: DDR4-2400 Speed Bins

Speed Bin				DDR4-2400T		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16[14] (13.75)[5,12]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 3nCK	tAA(max) +3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.16 (13.75)[5,12]	-	ns	12
PRE command period			tRP	14.16 (13.75)[5,12]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.16 (45.75)[5,12]	-	ns	12
	Normal	Read DBI					
CWL =9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.938	<1.071	ns	1,2,3,4,8
				(Optional)[5,12]			
	CL = 16	CL = 19	tCK(AVG)	0.938	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.938	ns	
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.938	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

Speed Bin Table Notes

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V

- VPP = 2.5V +0.25/-0.125 V

- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Reserved for DDR4-2666 speed bin.
10. Reserved for DDR4-3200 speed bin.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameter apply from tCK(avg)min to tCH(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

2.4 Electrical Characteristics & AC Timing

2.4.1 Reference Load for AC Timing and Output Slew Rate

Figure 3 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.
It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

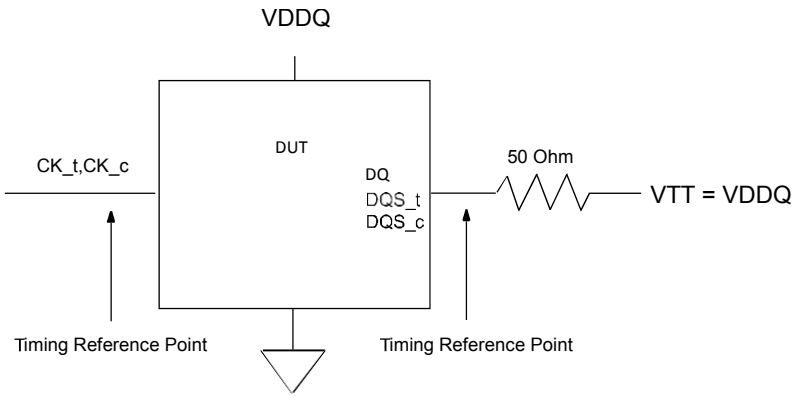


Figure 3. Reference Load for AC Timing and Output SlewRate

2.4.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

Table 27 : tREFI by device density

Parameter	Symbol		4Gb	Units
Average periodic refresh interval	tREFI	0°C ≤ TCASE ≤ 85°C	7.8	µs
		85°C < TCASE ≤ 95°C	3.9	µs

2.4.3. Timing Parameters by Speed Grade

Table 28 : Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	0.833	<0.938	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)min + tJIT(per)min _ tot	tCK(avg)max + tJIT(per)max _ tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	25
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	125		107		94		83		ps	25
Cycle to Cycle Period Jitterdetermin-istic	tJIT(cc)_dj	63		54		47		42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	180	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$t_{ERR(nper)min} = ((1 + 0.68ln(n)) * {}^{t}JIT(per)\_total\ min)$ $t_{ERR(nper)max} = ((1 + 0.68ln(n)) * {}^{t}JIT(per)\_total\ max)$								ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) /Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps	
Command and Address hold timeto CK_t, CK_c referenced to Vih(dc) /Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	
Command and AddressTiming											
CAS_n to CAS_n command delay for same bank group	tCCD_L	Max(5nCK, 6.250ns)	-	Max(5nCK, 5.355ns)	-	Max(5nCK, 5.355ns)	-	Max(5nCK, 5.000ns)	-	nCK	34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK, 5ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK, 5ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 7.5ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/ 2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 35ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 25ns)	-	Max(20nCK, 23ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 20ns)	-	Max(16nCK, 17ns)	-	Max(16nCK, 15ns)	-	Max(16nCK, 13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tW TR_S	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max (2nCK, 2.5ns)	-		1,2, 34
Delay from start of internal write transaction to internal read command for same bank group	tW TR_L	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	Max(4nCK, 7.5ns)	-		
WRITE recovery time	tW R	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tW R_CRC _DM	tW R+max (4nCK,3.75ns)	-	tW R+max (5nCK,3.75ns)	-	tW R+max (5nCK,3.75ns)	-	tW R+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write trans-action to internal read command for different bank group with both CRC and DM enabled	tW TR_S_C RC_DM	tW TR_S+max (4nCK,3.75ns)	-	tW TR_S+max (5nCK,3.75ns)	-	tW TR_S+max (5nCK,3.75ns)	-	tW TR_S+max (5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write trans-action to internal read command for same bank group with both CRC and DM enabled	tW TR_L_C RC_DM	tW TR_L+max (4nCK,3.75ns)	-	tW TR_L+max (5nCK,3.75ns)	-	tW TR_L+max (5nCK,3.75ns)	-	tW TR_L+max (5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register W rite Recov-ery Time	tW R_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	5	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew,per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	-	TBD	tCK(avg) /2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD	-	TBD	-	TBD	-	tCK(avg) /2	13,17, 18
DQS_t, DQS_c differential READ Preamble(1 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	0.9	TBD	tCK	
DQS_t, DQS_c differential READ Preamble(2 clock preamble)	tRPRE	NA	NA	NA	NA	NA	NA	1.8	TBD	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t,DQS_c differential outputlow time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-300	150	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	150	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK	-225	225	-195	195	-180	180	-175	175	ps	
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)		tCKSRX(min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD		TBD		TBD		TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-	TBD	-		
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-		
SRX to commands not requiring a locked DLL in Self RefreshABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) orPower-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)			
Valid Clock Requirement after Self Refresh Entry (SRE) orPower-Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL			
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)			

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Valid Clock Requirement after Self Refresh Entry (SRE) orPower-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) orPower-Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-		
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tW RPDEN	WL+4+(tW R/ tCK(avg))	-	WL+4+(tW R/ tCK(avg))	-	WL+4+(tW R/ tCK(avg))	-	WL+4+(tW R/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tW RAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tW RP-BC4DEN	WL+2+(tW R/ tCK(avg))	-	WL+2+(tW R/ tCK(avg))	-	WL+2+(tW R/ tCK(avg))	-	WL+2+(tW R/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tW RAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD			
ODT Timing											
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE									ns	
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_UN-KNOW N	-	PL	-	PL	-	PL	-	PL		

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	
CRC Error Reporting											
CRC error to ALERT_nlatency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulsewidth	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns	34

NOTE :

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after W L.

For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after W L.

2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TCASE.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled, tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled, tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method TBD.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2.

3. DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Table 29 : Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	x16	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V		

Table 30 : Function Matrix (By Speed. V:Supported, Blank:Not supported)

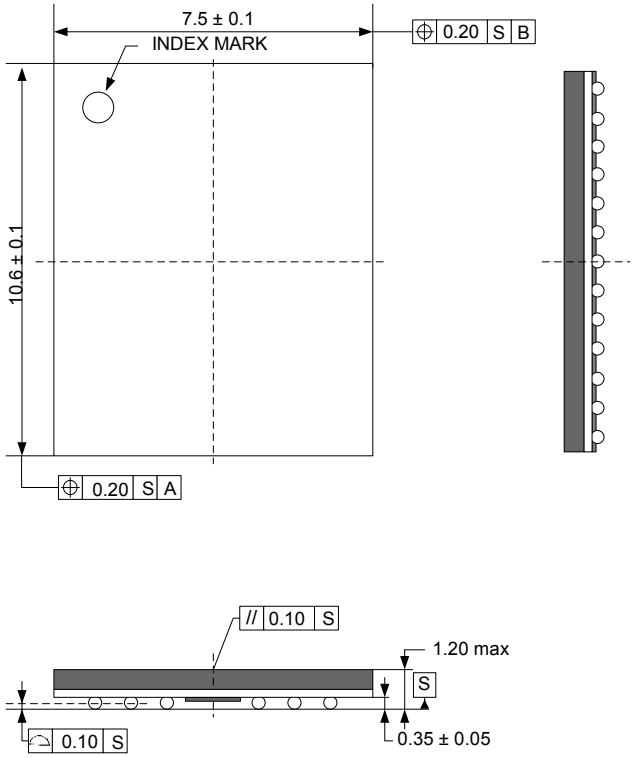
Functions	DLL Off mode	DLL On mode		NOTE
	equal or slower than 250Mbps	1600/1866/2133 Mbps	2400 Mbps	
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask	V	V	V	
Data Bus Inversion	V	V	V	
TDQS		V	V	
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability		V	V	
Mode Register Readout	V	V	V	
CAL		V	V	
WRITE CRC		V	V	
CA Parity		V	V	
Control Gear Down Mode				
Programmable Preamble (= 2tCK)			V	
Maximum Power Down Mode		V	V	
Boundary Scan Mode	V	V	V	

4. Package Drawing

4.1 78-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

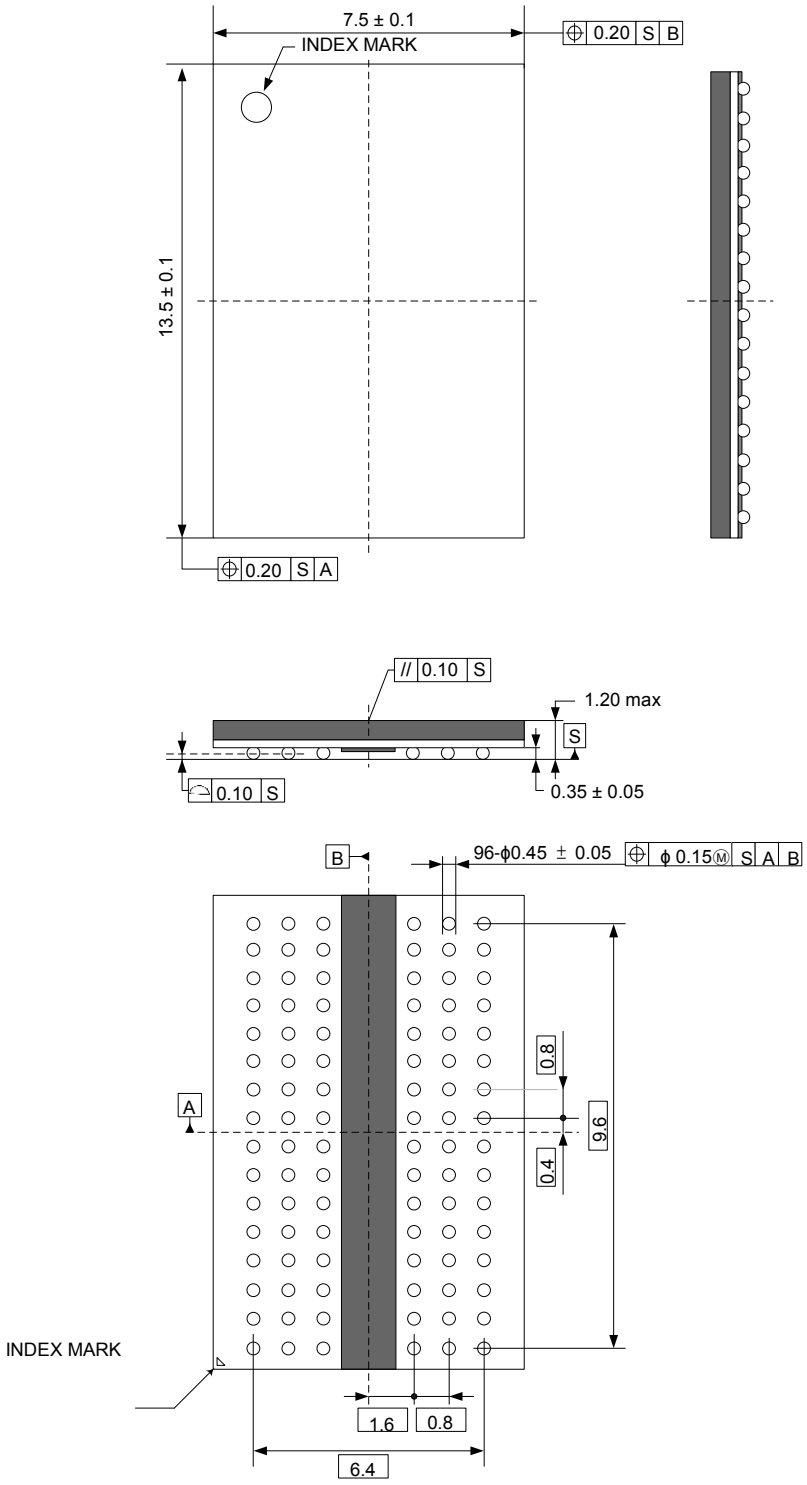
Unit: mm



4.2 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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[Usage environment]
Usage in environments with special characteristics as listed below was not considered in the design.
Accordingly, our company assumes no responsibility for loss of a customer or a third party when used in environments with the special characteristics listed below.

Example:
1) Usage in liquids, including water, oils, chemicals and organic solvents.
2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL2, H2S, NH3, SO2, and NOx.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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