CYW20736E

Bluetooth Low Energy System-in-Package Module

Doc. # 002-15223 Rev. *B

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): +1.408.943.2600
www.cypress.com

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Preface

This document provides descriptions of the interfaces, pin assignments, and specifications of CYW20736E Bluetooth Low Energy (BLE) System-in-Package (SiP) module. It is intended for designers who are responsible for adding the CYW20736E module to wireless input devices including heart-rate monitors, blood pressure monitors, proximity sensors, temperature sensors, and battery monitors.

Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 2-1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20736	CYW20736
BCM20736E	CYW20736E

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Cypress documents, go to http://www.cypress.com/glossary.

Document Conventions

The following conventions may be used in this document:

Convention	Description
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
Monospace	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

Technical Support

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

Contents

1. Introduction

1.1 Overview

The CYW20736E is a compact, highly integrated Bluetooth low energy (BLE) system-in-package (SiP) module. The CYW20736E SiP includes a 24 MHz clock and 512 Kb EEPROM, so only a minimal set of external components is needed to create a standalone BLE device.

The CYW20736E is designed to accelerate time to market. The Bluetooth stack and several application profiles are built into the module, allowing customers to focus on their core applications. To further reduce application development time, the CYW20736E includes integrated software support, with one-click installation of the complete environment and a one-click compile/build/link/load cycle. All this, coupled with an ultrasmall form factor and support for a wide voltage range, makes the CYW20736E well suited for virtually any Bluetooth Smart application.

1.1.1 Features

- ARM Cortex-M3 microcontroller unit (MCU)
- Embedded 512 Kb EEPROM
- Broadcom Serial Control (BSC), SPI, and UART interfaces
- FCC and CE compliant
- RoHS compliant, certified lead- and halogen-free
- Moisture Sensitivity Level (MSL) 3 compliant
- 6.5 mm × 6.5 mm × 1.2 mm Land Grid Array (LGA) 48-pin package

1.1.2 Application Profiles

The following profiles are supported in CYW20736E ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time
- Blood glucose monitor

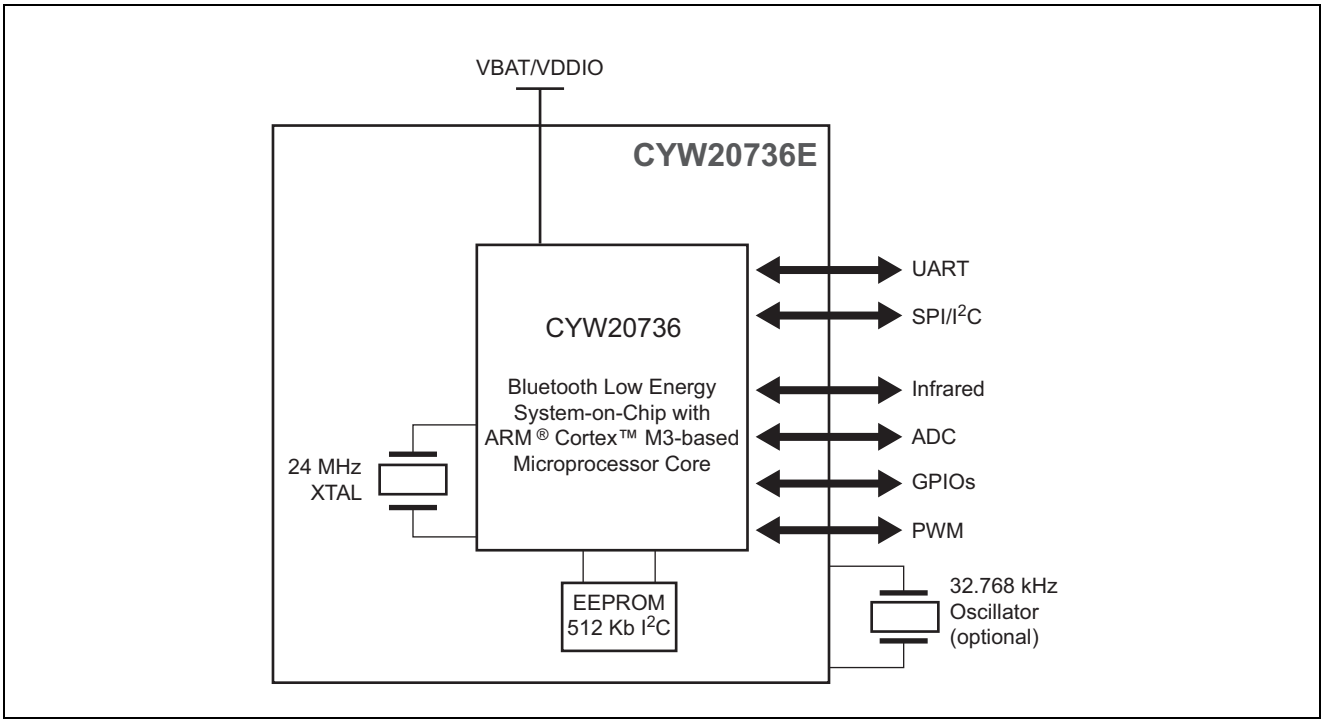
Additional profiles that can be supported in CYW20736E RAM include:

- Blood glucose monitor
- Temperature alarm
- Location
- Other custom profiles

1.1.3 Block Diagram

A block diagram of the CYW20736E BLE SiP is shown in Figure 1-1.

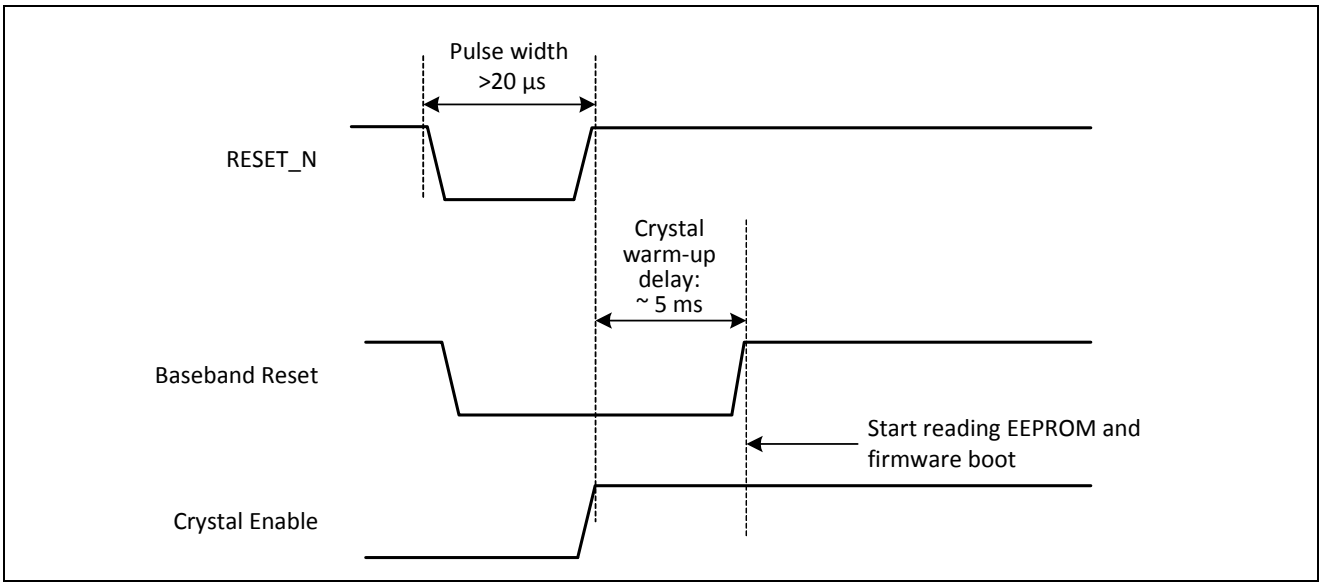
Figure 1-1. CYW20736E BLE SiP Block Diagram



1.2 External Reset

External reset timing for the CYW20736E is illustrated in Figure 1-2.

Figure 1-2. External Reset Timing



1.2.1 32.768 kHz Oscillator

The CYW20736E includes a standard Pierce oscillator. The oscillator circuit includes a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis eliminates chatter when the input is near the comparator threshold (~100 mV). The oscillator circuit can is designed for a 32 kHz or 32.768 kHz crystal oscillator, and can also be driven by an external clock input with a similar frequency. Characteristics for a 32 kHz oscillator are defined in Table 1-1.

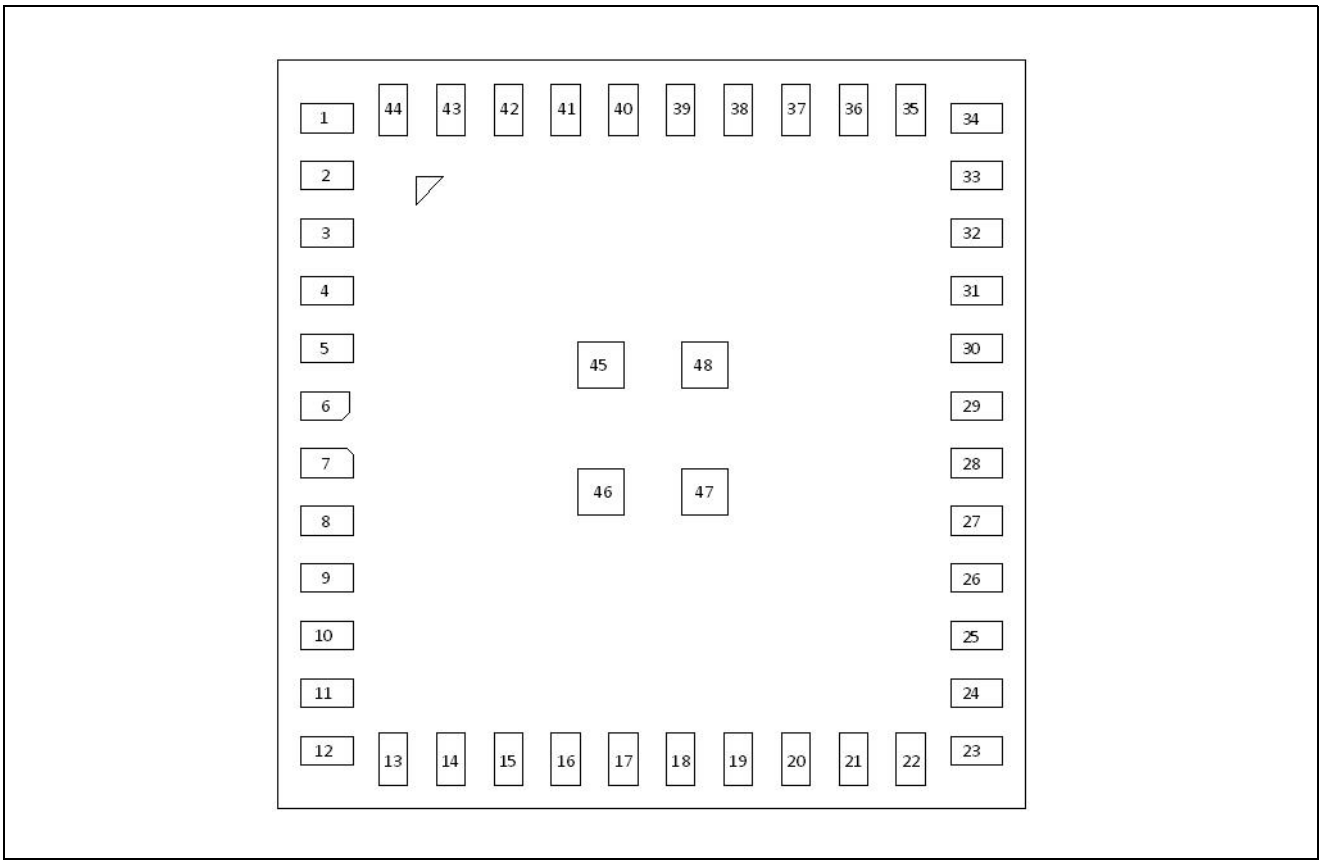
Table 1-1. 32 kHz Crystal Oscillator Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	F_{tol}	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	µs
Crystal drive level	P_{drv}	For crystal selection	0.5	–	–	µW
Crystal series resistance	R_{series}	For crystal selection	–	–	70	kΩ
Crystal shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

1.3 Pin Map and Signal Descriptions

The CYW20736E pin map is shown in Figure 1-3.

Figure 1-3. CYW20736E (TOP View)



The signal name, type, and description of each pin in the CYW20736E is listed in Table 1-2 . The symbols shown under I/O Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 1-2. Pin Descriptions

Pin	Name	I/O Type	Description
1	GPIO: P27 PWM1	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate function: MOSI (master and slave) for SPI_2
2	GND	GND	GND
3	VBAT	I	Battery supply input.
4	GND	GND	GND
5	GND	GND	GND
6	GND	GND	GND
7	GND	GND	GND
8	GND	GND	GND

Table 1-2. Pin Descriptions (Cont.)

Pin	Name	I/O Type	Description
9	GND	GND	GND
10	ANT	O	External antenna connection (must be 50Ω)
11	GND	GND	GND
12	GND	GND	GND
13	GND	GND	GND
14	GND	GND	GND
15	GND	GND	GND
16	GND	GND	GND
17	GND	GND	GND
18	UART_RX	I	UART_RX. This pin is pulled low through an internal 10 kΩ resistor.
19	UART_TX	O, PU	UART_TX
20	GND	GND	GND
21	SCL	I/O, PU	SCL I/O, PU clock signal for an external I^2C device
22	SDA	I/O, PU	SDA I/O, PU data signal for an external I^2C device
23	GND	GND	GND
24	GND	GND	GND
25	GPIO: P1	I	Default direction: Input. After POR state: Input floating. This pin is tied to the WP pin of the embedded EEPROM and requires an external 10 kΩ pull-up
26	TMC	I	Test mode control. Pull this pin high to invoke test mode; leave it floating if not used. This pin is connected to GND through an internal 10 kΩ resistor.
27	RESET_N	I/O PU	Active-low system reset with open-drain output
28	GPIO: P0	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ Peripheral UART TX (PUART_TX) ■ MOSI (master and slave) for SPI_2 ■ IR_RX ■ 60Hz_main
29	GND	GND	GND
30	GPIO: P3	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART CTS (PUART_CTS) ■ SPI_CLK (master and slave) for SPI_2
31	GPIO: P2	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART RX (PUART_RX) ■ SPI_CS (slave only) for SPI_2 ■ SPI_MOSI (master only) for SPI_2

Table 1-2. Pin Descriptions (Cont.)

Pin	Name	I/O Type	Description
32	GPIO: P4	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ Peripheral UART RX (PUART_RX) ■ MOSI (master and slave) for SPI_2. ■ IR_TX
33	GPIO: P8	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input. ■ External T/R switch control (~tx_pd)
34	GPIO: P33	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ MOSI (slave only) for SPI_2 ■ Auxiliary clock output (ACLK1) ■ Peripheral UART RX (PUART_RX)
35	GPIO: P32	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ SPI_CS (slave only) for SPI_2. ■ Auxiliary clock output (ACLK0) ■ Peripheral UART TX (PUART_TX)
36	GPIO: P25	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ MISO (master and slave) for SPI_2 ■ Peripheral UART RX (PUART_RX)
37	GPIO: P24	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ SPI_CLK (master and slave) for SPI_2 ■ Peripheral UART TX (PUART_TX)
38	GND	GND	GND
39	GPIO: P13 PWM3	I	Default Direction: Input After POR State: Input Floating Drain current: 16 mA Alternate function: A/D converter input
	GPIO: P28 PWM2	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate functions: ■ A/D converter input ■ LED1 ■ IR_TX

Table 1-2. Pin Descriptions (Cont.)

Pin	Name	I/O Type	Description
40	GPIO: P14 PWM2	I	Default direction: Input. After POR state: Input floating. Alternate function: A/D converter input
	GPIO: P38	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ MOSI (master and slave) for SPI_2 ■ IR_TX
41	GPIO: P15	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ IR_RX ■ 60 Hz_main
42	GPIO: P26 PWM0	I	Default direction: Input. After POR state: Input floating. Drain current: 16 mA Alternate function: SPI_CS (slave only) for SPI_2
43	GPIO: P12	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ XTALO32K
	XTALO32K	O	Low-power oscillator (LPO) output. Alternate functions: P12 P26
44	GPIO: P11	I	Default direction: Input. After POR state: Input floating. Alternate functions: ■ A/D converter input ■ XTALI32K
	XTALI32K	I	Low-power oscillator (LPO) input. Alternate functions: ■ P11 ■ P27
45	GND	GND	GND
46	GND	GND	GND
47	GND	GND	GND
48	GND	GND	GND

1.4 Electrical Specifications

Absolute maximum ratings are defined in Table 1-3.

Table 1-3. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply power	NA	3.63	V
Storage temperature	–40	125	°C
Voltage ripple	0	±2	%
Power supply (VBAT absolute maximum rating)	1.62	3.63	V

Power for the CYW20736E module is provided by the host through the power pins.

Table 1-4. Voltage

Symbol	Parameter	Min.	Typ.	Max.	Unit
VBAT	Battery voltage	1.62	–	3.63	V

Table 1-5. Current Consumption

Operating Mode	Condition	Nominal	Maximum	Unit
Receive	Receiver and baseband are both operating, 100%	24	28	mA
Transmit	Transmitter and baseband are both operating, 100%	24	28	mA
Sleep	Wake in < 5 ms	55	60	µA
Deep Sleep	Wake on interrupt	2.0	2.5	µA
Note: All measurements taken at 25°C				

Based on the current measurements in Table 1-5 , CYW20736E peak power values are:

- RX: 39.6 mW
- TX: 37.8 mW
- Sleep mode: 36 µW
- Deep Sleep mode: 2.4 µW

1.5 RF Specifications

CYW20736E receiver specifications are defined in Table 1-6.

Table 1-6. Receiver Specifications

Parameter	Mode and Conditions	Min.	Typ.	Max.	Unit
Frequency range	–	2402	–	2480	MHz
RX sensitivity (standard)	Packets: 200 Payload: PRBS 9 Length: 37 Bytes Dirty Transmitter: off. PER: 30.8%	–	–94	–	dBm
Maximum input	–	–10	–	–	dBm
Note: All measurements taken at 3.0V (default voltage)					

RF transmitter specifications are defined in Table 1-7.

Table 1-7. Transmitter Specifications

Parameter	Min.	Typ.	Max.	Unit
Transmitter				
Frequency range[a]	2402	–	2480	MHz
Output power adjustment range	–20	–	4	dBm
Output power	–	2	–	dBm
Output power variation	–	2.5	–	dB
LO Performance				
Initial carrier frequency tolerance	–	–	±150	kHz
Frequency Drift				
Frequency drift	–	–	±50	kHz
Drift rate	–	–	20	kHz/50 µs
Frequency Deviation				
Average deviation in payload (sequence: 00001111)	225	–	275	kHz
Average deviation in payload (sequence: 10101010)	185	–	–	kHz
Channel spacing	–	2	–	MHz

a. This parameter is taken from the Bluetooth 4.0 specification.

1.6 ADC Specifications

CYW20736E ADC specifications are defined in Table 1-8.

Table 1-8. ADC Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Number of input channels	–	–	–	9	–	-
Channel switching rate	f_{ch}	–	–	–	133.33	Kch/s
Input signal range	V_{inp}	–	0	–	3.63	V
Reference settling time	–	Charging refsel	7.5	–	–	µs
Input resistance	R_{inp}	Effective, single-ended	–	500	–	kΩ
Input capacitance	C_{inp}	–	–	–	5	pF
Conversion rate	F_c	–	5.859	–	187	kHz
Conversion time	T_c	–	5.35	–	170.7	µs
Resolution	R	–		16		Bits
Absolute voltage measurement error	–	Using on–chip ADC firmware driver	–	±2	–	%
Current	I	$I_{avdd1p2} + I_{avdd3p3}$	–	–	1	mA
Power	P	–	–	1.5	–	mW
Leakage Current	$I_{leakage}$	T = 25°C	–	–	100	nA
Power-up time	$T_{powerup}$	–	–	–	200	µs
Integral nonlinearity	I_{NL}	In the guaranteed performance range	–1	–	1	LSB[a]
Differential nonlinearity	D_{NL}	In the guaranteed performance range	–1	–	1	LSB[a]

a. LSBs are expressed at the 10-bit level.

1.7 Timing and AC Characteristics

1.7.1 SPI Timing

SPI interface timing is illustrated in Figure 1-4 and Figure 1-5 and defined in Table 1-9 .

Figure 1-4. SPI Timing—Modes 0 and 2

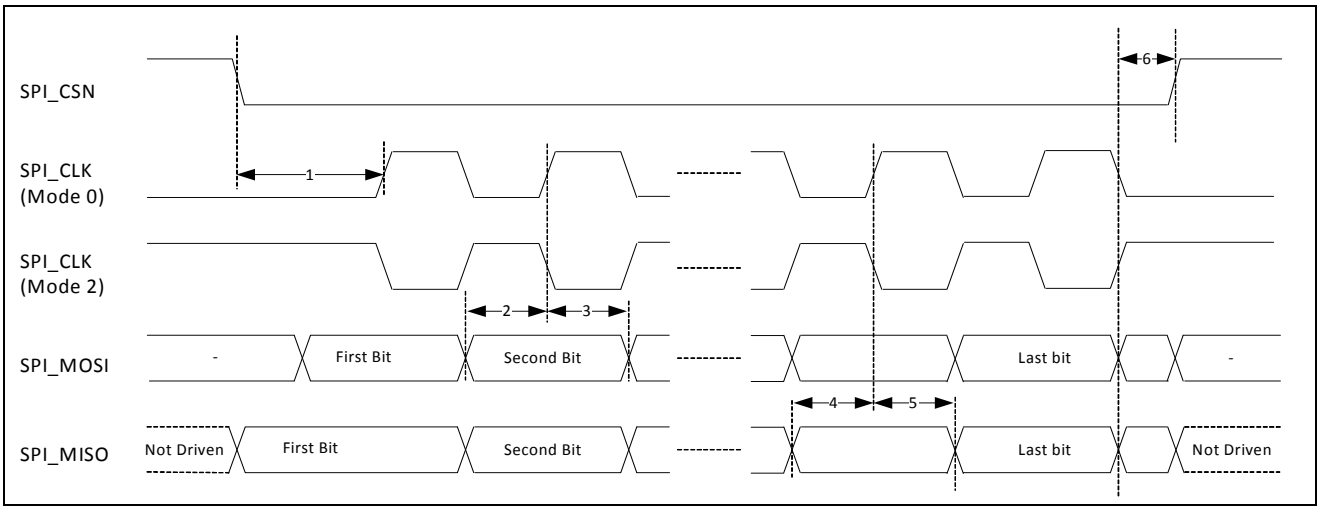


Figure 1-5. SPI Timing—Modes 1 and 3

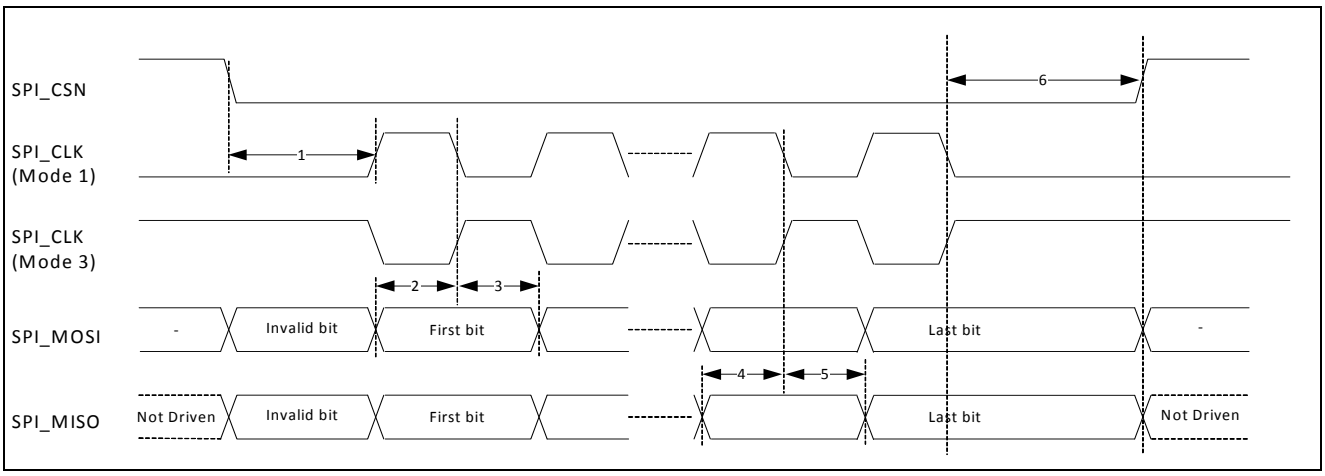


Table 1-9. SPI Interface Timing Specifications

Reference	Characteristics	Min.	Typ.	Max.
1	Time from CSN asserted to first clock edge	1 SCK	100	∞
2	Master setup time	–	1/2SCK	–
3	Master hold time	1/2SCK	-	–
4	Slave setup time	–	1/2 SCK	–
5	Slave hold time	1/2 SCK	–	–
6	Time from last clock edge to CSN deasserted	SCK	10 SCK	100

1.7.2 BSC Interface Timing

BSC interface timing is illustrated in Figure 1-6 and is defined in Table 1-10.

Figure 1-6. BSC Interface Timing

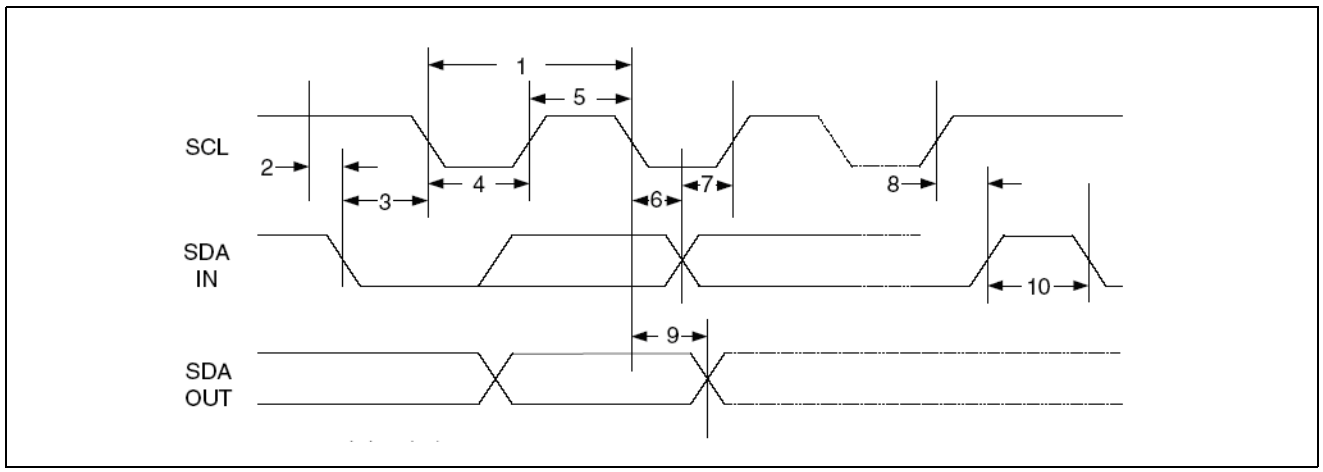


Table 1-10. BSC Interface Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Clock frequency	–	100, 400, 800, 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time	650	–	ns

1.7.3 UART Timing

UART timing is illustrated in Figure 1-7 and defined in Table 1-11.

Figure 1-7. UART Timing

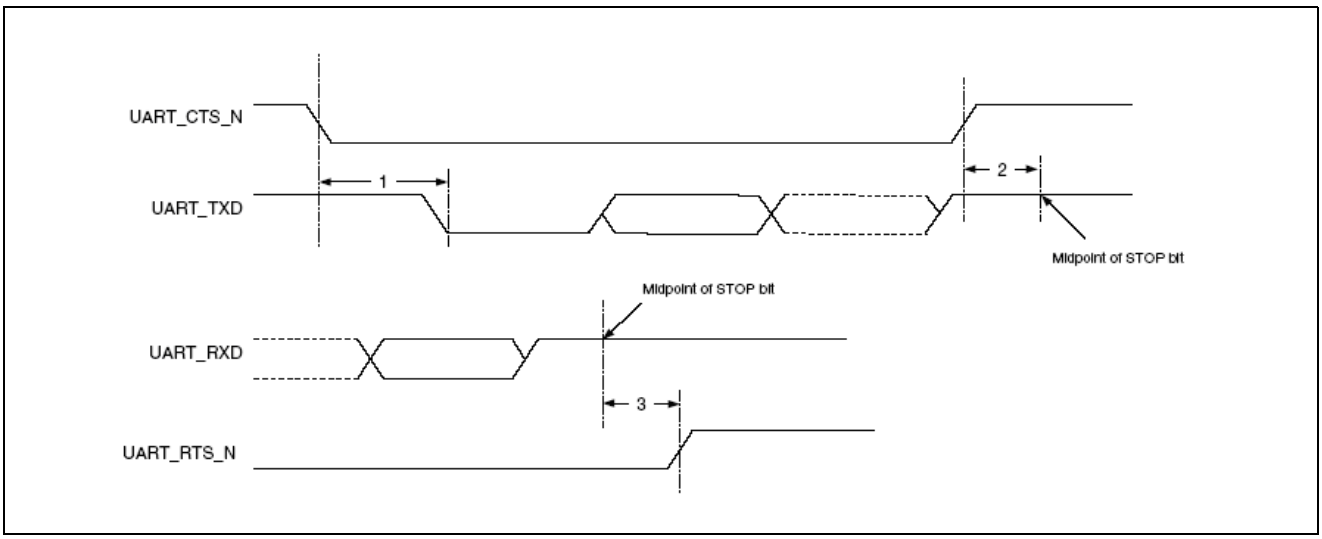


Table 1-11. UART Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baudout cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baudout cycles

1.8 PCB Design and Manufacturing Recommendations

1.8.1 Pad and Solder Mask Opening Dimensions

CYW20736E pad and solder mask opening dimensions are defined in Table 1-12.

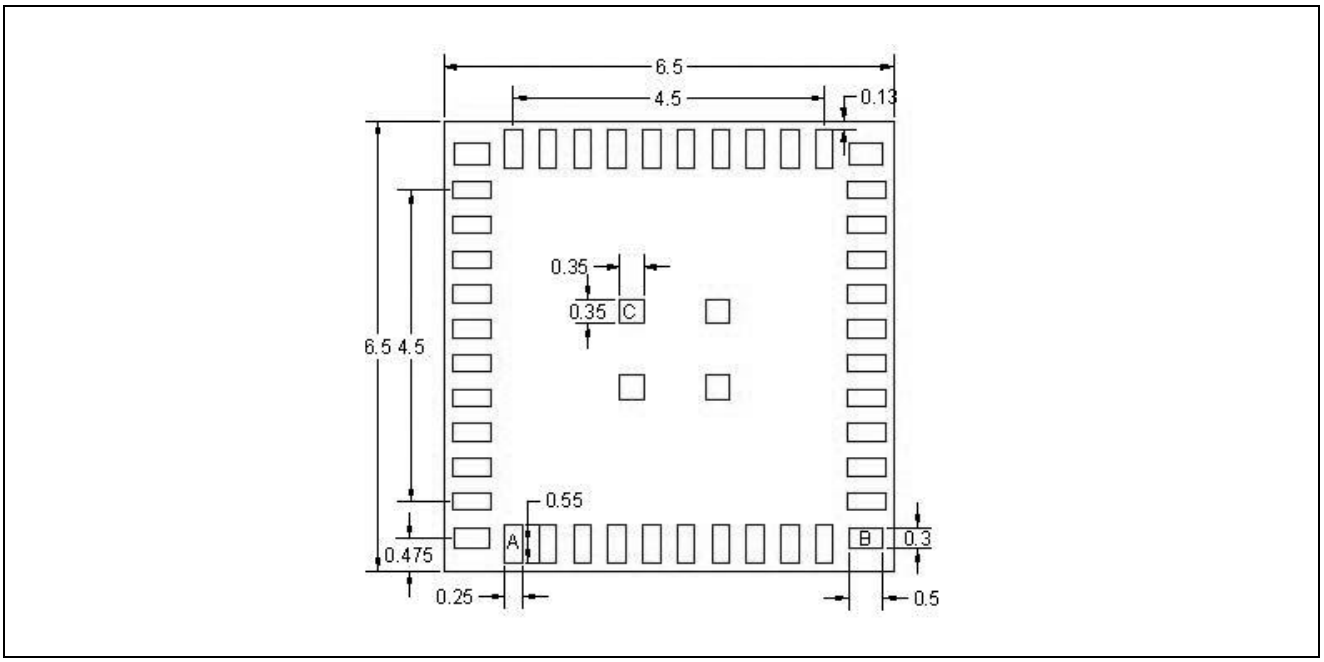
Table 1-12. Pad and Solder Mask Dimensions

Pad Type	Pad Dimensions	Solder Mask Opening Dimensions	Unit
Type A	0.6 × 0.25	0.7 × 0.35	mm
Type B	0.55 × 0.3	0.65 × 0.4	
Type C	0.4 × 0.4	0.5 × 0.5	

1.8.2 PCB Stencil

The recommended PCB stencil is shown in Figure 1-8 (all measurements in mm). Use an unsolder mask to set the module footprint.

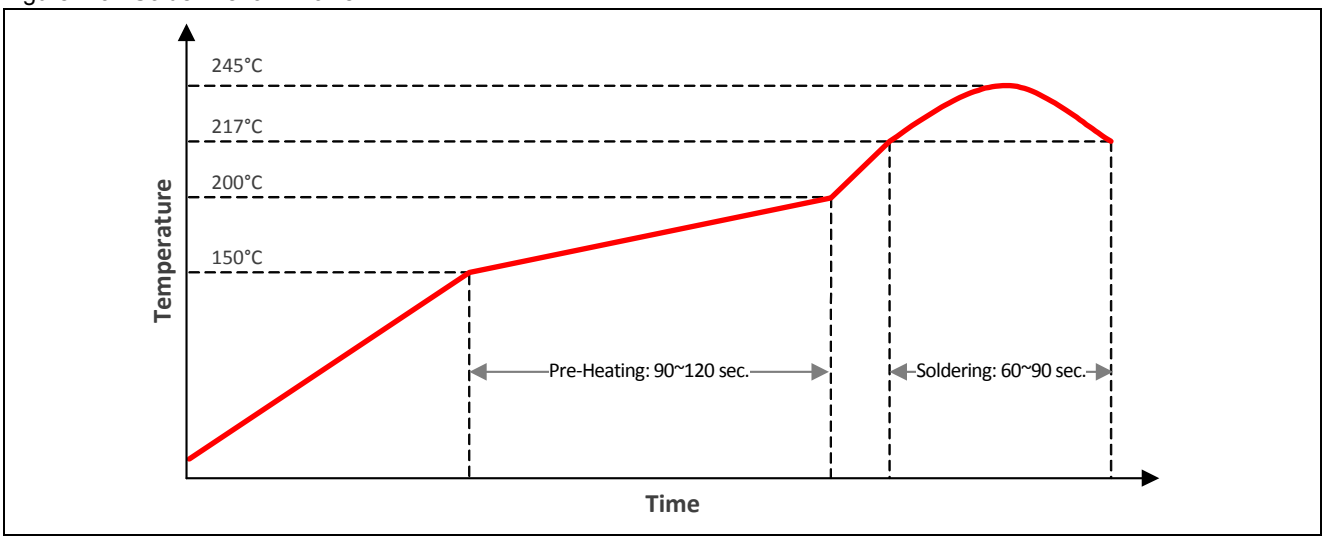
Figure 1-8. CYW20736E Stencil (Bottom View)



1.8.3 Solder Reflow

The recommended solder reflow profile for the CYW20736E is defined in Figure 1-9.

Figure 1-9. Solder Reflow Profile



1.9 Packaging and Storage Information

The CYW20736E is available in a tape and reel package and is shipped in an ESD-protected moisture-resistant (MSL-3) bag as shown in Figure 1-10. The storage temperature range is –40°C to +125°C.

Figure 1-10. CYW20736E ESD/Moisture Packaging

The moisture sensitivity label on the CYW20736E shipping bag is shown in Figure 1-11.

Figure 1-11. CYW20736E Moisture Sensitivity Label

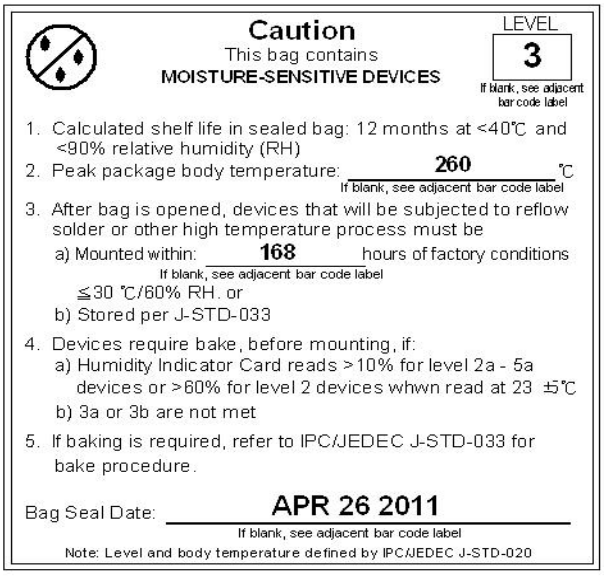
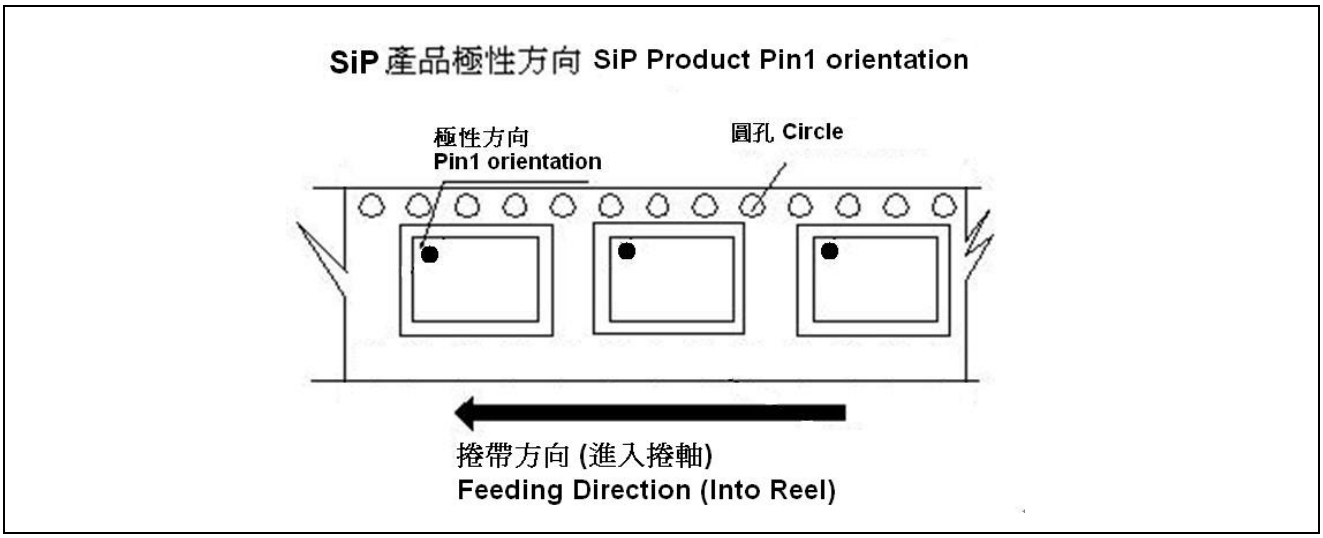


Figure 1-12 shows the location of pin 1 on the CYW20736E relative to its orientation on the tape packaging.

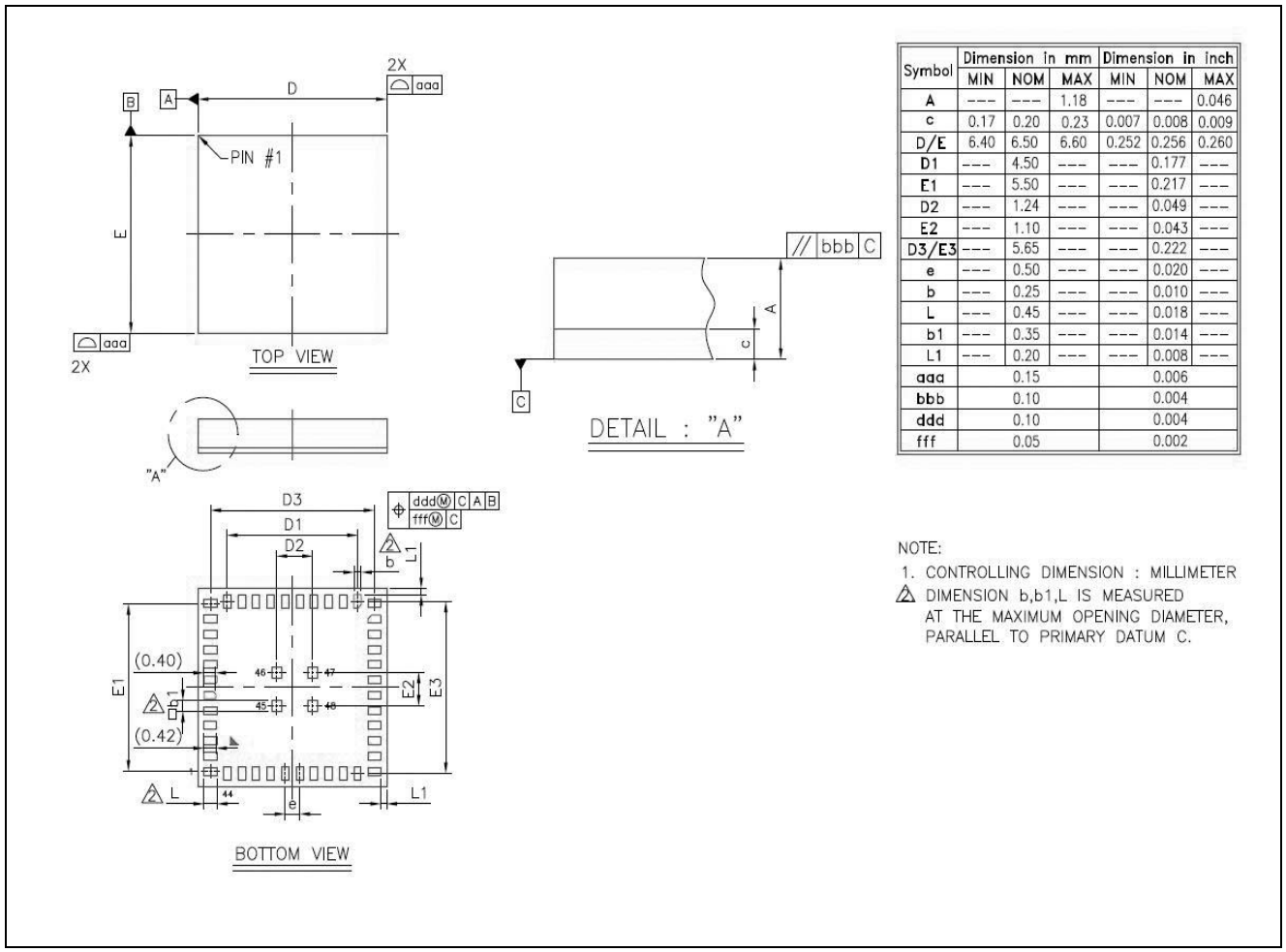
Figure 1-12. CYW20736E Tape and Reel Pin 1 Location



1.10 Mechanical Information

Package dimensions for the CYW20736E are shown in Figure 1-13.

Figure 1-13. CYW20736E Package Dimensions

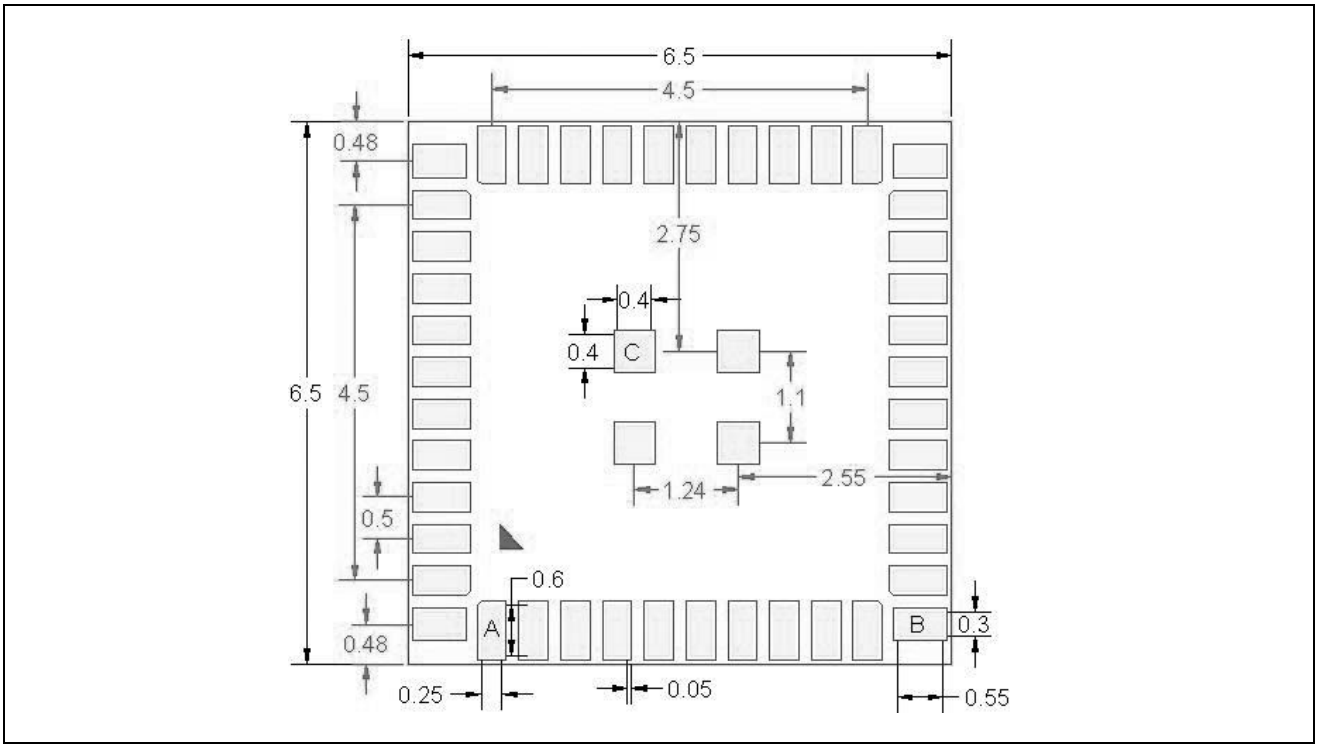


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.18	---	---	0.046
c	0.17	0.20	0.23	0.007	0.008	0.009
D/E	6.40	6.50	6.60	0.252	0.256	0.260
D1	---	4.50	---	---	0.177	---
E1	---	5.50	---	---	0.217	---
D2	---	1.24	---	---	0.049	---
E2	---	1.10	---	---	0.043	---
D3/E3	---	5.65	---	---	0.222	---
e	---	0.50	---	---	0.020	---
b	---	0.25	---	---	0.010	---
L	---	0.45	---	---	0.018	---
b1	---	0.35	---	---	0.014	---
L1	---	0.20	---	---	0.008	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. DIMENSION b,b1,L IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.

Additional CYW20736E package dimensions are shown in Figure 1-14.

Figure 1-14. CYW20736E Pin Dimensions (Bottom View)



1.11 Ordering Information

Table 1-13. Ordering Information

Part	Package	Operating Temperature	Humidity
CYW20736E	48-pin LGA	–40°C to +85°C	95% max., noncondensing

Revision History

Document Revision History

Document Title: CYW20736E Bluetooth Low Energy System-in-Package Module Document Number: 002-15223				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	-	08/17/2015	-	MMP20736E-TRM100-R: Initial Release
*A	-	04/11/2016	-	MMP20736E-TRM101-R **Updated:** Table 5, “Current Consumption”
*B	5561731	01/27/2017	UTSV	Updated to Cypress Template.