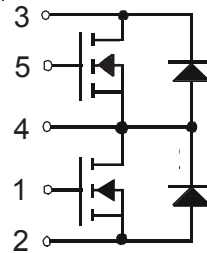


TrenchT2™ HiperFET N-Channel Power MOSFET

FMM150-0075X2F

$$\begin{aligned} V_{DSS} &= 75V \\ I_{D25} &= 120A \\ R_{DS(on)} &\leq 5.8m\Omega \\ t_{rr(typ)} &= 66ns \end{aligned}$$

Phase Leg Topology

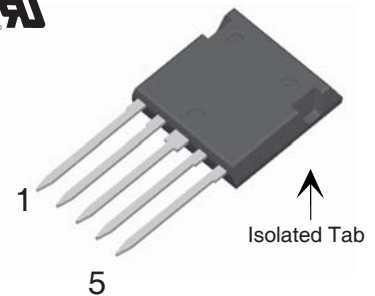


Symbol	Test Conditions	Maximum Ratings	
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +175	°C
V_{ISOL}	50/60Hz, RMS, t = 1min, Leads-to-Tab	2500	~V
T_L	1.6mm (0.062 in.) from Case for 10s	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
F_C	Mounting Force	20..120 / 4.5..27	N/lb.

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 175°C	75	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 175°C , $R_{GS} = 1M\Omega$	75	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	120	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	500	A
I_A	$T_C = 25^\circ\text{C}$	115	A
E_{AS}	$T_C = 25^\circ\text{C}$	850	mJ
dV/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 175^\circ\text{C}$	20	V/ns
P_D	$T_C = 25^\circ\text{C}$	170	W

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
C_p	Coupling Capacitance Between Shorted Pins and Mounting Tab in the Case		40	pF
d_S, d_A	Pin - Pin	1.7		mm
d_S, d_A	Pin - Backside Metal	5.5		mm
Weight			9	g

ISOPLUS i4-Pak™



Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
 - UL Recognized Package
 - Isolated Mounting Surface
 - 2500V Electrical Isolation
- Avalanche Rated
- Low Q_G
- Low Drain-to-Tab Capacitance
- Low Package Inductance

Advantages

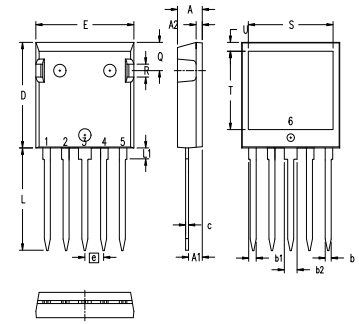
- Easy to Mount
- Space Savings
- High Power Density

Applications

- DC-DC Converters
- Battery Chargers
- Switched-Mode and Resonant-Mode Power Supplies
- DC Choppers
- AC Motor Drives
- Uninterruptible Power Supplies
- High Speed Power Switching Applications

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	75		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0		4.0 V
I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}, V_{GS} = 0V$ $T_J = 150^\circ\text{C}$			25 μA 250 μA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 100A$, Note 1			5.8 m Ω
g_{fs}	$V_{DS} = 10V, I_D = 60A$, Note 1	50	83	S
C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1\text{ MHz}$		10.5	nF
C_{oss}			1165	pF
C_{rss}			125	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 115A$ $R_G = 2\Omega$ (External)		23	ns
t_r			18	ns
$t_{d(off)}$			33	ns
t_f			15	ns
$Q_{g(on)}$	$V_{GS} = 10V, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 100A$		178	nC
Q_{gs}			37	nC
Q_{gd}			55	nC
R_{thJC}				0.88 $^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

ISOPLUS i4-Pak™ Outline



NOTE: Bottom heatsink meets 3000 Volts AC 1 sec isolation to the other pins.

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
b2	.100	.110	2.54	2.79
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

Ref: IXYS CO 0077 R0

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0V$			230 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			900 A
V_{SD}	$I_F = 75A, V_{GS} = 0V$, Note 1			1.5 V
t_{rr}	$I_F = 115A, -di/dt = 100A/\mu s$ $V_R = 37V, V_{GS} = 0V$		66	ns
I_{RM}			4.4	A
Q_{RM}			145	nC

Note 1. Pulse test, $t \leq 300\mu s$, duty cycle, $d \leq 2\%$.

ADVANCE TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated objective result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves The Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
by one or more of the following U.S. patents: 4,850,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

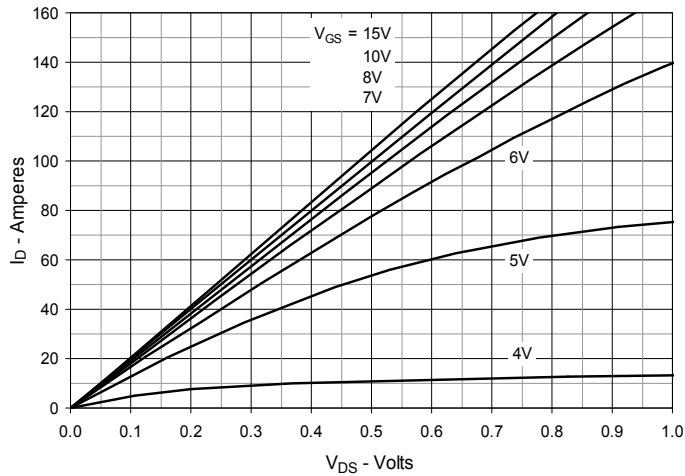
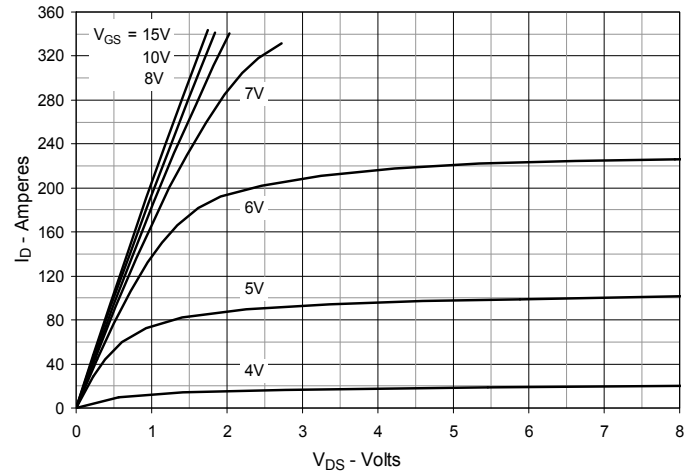
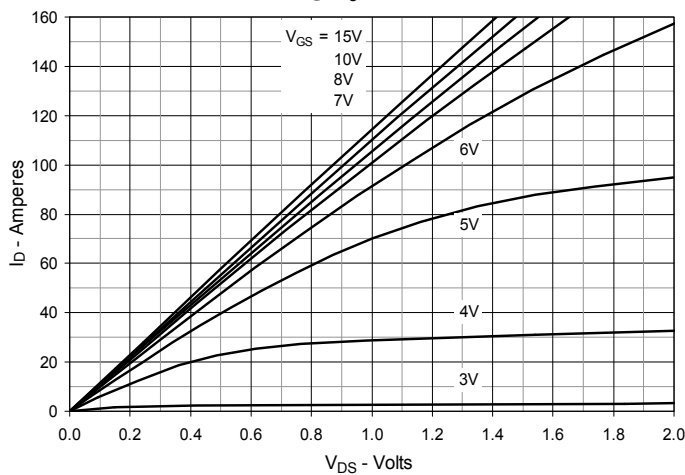
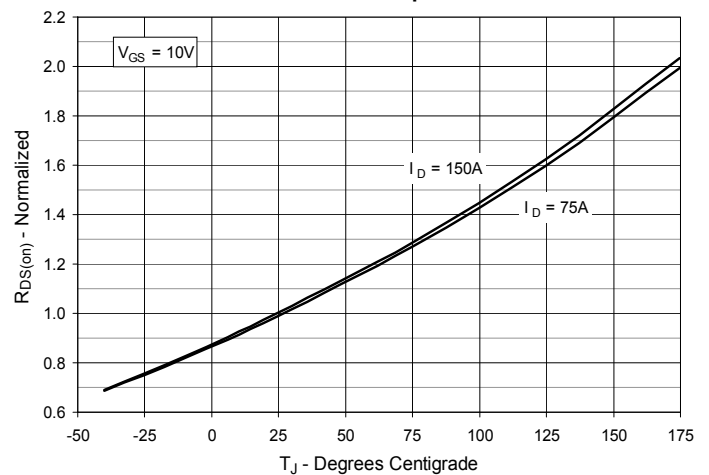
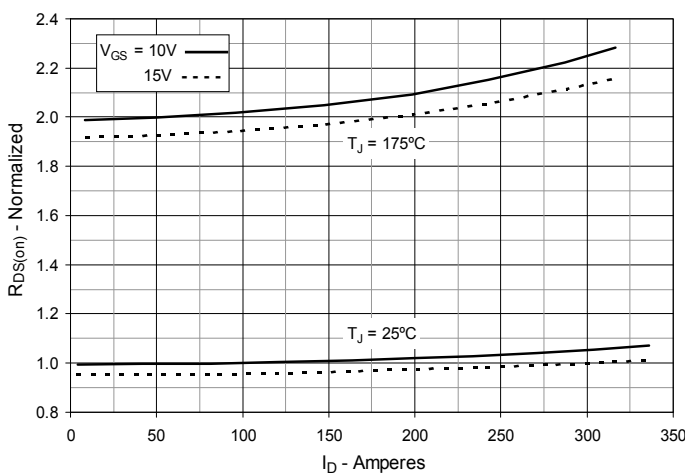
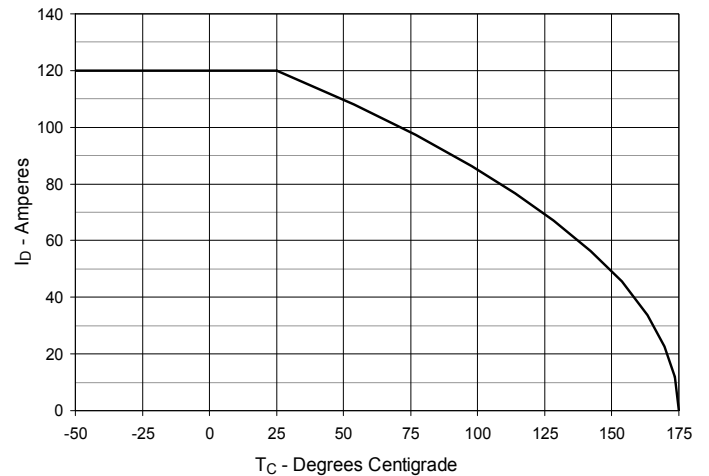
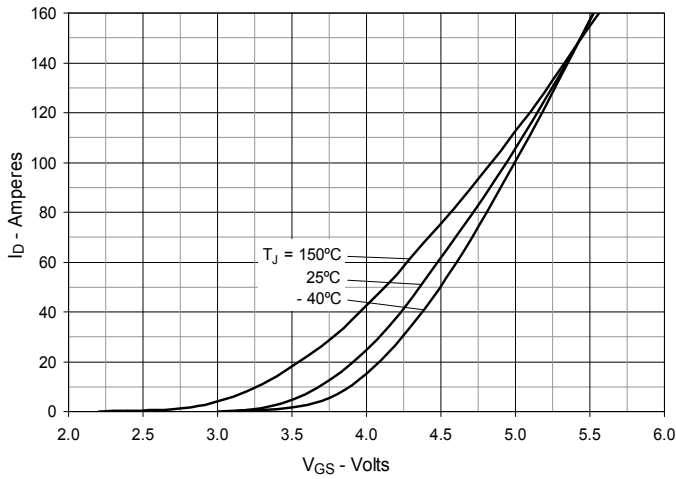
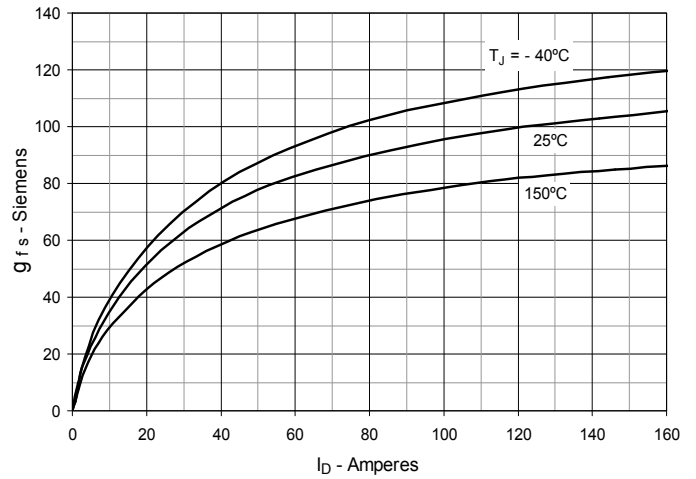
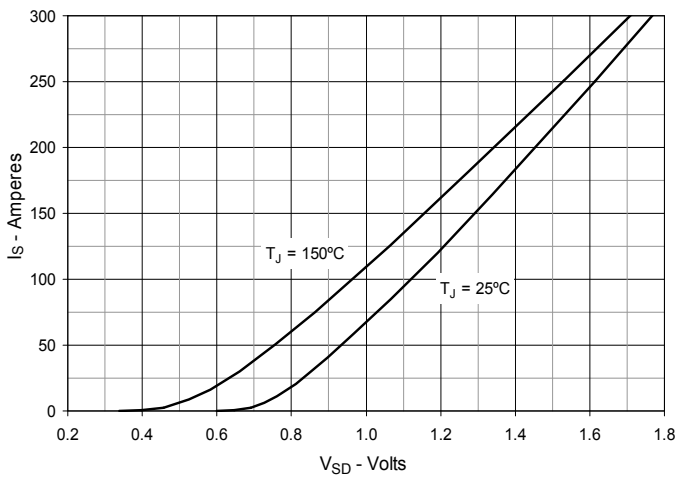
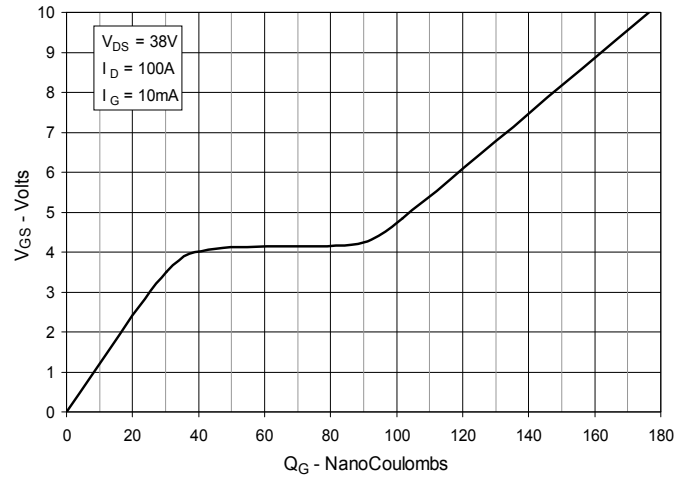
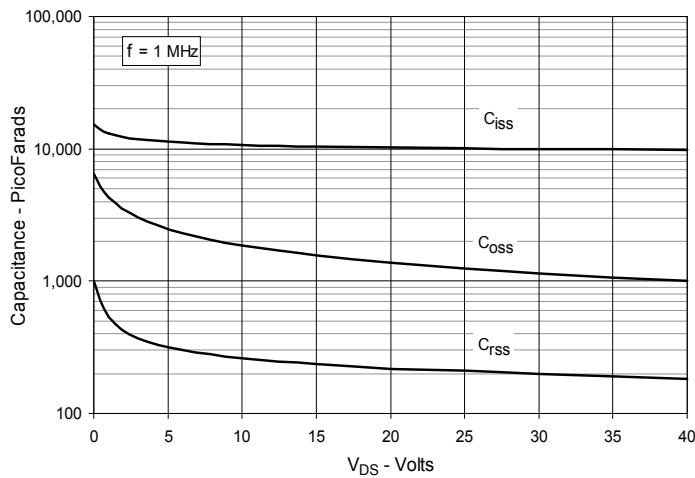
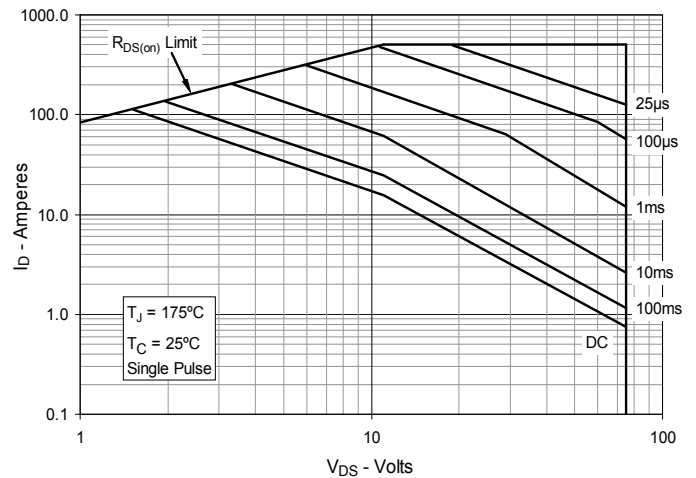
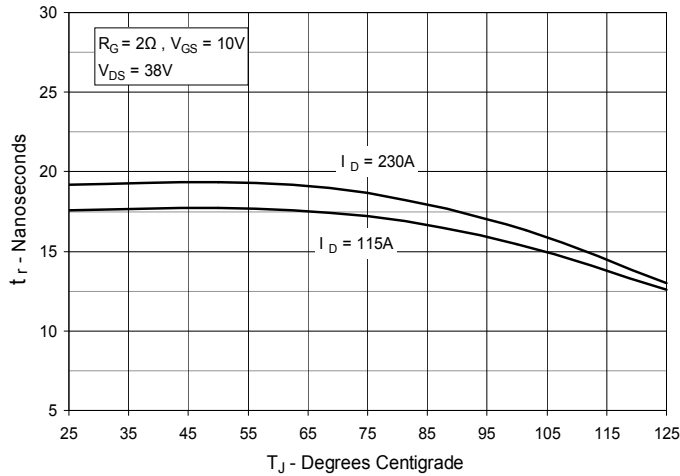
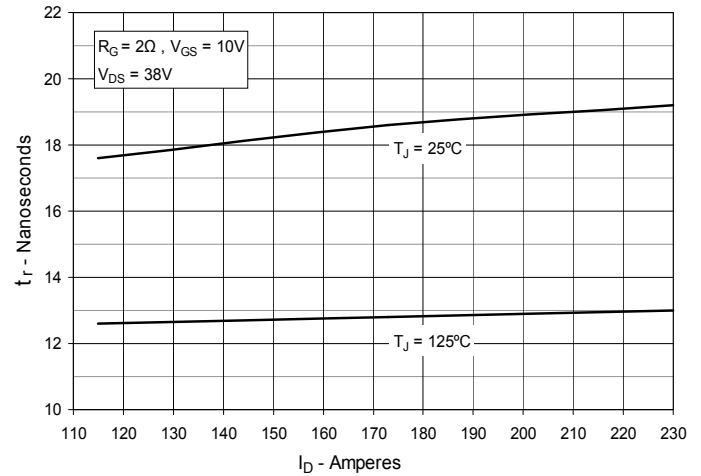
Fig. 1. Output Characteristics
@ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics
@ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics
@ $T_J = 150^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 75\text{A}$ Value vs.
Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 75\text{A}$ Value vs. Drain Current

Fig. 6. Drain Current vs. Case Temperature


Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


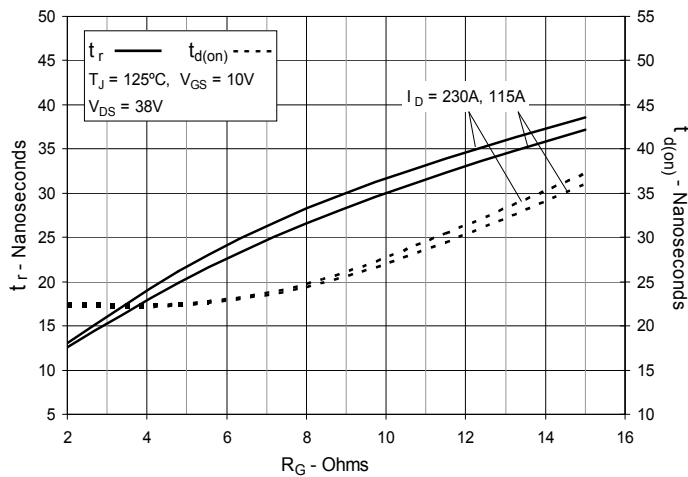
**Fig. 13. Resistive Turn-on
Rise Time vs. Junction Temperature**



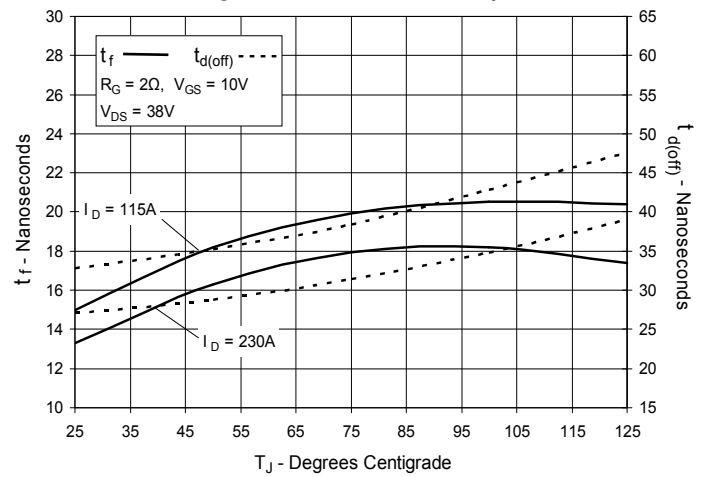
**Fig. 14. Resistive Turn-on
Rise Time vs. Drain Current**



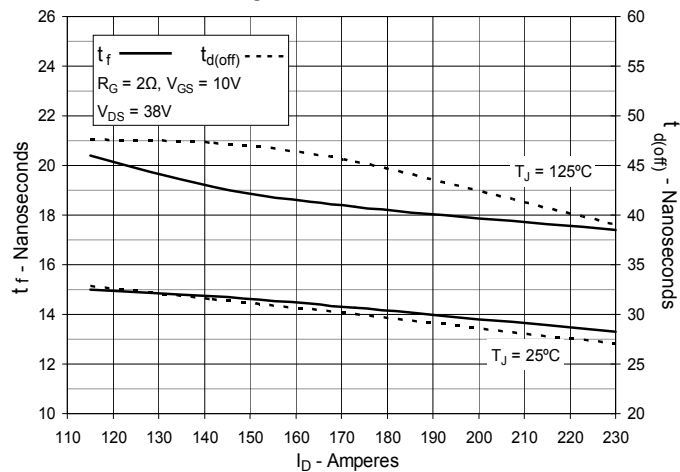
**Fig. 15. Resistive Turn-on
Switching Times vs. Gate Resistance**



**Fig. 16. Resistive Turn-off
Switching Times vs. Junction Temperature**



**Fig. 17. Resistive Turn-off
Switching Times vs. Drain Current**



**Fig. 18. Resistive Turn-off
Switching Times vs. Gate Resistance**

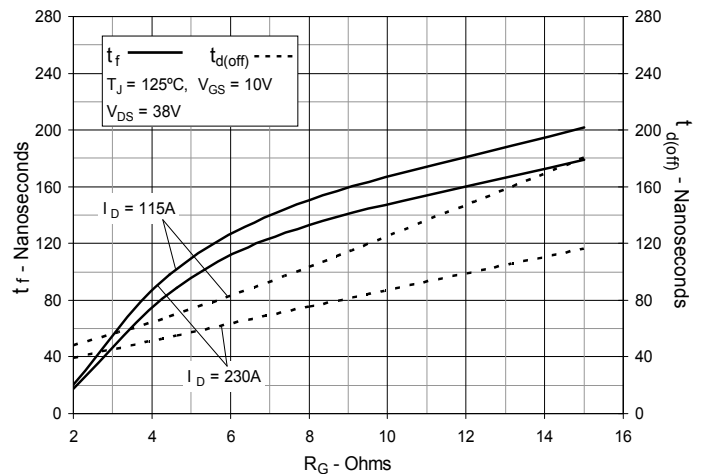


Fig. 19. Maximum Transient Thermal Impedance

