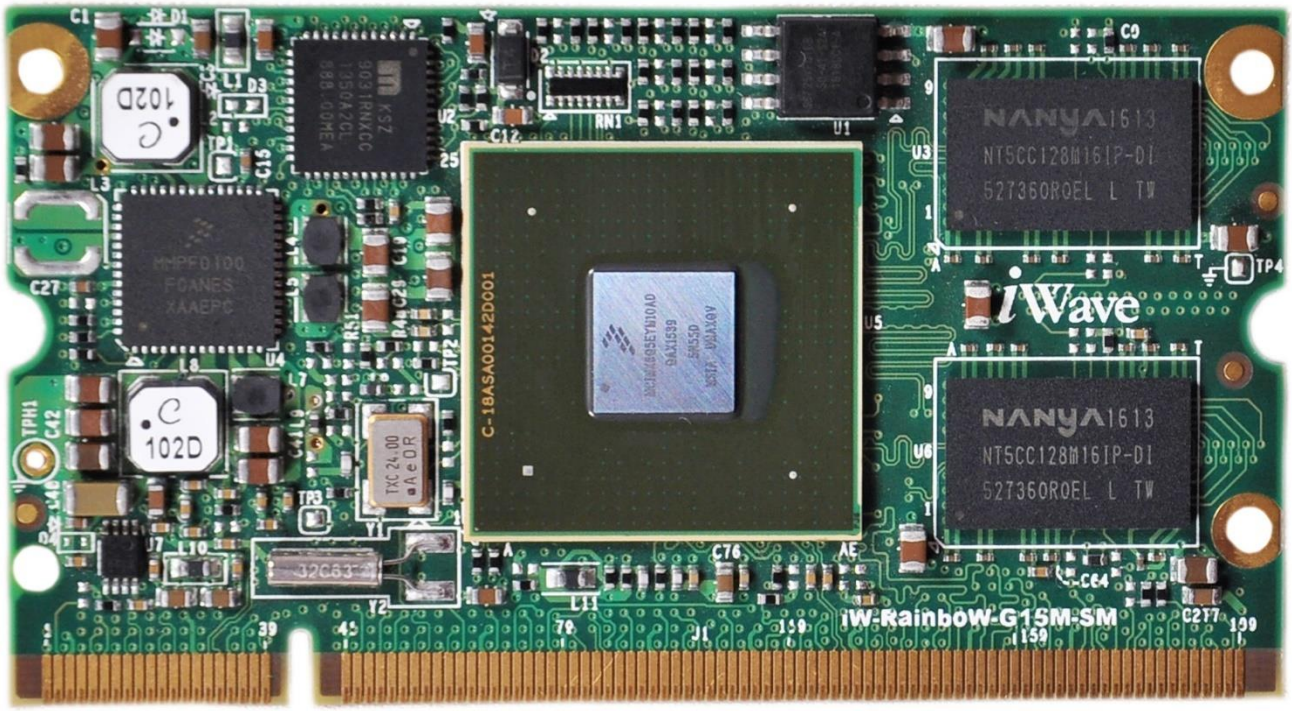
iW-RainboW-G15M-SM
i.MX6 SODIMM System On Module
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX6 SODIMM System On Module based on the NXP's i.MX6 Applications Processor with PMIC. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX6 SODIMM System On Module from a Hardware Systems perspective.

1.2 SODIMM SOM Overview

The i.MX6 SODIMM SOM is extension of i.MX6 CPU. Also with the SOM approach one can reduce the cost and time required for the development of customised solution on i.MX6 SODIMM platform. SODIMM module has a form factor of 67.6mm x 37mm and provides the functional requirements for an embedded application. A single ruggedized SODIMM connector provides the carrier board interface to carry all the I/O signals to and from the SODIMM module.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BPP	Bits Per Pixel
BSP	Board Support Package
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3	Double Data Rate 3
eCSPI	Enhanced Configurable Serial Peripheral Interface
eMMC	Enhanced Multi Media Card
FLEXCAN	Flexible Controller Area Network
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second

Acronyms	Abbreviations
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signal
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec
MHz	Mega Hertz
NC	No Connect
PCB	Printed Circuit Board
PCIe	Peripheral Component Interface Express
PMIC	Power Management Integrated Circuit
PWM	Pulse Width Modulation
RTC	Real Time Clock
SAI	Synchronous Audio Interface
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SOM	System On Module
SODIMM	Small Outline Dual in-line Memory Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- i.MX6 Applications Processors Datasheet
- i.MX6 Applications Processors Reference Manual

1.6 Important Note

i.MX6 SODIMM Edge connector pin name mentioned in ***Table 5*** is followed as per below format for easy understanding.

- If CPU pin functionality name and CPU pad name is same, Signal name is mentioned as

  "CPU Pad Name"

  Example: SD1_DATA1

  In this signal, functionality which we are using and CPU Pad name is ***SD1_DATA1*.**

- If CPU pin functionality name and pad name is different, Signal name is mentioned as

  "Functionality name (CPU Pad name)"

  Example: CAN1_RXD (UART3_RTS_B)

  In this signal, ***CAN1_RXD*** is the functionality which we are using and ***UART3_RTS_B*** is the CPU Pad name.

- If CPU pin functionality is GPIO, Signal name is mentioned as

  "FunctionalityDescription (CPU Pad name)"

  Example: PWM4_OUT (GPIO1_IO05)

  In this signal, ***PWM4_OUT*** is the functionality which we are using and ***GPIO1_IO05*** is the CPU pad name.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX6 SODIMM SOM Features and Hardware architecture with high level block diagram. Also this section provides detailed information about SODIMM edge connector pin assignment and usage.

2.1 i.MX6 SODIMM SOM Block Diagram

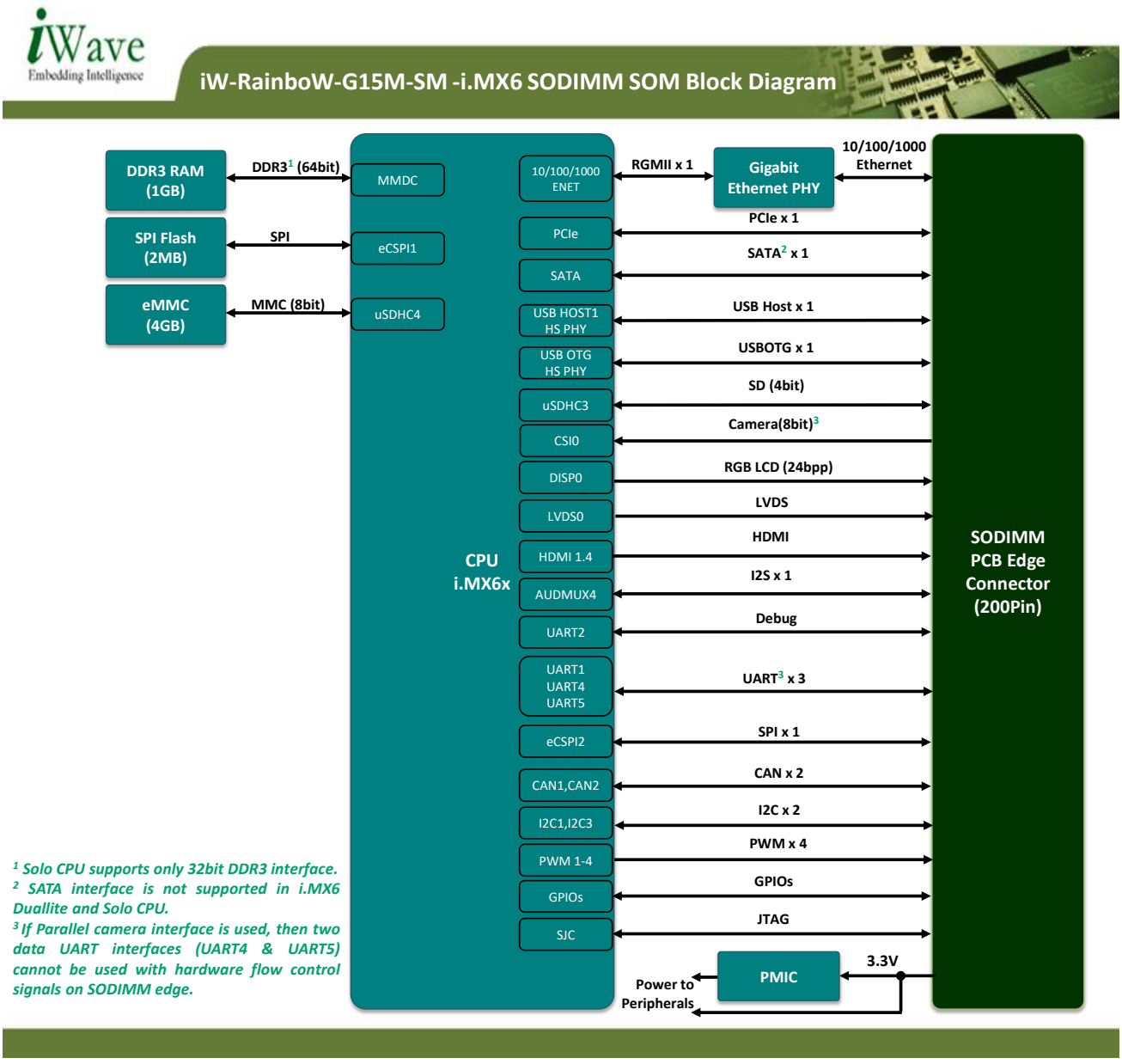

Figure 1: i.MX6 SODIMM SOM Block Diagram

2.2 i.MX6 SODIMM SOM Features

The i.MX6 SODIMM SOM supports the following features.

CPU

- NXP's i.MX6 Quad/Dual/Duallite/Solo ARM™ Cortex-A9 based CPU @ up to 1.2GHz/Core

PMIC

- NXP's MMPF0100 PMIC

Memory

- 1GB DDR3 RAM (Expandable)
- 2MB SPI NOR Flash (Expandable)
- 4GB eMMC Flash (Expandable)

SODIMM PCB Edge Interfaces

- Boot Mode Control Signals
- Gigabit Ethernet through On-SOM Ethernet PHY Transceiver x 1 Port
- PCIe x 1 Port
- SATA II (3.0 Gbps) x 1 Port [1]
- USB2.0 OTG x 1 Port
- USB2.0 Host x 1 Port
- SD (4bit) x 1 Port
- Parallel Camera Port (8bit) x 1 Port [2,3]
- Parallel RGB Display (24bpp) x 1 Port [4]
- LVDS x 1 Port [4]
- HDMI 1.4 x 1 Port [4]
- I2S Audio Interface x 1 Port
- Debug UART
- Data UART x 3 Ports [2]
- SPI x 1 Port [3]
- CAN x 2 Ports
- I2C x 2 Ports
- PWM x 4 Ports
- General Purpose IOs
- JTAG x 1 Port

General Specification

- Power Supply : 3.3V
- Form Factor : 67.6mm x 37mm

[1] *SATA interface is not supported in i.MX6 Duallite and Solo CPU.*

[2] *If Parallel camera interface is used, then two data UART interfaces (UART4 & UART5) cannot be used with hardware flow control signals on SODIMM edge.*

[3] *If Parallel camera is used with 12bit interface, then SPI interface (eCSPI2) cannot be used on SODIMM edge.*

[4] *i.MX6 Duallite and i.MX6 Solo CPU supports only one IPU and so at any time only two display interfaces (including LVDS, HDMI & Parallel RGB) can be supported.*

2.3 i.MX6 CPU

i.MX6 SODIMM SOM is based on i.MX 6 series of applications processors is a feature and performance scalable multicore platform that includes single-, dual- and quad-core families based on the ARM® Cortex® architecture, including Cortex-A9 based solutions up to 1.2 GHz. i.MX6 CPU is NXP's latest achievement in integrated multimedia application processors which is part of growing multimedia-focused products that offers high performance processing and are optimized for lowest power consumption. The Block Diagram of i.MX6 CPU from the NXP's i.MX6 (Quad/Dual) datasheet is shown below for reference.

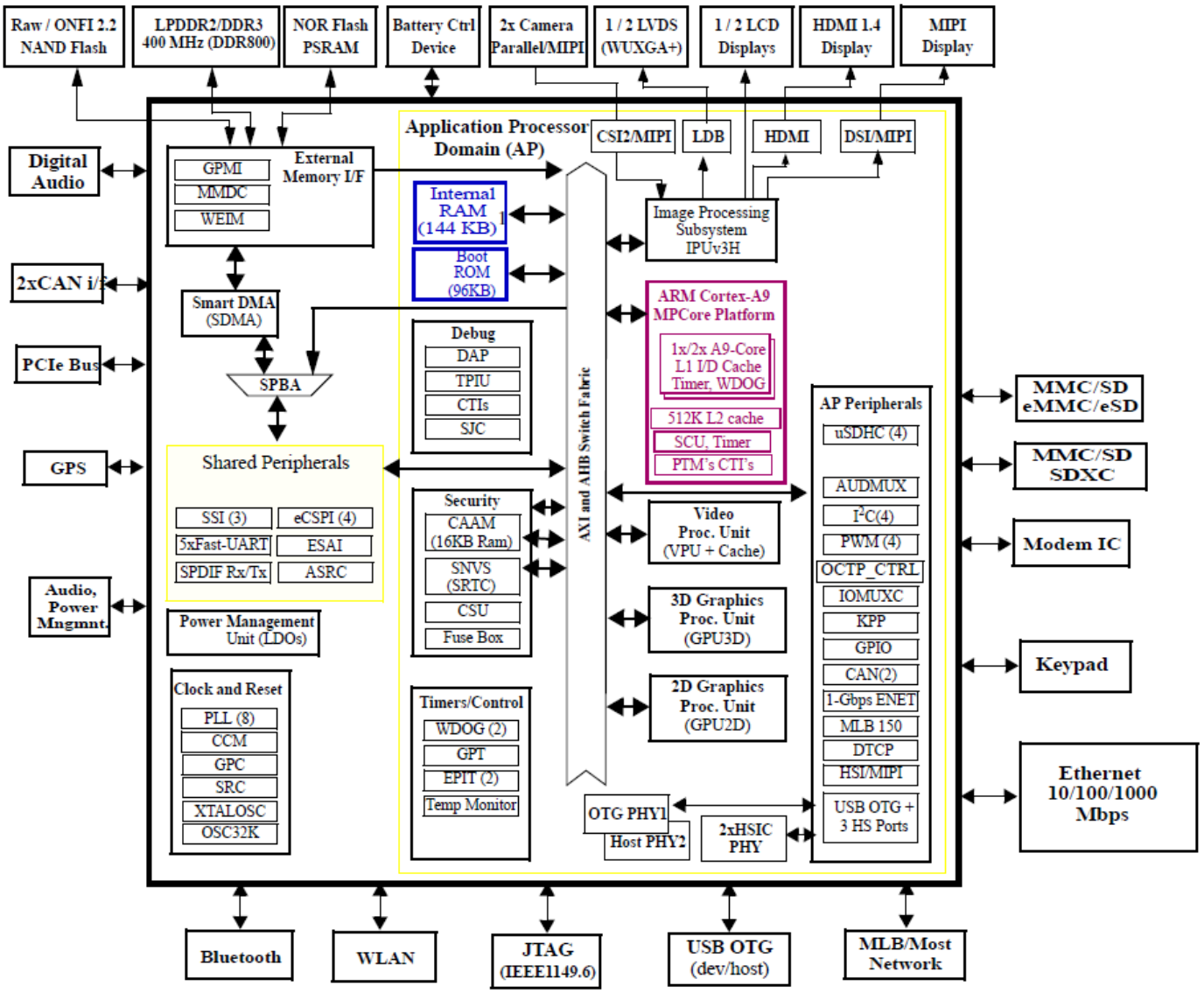

Figure 2: i.MX6 Simplified Block Diagram

Note: Please refer the latest i.MX6 Datasheet & Reference Manual from NXP website for Electrical characteristics of i.MX6 Application CPU which may be revised from time to time.

2.4 PMIC

i.MX6 SODIMM SOM supports NXP's PF0100 PMIC for On-SOM power management. The PF0100 is a Power Management Integrated Circuit (PMIC) designed specifically for always ON application with the NXP i.MX6 application processors.

This PMIC supports up to six buck converters, six linear regulators, RTC supply and coin-cell charger with programmable output voltage, sequence and timing. i.MX6 CPU's I2C1 interface is used for PMIC programmable. I2C address for PMIC is 0x08.

2.5 Memory

2.5.1 DDR3 SDRAM

i.MX6 SODIMM SOM by default supports 1GB DDR3 RAM memory in 64bit mode. To support this, it uses four 256MB DDR3 SDRAM ICs. These devices operate at 1.5V voltage level. Each pair of DDR3 ICs is physically located on either side of the iMX6 SODIMM SOM. The RAM size can be expandable up to maximum of 4GB.

Note: By default, 512MB DDR3 with 32bit mode only supported in i.MX6 Solo CPU based SODIMM SOM.

2.5.2 SPI NOR Flash

The i.MX6 SODIMM SOM supports 2MB SPI NOR Flash as default boot device. This is connected to eCSPI1 controller of the i.MX6 CPU and operates at 3.3 Voltage level. The SPI flash memory is physically located on top side of the SODIMM SOM. The memory size of the SPI Flash can be expandable.

2.5.3 eMMC Flash

i.MX6 SODIMM SOM supports 4GB eMMC (expandable) memory as mass. eMMC is directly connected to the uSDHC4 of the i.MX6 CPU and operating at 3.3V Voltage level. The eMMC flash memory is physically located on bottom side of the SODIMM SOM. The memory size of the eMMC Flash can be expandable.

2.6 i.MX6 SODIMM PCB Edge Connector

i.MX6 SODIMM SOM Supports JEDEC Physical Standard 200pin SODIMM PCB edge connector for interfaces expansion. The interfaces which are available at SODIMM Edge connector are explained in the following sections.

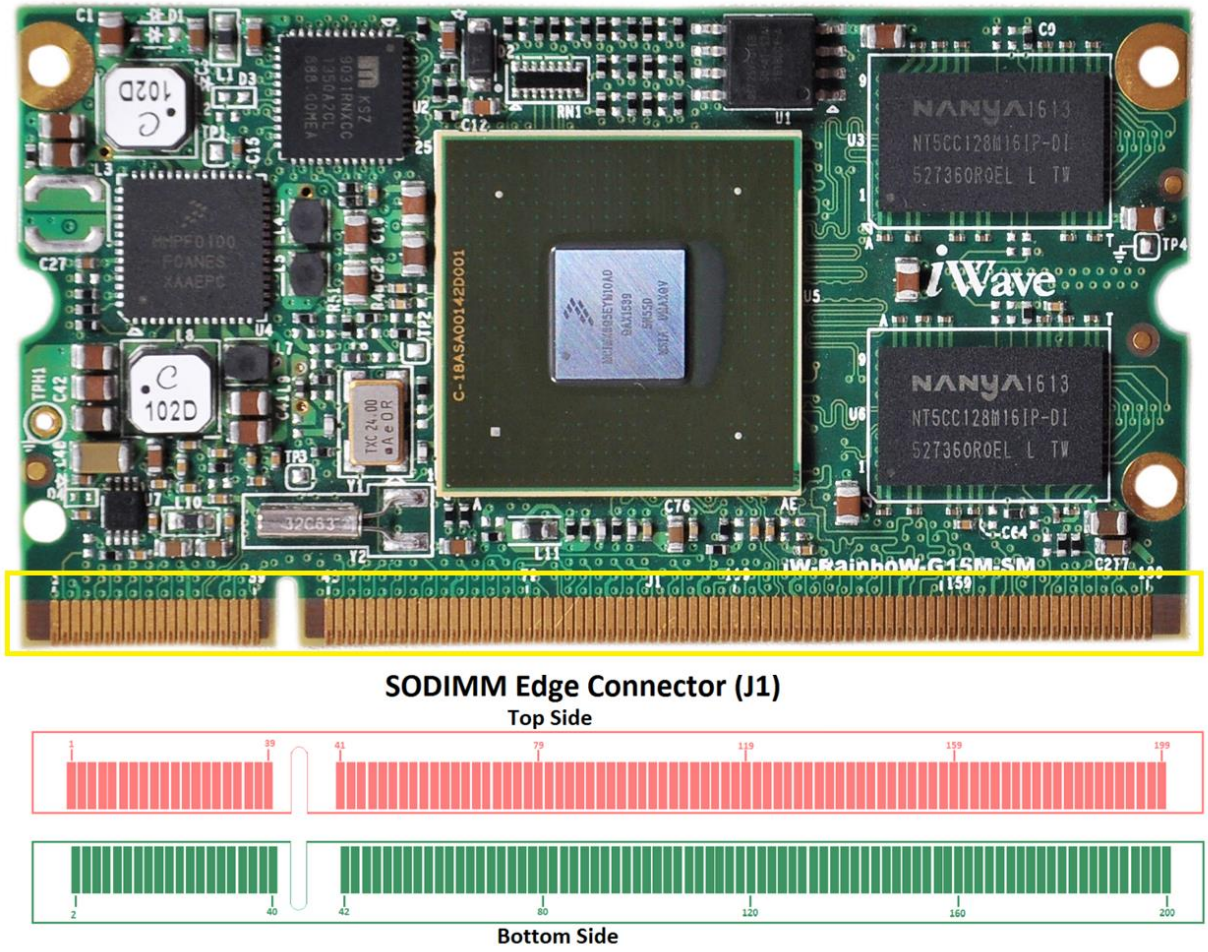

Figure 3: i.MX6 SODIMM PCB Edge Connector

Number of Pins	- 200
Connector Part	- Not Applicable (On Board PCB Edge connector)
Mating Connector	- 1473005-1 from TE Connectivity

2.6.1 Boot Setting

i.MX6 CPU boot process begins at Power On Reset (POR) where the hardware reset logic forces the ARM core to begin execution starting from the on-chip boot ROM. i.MX6 CPU Boot ROM code uses the state of the internal register BOOT_MODE [1:0] as well as the state of various eFUSEs and/or GPIO settings to determine the boot flow behaviour of the device. i.MX6 SODIMM SOM boot media is fixed as SPI flash by On-SOM GPIO setting in hardware.

Note: Contact iWave if different boot media support is required other than SPI flash.

i.MX6 SODIMM SOM supports two boot mode signals on SODIMM Edge Connector. BOOT_MODE is initialized by sampling the BOOT_MODE0 and BOOT_MODE1 inputs on the rising edge of POR_B. These Boot mode selection signals are connected to SODIMM Edge connector and desired boot mode must be set from the carrier board as explained in the below table.

For more details, refer SODIMM Edge connector pins 182 & 184 on ***Table 5***.

Table 3: Boot Mode Pin Settings Truth Table

BOOT_MODE [1] (SODIMM Edge Pin 184)	BOOT_MODE [0] (SODIMM Edge Pin 182)	Boot Type	Description
1	0	Internal Boot Mode	In this mode, i.MX6 boots from the boot media selected by Boot media GPIO pin's settings. By default, SPI is selected as boot media in i.MX6 SODIMM SOM hardware.
0	0	Boot From eFuses	In this mode, i.MX6 boots from the boot media selected by i.MX6 eFUSE settings. *Note: i.MX6 eFuse setting is not modified by iWave from silicon shipped value.*
0	1	Serial Downloader Mode	In this mode, i.MX6 boot media can be Programmed through its USB OTG interface using manufacturing tool supported by NXP/Freescale (MFG Tool).

Important Note: To make i.MX6 SODIMM SOM boots as expected, make sure to set the desired boot mode from the carrier board.

2.6.2 Gigabit Ethernet

i.MX6 SODIMM SOM supports one 10/100/1000Mbps Ethernet interface on SODIMM Edge connector through RGMII interface. The MAC is integrated in the i.MX6 CPU and connected to the external Ethernet PHY on SOM. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. i.MX6 SODIMM SOM also supports Link and Speed indication LED control signals to SODIMM Edge.

i.MX6 SODIMM SOM supports one "KSZ9031RNXCA" Ethernet PHY from Micrel. These PHY's are interfaced with i.MX6 CPU using RGMII interface and works at 1.8V IO voltage level. Since this PHY doesn't require center tap supply to the magnetics, CTREF voltage to SODIMM Edge is not supported on SOM. It is recommended that center tap pins of magnetics should be separated from one another and connected through separate 0.1uF common mode capacitors to ground. The below table provides the compatible magnetics recommended by PHY Manufacturer.

Table 4: Compatible Magnetics

Part Description	Part Number	Manufacturer	Temperature
Gigabit Ethernet Discrete Transformer	TG1G-E001NZRL	HALO	-40°C to 85°C
Gigabit Ethernet Discrete Transformer	HX5008NL	Pulse	-40°C to 85°C
RJ45 Magjack with two Green LED	JK0654219NL	Pulse	0°C to 70°C
RJ45 Magjack with two Green LED	0826-1G1T-23F	Bel Fuse	0°C to 70°C
Gigabit Ethernet Discrete Transformer	000-7093-37R-LF1	Wurth	0°C to 70°C

For more details, refer SODIMM Edge connector pins 2, 4, 6, 8, 14, 16, 15 & 17 on ***Table 5.***

Note: As per i.MX6 CPU Errata ERR004512, Gigabit Ethernet MAC has throughout limitation. The theoretical maximum performance of 1Gbps ENET is limited to 470 Mbps (total for Tx and Rx). The actual measured performance in an optimized environment is up to 400 Mbps.

2.6.3 PCIe Interface

i.MX6 SODIMM SOM supports one PCI Express Gen2.0 lane on SODIMM Edge connector. i.MX6 CPU's PCIe Express core with integrated PHY is used for PCIe Interface which can support PCIe Gen2.0 at 5Gbps data rate and are backward compatible to Gen1.1 at 2.5Gbps data rate. PCIe wake input and PCIe reset output are supported on SODIMM Edge connector from i.MX6 CPU GPIOs GPIO_2 & GPIO_16 correspondingly.

For more details, refer SODIMM Edge connector pins 127, 128, 129, 130, 132, 134, 135 & 137 on ***Table 5.***

Note: Termination is required on the PCIe differential clock lines and should be placed as close as possible to the receiver device input or PCIe connector. Connect two 49.9 Ω resistors between REFCLK- and GND & REFCLK+ and GND. Alternately, Connect a 100 Ω resistor between REFCLK- and REFCLK+. PCIe differential transmitter lines are ac coupled on SOM itself.

2.6.4 SATA Interface

i.MX6 SODIMM SOM supports one SATA II lane on SODIMM Edge connector. i.MX6 CPU's SATA controller core with integrated PHY is used for SATA Interface which can support SATA II with transfer rate of 3Gbps and backward compatible to SATA I with transfer rate of 1.5Gbps.

For more details, refer SODIMM Edge connector pins 82, 84, 85 & 87 on ***Table 5.***

Note: SATA interface is not supported in i.MX6 Duallite and i.MX6 Solo CPU.

2.6.5 USB2.0 OTG Interface

i.MX6 SODIMM SOM supports one High Speed USB2.0 OTG interfaces on SODIMM Edge connector. i.MX6 CPU's USB2.0 OTG controller core with integrated PHY is used for USB2.0 OTG interface which can operate in High Speed operation (480 Mbps), Full Speed operation (12Mbps) and Low Speed operation (1.5 Mbps). i.MX6 CPU's OTG controller core can operate in Host mode and Device (Peripheral) mode. Also USB ID input from SODIMM Edge connector is connected to i.MX6 CPU's USB_OTG_ID for auto USB host or device detection.

For more details, refer SODIMM Edge connector pins 74, 77, 81 & 83 on ***Table 5.***

2.6.6 USB2.0 Host Interface

i.MX6 SODIMM SOM supports one USB2.0 Host interface on SODIMM Edge connector. i.MX6 CPU's USB2.0 Host controller core with integrated PHY is used for USB2.0 Host interface which can operate in High Speed operation (480 Mbps), Full Speed operation (12Mbps) and Low Speed operation (1.5 Mbps).

For more details, refer SODIMM Edge connector pins 39, 140, 188 & 190 on ***Table 5.***

2.6.7 SD Interface

I.MX6 SODIMM SOM supports one SDIO interface port on SODIMM Edge connector. i.MX6 CPU's uSDHC3 controller is used for SD interface which is fully compliant with SD Memory Card Specifications v3.0 including high-capacity SDHC cards up to 32 GB & SDXC cards up to 2TB and SDIO Card Specification Part E1, v1.10. It supports 1-bit or 4-bit transfer mode for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max). i.MX6 SODIMM SOM can also support SDIO card detect input from SODIMM Edge connector through i.MX6 CPU pin EIM_D25 .

For more details, refer SODIMM Edge connector pins 105, 107, 108, 109, 111, 112 & 114 on ***Table 5.***

Note: If EIM_D25 is not used for SDIO card detect, the same pins can be used for SS3 chip select (eCSPI2_SS3(EIM_D25) of eCSPI2 interface.

Note: If more SDIO interfaces are required on SODIMM edge, it can be supported by modifying the CPU IOMUX setting on SODIMM edge pins. Contact iWave for more details.

2.6.8 Parallel Camera Interface

i.MX6 SODIMM SOM supports one 8bit/12bit camera interface on SODIMM Edge Connector. i.MX6 CPU's CSI parallel port is used for camera interface which provides direct connectivity to most relevant CMOS sensors and CCIR656 video interface. The sensor is the master of the pixel clock (PIXCLK) & synchronization signals where synchronization signals can be received using dedicated control signals method (HSYNC & VSYNC) or controls embedded in data stream method (CCIR.656 protocol).

For more details, refer SODIMM Edge connector pins 38, 75, 93, 96, 100, 101, 104, 119,120, 121, 123 & 126 for 8bit camera interface on ***Table 5*****.** For 12bit camera, please refer pins 63, 66, 70 & 110 for extra 4bits on ***Table 5***

Note: If Parallel camera interface is used on SODIMM edge, then UART4 & UART5 cannot be used with hardware flow control for request to send and clear to send signals.

Note: If Parallel camera is used with 12bit interface on SODIMM edge, then eCSPI2 interface cannot be used.

2.6.9 Parallel RGB Display Interface

i.MX6 SODIMM SOM supports one 24bpp Parallel RGB display interface on SODIMM Edge connector. i.MX6 CPU's IPU is used for parallel LCD display interface which supports upto 24bit data bus (8bits/colour). i.MX6 CPU's LCD can support data rate up to up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz).

For more details, refer SODIMM Edge Connector pins 143, 144, 145, 146, 148, 149, 150, 152, 153, 154, 155, 156, 157, 158, 159, 161, 162, 163, 164, 165, 166, 167, 168, 170, 171, 172, 173, 174 on ***Table 5.***

Note: i.MX6 Duallite and i.MX6 Solo CPU supports only one IPU and so at any time only two display interfaces (including LVDS, HDMI & Parallel RGB) can be supported.

2.6.10LVDS Interface

i.MX6 SODIMM SOM supports one LVDS display port on SODIMM Edge connector. i.MX6 CPU's IPU with LDB is used for LVDS interface. The purpose of the LDB is to support flow of synchronous RGB data from the IPU to external display devices through the LVDS interface. It consists of one clock pair & four data pairs and can support data rate up to 170Mhz (WUXGA 1920x1200). i.MX6 CPU LVDS interface supports 18bit RGB and 24bit RGB colour mapping.

i.MX6 CPU LVDS0 is directly connected to SODIMM Edge connector. LVDS backlight enable and LVDS backlight brightness control (PWM) are supported on SODIMM Edge connector from i.MX6 CPU pins NANDF_ALE and GPIO_9.

For more details, refer SODIMM Edge connector pins 47, 48, 50, 52, 53, 54, 55, 56, 57, 58, 59 & 138 on ***Table 5.***

Note: i.MX6 Duallite and i.MX6 Solo CPU supports only one IPU and so at any time only two display interfaces (including LVDS, HDMI & Parallel RGB) can be supported.

2.6.11HDMI Interface

i.MX6 SODIMM SOM supports one HDMI display port (Ver. 1.4) on SODIMM Edge connector. HDMI is a compact audio/video interface for transmitting uncompressed digital video data and uncompressed/compressed digital audio data. HDMI is electrically compatible with the signals used by DVI and so no signal conversion is necessary, nor is there a loss of video quality when a DVI-to-HDMI adapter is used.

i.MX6 CPU's HDMI TX controller with integrated PHY is used for HDMI interface which can support video formats up to 1080p at 60Hz and 720p/1080i at 120Hz. It can also support CEC interface & HDCP. i.MX6 CPU's HDMI TX PHY output is directly connected to SODIMM Edge connector HDMI port. Also i.MX6 CPU supports HDMI Hot plug detect & HDMI CEC and connected to SODIMM Edge pins 25 & 10 correspondingly.

i.MX6 CPU's I2C1 interface on SODIMM edge can be used as HDMI DDC interface. When HDCP is enabled, a dedicated I2C controlled by the HDMI PHY should be used to exchange the HDCP encryption key & must sync several times per second (not like a common I2C) and so i.MX6 I2C1 interface pins should be configured as HDMI_DDC.

Make sure to use suitable level shifter and driver to interface the I2C with the HDMI monitor since i.MX6 CPU's I2C cannot operate at the 5 V required by HDMI EDID. In addition, ESD protection must be used on all HDMI single-ended and differential signals mounted near the HDMI connector. CM2020 from ON semiconductor or similar part could be considered for ESD protection and I2C level conversion.

For more details, refer SODIMM Edge connector pins 18, 19, 21, 22, 23, 24, 25, 26, 28, 29, & 31 on ***Table 5.***

Note: Customers who develop products using HDMI need to work with DCP (http://www.digital-cp.com/licensing) to get the HDCP license and related device keys.

Note: i.MX6 Duallite and i.MX6 Solo CPU supports only one IPU and so at any time only two display interfaces (including LVDS, HDMI & Parallel RGB) can be supported.

2.6.12I2S Audio Interface

i.MX6 SODIMM SOM supports one I2S/SSI audio interface port on SODIMM Edge connector. i.MX6 CPU's AUDMUX4 port is used for audio interface which provides a programmable interconnect device for voice, audio and synchronous data routing between i.MX6 CPU's SSI Controller and external audio/voice codec's (also known as coder-decoders). i.MX6 CPU's SSI controller can be configured as AC'97 mode or I2S mode. I2S mode supports sampling rate from 8KHz to 196KHz.

For more details, refer SODIMM Edge connector pins 61, 64, 67, 89 & 90 on ***Table 5.***

Note: If AUDMUX4 interface is not required on SODIMM edge, the same pins can be configured as uSDHC2 interface.

2.6.13 UART Interface

i.MX6 SODIMM SOM supports four UART interface on SODIMM Edge connector in which one for Debug UART interface and other three for Data UART interface. i.MX6 CPU's UART2 controller is used for Debug UART interface and UART1, UART4 & UART5 controller is used for Data UART interface on SODIMM Edge connector. Also i.MX6 SODIMM SOM supports hardware flow control for request to send and clear to send signals on UART1, UART4 & UART5 interface.

i.MX6 CPU UART controller supports Serial RS-232NRZ mode, 9-bit RS-485 mode and IrDA mode. It is compatible with High-speed TIA/EIA-232-F (up to 5.0 Mbit/s) with auto baud rate detection (up to 115.2 Kbit/s). It supports 7 or 8 data bits for RS-232 characters (9-bit RS-485 format), 1 or 2 stop bits and programmable parity (even, odd, and no parity).

For more details, refer SODIMM Edge connector pins 117 & 118 for Debug UART, pins 7, 9, 97 & 94 for UART1 interface, pins 98, 99, 100 & 101 for UART4 interface, and pins 38, 75, 102 & 103 for UART5 interface on ***Table 5.***

Note: If Parallel camera interface is used on SODIMM edge, then UART4 & UART5 cannot be used with hardware flow control for request to send and clear to send signals.

2.6.14 SPI Interface

i.MX6 SODIMM SOM supports one SPI interface with three chip selects on SODIMM Edge connector. i.MX6 CPU's eCSPI2 is used for SPI interface which supports full-duplex synchronous four-wire serial interface with DMA. It supports 32bit x 64 entry FIFO for both transmit and receive data. It can be configured as Master or Slave. Also polarity and phase of the Chip Select and SPI Clock are configurable.

For more details, refer SODIMM Edge connector pins 62, 63, 66, 70, 71 & 110 on ***Table 5.***

Note: If Parallel camera is used with 12bit interface on SODIMM edge, then eCSPI2 interface cannot be used.

Note: If SDIO card detect is not used on SODIMM Edge connector pin 105, the same pin can be used as fourth chip select of eCSPI2 interface (eCSPI2_SS3(EIM_D25)).

2.6.15 CAN Interface

i.MX6 SODIMM SOM supports two CAN interface on SODIMM Edge connector. i.MX6 CPU's FLEXCAN1 & FLEXCAN2 module is used for CAN interface which supports CAN protocol according to the CAN 2.0B protocol specification. It supports programmable bit rate up to 1 Mb/sec with both standard and extended message frames. Also it supports 64 Message Buffers. To connect external CAN module to this bus, it is necessary to add transceiver in between.

For more details, refer SODIMM Edge connector pins 175, 176, 177 & 178 on ***Table 5.***

2.6.16I2C Interface

i.MX6 SODIMM SOM supports two I2C interface on SODIMM Edge connector. i.MX6 CPU's I2C1 and I2C3.channels are used for general purpose I2C interface which is compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps.

Since flexible I2C standard allows multiple devices to be connected to the single bus, i.MX6 CPU's I2C1 and I2C3 can be connected to more than one device on the carrier board. I2C1 interface is also connected to On-SOM PMIC with I2C address 0x08 in the i.MX6 SODIMM SOM.

For more details, refer SODIMM Edge connector pins 18 & 19 for I2C1, pins 115 & 116 for I2C3 on ***Table 5.***

2.6.17PWM Interface

i.MX6 SODIMM SOM supports four PWM interface on SODIMM Edge connector. i.MX6 CPU's PWM1 PWM2, PWM3 and PWM4 module are used for PWM interface which has a 16-bit counter and optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4 x 16 data FIFO.

For more details, refer SODIMM Edge connector pins 125, 138, 141, & 147 on ***Table 5.***

2.6.18GPIO Interface

Most of the i.MX6 CPU Pins which are connected to SODIMM Edge connector can be configured as GPIO with interrupt capable (if not used as other interface). i.MX6 CPU GPIO controller provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce Core interrupts.

2.6.19JTAG Interface

i.MX6 SODIMM SOM supports one JTAG interface on SODIMM Edge Connector. i.MX6 CPU implements JTAG Security modes internal to System JTAG Controller. The System JTAG Controller provides debug and test control with the maximum security. The test access port is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG). The SJC module of the processor provides the bridge between external development and test instrumentation and the internal JTAG-accessible debug and test resources.

For more details, refer SODIMM Edge connector pins 191, 193, 195, 197 & 199 on ***Table 5.***

2.6.20 Power Input

i.MX6 SODIMM SOM works with single 3.3V power input (VIN_3V3) from SODIMM Edge connector and generates all other required powers internally On-SOM itself. i.MX6 SODIMM SOM uses VRTC_3V0 coin cell power input from SODIMM Edge connector to i.MX6 CPU's RTC controller for real time clock (when VIN_3V3 is off).

For more details, refer SODIMM Edge connector pins 20, 32, 46, 60, 72, 88, 106, 124, 142, 160, 180 & 192 for 3.3V power input (VIN_3V3) and pin 183 for VRTC_3V0 on ***Table 5.***

2.6.21 Reset Button Input

i.MX6 SODIMM SOM supports reset button input on SODIMM Edge connector. Reset button input from SODIMM Edge connector is the active low signal which is connected to i.MX6 CPU's POR pin in i.MX6 SODIMM SOM. This pin can be used to reset the i.MX6 CPU by connecting push button in the carrier board.

For more details, refer SODIMM Edge connector pin 187 on ***Table 5***.

2.6.22 Power Button Input

i.MX6 SODIMM SOM supports PWRBTN# input from Edge connector which is the active low signal and connected to i.MX6 CPU's ONOFF pin. This pin can be used to On/Off the i.MX6 CPU by connecting push button in the carrier board. When the board power is On, a button press between 750ms to 5s will send an interrupt to core to request software to bring down the i.MX6 safely (if software supports). Otherwise, button press greater than 5s results in a direct hardware power down which is applicable when software is unable to power Off the device. When the i.MX6 CPU power supply is Off, a button press greater in duration than 750ms asserts an output signal to request power from a power IC to power up the i.MX6 CPU.

For more details, refer SODIMM Edge connector pin 196 on ***Table 5***.

Table 5: 200-Pin PCB Edge Connector Pin Assignment

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	NA	Power	Ground.
2	GPHY_ATXRXM	NA	IO, DIFF	Ethernet transmit differential pair 0 negative.
3	VDVDH_GPHY	NA	-	NC.
4	GPHY_ATXRXP	NA	IO, DIFF	Ethernet transmit differential pair 0 positive.
5	GND	NA	Power	Ground.
6	GPHY_BTXRXM	NA	IO, DIFF	Ethernet receive differential pair 1 negative.
7	UART1_RXD(SD3_DAT6)	SD3_DAT6/ E13	I, 3.3V CMOS	UART1 serial data receiver.
8	GPHY_BTXRXP	NA	IO, DIFF	Ethernet receive differential pair 1 positive.
9	UART1_TXD(SD3_DAT7)	SD3_DAT7/ F13	O, 3.3V CMOS	UART1 serial data transmitter.
10	GPIO1_IO21(SD1_DAT3)	SD1_DAT3/ F18	IO, 3.3V CMOS	General Purpose Input/Output.
11	GPHY_LINK_LED2	NA	O, 3.3V CMOS	Ethernet link status LED.
12	GPHY_ACTIVITY_LED1	NA	O, 3.3V CMOS	Ethernet speed status LED.
13	GND	NA	Power	Ground.
14	GPHY_CTXRXM	NA	IO, DIFF	Ethernet receive differential pair 2 negative.
15	GPHY_DTXRXM	NA	IO, DIFF	Ethernet receive differential pair 3 negative.
16	GPHY_CTXRXP	NA	IO, DIFF	Ethernet receive differential pair 2 positive.
17	GPHY_DTXRXP	NA	IO, DIFF	Ethernet receive differential pair 3 positive.
18	I2C1_SCL(EIM_D21)	EIM_D21/ H20	O, 3.3V OD/ 4.7K PU	I2C1 Clock signal. *Note: I2C1_SCL(EIM_D21) is also connected to On-SOM PMIC.*
19	I2C1_SDA(EIM_D28)	EIM_D28/ G23	IO, 3.3V OD/ 4.7K PU	I2C1 Data signal. *Note: I2C1_SDA(EIM_D28) is also connected to On-SOM PMIC.*
20	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
21	HDMI_D0P	HDMI_D0P/ K6	O, TMDS	HDMI differential data lane 0 positive.
22	HDMI_D1P	HDMI_D1P/ J4	O, TMDS	HDMI differential data lane 1 positive.
23	HDMI_D0M	HDMI_D0M/ K5	O, TMDS	HDMI differential data lane 0 negative.
24	HDMI_D1M	HDMI_D1M/ J3	O, TMDS	HDMI differential data lane 1 negative.
25	HDMI_HPD	HDMI_HPD/ K1	I, 3.3V CMOS	HDMI Hot plug detect.
26	HDMI_D2P	HDMI_D2P/ K4	O, TMDS	HDMI differential data lane 2 positive.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
27	GND	NA	Power	Ground.
28	HDMI_D2M	HDMI_D2M/ K3	O, TMDS	HDMI differential data lane 2 negative.
29	HDMI_CLKP	HDMI_CLKP/ J6	O, TMDS	HDMI differential clock positive.
30	GPIO2_IO03(NANDF_D3)	NANDF_D3/ D17	IO, 3.3V CMOS	General Purpose Input/Output.
31	HDMI_CLKM	HDMI_CLKM/ J5	O, TMDS	HDMI differential clock negative.
32	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
33	GPIO6_IO09(NANDF_WP_B)	NANDF_WP_B/ E15	IO, 3.3V CMOS	General Purpose Input/Output.
34	GPIO2_IO06(NANDF_D6)	NANDF_D6/ E17	IO, 3.3V CMOS	General Purpose Input/Output.
35	GPIO5_IO02(EIM_A25)	EIM_A25/ H19	IO, 3.3V CMOS	General Purpose Input/Output.
36	GPIO6_IO11(NANDF_CS0)	NANDF_CS0/ F15	IO, 3.3V CMOS	General Purpose Input/Output.
37	GPIO2_IO02(NANDF_D2)	NANDF_D2/ F16	IO, 3.3V CMOS	General Purpose Input/Output.
38	UART5_RTS_B(CSI0_DAT18)	CSI0_DAT18/ M6	I, 3.3V CMOS	Parallel camera data 6.
39	USB_H1_OC(EIM_D30)	EIM_D30/ J20	I, 3.3V CMOS	Over current sense for USB Host Port 1.
40	GND	NA	Power	Ground.
41	GND	NA	Power	Ground.
42	GPIO1_IO20(SD1_CLK)	SD1_CLK/ D20	IO, 3.3V CMOS	General Purpose Input/Output.
43	GPIO2_IO04(NANDF_D4)	NANDF_D4/ A19	IO, 3.3V CMOS	General Purpose Input/Output.
44	GPIO6_IO07(NANDF_CLE)	NANDF_CLE/ C15	IO, 3.3V CMOS	General Purpose Input/Output.
45	GPIO1_IO16(SD1_DAT0)	SD1_DAT0/ A21	IO, 3.3V CMOS	General Purpose Input/Output.
46	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
47	GPIO6_IO08(NANDF_ALE)	NANDF_ALE/ A16	IO, 3.3V CMOS	General Purpose Input/Output. *Note: Same signal is optionally connected to Reset input of On-SOM eMMC through resistor and default not populated.*
48	LVDS0_TX0_N	LVDS0_TX0_N/ U2	O, 2.5V LVDS	LVDS primary channel differential pair 0 negative.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
49	GPIO2_IO01(NANDF_D1)	NANDF_D1/ C17	IO, 3.3V CMOS	General Purpose Input/Output.
50	LVDS0_TX0_P	NALVDS0_TX0_P/ U1	O, 2.5V LVDS	LVDS primary channel differential pair 0 positive.
51	GND	NA	Power	Ground.
52	LVDS0_TX1_N	LVDS0_TX1_N/ U4	O, 2.5V LVDS	LVDS primary channel differential pair 1 negative.
53	LVDS0_TX2_N	LVDS0_TX2_N/ V2	O, 2.5V LVDS	LVDS primary channel differential pair 2 negative.
54	LVDS0_TX1_P	LVDS0_TX1_P/ U3	O, 2.5V LVDS	LVDS primary channel differential pair 1 positive.
55	LVDS0_TX2_P	LVDS0_TX2_P/ V1	O, 2.5V LVDS	LVDS primary channel differential pair2 positive.
56	LVDS0_TX3_N	LVDS0_TX3_N/ W2	O, 2.5V LVDS	LVDS primary channel differential pair 3 negative.
57	LVDS0_CLK_N	LVDS0_CLK_N/ V4	O, 2.5V LVDS	LVDS primary channel differential clock negative.
58	LVDS0_TX3_P	LVDS0_TX3_P/ W1	O, 2.5V LVDS	LVDS primary channel differential pair 3 positive.
59	LVDS0_CLK_P	LVDS0_CLK_P/ V3	O, 2.5V LVDS	LVDS primary channel differential clock positive.
60	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
61	AUD4_RXD(SD2_DAT0)	SD2_DAT0/ A22	I, 3.3V CMOS	Audio receive data.
62	eCSPI2_SS1(EIM_LBA)	EIM_LBA/ K22	O, 3.3V CMOS/ 10K PD	SPI2 chip select 1. *Important Note: This signal is also used for i.MX6 CPU bootstrap setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to this pin which will change the boot configuration.*
63	eCSPI2_MISO(CSI0_DAT10)	CSI0_DAT10/ M1	I, 3.3V CMOS	SPI2 Master Input Slave Output.
64	CCM_CLKO1(GPIO_19)	GPIO_19/ P5	O, 3.3V CMOS	Observability clock 1 output.
65	GND	NA	Power	Ground.
66	eCSPI2_SCLK(CSI0_DAT8)	CSI0_DAT8/ N6	O, 3.3V CMOS	SPI2 clock signal.
67	AUD4_TXD(SD2_DAT2)	SD2_DAT2/ A23	O, 3.3V CMOS	Audio Transmit data.
68	GPIO6_IO10(NANDF_RB0)	NANDF_RB0/ B16	IO, 3.3V CMOS	General Purpose Input/Output.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
69	GPIO6_IO14(NANDF_CS1)	NANDF_CS1/ C16	IO, 3.3V CMOS	General Purpose Input/Output.
70	eCSPI2_MOSI(CSI0_DAT9)	CSI0_DAT9/ N5	O, 3.3V CMOS	SPI2 Master Output Slave Input.
71	eCSPI2_SS2(EIM_D24)	EIM_D24/ F22	O, 3.3V CMOS	SPI2 Chip select signal.
72	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
73	GPIO2_IO00(NANDF_D0)	NANDF_D0/ A18	IO, 3.3V CMOS	General Purpose Input/Output.
74	USB_OTG_CHD_B	USB_OTG_CHD_B B8	O, 3.3V CMOS	USB Charge Detect.
75	UART5_CTS_B(CSI0_DAT19)	CSI0_DAT19/ L6	I, 3.3V CMOS	Parallel camera0 data 7.
76	GPIO2_IO05(NANDF_D5)	NANDF_D5/ B18	IO, 3.3V CMOS	General Purpose Input/Output.
77	USBOTG_ID(GPIO_1)	GPIO_1/ T4	I, 3.3V CMOS	USB OTG ID to identify Host & Device.
78	GPIO2_IO07(NANDF_D7)	NANDF_D7/ C18	IO, 3.3V CMOS	General Purpose Input/Output.
79	GND	NA	Power	Ground.
80	GPIO4_IO20(DI0_PIN4)	DI0_PIN4/ P25	IO, 3.3V CMOS	General Purpose Input/Output.
81	USB_OTG_DP	USB_OTG_DP/ A6	IO, DIFF	USB OTG data positive.
82	SATA_TXP	SATA_TXP/ A12	O, DIFF/ 0.01uF AC coupled	SATA0 transmit output differential positive.
83	USB_OTG_DN	USB_OTG_DN/ B6	IO, DIFF	USB OTG data negative.
84	SATA_TXM	SATA_TXM/ B12	O, DIFF/ 0.01uF AC coupled	SATA0 transmit output differential negative.
85	SATA_RXP	SATA_RXP/ B14	I, DIFF/ 0.01uF AC coupled	SATA0 receive input differential positive.
86	GPIO6_IO31(EIM_BCLK)	EIM_BCLK/ N22	IO, 3.3V CMOS	General Purpose Input/Output.
87	SATA_RXM	SATA_RXM/ A14	I, DIFF/ 0.01uF AC coupled	SATA0 receive input differential negative.
88	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
89	AUD4_TXFS(SD2_DAT1)	SD2_DAT1/ E20	O, 3.3V CMO	Audio transmit frame synchronization.
90	AUD4_TXC(SD2_DAT3)	SD2_DAT3/ B22	O, 3.3V CMOS	Audio transmit clock.
91	AUD4_RXC(SD2_CMD)	SD2_CMD/ F19	I, 3.3V CMOS	Audio receive clock.
92	AUD4_RXFS(SD2_CLK)	SD2_CLK/ C21	I, 3.3V CMOS	Audio receive frame synchronization.
93	GPIO6_IO01(CSI0_DAT15)	CSI0_DAT15/ M5	I, 3.3V CMOS	Parallel camera0 data 3.
94	UART1_RTS_B(EIM_D20)	EIM_D20/ G20	I, 3.3V CMOS	UART1 ready to send data.
95	GND	NA	Power	Ground.
96	GPIO6_IO00(CSI0_DAT14)	CSI0_DAT14/ M4	I, 3.3V CMOS	Parallel camera0 data 2.
97	UART1_CTS_B(EIM_D19)	EIM_D19/ G21	O, 3.3V CMOS	UART1 clear to send data.
98	UART4_TXD(KEY_COL0)	KEY_COL0/ W5	O, 3.3V CMOS	UART4 serial data transmitter.
99	UART4_RXD(KEY_ROW0)	KEY_ROW0/ V6	I, 3.3V CMOS	UART4 serial data receiver.
100	UART4_CTS_B(CSI0_DAT17)	CSI0_DAT17/ L3	I, 3.3V CMOS	Parallel camera0 data 5.
101	UART4_RTS_B(CSI0_DAT16)	CSI0_DAT16/ L4	I, 3.3V CMOS	Parallel camera0 data 4.
102	UART5_TXD(KEY_COL1)	KEY_COL1/ U7	O, 3.3V CMOS	UART5 serial data transmitter.
103	UART5_RXD(KEY_ROW1)	KEY_ROW1/ U6	I, 3.3V CMOS	UART5 serial data receiver.
104	GPIO5_IO31(CSI0_DAT13)	CSI0_DAT13/ L1	I, 3.3V CMOS	Parallel camera0 data 1.
105	eCSPI2_SS3(EIM_D25)	EIM_D25/ G22	O, 3.3V CMOS	General Purpose Input/Output. Assigned for SD3 Card detect.
106	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
107	SD3_DAT0	SD3_DAT0/ E14	IO, 3.3V CMOS	SD3 Data0.
108	SD3_CMD	SD3_CMD/ B13	IO, 3.3V CMOS	SD3 command.
109	SD3_CLK	SD3_CLK/ D14	O, 3.3V CMOS	SD3 clock.
110	eCSPI2_SS0(CSI0_DAT11)	CSI0_DAT11/ M3	O, 3.3V CMOS	SPI2 Chip select 2.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
111	SD3_DAT1	SD3_DAT1/ F14	IO, 3.3V CMOS	SD3 Data1.
112	SD3_DAT2	SD3_DAT2/ A15	IO, 3.3V CMOS	SD3 Data2.
113	GND	NA	Power	Ground.
114	SD3_DAT3	SD3_DAT3/ B15	IO, 3.3V CMOS	SD3 Data3.
115	I2C3_SDA(GPIO_6)	GPIO_6/ T3	IO, 3.3V OD/ 4.7K PU	I2C3 data.
116	I2C3_SCL(GPIO_3)	GPIO_3/ R7	O, 3.3V OD/ 4.7K PU	I2C3 clock.
117	UART2_RXD(EIM_D27)	EIM_D27/ E25	I, 3.3V CMOS	UART2 serial data receiver.
118	UART2_TXD(EIM_D26)	EIM_D26/ E24	O, 3.3V CMOS	UART2 serial data transmitter.
119	GPIO5_IO18(CSI0_PIXCLK)	CSI0_PIXCLK/ P1	I, 3.3V CMOS	Parallel camera0 PIXCLK.
120	GPIO5_IO30(CSI0_DAT12)	CSI0_DAT12/ M2	I, 3.3V CMOS	Parallel camera0 data 0.
121	GPIO5_IO21(CSI0_VSYNC)	CSI0_VSYNC/ N2	I, 3.3V CMOS	Parallel camera0 VSYNC.
122	GPIO7_IO13(GPIO_18)	GPIO_18/ P6	IO, 3.3V CMOS	General Purpose Input/Output.
123	GPIO5_IO19(CSI0_MCLK)	CSI0_MCLK/ P4	I, 3.3V CMOS	Parallel Camera0 HSYNC.
124	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
125	PWM2_OUT(SD1_DAT2)	SD1_DAT2/ E19	O, 3.3V CMOS	Pulse Width Modulation 2 Output.
126	GPIO5_IO20(CSI0_DATA_EN)	CSI0_DATA_EN/ P3	I, 3.3V CMOS	Parallel Camera0 Data Enable.
127	PCIE_TXP	PCIE_TXP/ B3	O, DIFF/ 0.1uf AC coupled	PCIe differential transmit line positive.
128	PCIE_RXP	PCIE_RXP/ B2	O, DIFF	PCIe differential receive line positive
129	PCIE_TXM	PCIE_TXM/ A3	O, DIFF/ 0.1uf AC coupled	PCIe differential transmit line negative.
130	PCIE_RXM	PCIE_RXM/ B1	O, DIFF	PCIe differential receive line negative.
131	GND	NA	Power	Ground.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
132	GPIO7_IO11(GPIO_16)	GPIO_16/ R2	O, 3.3V CMOS	General Purpose Input/Output. Assigned for PCIe RESET.
133	GPIO7_IO12(GPIO_17)	GPIO_17/ R1	IO, 3.3V CMOS	General Purpose Input/Output.
134	GPIO1_IO02(GPIO_2)	GPIO_2/ T1	I, 3.3V CMOS	General Purpose Input/Output. Assigned for PCIe WAKE.
135	PCIE_REFCLK_DP(CLK1_P)	CLK1_P/ D7	O, DIFF	PCIe differential reference clock positive.
136	GPIO4_IO13(KEY_ROW3)	KEY_ROW3/ T7	IO, 3.3V CMOS	General Purpose Input/Output.
137	PCIE_REFCLK_DM(CLK1_N)	CLK1_N/ C7	O, DIFF	PCIe differential reference clock negative.
138	PWM1_OUT(GPIO_9)	GPIO_9/ T2	O, 3.3V CMOS	Pulse Width Modulation 1 Output.
139	GPIO4_IO12(KEY_COL3)	KEY_COL3/ U5	IO, 3.3V CMOS	General Purpose Input/Output.
140	USB_H1_PWR(GPIO_0)	GPIO_0/ T5	O, 3.3V CMOS	General Purpose Input/Output. Assigned for USB Host1 Power enable signal to control USB Host1 VBUS voltage.
141	PWM4_OUT(SD1_CMD)	SD1_CMD/ B21	O, 3.3V CMOS	Pulse Width Modulation 4 Output.
142	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
143	DI0_PIN3	DI0_PIN3/ N20	O, 3.3V CMOS	Parallel LCD VSYNC.
144	DI0_PIN2	DI0_PIN2/ N25	O, 3.3V CMOS	Parallel LCD HSYNC.
145	DI0_DISP_CLK	DI0_DISP_CLK/ N19	O, 3.3V CMOS	Parallel LCD Clock.
146	DI0_PIN15	DI0_PIN15/ N21	O, 3.3V CMOS	Parallel LCD Enable.
147	PWM3_OUT(SD1_DAT1)	SD1_DAT1/ C20	O, 3.3V CMOS	Pulse Width Modulation 3 Output.
148	DISP0_DAT16	DISP0_DAT16/ T21	O, 3.3V CMOS	Parallel LCD data 16 (Red data0).
149	DISP0_DAT17	DISP0_DAT17/ U24	O, 3.3V CMOS	Parallel LCD data 17 (Red data1).
150	DISP0_DAT18	DISP0_DAT18/ V25	O, 3.3V CMOS	Parallel LCD data 18 (Red data2).
151	GND	NA	Power	Ground.
152	DISP0_DAT19	DISP0_DAT19/ U23	O, 3.3V CMOS	Parallel LCD data 19 (Red data3).

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
153	DISP0_DAT20	DISP0_DAT20/ U22	O, 3.3V CMOS	Parallel LCD data 20 (Red data4).
154	DISP0_DAT21	DISP0_DAT21/ T20	O, 3.3V CMOS	Parallel LCD data 21 (Red data5).
155	DISP0_DAT22	DISP0_DAT22/ V24	O, 3.3V CMOS	Parallel LCD data 22 (Red data6).
156	DISP0_DAT23	DISP0_DAT23/ W24	O, 3.3V CMOS	Parallel LCD data 23 (Red data7).
157	DISP0_DAT8	DISP0_DAT8/ R22	O, 3.3V CMOS	Parallel LCD data 8 (Green data0).
158	DISP0_DAT9	DISP0_DAT9/ T25	O, 3.3V CMOS	Parallel LCD data 9 (Green data1).
159	DISP0_DAT10	DISP0_DAT10/ R21	O, 3.3V CMOS	Parallel LCD data 10 (Green data2).
160	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
161	DISP0_DAT11	DISP0_DAT11/ T23	O, 3.3V CMOS	Parallel LCD data 11 (Green data3).
162	DISP0_DAT12	DISP0_DAT12/ T24	O, 3.3V CMOS	Parallel LCD data 12 (Green data4).
163	DISP0_DAT13	DISP0_DAT13/ R20	O, 3.3V CMOS	Parallel LCD data 13 (Green data5).
164	DISP0_DAT14	DISP0_DAT14/ U25	O, 3.3V CMOS	Parallel LCD data 14 (Green data6).
165	DISP0_DAT15	DISP0_DAT15/ T22	O, 3.3V CMOS	Parallel LCD data 15 (Green data7).
166	DISP0_DAT0	DISP0_DAT0/ P24	O, 3.3V CMOS/	Parallel LCD data 0 (Blue data0).
167	DISP0_DAT1	DISP0_DAT1/ P22	O, 3.3V CMOS	Parallel LCD data 1 (Blue data1).
168	DISP0_DAT2	DISP0_DAT2/ P23	O, 3.3V CMOS	Parallel LCD data 2 (Blue data2).
169	GND	NA	Power	Ground.
170	DISP0_DAT3	DISP0_DAT3/ P21	O, 3.3V CMOS	Parallel LCD data 3 (Blue data3).
171	DISP0_DAT4	DISP0_DAT4/ P20	O, 3.3V CMOS	Parallel LCD data 4 (Blue data4).
172	DISP0_DAT5	DISP0_DAT5/ R25	O, 3.3V CMOS/	Parallel LCD data 5 (Blue data5).
173	DISP0_DAT6	DISP0_DAT6/ R23	O, 3.3V CMOS	Parallel LCD data 6 (Blue data6).
174	DISP0_DAT7	DISP0_DAT7/ R24	O, 3.3V CMOS	Parallel LCD data 7 (Blue data7).

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
175	CAN2_RX(KEY_ROW4)	KEY_ROW4/ V5	I, 3.3V CMOS	Receive input for CAN2 bus.
176	CAN1_RX(GPIO_8)	GPIO_8/ R5	I, 3.3V CMOS	Receive input for CAN1 bus.
177	CAN2_TX(KEY_COL4)	KEY_COL4/ T6	O, 3.3V CMOS	Transmit output for CAN2 bus.
178	CAN1_TX(GPIO_7)	GPIO_7/ R3	O, 3.3V CMOS	Transmit output for CAN1 bus.
179	GPIO4_IO10(KEY_COL2)	KEY_COL2/ W6	IO, 3V CMOS	General Purpose Input/Output. *Note: KEY_COL2 is connected to this pin through resistor and default populated. KEY_COL2 is also connected to Edge connector pin196 through resistor and default not populated.* *Note: CPU_ON_OFF is connected to this pin through resistor and default not populated. CPU_ON_OFF is also connected to Edge connector pin196 through resistor and default populated.*
180	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
181	GPIO4_IO11(KEY_ROW2)	KEY_ROW2/ W4	IO, 3V CMOS	General Purpose Input/Output.
182	BOOT_MODE0	BOOT_MODE0/ C12	I, 3.3V CMOS/ 4.7K PU	Boot Mode Select bit0. *Important Note: This pin is directly connected to i.MX6 CPU's BOOT_MODE0 pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin. Make sure to use this pin in carrier board to select desired boot mode by driving only low if required.*
183	VRTC_3V0	NA	I, 3V Power	3V backup coin cell input for RTC.
184	BOOT_MODE1	BOOT_MODE1/ F12	I, 3.3V CMOS/ 4.7K PU	Boot Mode Select bit1. *Important Note: This pin is directly connected to i.MX6 CPU's BOOT_MODE1 pin with On-SOM pullup and so don't add any external pullup in carrier board on this pin. Make sure to use this pin in carrier board to select desired boot mode by driving only low if required.*
185	GND	NA	Power	Ground.
186	GND	NA	Power	Ground.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
187	n_RST_OUT	POR_B/ C11	I, 3V CMOS/ 10K PU	Active low reset button input. *Important Note: This reset input is connected to i.MX6 CPU's POR input with On-SOM pullup and so don't add any external pullup in carrier board on this pin.* *Note: NANDF_CS3 is optionally connected to this pin through resistor and default not populated.*
188	USB_H1_DP	USB_H1_DP/ E10	IO, DIFF	USB Host Port 1 data positive.
189	GPIO1_IO04_BRD_CFG2(GPIO_4)	GPIO_4/ R6	IO, 3.3V CMOS	General Purpose Input/Output. *Note: GPIO_4 is connected to this pin through resistor and default populated.*
190	USB_H1_DN	USB_H1_DN/ F10	IO, DIFF	USB Host Port 1 data negative.
191	JTAG_TDO	JTAG_TDO/ G6	O, 3.3V CMOS	JTAG Test Data Output.
192	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
193	JTAG_TRSTB	JTAG_TRSTB/ C2	I, 3.3V CMOS	JTAG Test Reset.
194	GPIO1_IO05_BRD_CFG3(GPIO_5)	GPIO_5/ R4	IO, 3.3V CMOS	General Purpose Input/Output. *Note: GPIO_5 is connected to this pin through resistor and default populated.*
195	JTAG_TDI	JTAG_TDI/ G5	I, 3.3V CMOS	JTAG Test Data Input.
196	CPU_ON_OFF	ONOFF/ D12	I, 3.3V CMOS	CPU_ON_OFF signal. *Note: CPU_ON_OFF is connected to this pin through resistor and default populated. CPU_ON_OFF is also connected to Edge connector pin179 through resistor and default not populated.* *Note: ENET_RX_ER is connected to this pin through resistor and default not populated.* *Note: KEY_COL2 is connected to this pin through resistor and default not populated. KEY_COL2 is also connected to Edge connector pin179 through resistor and default populated.*
197	JTAG_TCK	JTAG_TCK/ H5	I, 3.3V CMOS	JTAG Test Clock.
198	GND	NA	Power	Ground.

Pin No.	SODIMM Edge Connector Pin Name	i.MX6 Ball Name/ Pin Number	Signal Type/ Termination	Description
199	JTAG_TMS	JTAG_TMS/ C3	I, 3.3V CMOS	JTAG Test Mode Select.
200	VBUS_5V	USB_OTG_VBUS/ E9 & USB_H1_VBUS/ D10	I, Power 5V	USB VBUS Power. *Important Note: Recommended to connect always available 5V power on this pin in carrier board.*

2.7 i.MX6 Pin Multiplexing on SODIMM Edge

The i.MX6 CPU's IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of the i.MX6 CPU's IO pins can be configured as GPIO if required. The below table provides the details of i.MX6 CPU pin connections to the SOM edge connector with selected pin function and available alternate functions. This table has been prepared by referring NXP's i.MX6 Applications Processor Reference Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the i.MX6 SOIDMM SOM Edge connector for iWave's BSP reusability and to have compatible SODIMM modules in future for upgradability.

Table 6: IOMUX Configuration of i.MX6 SODIMM SOM Edge Connector interfaces

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
Control Signals	182	BOOT_MODE0											SRC_BOOT_MODE0
	184	BOOT_MODE1											SRC_BOOT_MODE1
	187	POR_B											SRC_POR_B
SD	107	SD3_DAT0	SD3_DATA0	UART1_CTS_B	FLEXCAN2_TX			GPIO7_IO04					GPIO7_IO04
	111	SD3_DAT1	SD3_DATA1	UART1_RTS_B	FLEXCAN2_RX			GPIO7_IO05					GPIO7_IO05
	112	SD3_DAT2	SD3_DATA2					GPIO7_IO06					GPIO7_IO06
	114	SD3_DAT3	SD3_DATA3	UART3_CTS_B				GPIO7_IO07					GPIO7_IO07
	108	SD3_CMD	SD3_CMD	UART2_CTS_B	FLEXCAN1_TX			GPIO7_IO02					GPIO7_IO02
	109	SD3_CLK	SD3_CLK	UART2_RTS_B	FLEXCAN1_RX			GPIO7_IO03					GPIO7_IO03
	105	EIM_D25	EIM_DATA25	ECSPI4_SS3	UART3_RX_DATA	ECSPI1_SS3	ECSPI2_SS3	GPIO3_IO25	AUD5_RXC	UART1_DSR_B	EPDC_SDCE8		GPIO3_IO25

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
PCIe	128	PCIE_RXP											PCIE_RX_P
	130	PCIE_RXM											PCIE_RX_N
	127	PCIE_TXP											PCIE_TX_P
	129	PCIE_TXM											PCIE_TX_N
	135	CLK1_P											XTALOSC_CLK1_P
	137	CLK1_N											XTALOSC_CLK1_N
	134	GPIO_2	ESAI_TX_FS		KEY_ROW6			GPIO1_IO02	SD2_WP	MLB_DATA			GPIO1_IO02
	133	GPIO_17	ESAI_TX0	ENET_1588_EVENT3_IN	CCM_PMIC_READY	SDMA_EXT_EVENT0	SPDIF_OUT	GPIO7_IO12					GPIO7_IO12
SATA	82	SATA_TXP											SATA_PHY_TX_P
	84	SATA_TXM											SATA_PHY_TX_N
	85	SATA_RXP											SATA_PHY_RX_P
	87	SATA_RXM											ATA_PHY_RX_N
USB OTG2.0	74	USB_OTG_CHD_B											USB_OTG_CHD_B
	77	GPIO_1	ESAI_RX_CLK	WDOG2_B	KEY_ROW5	USB_OTG_ID	PWM2_OUT	GPIO1_IO01	SD1_CD_B				GPIO1_IO01
	81	USB_OTG_DP											USB_OTG_DP
	83	USB_OTG_DN											USB_OTG_DN

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
USB2.0 Host	39	EIM_D30	EIM_DATA30	IPU1_DISP1_DATA21	IPU1_DI0_PIN11	IPU1_CSI0_DATA03	UART3_CTS_B	GPIO3_IO30	USB_H1_OC		EPDC_SDOEZ		GPIO3_IO30
	140	GPIO_0	CCM_CLKO1		KEY_COL5	ASRC_EXT_CLK	EPIT1_OUT	GPIO1_IO00	USB_H1_PWR	SNVS_VIO_5			GPIO1_IO00
	188	USB_H1_DP											USB_H1_DP
	190	USB_H1_DN											USB_H1_DN
Camera	120	CSI0_DAT12	IPU1_CSI0_DATA12	EIM_DATA08		UART4_TX_DATA		GPIO5_IO30		ARM_TRACE09			GPIO5_IO30
	104	CSI0_DAT13	IPU1_CSI0_DATA13	EIM_DATA09		UART4_RX_DATA		GPIO5_IO31		ARM_TRACE10			GPIO5_IO31
	96	CSI0_DAT14	IPU1_CSI0_DATA14	EIM_DATA10		UART5_TX_DATA		GPIO6_IO00		ARM_TRACE11			GPIO6_IO00
	93	CSI0_DAT15	IPU1_CSI0_DATA15	EIM_DATA11		UART5_RX_DATA		GPIO6_IO01		ARM_TRACE12			GPIO6_IO01
	101	CSI0_DAT16	IPU1_CSI0_DATA16	EIM_DATA12		UART4_RTS_B		GPIO6_IO02		ARM_TRACE13			GPIO6_IO02
	100	CSI0_DAT17	IPU1_CSI0_DATA17	EIM_DATA13		UART4_CTS_B		GPIO6_IO03		ARM_TRACE14			GPIO6_IO03
	38	CSI0_DAT18	IPU1_CSI0_DATA18	EIM_DATA14		UART5_RTS_B		GPIO6_IO04		ARM_TRACE15			GPIO6_IO04
	75	CSI0_DAT19	IPU1_CSI0_DATA19	EIM_DATA15		UART5_CTS_B		GPIO6_IO05					GPIO6_IO05
	119	CSI0_PIXCLK	IPU1_CSI0_PIXCLK					GPIO5_IO18		ARM_EVENTO			GPIO5_IO18
	123	CSI0_MCLK	IPU1_CSI0_HSYNC			CCM_CLKO1		GPIO5_IO19		ARM_TRACE_CTL			GPIO5_IO19
	121	CSI0_VSYNC	IPU1_CSI0_VSYNC	EIM_DATA01				GPIO5_IO21		ARM_TRACE00			GPIO5_IO21
	126	CSI0_DATA_EN	IPU1_CSI0_DATA_EN	EIM_DATA00				GPIO5_IO20		ARM_TRACE_CLK			GPIO5_IO20

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
Audio	61	SD2_DAT0	SD2_DATA0	ECSPI5_MISO		AUD4_RXD	KEY_ROW7	GPIO1_IO15	DCIC2_OUT				GPIO1_IO15
	89	SD2_DAT1	SD2_DATA1	ECSPI5_SS0	EIM_CS2_B	AUD4_TXFS	KEY_COL7	GPIO1_IO14					GPIO1_IO14
	67	SD2_DAT2	SD2_DATA2	ECSPI5_SS1	EIM_CS3_B	AUD4_TXD	KEY_ROW6	GPIO1_IO13					GPIO1_IO13
	90	SD2_DAT3	SD2_DATA3	ECSPI5_SS3	KEY_COL6	AUD4_TXC		GPIO1_IO12					GPIO1_IO12
	91	SD2_CMD	SD2_CMD	ECSPI5_MOSI	KEY_ROW5	AUD4_RXC		GPIO1_IO11					GPIO1_IO11
	92	SD2_CLK	SD2_CLK	ECSPI5_SCLK	KEY_COL5	AUD4_RXFS		GPIO1_IO10					GPIO1_IO10
LVDS	50	LVDS0_TX0_P											LVDS0_DATA0_P
	48	LVDS0_TX0_N											LVDS0_DATA0_N
	54	LVDS0_TX1_P											LVDS0_DATA1_P
	52	LVDS0_TX1_N											LVDS0_DATA1_N
	55	LVDS0_TX2_P											LVDS0_DATA2_P
	53	LVDS0_TX2_N											LVDS0_DATA2_N
	58	LVDS0_TX3_P											LVDS0_DATA3_P
	56	LVDS0_TX3_N											LVDS0_DATA3_N
	57	LVDS0_CLK_N											LVDS0_CLK_N
	59	LVDS0_CLK_P											LVDS0_CLK_P

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
DISP0_RGB LCD	166	DISP0_DAT0	IPU1_DISP0_ DATA00	IPU2_DISP0_ DATA00	ECSPI3_SCLK			GPIO4_IO21					GPIO4_IO21
	167	DISP0_DAT1	IPU1_DISP0_ DATA01	IPU2_DISP0_ DATA01	ECSPI3_MOSI			GPIO4_IO22					GPIO4_IO22
	168	DISP0_DAT2	IPU1_DISP0_ DATA02	IPU2_DISP0_ DATA02	ECSPI3_MISO			GPIO4_IO23					GPIO4_IO23
	170	DISP0_DAT3	IPU1_DISP0_ DATA03	IPU2_DISP0_ DATA03	ECSPI3_SS0			GPIO4_IO24					GPIO4_IO24
	171	DISP0_DAT4	IPU1_DISP0_ DATA04	IPU2_DISP0_ DATA04	ECSPI3_SS1			GPIO4_IO25					GPIO4_IO25
	172	DISP0_DAT5	IPU1_DISP0_ DATA05	IPU2_DISP0_ DATA05	ECSPI3_SS2	AUD6_RXFS		GPIO4_IO26					GPIO4_IO26
	173	DISP0_DAT6	IPU1_DISP0_ DATA06	IPU2_DISP0_ DATA06	ECSPI3_SS3	AUD6_RXC		GPIO4_IO27					GPIO4_IO27
	174	DISP0_DAT7	IPU1_DISP0_ DATA07	IPU2_DISP0_ DATA07	ECSPI3_RDY			GPIO4_IO28					GPIO4_IO28
	157	DISP0_DAT8	IPU1_DISP0_ DATA08	IPU2_DISP0_ DATA08	PWM1_OUT	WDOG1_B		GPIO4_IO29					GPIO4_IO29
	158	DISP0_DAT9	IPU1_DISP0_ DATA09	IPU2_DISP0_ DATA09	PWM2_OUT	WDOG2_B		GPIO4_IO30					GPIO4_IO30
	159	DISP0_DAT10	IPU1_DISP0_ DATA10	IPU2_DISP0_ DATA10				GPIO4_IO31					GPIO4_IO31
	161	DISP0_DAT11	IPU1_DISP0_ DATA11	IPU2_DISP0_ DATA11				GPIO5_IO05					GPIO5_IO05
	162	DISP0_DAT12	IPU1_DISP0_ DATA12	IPU2_DISP0_ DATA12				GPIO5_IO06					GPIO5_IO06
	163	DISP0_DAT13	IPU1_DISP0_ DATA13	IPU2_DISP0_ DATA13		AUD5_RXFS		GPIO5_IO07					GPIO5_IO07
	164	DISP0_DAT14	IPU1_DISP0_ DATA14	IPU2_DISP0_ DATA14		AUD5_RXC		GPIO5_IO08					GPIO5_IO08
	165	DISP0_DAT15	IPU1_DISP0_ DATA15	IPU2_DISP0_ DATA15	ECSPI1_SS1	ECSPI2_SS1		GPIO5_IO09					GPIO5_IO09
	148	DISP0_DAT16	IPU1_DISP0_ DATA16	IPU2_DISP0_ DATA16	ECSPI2_MOSI	AUD5_TXC	SDMA_EXT_ EVENT0	GPIO5_IO10					GPIO5_IO10

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
DISP0_RGB LCD	149	DISP0_DAT17	IPU1_DISP0_DATA17	IPU2_DISP0_DATA17	ECSPI2_MISO	AUD5_TXD	SDMA_EXT_EVENT1	GPIO5_IO11					GPIO5_IO11
	150	DISP0_DAT18	IPU1_DISP0_DATA18	IPU2_DISP0_DATA18	ECSPI2_SS0	AUD5_TXFS	AUD4_RXFS	GPIO5_IO12		EIM_CS2_B			GPIO5_IO12
	152	DISP0_DAT19	IPU1_DISP0_DATA19	IPU2_DISP0_DATA19	ECSPI2_SCLK	AUD5_RXD	AUD4_RXC	GPIO5_IO13		EIM_CS3_B			GPIO5_IO13
	153	DISP0_DAT20	IPU1_DISP0_DATA20	IPU2_DISP0_DATA20	ECSPI1_SCLK	AUD4_TXC		GPIO5_IO14					GPIO5_IO14
	154	DISP0_DAT21	IPU1_DISP0_DATA21	IPU2_DISP0_DATA21	ECSPI1_MOSI	AUD4_TXD		GPIO5_IO15					GPIO5_IO15
	155	DISP0_DAT22	IPU1_DISP0_DATA22	IPU2_DISP0_DATA22	ECSPI1_MISO	AUD4_TXFS		GPIO5_IO16					GPIO5_IO16
	156	DISP0_DAT23	IPU1_DISP0_DATA23	IPU2_DISP0_DATA23	ECSPI1_SS0	AUD4_RXD		GPIO5_IO17					GPIO5_IO17
	145	DI0_DISP_CLK	IPU1_DI0_DISP_CLK	IPU2_DI0_DISP_CLK				GPIO4_IO16					GPIO4_IO16
	144	DI0_PIN2	IPU1_DI0_PIN02	IPU2_DI0_PIN02	AUD6_TXD			GPIO4_IO18					GPIO4_IO18
	143	DI0_PIN3	IPU1_DI0_PIN03	IPU2_DI0_PIN03	AUD6_TXFS			GPIO4_IO19					GPIO4_IO19
	146	DI0_PIN15	IPU1_DI0_PIN15	IPU2_DI0_PIN15	AUD6_TXC			GPIO4_IO17					GPIO4_IO17

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
HDMI	21	HDMI_D0P											HDMI_TX_DATA0_P
	23	HDMI_D0M											HDMI_TX_DATA0_N
	22	HDMI_D1P											HDMI_TX_DATA1_P
	24	HDMI_D1M											HDMI_TX_DATA1_N
	26	HDMI_D2P											HDMI_TX_DATA2_P
	28	HDMI_D2M											HDMI_TX_DATA2_N
	29	HDMI_CLKP											HDMI_TX_CLK_P
	31	HDMI_CLKM											HDMI_TX_CLK_N
	25	HDMI_HPD											HDMI_TX_HPD
SPI	66	CSI0_DAT8	IPU1_CSI0_DATA08	EIM_DATA06	ECSPI2_SCLK	KEY_COL7	I2C1_SDA	GPIO5_IO26		ARM_TRACE05			GPIO5_IO26
	70	CSI0_DAT9	IPU1_CSI0_DATA09	EIM_DATA07	ECSPI2_MOSI	KEY_ROW7	I2C1_SCL	GPIO5_IO27		ARM_TRACE06			GPIO5_IO27
	63	CSI0_DAT10	IPU1_CSI0_DATA10	AUD3_RXC	ECSPI2_MISO	UART1_TX_DATA		GPIO5_IO28		ARM_TRACE07			GPIO5_IO28
	110	CSI0_DAT11	IPU1_CSI0_DATA11	AUD3_RXFS	ECSPI2_SS0	UART1_RX_DATA		GPIO5_IO29		ARM_TRACE08			GPIO5_IO29
	62	EIM_LBA	EIM_LBA	IPU1_DI1_PIN17	ECSPI2_SS1			GPIO2_IO27		SRC_BOOT_CFG26	EPDC_DATA04		EIM_LBA
	71	EIM_D24	EIM_DATA24	ECSPI4_SS2	UART3_TX_DATA	ECSPI1_SS2	ECSPI2_SS2	GPIO3_IO24	AUD5_RXFS	UART1_DTR_B	EPDC_SDCE7		GPIO3_IO24

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
UART1	7	SD3_DAT6	SD3_DATA6	UART1_RX_DATA				GPIO6_IO18					GPIO6_IO18
	9	SD3_DAT7	SD3_DATA7	UART1_TX_DATA				GPIO6_IO17					GPIO6_IO17
	97	EIM_D19	EIM_DATA19	ECSPI1_SS1	IPU1_DI0_PIN08	IPU2_CSI1_DATA16	UART1_CTS_B	GPIO3_IO19	EPIT1_OUT		EPDC_DATA12		GPIO3_IO19
	94	EIM_D20	EIM_DATA20	ECSPI4_SS0	IPU1_DI0_PIN16	IPU2_CSI1_DATA15	UART1_RTS_B	GPIO3_IO20	EPIT2_OUT				GPIO3_IO20
UART2	117	EIM_D27	EIM_DATA27	IPU1_DI1_PIN13	IPU1_CSI0_DATA00	IPU2_CSI1_DATA13	UART2_RX_DATA	GPIO3_IO27	IPU1_SISG3	IPU1_DISP1_DATA23			GPIO3_IO27
	118	EIM_D26	EIM_DATA26	IPU1_DI1_PIN11	IPU1_CSI0_DATA01	IPU2_CSI1_DATA14	UART2_TX_DATA	GPIO3_IO26	IPU1_SISG2	IPU1_DISP1_DATA22			GPIO3_IO26
UART4	98	KEY_COL0	ECSPI1_SCLK	ENET_RX_DATA3	AUD5_TXC	KEY_COL0	UART4_TX_DATA	GPIO4_IO06	DCIC1_OUT				GPIO4_IO06
	99	KEY_ROW0	ECSPI1_MOSI	ENET_TX_DATA3	AUD5_TXD	KEY_ROW0	UART4_RX_DATA	GPIO4_IO07	DCIC2_OUT				GPIO4_IO07
UART5	102	KEY_COL1	ECSPI1_MISO	ENET_MDIO	AUD5_TXFS	KEY_COL1	UART5_TX_DATA	GPIO4_IO08	SD1_VSELECT				GPIO4_IO08
	103	KEY_ROW1	ECSPI1_SS0	ENET_COL	AUD5_RXD	KEY_ROW1	UART5_RX_DATA	GPIO4_IO09	SD2_VSELECT				GPIO4_IO09
I2C1	19	EIM_D28	EIM_DATA28	I2C1_SDA	ECSPI4_MOSI	IPU2_CSI1_DATA12	UART2_CTS_B	GPIO3_IO28	IPU1_EXT_TRIG	IPU1_DI0_PIN13	EPDC_PWR_CTRL3		GPIO3_IO28
	18	EIM_D21	EIM_DATA21	ECSPI4_SCLK	IPU1_DI0_PIN17	IPU2_CSI1_DATA11	USB_OTG_OC	GPIO3_IO21	I2C1_SCL	SPDIF_IN			GPIO3_IO21
I2C2	116	GPIO_3	ESAI_RX_HF_CLK		I2C3_SCL	XTALOSC_REF_CLK_24M	CCM_CLKO2	GPIO1_IO03	USB_H1_OC	MLB_CLK			GPIO1_IO03
	115	GPIO_6	ESAI_TX_CLK		I2C3_SDA			GPIO1_IO06	SD2_LCTL	MLB_SIG			GPIO1_IO06
CAN1	176	GPIO_8	ESAI_TX5_RX0	XTALOSC_REF_CLK_32K	EPIT2_OUT	FLEXCAN1_RX	UART2_RX_DATA	GPIO1_IO08	SPDIF_SR_CLK	USB_OTG_PWR_CTL_WAKE	I2C4_SDA		GPIO1_IO08
	178	GPIO_7	ESAI_TX4_RX1	ECSPI5_RDY	EPIT1_OUT	FLEXCAN1_TX	UART2_TX_DATA	GPIO1_IO07	SPDIF_LOCK	USB_OTG_HOST_MODE	I2C4_SCL		GPIO1_IO07

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
CAN2	175	KEY_ROW4	FLEXCAN2_RX	IPU1_SISG5	USB_OTG_PWR	KEY_ROW4	UART5_CTS_B	GPIO4_IO15					GPIO4_IO15
	177	KEY_COL4	FLEXCAN2_TX	IPU1_SISG4	USB_OTG_OC	KEY_COL4	UART5_RTS_B	GPIO4_IO14					GPIO4_IO14
PWM	138	GPIO_9	ESAI_RX_FS	WDOG1_B	KEY_COL6	CCM_REF_EN_B	PWM1_OUT	GPIO1_IO09	SD1_WP				GPIO1_IO09
	125	SD1_DAT2	SD1_DATA2	ECSPI5_SS1	GPT_COMPARE2	PWM2_OUT	WDOG1_B	GPIO1_IO19	WDOG1_RESET_B_DEB				GPIO1_IO19
	147	SD1_DAT1	SD1_DATA1	ECSPI5_SS0	PWM3_OUT	GPT_CAPTURE2		GPIO1_IO17					GPIO1_IO17
	141	SD1_CMD	SD1_CMD	ECSPI5_MOSI	PWM4_OUT	GPT_COMPARE1		GPIO1_IO18					GPIO1_IO18
JTAG	195	JTAG_TDI											JTAG_TDI
	191	JTAG_TDO											JTAG_TDO
	199	JTAG_TMS											JTAG_TMS
	193	JTAG_TRSTB											JTAG_TRSTB
	197	JTAG_TCK											JTAG_TCK

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
GPIOs	33	NANDF_WP_B	NAND_WP_B	IPU2_SISG5				GPIO6_IO09				I2C4_SCL	GPIO6_IO09
	35	EIM_A25	EIM_ADDR25	ECSPI4_SS1	ECSPI2_RDY	IPU1_DI1_PIN12	IPU1_DI0_D1_CS	GPIO5_IO02	HDMI_TX_CEC_LINE		EPDC_DATA15	EIM_ACLK_FREERUN	GPIO5_IO02
	37	NANDF_D2	NAND_DATA02	SD1_DATA6				GPIO2_IO02					GPIO2_IO02
	43	NANDF_D4	NAND_DATA04	SD2_DATA4				GPIO2_IO04					GPIO2_IO04
	45	SD1_DAT0	SD1_DATA0	ECSPI5_MISO		GPT_CAPTURE1		GPIO1_IO16					GPIO1_IO16
	47	NANDF_ALE	NAND_ALE	SD4_RESET				GPIO6_IO08					GPIO6_IO08
	49	NANDF_D1	NAND_DATA01	SD1_DATA5				GPIO2_IO01					GPIO2_IO01
	69	NANDF_CS1	NAND_CE1_B	SD4_VSELECT	SD3_VSELECT			GPIO6_IO14					GPIO6_IO14
	73	NANDF_D0	NAND_DATA00	SD1_DATA4				GPIO2_IO00					GPIO2_IO00
	122	GPIO_18	ESAI_TX1	ENET_RX_CLK	SD3_VSELECT	SDMA_EXT_EVENT1	ASRC_EXT_CLK	GPIO7_IO13	SNVS_VIO_5_CTL				GPIO7_IO13
	10	SD1_DAT3	SD1_DATA3	ECSPI5_SS2	GPT_COMPARE3	PWM1_OUT	WDOG2_B	GPIO1_IO21	WDOG2_RESET_B_DEB				GPIO1_IO21
	30	NANDF_D3	NAND_DATA03	SD1_DATA7				GPIO2_IO03					GPIO2_IO03
	34	NANDF_D6	NAND_DATA06	SD2_DATA6				GPIO2_IO06					GPIO2_IO06
	36	NANDF_CS0	NAND_CE0_B					GPIO6_IO11					GPIO6_IO11
	42	SD1_CLK	SD1_CLK	ECSPI5_SCLK	XTALOSC_OSC32K_32K_OUT	GPT_CLKIN		GPIO1_IO20					GPIO1_IO20
	44	NANDF_CLE	NAND_CLE	IPU2_SISG4				GPIO6_IO07					GPIO6_IO07
	64	GPIO_19	KEY_COL5	ENET_1588_EVENT0_OUT	SPDIF_OUT	CCM_CLKO1	ECSPI1_RDY	GPIO4_IO05	ENET_TX_ER				GPIO4_IO05

Interface/ Function	SODIMM Edge Pin No	i.MX6 CPU Pad Name	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Default/ Reset State
GPIOs	68	NANDF_RB0	NAND_READY_B	IPU2_DI0_PIN01				GPIO6_IO10					GPIO6_IO10
	76	NANDF_D5	NAND_DATA05	SD2_DATA5				GPIO2_IO05					GPIO2_IO05
	78	NANDF_D7	NAND_DATA07	SD2_DATA7				GPIO2_IO07					GPIO2_IO07
	80	DI0_PIN4	IPU1_DI0_PIN04	DI0_PIN04	AUD6_RXD	SD1_WP		GPIO4_IO20					GPIO4_IO20
	86	EIM_BCLK	EIM_BCLK	IPU1_DI1_PIN16				GPIO6_IO31			EPDC_SDCE9		GPIO6_IO31
	132	GPIO_16	ESAI_TX3_RX2	ENET_1588_EVENT2_IN	ENET_REF_CLK	SD1_LCTL	SPDIF_IN	GPIO7_IO11	I2C3_SDA	JTAG_DE_B			GPIO7_IO11
	136	KEY_ROW3	XTALOSC_OSC32K_32K_OUT	ASRC_EXT_CLK	HDMI_TX_DDC_SDA	KEY_ROW3	I2C2_SDA	GPIO4_IO13	SD1_VSELECT				GPIO4_IO13
	139	KEY_COL3	ECSPI1_SS3	ENET_CRS	HDMI_TX_DDC_SCL	KEY_COL3	I2C2_SCL	GPIO4_IO12	SPDIF_IN				GPIO4_IO12
	179	KEY_COL2	ECSPI1_SS1	ENET_RX_DATA2	FLEXCAN1_TX	KEY_COL2	ENET_MDC	GPIO4_IO10	USB_H1_PWR_CTL_WAKE				GPIO4_IO10
	181	KEY_ROW2	ECSPI1_SS2	ENET_TX_DATA2	FLEXCAN1_RX	KEY_ROW2	SD2_VSELECT	GPIO4_IO11	HDMI_TX_CEC_LINE				GPIO4_IO11

Note:

**Purple Coloured ALT functions are not supported in i.MX6 Quad and Dual core CPUs.*

** Green Coloured ALT functions are not supported in i.MX6 Solo and Duallite CPUs.*

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX6 SODIMM SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX6 SODIMM SOM.

Table 7: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VIN_3V3[1]	3.15	3.3	3.45	±50mV
2	VRTC_3V0[2]	2.8	3	3.3	±20 mV
3	VBUS_5V[3]	4.4	5	5.25	±50mV

[1] i.MX6 SODIMM SOM is designed to work with VIN_3V3 input power rail from SODIMM Edge connector.

[2] i.MX6 SODIMM SOM uses this voltage as backup power source to RTC when VIN_3V3 is off. This is an optional power and required only if RTC functionality is used.

[3] This power is used as supply voltage to both USB OTG and USB HOST1 block of i.MX6 CPU. It is recommended to connect always available 5V power to this pin from carrier board.

3.1.2 Power Input Sequencing

i.MX6 SODIMM SOM's Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VIN_3V3 comes up.

Power down Sequence:

- VIN_3V3 must go down at the same time or before VRTC_3V0 goes down.

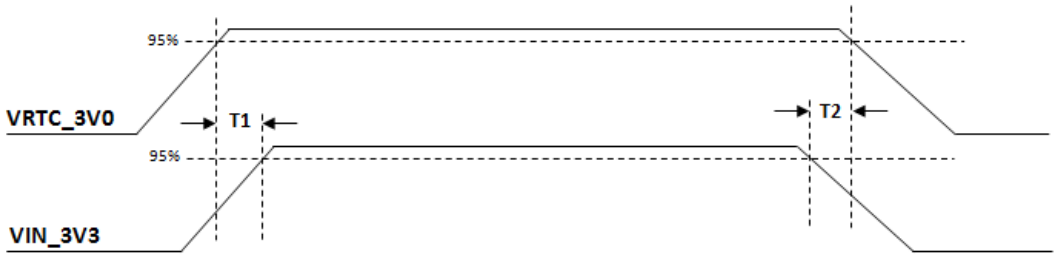

Figure 4: i.MX6 SODIMM SOM Power Sequence

Note: VBUS_5V is not part of the power supply sequence and can be powered at any time.

Table 8: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0 rise time to VIN_3V3 rise time	≥ 0 ms
T2	VIN_3V3 fall time to VRTC_3V0 fall time	≥ 0 ms

Important Note: All the carrier board power supplies should be powered ON only after the SOM is powered ON completely. Otherwise it can cause internal latch-up and malfunctions/bootup issues due to reverse current flows.

3.1.3 Power Consumption

Table 9: Power Consumption

Task/Status	Power Rail	Current Drawn (A)/ Power Consumption (W)
Run Mode Power Consumption[1]		
Play Video	VIN_3V3	0.49/1.617
	VIN_3V3	0.33/1.089
Play Graphics 3D Demo	VIN_3V3	0.46/1.518
Play Audio	VIN_3V3	0.27/0.891
File Transfer	VIN_3V3	0.39/1.287
Dhrystone	VIN_3V3	1.02/3.366
Maximum Power Test: • HDMI - Run the 1080p video (creature.mp4) • LVDS - Run the video (akiyo.mp4) on LVDS • Ethernet - Run the ping test • FileTransfer - Transfer the 1MB file between USB and Micro SD with 1000 count • Audio - Run the mp3 file using Gplay • Powermeasurement1.sh - Run the dry2 application on back ground • Powermeasurement2.sh - Run the Graphics (OpenGL) application (tiger) on LVDS	VIN_3V3	1.18/3.894
All above with below mentioned one change, HDMI - Run the VGA video (akiyo.mp4) on HDMI using VPU Decoder library	VIN_3V3	1.09/3.597
Low Power Mode Power Consumption[2]		
System Idle Mode.	VIN_3V3	0.2/0.66
Deep Sleep Mode.	VIN_3V3	0.05/0.165
User Idle Mode - Enable the Bus frequency	VIN_3V3	0.3/0.99
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	500uA[3]

[1] Power consumption measurements have been done in iWave's i.MX6 Quad CPU based SODIMM SOM with iWave's Generic SODIMM Carrier board running iWave's Linux3.14.38 BSP (iW-PREPZ-DF-01-R2.0-REL1.0-Linux3.14.38).

[2] Only i.MX6 CPU related power management is implemented in the BSP for low power modes.

[3] i.MX6 RTC controller draws more power from VCC_RTC coin cell power input and so could drain the coin cell faster.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX6 SODIMM SOM.

Table 10: Environmental Specification

Parameters	Min	Max
Operating temperature range (Industrial)[1]	-40°C	85°C
Operating temperature range (Commercial)[1]	0°C	70°C
Humidity - Operating	10%RH	90%RH
Humidity - Storage	5%RH	95%RH

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS Compliance

iWave's i.MX6 SODIMM SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's i.MX6 SODIMM SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX6 SODIMM SOM Mechanical Dimensions

i.MX6 SODIMM SOM PCB size is 67.6mm x 37mm x 1mm. SODIMM SOM mechanical dimension is shown below. Please refer the JEDEC Physical standard DDR SODIMM specification for SODIMM Edge connector mechanical details.

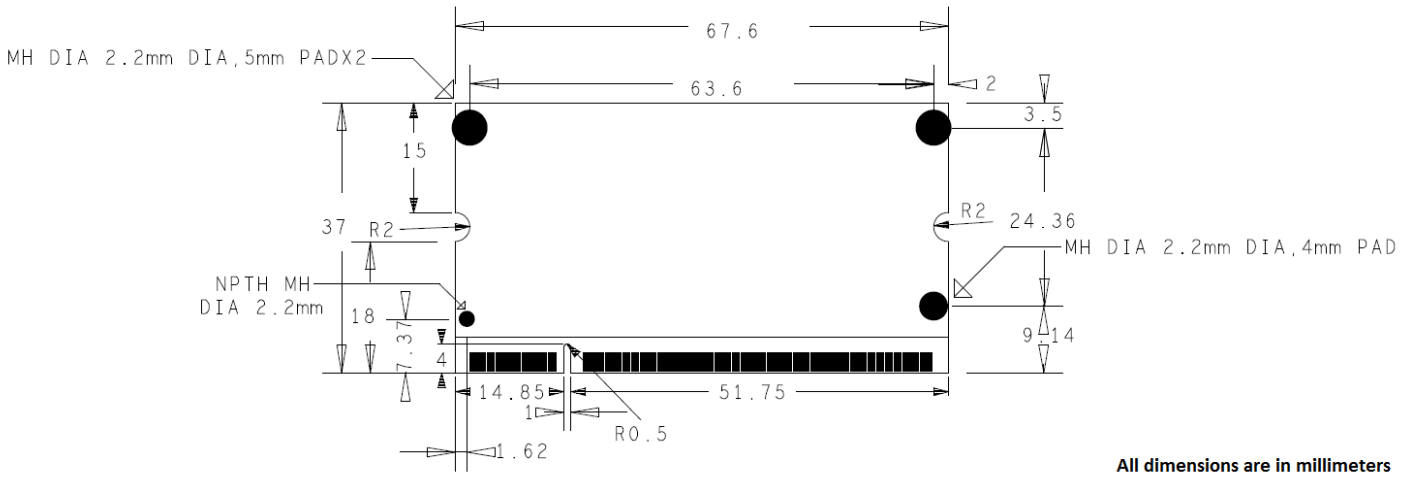

Figure 5: Mechanical dimension of i.MX6 SODIMM SOM - Top View

i.MX6 SODIMM SOM PCB thickness is 1±0.1mm, top side maximum height component is SPI flash (2.16mm) followed by iMX6 CPU (2.10mm) and bottom side maximum height component is Capacitor (1.25mm) followed by DDR3 SDRAM (1.0mm). Please refer the below figure which gives height details of the i.MX6 SODIMM SOM.

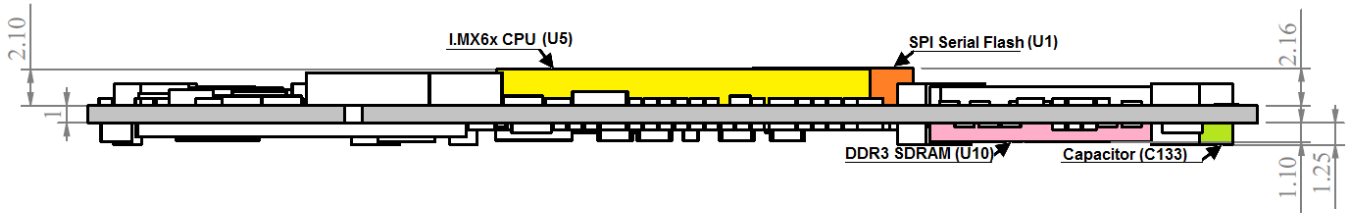

Figure 6: Mechanical dimension of i.MX6 SODIMM SOM - Side View

4. ORDERING INFORMATION

i.MX6 SODIMM SOM is available in different variations. The below table provides the standard orderable part numbers for different i.MX6 SODIMM SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 11: Orderable Product Part Numbers

Product Part Number	Description	Temperature
i.MX6 Quad CPU based SODIMM SOMs		
iW-G15M-SM04-3D001G-E004G-LCC	i.MX6 Quad Core CPU, 1GB RAM, 4GB eMMC with Linux	Commercial
iW-G15M-SM04-3D001G-E004G-ACC	i.MX6 Quad Core CPU, 1GB RAM, 4GB eMMC with Android	Commercial
iW-G15M-SM04-3D001G-E004G-BCC	i.MX6 Quad Core CPU, 1GB RAM, 4GB eMMC with Boot code	Commercial
iW-G15M-SM04-3D001G-E004G-LIC	i.MX6 Quad Core CPU, 1GB RAM, 4GB eMMC with Linux	Industrial
iW-G15M-SM04-3D001G-E004G-AIC	i.MX6 Quad Core CPU, 1GB RAM, 4GB eMMC with Android	Industrial
iW-G15M-SM04-3D001G-E004G-BIC	i.MX6 Quad Core CPU, 1GB RAM, 4GB eMMC with Boot code	Industrial
i.MX6 Dual CPU based SODIMM SOMs		
iW-G15M-SM02-3D001G-E004G-LCC	i.MX6 Dual Core CPU, 1GB RAM, 4GB eMMC with Linux	Commercial
iW-G15M-SM02-3D001G-E004G-ACC	i.MX6 Dual Core CPU, 1GB RAM, 4GB eMMC with Android	Commercial
iW-G15M-SM02-3D001G-E004G-BCC	i.MX6 Dual Core CPU, 1GB RAM, 4GB eMMC with Boot code	Commercial
iW-G15M-SM02-3D001G-E004G-LIC	i.MX6 Dual Core CPU, 1GB RAM, 4GB eMMC with Linux	Industrial
iW-G15M-SM02-3D001G-E004G-AIC	i.MX6 Dual Core CPU, 1GB RAM, 4GB eMMC with Android	Industrial
iW-G15M-SM02-3D001G-E004G-BIC	i.MX6 Dual Core CPU, 1GB RAM, 4GB eMMC with Boot code	Industrial
i.MX6 Duallite CPU based SODIMM SOMs		
iW-G15M-SM2L-3D001G-E004G-LCC	i.MX6 Duallite Core CPU, 1GB RAM, 4GB eMMC with Linux	Commercial
iW-G15M-SM2L-3D001G-E004G-ACC	i.MX6 Duallite Core CPU, 1GB RAM, 4GB eMMC with Android	Commercial
iW-G15M-SM2L-3D001G-E004G-BCC	i.MX6 Duallite Core CPU, 1GB RAM, 4GB eMMC with Boot code	Commercial

Product Part Number	Description	Temperature
iW-G15M-SM2L-3D001G-E004G-LIC	i.MX6 Duallite Core CPU, 1GB RAM, 4GB eMMC with Linux	Industrial
iW-G15M-SM2L-3D001G-E004G-AIC	i.MX6 Duallite Core CPU, 1GB RAM, 4GB eMMC with Android	Industrial
iW-G15M-SM2L-3D001G-E004G-BIC	i.MX6 Duallite Core CPU, 1GB RAM, 4GB eMMC with Boot code	Industrial
i.MX6 Solo CPU based SODIMM SOMs		
iW-G15M-SM01-3D512M-E004G-LCC	i.MX6 Solo Core CPU, 512MB RAM, 4GB eMMC with Linux	Commercial
iW-G15M-SM01-3D512M-E004G-ACC	i.MX6 Solo Core CPU, 512MB RAM, 4GB eMMC with Android	Commercial
iW-G15M-SM01-3D512M-E004G-BCC	i.MX6 Solo Core CPU, 512MB RAM, 4GB eMMC with Boot code	Commercial
iW-G15M-SM01-3D512M-E004G-LIC	i.MX6 Solo Core CPU, 512MB RAM, 4GB eMMC with Linux	Industrial
iW-G15M-SM01-3D512M-E004G-AIC	i.MX6 Solo Core CPU, 512MB RAM, 4GB eMMC with Android	Industrial
iW-G15M-SM01-3D512M-E004G-BIC	i.MX6 Solo Core CPU, 512MB RAM, 4GB eMMC with Boot code	Industrial

Important Note: Some of the above mentioned Part Number is subject to MOQ purchase. Please contact iWave for further details.

Note: For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX I

5.1 Guidelines to insert the SODIMM SOM into Carrier board

- Make sure that power is not provided to the Carrier board.
- Insert the module into the socket at a slight angle (approximately 30 degrees). Note that the socket and module are both keyed, which means the module can be installed one way only.
- To seat the module into the socket, apply firm, even pressure to each end of the module until you feel it slip down into the socket.
- With the module properly seated in the socket, rotate the module downward, as indicated in the illustration. Continue pressing downward until the clips at each end of the socket lock into position.
- Once the module has been installed, Carrier board can be Powered ON with 5V power supply.

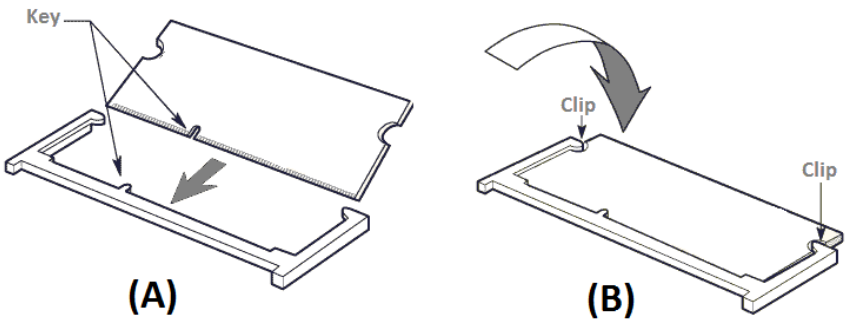

Figure 7: Module Insertion Procedure

5.2 Guidelines to remove the SODIMM SOM from Carrier board

- Make sure that power is not provided to the Carrier board.
- When you remove the module, pull away the retention clips (A) on each side of the memory module.
- The module pops up. Grasp the edge of the module (B) and gently pull the module out of the connector.

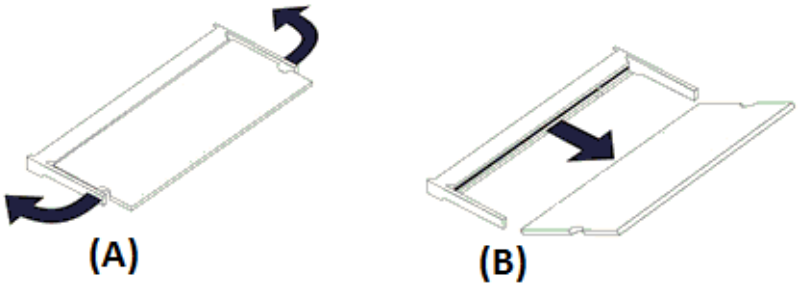

Figure 8: Module Removal Procedure

6. APPENDIX II

6.1 i.MX6 SODIMM SOM Development Platform

iWave Systems supports iW-RainboW-G15D-SM – i.MX6 SODIMM Development Platform which is targeted for quick validation of i.MX6 CPU with i.MX6 SODIMM SOM. iWave's i.MX6 SODIMM Development Board incorporates i.MX6 SODIMM SOM and SODIMM Carrier board for complete validation of i.MX6 SODIMM SOM functionality with complete BSP support.

Being a Pico-ITX form factor with 100mmx72mm size, the i.MX6 SODIMM Development Platform carrier board is highly packed with all the necessary on-board connectors to validate the i.MX6 CPU features with optional 4.3" resistive display kit. For more details on i.MX6 SODIMM SOM Development platform, visit the below web link.

http://www.iwavesystems.com/product/development-platform/imx6-sodimm-development-kit-17/imx6-sodimm-development-kit.html

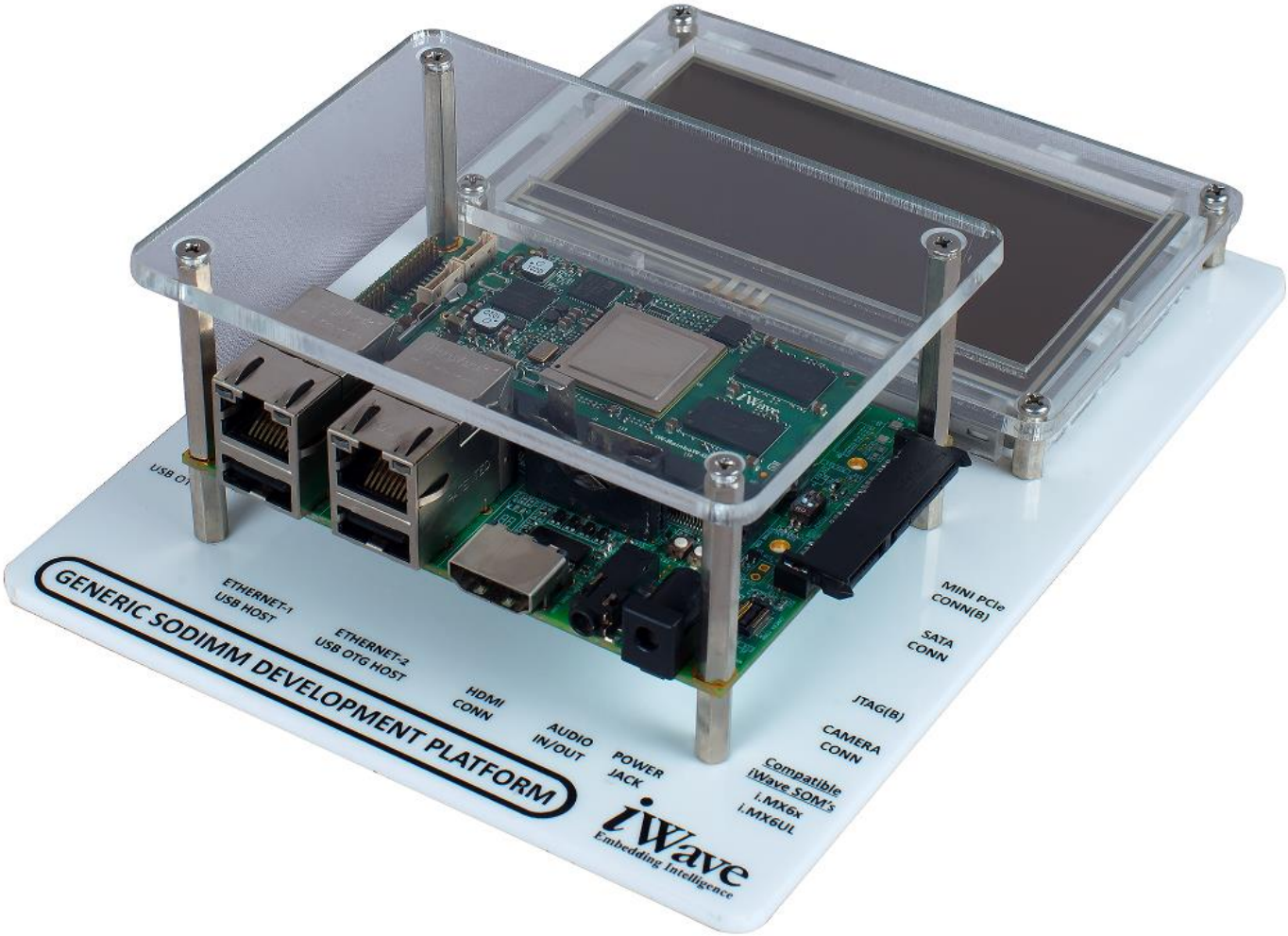

Figure 9: i.MX6 SODIMM SOM Development Platform


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