NAND Controller
GLS55LD040M

Advance Information

FEATURES:

- **Industry Standard PATA Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-4
  - Supports up to Multi-word DMA Mode-2
  - Supports up to Ultra DMA Mode-6
  - Supports 48-bit Address Feature Set
- **Interface for Standard NAND Flash Media**
  - Flash Media Interface: 8-bit per channel with 1, 2, or 4 channel options
    - Supports up to 16 flash media devices directly
    - Supports up to 64 flash media devices with external decoding logic
  - Supports Single-Level Cell (SLC) or Multi-Level Cell (MLC) flash media
  - Supports 4KByte and 8KByte program page size
    - Two-plane operation
- **Low Power, 3.3V Host and NAND Flash Media Interface**
- **Low Power Operation:**
  - Active mode: 60 mA (3.3V) (typical)
  - Sleep mode: 800 µA (3.3V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Expanded Data Protection**
  - Added data security through user-selectable protection zones
- **20-byte Unique ID for Enhanced Security**
  - Factory pre-programmed 10-Byte, unique ID
  - User-Programmable 10-Byte ID
- **Programmable, Multitasking NAND Flash Media Interface**
- **Firmware Storage in SuperFlash**
- **Pre-programmed Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard ATA/IDE commands
  - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  - Flash File System
- **Built-in Hardware ECC**
  - Corrects up to 12 random bits of error per 512-Byte sector; up to 24 random bits of error per 1-Kbyte sector
- **Internal or External System Clock**
- **Multi-tasking Technology enables Fast Sustained Read/Write Performance**
  - MLC NAND
    - Up to 105 MByte/sec Read, 73 MByte/sec Write (external clock)
    - Up to 92 MByte/sec Read, 73 MByte/sec Write (internal clock)
  - SLC NAND
    - Up to 109 MByte/sec Read/Write (external clock)
    - Up to 92 MByte/sec Read, 109 MByte/sec Write (internal clock)
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Packages Available**
  - 145-ball TFBGA – 12mm x 12mm x 1.07mm
- **All devices are RoHS compliant**

PRODUCT DESCRIPTION

The NAND Controller is the heart of a high-performance, flash media-based data storage system. The NAND Controller recognizes the control, address, and data signals on the ATA/IDE bus and translates them into memory accesses to the standard NAND-type flash media. The GLS55LD040M device supports Single-Level Cell (SLC) and Multi-Level Cell (MLC) flash media. This technology is ideal for solid-state mass storage applications offering, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The ATA/IDE interface is widely used in such products as portable and desktop computers, digital cameras, multimedia players, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, global positioning systems, and set-top boxes. The Greenliant NAND Controller supports standard ATA/IDE protocol with up to PIO Mode-4, Multi-word DMA Mode-2, and Ultra DMA Mode-6 interface.

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The NAND Controller uses Greenliant proprietary Super-Flash memory technology and is factory pre-programmed with a flash file system. Upon initial power-on, the NAND Controller recognizes attached flash media devices, sets up a bad block table, executes all necessary handshaking routines for flash media support, and performs the low-level format.

For added manufacturing flexibility, system debug, re-initialization, and user customization is accomplished through the ATA/IDE interface.

The GLS55LD040M offers sustained read and write performance up to 105 MByte/sec (MLC) and 109 MByte/sec (SLC). It directly supports up to 16 flash media devices or, through simple decoding logic, supports up to 64 flash media devices.

For confidential information stored in the flash media, the GLS55LD040M provides exceptional security protection. Four password-protected, protection zones can be set to Read/Write, Read-only, or Hidden (Read-disabled). The NAND Controller also provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites

The GLS55LD040M is available in an industry-standard, 145-ball TFBGA package for easy integration into an SMT manufacturing process.

GENERAL DESCRIPTION

The GLS55LD040M NAND Controller contains a microcontroller and a flash file system integrated in a TFBGA package. Refer to Figure 1 for the NAND Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

Performance-optimized NAND Controller

The heart of the flash drive is the NAND Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the NAND Controller's operation.

Microcontroller Unit (MCU)

The 32 bit RISC MCU transfers the ATA/IDE commands into required flash media operations.

Power Management Unit (PMU)

The power management unit controls the power consumption of the NAND Controller. The PMU dramatically reduces the power consumption of the NAND Controller by putting the part of the circuitry that is not in operation into sleep mode. The PMU is designed so that it has zero wake-up latency when using the internal clock.

SRAM Buffer

A contributor to the NAND Controller performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

Flash File System

The flash file system is an integral part of the NAND Controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.
2. Provides advanced flash media wear leveling to spread the flash writes across the entire memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.
4. Manages system security for the selected protection zones.
5. Stores the data in Flash media upon completion of a Write command. The NAND Controller does not do Post-Write operations, except for when the Write cache is enabled by the Host command.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to provide trace information during debugging processes.To aid in validation, always provide the SCI access to PCB design.

Media Interface Block (MIB)

The GLS55LD040M contains two Media Interface Blocks, MIB0 and MIB1. The MIB work independently to transfer data to and from the NAND Flash media. Each MIB controls two 8-bit channels.

Each Media Interface Block has three functions: DMA, ECC, and Programmable Multi-tasking NAND Interface.

Programmable, Multi-tasking NAND Interface The multi-tasking interface enables fast, sustained write performance by allowing multiple Read, Program, and Erase operations to multiple flash media devices. The ease with which the NAND interface can be programmed enables the quick support of new NAND devices.

Internal Direct Memory Access (DMA) The NAND Controller uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

Error Correction Code (ECC) The GLS55LD040M utilizes 24-bit, BCH Error detection Code (EDC) and Error Correction Code (ECC) algorithms. The ECC engine can provide, depending on settings, 6 or 12 bits of ECC for each 512-Byte block of data, and 12 or 24 bits of ECC for each 1KByte of data.

The ECC encoding and decoding operations occur during the data transfer.

External Clock The GLS55LD040M supports an external clock interface (XCLKI) that is enabled, or disabled, by the external clock enable (XCLKEN) input signal. With a 4.7KΩ pull-down resistor connected to the XCLKEN pin, and a 6.0 MHz external oscillator or clock source present at the XCLKI input pin, the GLS55LD040M uses the external oscillator as the internal clock reference.

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FUNCTIONAL BLOCKS

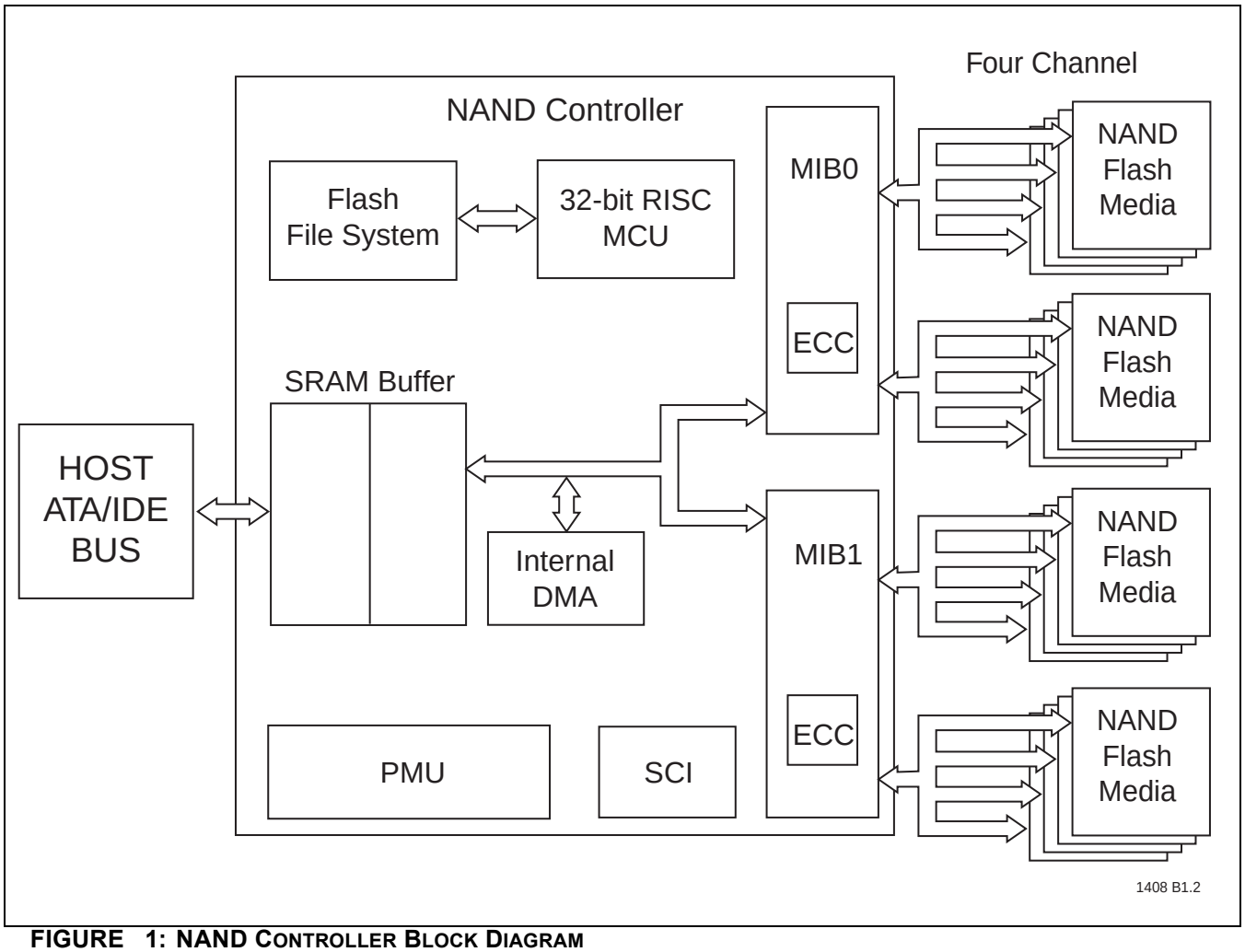

FIGURE 1: NAND CONTROLLER BLOCK DIAGRAM

PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NAND Controller sources are outputs.

The NAND Controller functions in ATA mode, which is compatible with IDE hard disk drives.

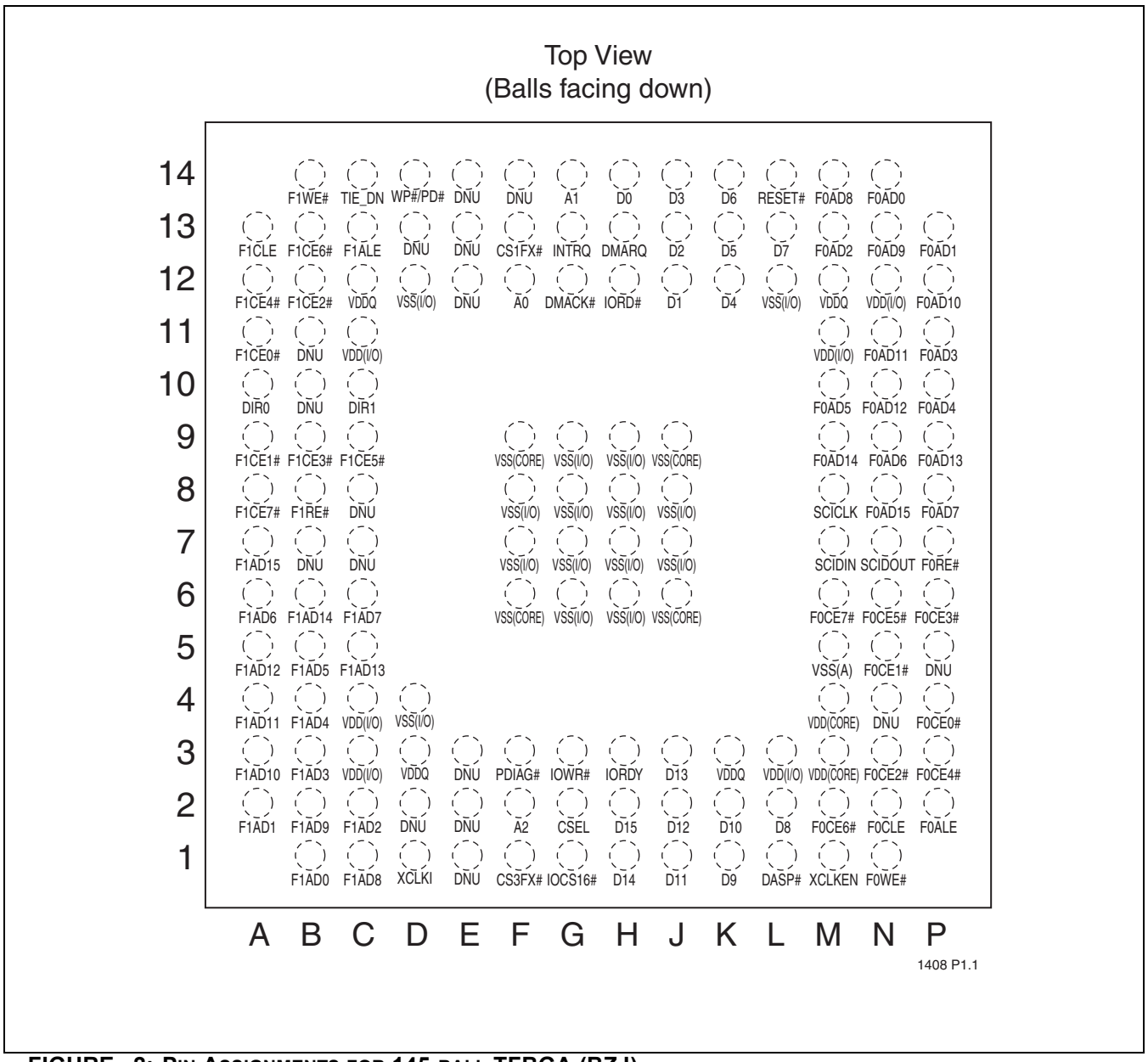

FIGURE 2: PIN ASSIGNMENTS FOR 145-BALL TFBGA (BZJ)

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TABLE 1: PIN ASSIGNMENTS (1 OF 5)

Symbol	Ball No. 145 TFBGA	Ball Type	I/O Type	Name and Functions
Host Interface				
A2	F2	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	G14			
A0	F12			
D15	H2	I/O	I1Z/O2	D[15:0] Data bus
D14	H1			
D13	J3			
D12	J2			
D11	J1			
D10	K2			
D9	K1			
D8	L2			
D7	L13			
D6	K14			
D5	K13			
D4	K12			
D3	J14			
D2	J13			
D1	J12			
D0	H14			
RESET#	L14	I	I2U	This input pin is the active low hardware reset from the host.
DASP#	L1	I/O	I1U/O4	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
IORDY	H3	O	O2	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions)
				DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
				DSTROBE: When Ultra DMA mode DMA Write is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
CS1FX#	F13	I	I2Z	CS1FX# is the chip select for the task file registers.
CS3FX#	F1			CS3FX# is used to select the Alternate Status register and the Device Control register.
CSEL	G2	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, or tied to V_{DDQ}, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
DMARQ	H13	O	O2	DMA Request to host
INTRQ	G13	O	O2	Ready/Busy or Interrupt Request to the host.

TABLE 1: PIN ASSIGNMENTS (CONTINUED) (2 OF 5)

Symbol	Ball No. 145 TFBGA	Ball Type	I/O Type	Name and Functions
DMACK#	G12	I	I2U	DMA Acknowledge - input from host
IORD#	H12	I	I2Z	IORD#: This is an I/O Read strobe generated by the host. While Ultra DMA mode is not active, this signal gates I/O data from the device.
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	G3	I	I2Z	IOWR#: This is an I/O Write strobe generated by the host. When Ultra DMA is not active, this signal clocks I/O into the device.
				STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.
IOCS16#	G1	O	O3	This output signal is asserted low when the device is indicating a word data transfer cycle.
PDIAG#	F3	I/O	I1U/O2	The Pass Diagnostic signal in the Master/Slave handshake protocol.
Flash Media Interface[1]				
F0RE#	P7	O	O7	Active Low Flash Media Chip Read [MIB0]
F0WE#	N1			Active Low Flash Media Chip Write [MIB0]
F0CLE	N2	O	O6	Active High Flash Media Chip Command Latch Enable [MIB0]
F0ALE	P2			Active High Flash Media Chip Address Latch Enable [MIB0]
F0AD15	N8	I/O	I3U/O6	Flash Media Chip High Byte Address/Data Bus pins [MIB0]
F0AD14	M9			
F0AD13	P9			
F0AD12	N10			
F0AD11	N11			
F0AD10	P12			
F0AD9	N13			
F0AD8	M14			
F0AD7	P8			Flash Media Chip Low Byte Address/Data Bus pins [MIB0]
F0AD6	N9			
F0AD5	M10			
F0AD4	P10			
F0AD3	P11			
F0AD2	M13			
F0AD1	P13			
F0AD0	N14			

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TABLE 1: PIN ASSIGNMENTS (CONTINUED) (3 OF 5)

Symbol	Ball No. 145 TFBGA	Ball Type	I/O Type	Name and Functions
F0CE7#	M6	O	O5	Active Low Flash Media Chip Enable pin [MIB0]
F0CE6#	M2			
F0CE5#	N6			
F0CE4#	P3			
F0CE3#	P6			
F0CE2#	N3			
F0CE1#	N5			
F0CE0#	P4			

TABLE 1: PIN ASSIGNMENTS (CONTINUED) (4 OF 5)

Symbol	Ball No. 145 TFBGA	Ball Type	I/O Type	Name and Functions
F1RE#	B8	O	O7	Active Low Flash Media Chip Read [MIB1]
F1WE#	B14			Active Low Flash Media Chip Write [MIB1]
F1CLE	A13	O	O6	Active High Flash Media Chip Command Latch Enable [MIB1]
F1ALE	C13			Active High Flash Media Chip Address Latch Enable [MIB1]
F1AD15	A7	I/O	I3U/O6	Flash Media Chip High Byte Address/Data Bus pins [MIB1]
F1AD14	B6			
F1AD13	C5			
F1AD12	A5			
F1AD11	A4			
F1AD10	A3			
F1AD9	B2			
F1AD8	C1			
F1AD7	C6			Flash Media Chip Low Byte Address/Data Bus pins [MIB1]
F1AD6	A6			
F1AD5	B5			
F1AD4	B4			
F1AD3	B3			
F1AD2	C2			
F1AD1	A2			
F1AD0	B1			
F1CE7#	A8	IO	O5	Active Low Flash Media Chip Enable pin [MIB1]
F1CE6#	B13			
F1CE5#	C9			
F1CE4#	A12			
F1CE3#	B9			
F1CE2#	B12			
F1CE1#	A9			
F1CE0#	A11			
DIR0	A10	O	O6	Bus direction of external decoder for MIB0 group of NAND[2]
DIR1	C10			Bus direction of external decoder for MIB1 group of NAND[2]
Serial Communication Interface (SCI)				
$SCID_{OUT}$	N7	O	O6	SCI Interface data output
$SCID_{IN}$	M7	I	I3U	SCI interface data input
SCICLK	M8	I	I3D	SCI Interface clock
Miscellaneous				
TIE_DN	C14			Pin needs to be connected to V_{SS}

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TABLE 1: PIN ASSIGNMENTS (CONTINUED) (5 OF 5)

Symbol	Ball No. 145 TFBGA	Ball Type	I/O Type	Name and Functions
V_{SS} (IO)	D4, D12, F7, F8, G6, G7, G8, G9, H6, H7, H8, H9, J7, J8, L12	PWR		Ground for I/O
V_{SS} (Core)	F6, F9, J6, J9,	PWR		Ground for core
V_{SS} (A)	M5	PWR		Analog ground
V_{DD} (IO)	C3, C4, C11, L3, M11, N12	PWR		3.3V for Media interface and SCI
V_{DD} (Core)	M3, M4	PWR		V_{DD} (3.3V) Power Supply
V_{DDQ}	C12, D3, K3, M12	PWR		3.3V for Host Interface
XCLKEN	M1	O	I3U/O5	External clock enable. Selects the internal or external clock source. The NAND Controller defaults to the internal clock source when XCLKEN is not connected, and XCLKI is connected to Vss. For assistance using external clock source, please contact Greenliant sales.
XCLKI	D1	I	I4Z	External clock input. This pin should not be left unconnected in any mode. When using the default internal clock, connect this pin to GND.
WP#/PD#	D14	I	I4U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting. This pin accepts only in the 3.3V V_{DD} signal level.
DNU[3]	B7, B10, B11, C7, C8, D2, D13, E1, E2, E3, E12, E13, E14, F14, N4, P5			Do Not Use, must be left unconnected.

T1.4 1408

1. MIB0 and MIB1 operations are mutually exclusive. Do not mix the two groups' signals or FxCE#.
2. To support up to 64 flash media devices
3. All DNU pins should not be connected.

CAPACITY SPECIFICATION

Table 2 shows the default capacity. To change the default settings, update the drive ID table (see Table 7). If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. When the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance is reduced.The GLS55LD040M NAND Controller can support up to 256 GByte.

TABLE 2: DEFAULT ATA FLASH DRIVE SETTINGS

Capacity	Total Bytes	Cylinders[1]	Heads[1]	Sectors[1]	Max LBA
1 GB	914,006,016	1771	16	63	1,785,168
2 GB	1,828,528,128	3543	16	63	3,571,344
4 GB	3,657,056,256	7086	16	63	7,142,688
8 GB	7,012,196,352	13587	16	63	13,695,696
16 GB	15,013,748,736	16383	16	63	29,323,728
32 GB	30,016,659,456	16383	16	63	58,626,288
64 GB	60,022,480,896	16383	16	63	117,231,408
128 GB	120,034,123,776	16383	16	63	234,441,648
256 GB	240,057,409,536	16383	16	63	468,826,128
512 GB	480,103,981,056	16383	16	63	937,703,088

T2.5 1408

1. Cylinders, Heads, and Sectors can be re-configured from the default settings during the manufacturing process.

Functional Specifications

Table 3 shows the performance of the GLS55LD040M NAND Controller.

TABLE 3: FUNCTIONAL SPECIFICATION OF GLS55LD040M

NAND Type	Clock Source	Sustained Read	Sustained Write
MLC NAND	External	Up to 105 MByte/sec	Up to 73 MByte/sec
	Internal	Up to 92 MByte/sec	Up to 73 MByte/sec
SLC NAND	External	Up to 109 MByte/sec	Up to 109 MByte/sec
	Internal	Up to 92 MByte/sec	Up to 109 MByte/sec

T3.5 1408

Advance Information

MANUFACTURING SUPPORT

The NAND Controller firmware contains a list of supported standard NAND flash media devices. Upon initial Power-on, the controller scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices in the NAND controller, the controller performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format. For Power-up timing specifications, please refer to Table 14.

Please contact Greenliant for the most current list of supported NAND Flash media devices.

In the event that the NAND flash media device ID is not recognized by the NAND Controller, the user can add this device to the controller device table through the manufacturing interface provided by Greenliant. Please contact Greenliant for the NAND Controller manufacturing interface software. If the drive initialization fails, and a visual inspection is unable to determine the problem, the GLS55LD040M NAND Controller provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

ATA/IDE Host Interface

The NAND Controller ATA/IDE host interface can be used for manufacturing support. Greenliant provides an example of a DOS-/Windows-based solution (an executable routine downloadable from www.greenliant.com) for manufacturing debug and rework.

Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can report manufacturing errors. The SCI consists of 3 active signals: $SCID_{OUT}$, $SCID_{IN}$, and SCICLK. The Serial Communication Interface (SCI) is designed to provide trace information during the debugging process. To aid in validation, always provide the SCI access to PCB design.

CLOCK SELECTION

The NAND Controller defaults to the internal clock source when XCLKEN is not connected and XCLKI is connected to V_{SS}. The external clock interface allows NAND controller operation from an external clock source generated by an oscillator circuit. Contact Greenliant for reference circuit and recommended external clock frequencies.

SECURITY FEATURES

The GLS55LD040M NAND Controller offers added data protection for applications where data security is of the utmost importance. The secure features are:

1. Protection zones - Customer can enable up to 4 independent protection zones, with two options: Read-only or Hidden (Read and Write protected) within each protected zone. If protection zones are not enabled the data is unprotected (default configuration).
2. Password protection - Accessing information within the protected zones can be only achieved through a customer-unique password.
3. Security Purge command - The system can issue a Security Purge command to erase all information stored in the flash media.

CONFIGURABLE WRITE PROTECT/POWER-DOWN MODES

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the pin will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

Write Protect Mode

When the WP#/PD# pin is configured in the Write Protect mode, the pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP#/PD# pin should be asserted prior to issuing all destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Multiple, Write-Sector(s), or Write-Verify. This will force the NAND Controller to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

Power-down Mode

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, the NAND Controller stops the current command, and immediately enters power-down mode. Afterwards, the device will not accept any other commands. Both a software or a hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Power-on and Brown-out Reset circuitry reset the device to a known state. Power-on Reset asserts when the device is turned on. Brown-out Reset asserts when the detected voltage falls below an acceptable level. For more information about the Power-on and Brown-out Reset timing, see Figure 3 and Table 4.

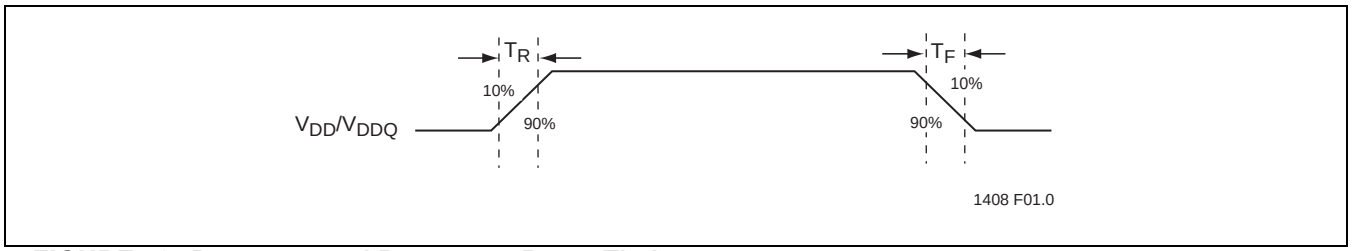

FIGURE 3: Power-on and Brown-out Reset Timing

TABLE 4: POWER-ON AND BROWN-OUT RESET TIMING

Item	Symbol	Min	Max	Units
V_{DD}/V_{DDQ} Rise Time[1]	T_R		250	ms
V_{DD}/V_{DDQ} Fall Time	T_F		250	ms

T4.0 1408

1. V_{DD}/V_{DDQ} power sequencing: V_{DDQ} power should come up at the same time as, or before, V_{DD} power. The time between V_{DDQ} and V_{DD} will not exceed 10 ms.

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I/O TRANSFER FUNCTION

Table 5 defines various I/O functions.

TABLE 5: I/O FUNCTION

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out

T5.0 1408

SOFTWARE INTERFACE

NAND Controller Command Description

This section defines the software requirements and the format of the commands the host sends to the NAND Controller. Commands are issued to the NAND Controller by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. With the exception of commands listed in Sections “Idle - 97H or E3H” , “Set-Sleep-Mode - 99H or E6H” , and “Set-WP#/PD#-Mode - 8BH” , NAND Controller complies with ATA-7 Specifications.

NAND Controller Command Set

Table 6 summarizes the NAND Controller command set.

TABLE 6: NAND CONTROLLER COMMAND SET (1 OF 2)

Command	Code	FR[1,2]	SC[2,3]	SN[2,4]	CY[2,5]	DH[6,7]	LBA[2,8]
Check-Power-Mode	E5H or 98H	-	-	-	-	D	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Flush-Cache	E7H	-	-	-	-	D	-
Flush-Cache-EXT	EAH	-	-	-	-	D	-
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-DMA-EXT	25H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Multiple-EXT	29H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Sector(s)-EXT	24H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)-EXT	42H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
SMART	B0H	Y	Y	Y	Y	D	-
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Set-WP#/PD#-Mode	8BH	Y	-	-	-	D	-

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TABLE 6: NAND CONTROLLER COMMAND SET (CONTINUED) (2 OF 2)

Command	Code	FR[1,2]	SC[2,3]	SN[2,4]	CY[2,5]	DH[6,7]	LBA[2,8]
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-DMA-EXT	35H	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-EXT	39H	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector(s)-EXT	34H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

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1. FR - Features register
2. Y - The register contains a valid parameter for this command.
3. SC - Sector Count register
4. SN - Sector Number register
5. CY - Cylinder registers
6. For the Drive/Head register, Y means both the Drive and Head parameters are used; D means only the Drive parameter is valid and not the Head parameter.
7. DH - Drive/Head register
8. LBA - Logical Block Address mode supported (see command descriptions for use)

Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the NAND Controller. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 7. All reserved bits or words are zero. Table 7 gives the definition for each field in the Identify-Drive information.

TABLE 7: IDENTIFY-DRIVE INFORMATION (1 OF 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	bbbbH[2]	2	Default number of sectors per track
7-8	bbbbH[3]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-14	eeeeH[4]	10	User-programmable serial number in ASCII
15-19	ddddH[5]	10	Greenliant preset, unique ID in ASCII
20	0000H	2	Retired
21	xxxxH	2	Vendor Unique
22	xxxxH	2	Vendor Unique
23-26	aaaaH[6]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[7]	40	User Definable Model number
47	8001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO Data Transfer Cycle Timing Mode
52	0000H	2	Reserved
53	0007H	2	Translation parameters are valid
54	nnnnH	2	Current numbers of cylinders
55	nnnnH	2	Current numbers of heads
56	nnnnH	2	Current sectors per track
57-58	nnnnH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010xH	2	Multiple sector setting
60-61	nnnnH	4	Total number of sectors addressable in LBA mode
62	0000H	2	Reserved
63	xx07H	2	DMA data transfer is supported in NAND Controller
64	0003H	2	Advanced PIO Transfer mode supported
65	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
66	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	00FEH	2	ATA major version number
81	0021H	2	ATA minor version number
82	706BH	2	Features/command sets supported
83	7408H	2	Features/command sets supported

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TABLE 7: IDENTIFY-DRIVE INFORMATION (CONTINUED) (2 OF 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	007FH	2	UDMA modes
89	xxxxH	2	Time required for security erase unit completion
90	xxxxH	2	Time required for enhanced security erase unit completion
91	0000H	2	Advanced Power Management Level value. This always returns 0000H.
92	0000H	2	Reserved
93	bbbbH	2	Hardware reset result
94-99	0000H	12	Reserved
100-103	nnnnH	8	Maximum user LBA for 48-bit Address feature set
104-127	0000H	48	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-216	0000H	114	Reserved
217	0001H	2	Nominal media rotation rate of the device
218-254	0000H	74	Reserved
255	bbA5H	2	Integrity word [15-8 Checksum, 7-0 Signature (A5H)]

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1. xxxx = Don't care. This field is subject to change by the host or the device.
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. eeee - the default value is '0000000000'
5. dddd - unique number of each device
6. aaaa - any unique Greenliant firmware revision
7. cccc - default value is "xxxMB ATA Flash Disk" or "xxxGB ATA Flash Disk" where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

Word 0: General Configuration This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

Word 1: Default Number of Cylinders This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track This field contains the number of sectors per track in the default translation mode.

Word 7-8: Number of Sectors This field contains the number of sectors per NAND Controller. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

Word 10-19: Serial Number The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are a Greenliant preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of 0000000000.

Word 23-26: Firmware Revision This field contains the revision of the firmware for this product.

Word 27-46: Model Number This field is reserved for the model number for this product.

Word 47: Read-/Write-Multiple Sector Count This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

Word 49: Capabilities BitFunction

13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: NAND Controller supports PIO Mode-4.
9	LBA support 1: NAND Controller supports LBA mode addressing.
8	DMA Support 1: DMA mode is supported.

Word 51: PIO Data Transfer Cycle Timing Mode This field contains the mode for PIO data transfer. NAND Controller supports PIO Mode-4.

Word 53: Translation Parameters Valid BitFunction

0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-3 and -4.
2	1: words 88 are valid to support Ultra DMA data transfer.

Word 54-56: Current Number of Cylinders, Heads, Sectors/Track These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Word 57-58: Current Capacity This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

Word 60-61: Total Sectors Addressable in LBA Mode This field contains the number of sectors addressable for the NAND Controller in LBA mode only.

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Word 63: Multi-word DMA Transfer Mode This field identifies the multi-word DMA transfer modes supported by the NAND Controller and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function
15-11	Reserved
10	Multi-word DMA mode 2 selected 1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-word DMA mode 2 is not selected.
9	Multi-word DMA mode 1 selected 1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0. 0: Multi-word DMA mode 1 is not selected.
8	Multi-word DMA mode 0 selected 1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0. 0: Multi-word DMA mode 0 is not selected.
7-3	Reserved
2	Multi-word DMA mode 2 supported 1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1	Multi-word DMA mode 1 supported 1: Multi-word DMA mode 1 and below are supported.
0	Multi-word DMA mode 0 supported 1: Multi-word DMA mode 0 is supported.

Word 64: Advanced PIO Data Transfer Mode Bits [7:0] is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits [7:2] are Reserved for future PIO modes.

Bit	Function
0	1: NAND Controller supports PIO Mode-3.
1	1: NAND Controller supports PIO Mode-4.

Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the NAND Controller supports when performing Multi-word DMA transfers on a per word basis. NAND Controller supports Multi-word DMA Mode-2, so this field is set to 120ns.

Note: NAND Controller is capable of supporting Multi-word DMA Mode-2 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 66: Device Recommended Multi-word DMA Cycle Time This field defines the NAND Controller recommended Multi-word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the NAND Controller may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. NAND Controller supports Multi-word DMA Mode-2, so this field is set to 120ns.

Note: NAND Controller is capable of supporting Multi-word DMA Mode-2 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 67: Minimum PIO Transfer Cycle Time Without Flow Control This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one.NAND Controller supports PIO Mode-4, so this field is set to 120ns.

Note: NAND Controller is capable of supporting PIO Mode-4 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 68: Minimum PIO Transfer Cycle Time With IORDY This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. NAND Controller supports PIO Mode-4, so this field is set to 120ns.

Note: NAND Controller is capable of supporting PIO Mode-4 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 80: Major Version Number If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits [6:1] being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. GLS55LD040M supports ATA-1 to ATA-7.

Word 81: Minor Version Number If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 should be 0000H or FFFFH.

A value of 0021H reported in word 81 indicates ATA-7 T13/1532D volume 1, revision 4b guided the implementation.

Words 82-84: Features/command sets supported Words 82, 83, and 84 indicate the features and command sets supported. A value of 706BH is reported.

Word 82	Bit	Function
	15	0: Obsolete
	14	1: NOP command is supported
	13	1: Read Buffer command is supported
	12	1: Write Buffer command is supported
	11	0: Obsolete
	10	0: Host Protected Area feature set is not supported
	9	0: Device Reset command is not supported
	8	0: Service interrupt is not supported
	7	0: Release interrupt is not supported
	6	1: Look-ahead is supported
	5	1: Write cache is supported
	4	0: Packet Command feature set is not supported
	3	1: Power Management feature set is supported
	2	0: Removable Media feature set is not supported
	1	1: Security Mode feature set is supported
	0	1: SMART feature set is supported

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Word 83 The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13	1: Flush Cache Ext command supported
12	1: Mandatory Flush Cache command supported
11	0: Device Configuration Overlay feature set not supported
10	1: 48-bit Address feature set supported
9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is supported. However, it is No Operation (NOP), and Word 91 will always return 0000H.
2	0: CFA feature set is not supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84 The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Words 85-87: Features/command sets enabled Words 85, 86, and 87 indicate features/command sets enabled. The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85	Bit	Function
	15	0: Obsolete
	14	0: NOP command is not enabled 1: NOP command is enabled
	13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
	12	0:Write Buffer command is not enabled 1: Write Buffer command is enabled
	11	0: Obsolete
	10	1: Host Protected Area feature set is enabled
	9	0: Device Reset command is not enabled
	8	0: Service interrupt is not enabled
	7	0: Release interrupt is not enabled
	6	0: Look-ahead is not enabled 1: Look-ahead is enabled
	5	0: Write cache is not enabled 1: Write cache is enabled
	4	0: Packet Command feature set is not enabled
	3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
	2	0: Removable Media feature set is not enabled
	1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
	0	0: SMART feature set is not enabled

Word 86	Bit	Function
	15-14	0: Reserved
	13	1: Flush Cache Ext command supported
	12	1: Mandatory Flush Cache command supported
	11	0: Device Configuration Overlay feature set not supported
	10	1: 48-bit Address feature set supported
	9	0: Reserved
	8	1: Set-Max security extension supported
	7-5	0: Reserved
	4	0: Removable Media Status feature set is not enabled
	3	0: Advanced Power Management feature set is not enabled
	2	0: CFA feature set is disabled
	1	0: Read DMA Queued and Write DMA Queued commands are not enabled
	0	0: Download Microcode command is not enabled

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Word 87 The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Word 88

Bit	Function
15	Reserved
14	1: Ultra DMA mode 6 is selected
	0: Ultra DMA mode 6 is not selected
13	1: Ultra DMA mode 5 is selected
	0: Ultra DMA mode 5 is not selected
12	1: Ultra DMA mode 4 is selected
	0: Ultra DMA mode 4 is not selected
11	1: Ultra DMA mode 3 is selected
	0: Ultra DMA mode 3 is not selected
10	1: Ultra DMA mode 2 is selected
	0: Ultra DMA mode 2 is not selected
9	1: Ultra DMA mode 1 is selected
	0: Ultra DMA mode 1 is not selected
8	1: Ultra DMA mode 0 is selected
	0: Ultra DMA mode 0 is not selected
7	Reserved
6	1: Ultra DMA mode 6 and below supported
5	1: Ultra DMA mode 5 and below supported
4	1: Ultra DMA mode 4 and below are supported
3	1: Ultra DMA mode 3 and below are supported
2	1: Ultra DMA mode 2 and below are supported
1	1: Ultra DMA mode 1 and below are supported
0	1: Ultra DMA mode 0 is supported

Word 89: Time required for Security erase unit completion Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 90: Time required for Enhanced security erase unit completion Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 91: Advanced Power Management NAND Controller support level value is 0000H.

Word 93: Hardware reset result BitFunction

The contents of bits [12:0] of this word will change only during the execution of the hardware reset.

15 Shall be cleared to zero

14 Shall be set to one

13 1: Device detected CBLID - above VIH

0: Device detected CBLIP - below VIL

12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:

- 12 Reserved.
- 11 0: Device 1 did not assert PDIAG-.
  1: Device 1 asserted PDIAG-.
- 10-9 These bits indicate how Device 1 determined the device number:
  00: Reserved.
  01: A jumper was used.
  10: The CSEL signal was used.
  11: Some other method was used or the method is unknown.
- 8 Shall be set to one.

7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:

- 7 Reserved.
- 6 0: Device 0 does not respond when Device 1 is selected.
  1: Device 0 responds when Device 1 is selected.
- 5 0: Device 0 did not detect the assertion of DASP-.
  1: Device 0 detected the assertion of DASP-.
- 4 0: Device 0 did not detect the assertion of PDIAG-.
  1: Device 0 detected the assertion of PDIAG-.
- 3 0: Device 0 failed diagnostics.
  1: Device 0 passed diagnostics.
- 2-1 These bits indicate how Device 0 determined the device number:
  00: Reserved.
  01: A jumper was used.
  10: The CSEL signal was used.
  11: Some other method was used or the method is unknown.
- 0 Shall be set to one.

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Word 128: Security Status BitFunction

8	Security Level 1: Security mode is enabled and the security level is maximum 0: and security mode is enabled, indicates that the security level is high
5	Enhanced security erase unit feature supported 1: Enhanced security erase unit feature set is supported
4	Expire 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset
3	Freeze 1: Security is frozen
2	Lock 1: Security is locked
1	Enable/Disable 1: Security is enabled 0: Security is disabled
0	Capability 1: NAND Controller supports security mode feature set 0: NAND Controller does not support security mode feature set

Word 217: Nominal Media Rotation Rate Word 217 indicates the nominal media rotation rate of the device. For NAND Controller, the value is always 0001H for this field to indicate non-rotating media.

Word 255: Integrity Word Word 255 is optional. When bits [7:0] of this word contain the signature A5h, bits [15:8] contain the data-structure checksum. The data-structure checksum value is the two's complement of the sum of all bytes in words [254:0] and the byte consisting of bits [7:0] in word 255. Add each byte with unsigned arithmetic, and ignore overflow. When the checksum is correct, the sum of all 512 bytes is zero.

Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 8 defines all features that are supported.

TABLE 8: FEATURES SUPPORTED

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache.
03H	Set transfer mode based on value in Sector Count register. Table 9 defines the values.
05H	Enable Advanced Power Management.
09H	Enable Extended Power Operations.
55H	Disable Read Look Ahead.
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H	Disable Write Cache.
85H	Disable Advanced Power Management.
89H	Disable Extended Power operations.
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
AAH	Enable Read-Look-Ahead.
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

T8.0 1408

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the NAND Controllers that implement write cache. When the subcommand Disable-Write-Cache is issued, the NAND Controller should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the NAND Controller. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

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Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

TABLE 9: TRANSFER MODE VALUES

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multi-word DMA mode	00100b	mode[1]
Ultra-DMA mode	01000b	mode[1]
Reserved	Other	N/A

T9.1 1408

1. Mode = transfer mode number, all other values are not valid

Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the NAND Controller to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NAND Controller to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

Set-WP#/PD#-Mode - 8BH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8BH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	6EH							
Cyl Low (4)	44H							
Sec Num (3)	72H							
Sec Cnt (2)	50H							
Feature (1)	55H or AAH							

This command configures the WP#/PD# pin for either the Write Protect mode or the Power-down mode. When the host sends this command to the device with the value AAH in the feature register, the WP#/PD# pin is configured for the Write Protect mode. The Write Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP#/PD# is configured for the Power-down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

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Error Posting

The following table summarizes the valid status and error values for the NAND Controller command set.

TABLE 10: ERROR AND STATUS REGISTER[1] (1 OF 2)

Command	Error Register					Status Register				
	ICRC/ BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic[2]						V		V		V
Flush-Cache				V		V	V	V		V
Flush-Cache-EXT				V		V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-DMA-EXT	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Multiple-EXT	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)-EXT	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)-EXT	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP#/PD#-Mode				V		V		V		V
SMART				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-DMA-EXT	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V

TABLE 10: ERROR AND STATUS REGISTER[1] (CONTINUED) (2 OF 2)

Command	Error Register					Status Register				
	ICRC/ BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Write-Multiple-EXT	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-EXT	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

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1. The host is required to reissue any media access command (such as Read-Sector and Write Sector) that ends with an error condition.
2. See Table 7
   V = valid on this command.

Advance Information

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Storage Temperature . . . . . -55°C to +125°C
D.C. Voltage on any pin to Ground Potential . . . . . -0.5V to V_{DD}/V_{DDQ}+0.5V
Transient Voltage (<20 ns) on any pin to Ground Potential . . . . . -2.0V to V_{DD}/V_{DDQ}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1] . . . . . 60 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 11: OPERATING RANGE

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.135-3.465V
Industrial	-40°C to +85°C	3.135-3.465V

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TABLE 12: AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load (FRE#, FWE#)	C_L = 180 pF
Output Load (all others)	C_L = 50 pF
See Figure 4	

Note: All AC specifications are guaranteed by design.

TABLE 13: ABSOLUTE MAXIMUM POWER PIN STRESS RATINGS

Parameter	Symbol	Conditions
Input Power	V_{DDQ}	-0.3V min to 4.0V max
	$V_{DD(core)}$ and $V_{DD(I/O)}$	-0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

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TABLE 14: RECOMMENDED SYSTEM POWER-ON TIMING

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$	Drive Initialization to Ready	7 sec for 16 GByte	100[1]	sec
$T_{PU-READ1}$[2]	Host Power-on/Reset to Read Operation	700	2000	ms
$T_{PU-WRITE1}$[2]	Host Power-on/Reset to Write Operation	700	2000	ms

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1. 100 seconds maximum for 32 GByte
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 15: CAPACITANCE (T_A = 25°C, f=1 MHz, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 16: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

DC Characteristics

TABLE 17: DC CHARACTERISTICS FOR HOST INTERFACE

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1}	I1	Input Voltage	2		V	V_{DDQ}=V_{DDQ} Max
V_{IL1}				0.8	V	V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	µA	V_I =V_{DDQ} Max or 0V
I_{U1}	I1U	Input Pull-Up Current	-120	-20	µA	V_{DDQ}=V_{DDQ} Max, V_{IN} = GND
V_{T+}	I2	Input Voltage Schmitt Trigger		1.75	V	V_{DDQ} = V_{DDQ} Max
V_{T-}			1.09		V	V_{DDQ} = V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	µA	V_I = V_{DDQ} Max or 0V
I_{U2}	I2U	Input Pull-Up Current	-120	-20	µA	V_{DDQ}=V_{DDQ} Max, V_{IN} = GND
V_{OH2}	O2	Output Voltage	2.4		V	I_{OH2}=I_{OH2} Min
V_{OL2}				0.4	V	I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL2}				4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH3}	O3	Output Voltage	2.4		V	I_{OH3}=I_{OH3}Min
V_{OL3}				0.4	V	I_{OL3}=I_{OL3} Max
I_{OH3}		Output Current	-8		mA	V_{DDQ}=V_{DDQ} Min
I_{OL3}				8	mA	V_{DDQ}=V_{DDQ} Min
V_{OH4}	O4	Output Voltage	2.4		V	I_{OH4}=I_{OH4} Min
V_{OL4}				0.4	V	I_{OL4}=I_{OL4} Max
I_{OH4}		Output Current	-8		mA	V_{DDQ}=V_{DDQ} Min
I_{OL4}				12	mA	V_{DDQ}=V_{DDQ} Min
I_{DD}	PWR	Power Supply Current (T_A = 0°C -+70°C)		100	mA	V_{DD} = V_{DD} Max, V_{DDQ} = V_{DDQ} Max
		Power Supply Current (T_A = -40°C -+85°C)		150	mA	V_{DD} = V_{DD} Max, V_{DDQ} = V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle Current (T_A = 0°C -+70°C)		3	mA	V_{DD} = V_{DD} Max, V_{DDQ} = V_{DDQ} Max
		Sleep/Standby/Idle Current (T_A = -40°C -+85°C)		5	mA	V_{DD} = V_{DD} Max, V_{DDQ} = V_{DDQ} Max

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TABLE 18: DC CHARACTERISTICS FOR MEDIA INTERFACE

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH3}	I3	Input Voltage	2		V	V_{DD}=V_{DDIO} Max, V_{IN} = GND
V_{IL3}				0.8	V	V_{DD}=V_{DD} Min
I_{U3}	I3U	Input Pull-Up Current	-120	-20	µA	V_{DDIO}=V_{DDIO} Max, V_{IN} = GND
I_{D3}	I3D	Input Pull-Down Current	20	120	µA	V_{DDIO}=V_{DDIO} Max, V_{IN} = V_{DDIO} Max
V_{T+}	I4	Input Voltage Schmitt Trigger		1.75	V	V_{DDIO} = V_{DDIO} Max
V_{T-}			1.09		V	V_{DDIO} = V_{DDIO} Min
I_{IL4}	I4Z	Input Leakage Current	-10	10	µA	V_I = V_{DDIO} Max or 0V
I_{U4}	I4U	Input Pull-Up Current	-120	-20	µA	V_{DDIO}=V_{DDIO} Max, V_{IN} = GND
V_{OH5}	O5	Output Voltage	2.4		V	I_{OH5}=I_{OH5} Min
V_{OL5}				0.4	V	I_{OL5}=I_{OL5} Max
I_{OH5}		Output Current	-2		mA	V_{DDIO}=V_{DDIO} Min
I_{OL5}				2	mA	V_{DDIO}=V_{DDIO} Min
V_{OH6}	O6	Output Voltage	2.4		V	I_{OH6}=I_{OH6}Min
V_{OL6}				0.4	V	I_{OL6}=I_{OL6} Max
I_{OH6}		Output Current	-4		mA	V_{DDIO}=V_{DDIO} Min
I_{OL6}				4	mA	V_{DDIO}=V_{DDIO} Min
V_{OH7}	O7	Output Voltage	2.4		V	I_{OH7}=I_{OH7} Min
V_{OL7}				0.4	V	I_{OL7}=I_{OL7} Max
I_{OH7}		Output Current	-8		mA	V_{DDIO}=V_{DDIO} Min
I_{OL7}				8	mA	V_{DDIO}=V_{DDIO} Min

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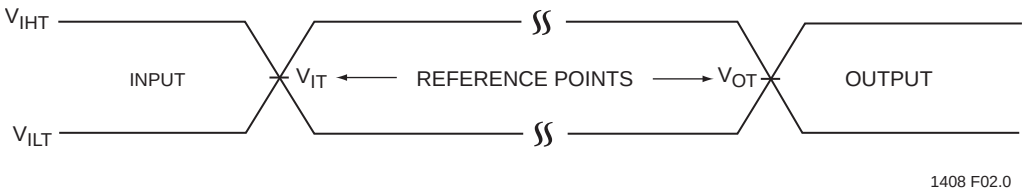
AC Characteristics



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 4: AC Input/Output Reference Waveforms

Media Side Interface Timing Specifications

TABLE 19: GLS55LD040M TIMING SPECIFICATIONS (25NS FLASH MEDIA ONLY)

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	6	-	ns
T_{CLH}	FCLE Hold Time	25	-	ns
T_{CS}	FCE# Setup Time	40	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	25	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{ALS}	FALE Setup Time	6	-	ns
T_{ALH}	FALE Hold Time	25	-	ns
T_{WP}	FWE# Pulse Width	12	-	ns
T_{WH}	FWE# High Hold Time	10	-	ns
T_{WC}	Write Cycle Time	26	-	ns
T_{DS}	FAD[15:0] Setup Time	12	-	ns
T_{DH}	FAD[15:0] Hold Time	8	-	ns
T_{RP}	FRE# Pulse Width	12	-	ns
T_{RR}	Ready to FRE# Low	20	-	ns
T_{REA}	FRE# Data Setup Time	-	15	ns
T_{REH}	FRE# High Hold Time	8	-	ns
T_{RC}	Read Cycle Time	26	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	-	100	ns

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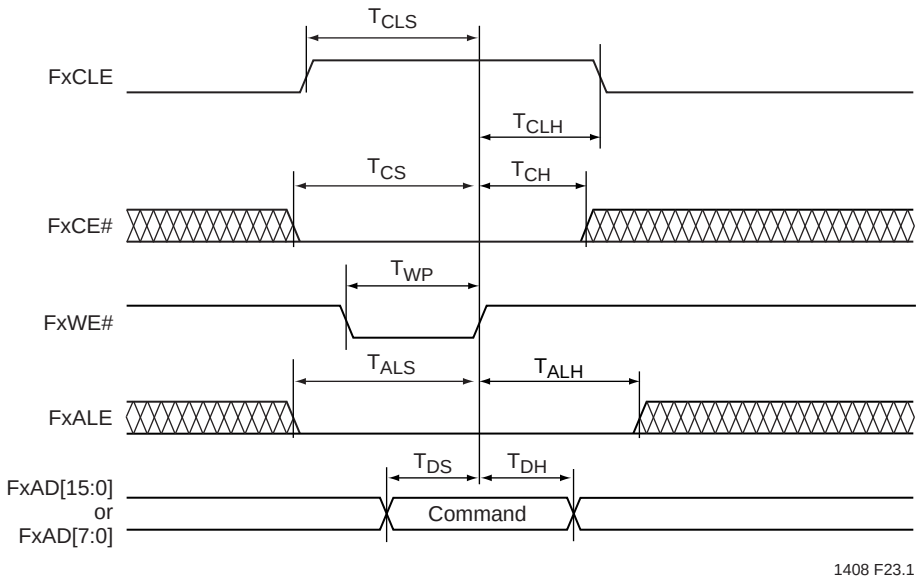
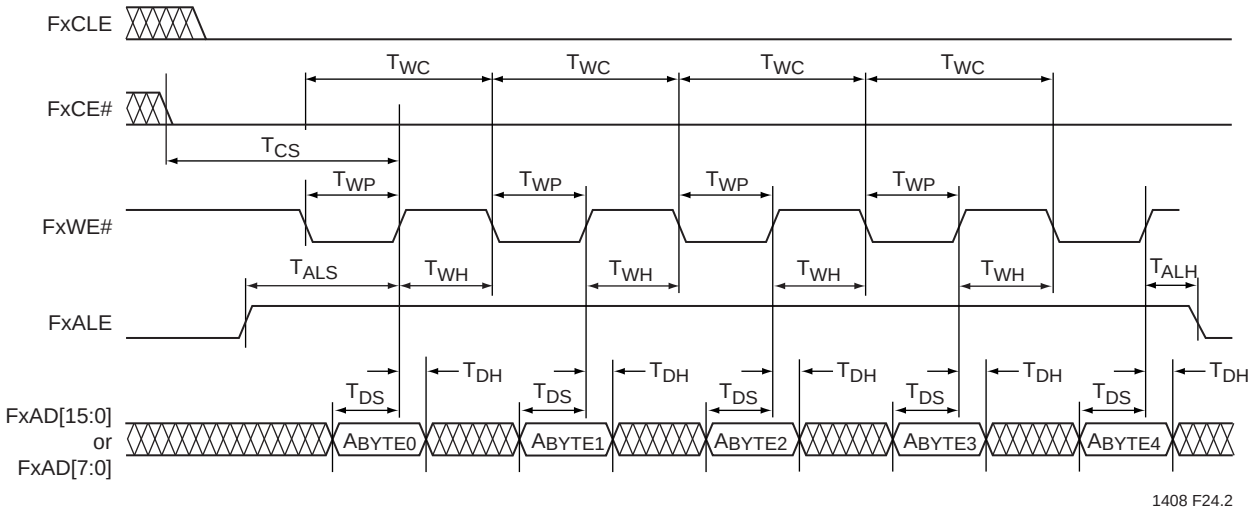
Note: All AC specifications are guaranteed by design.
GLS55LD040M can be programed to access 20ns to 50ns Flash media. Please refer to Greenliant application notes for timing details.

Advance Information



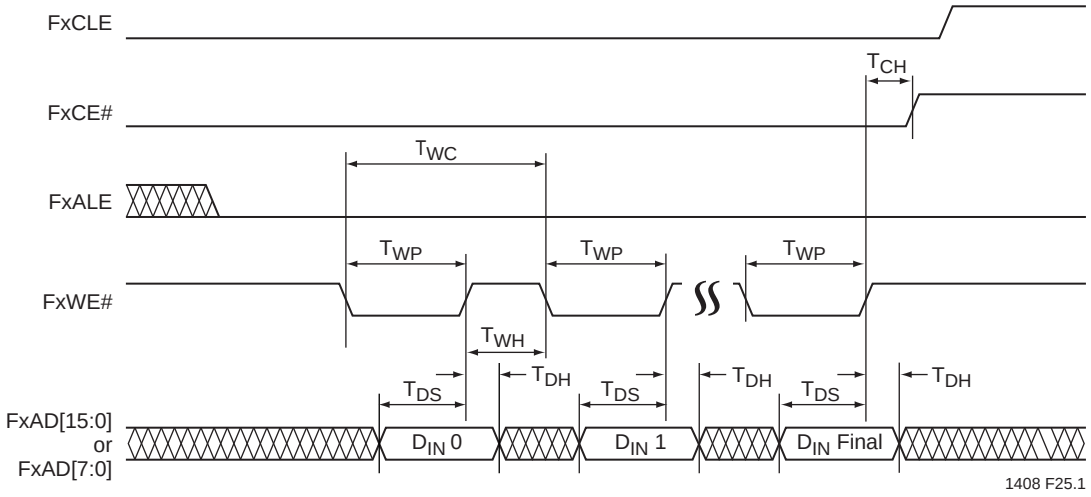
Note: In signal names, x = either 0 or 1.

FIGURE 5: Media Command Latch Cycle



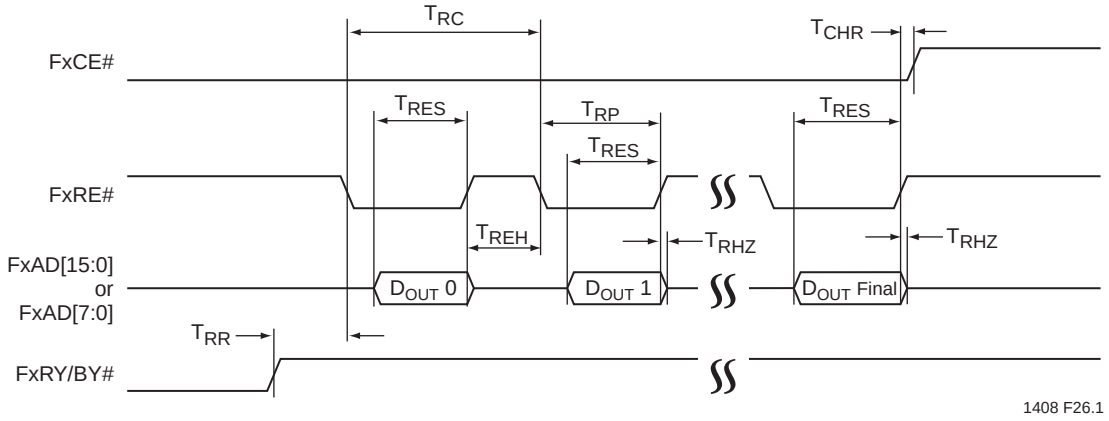
Note: In signal names, x = either 0 or 1.

FIGURE 6: Media Address Latch Cycle



Note: In signal names, x = either 0 or 1.

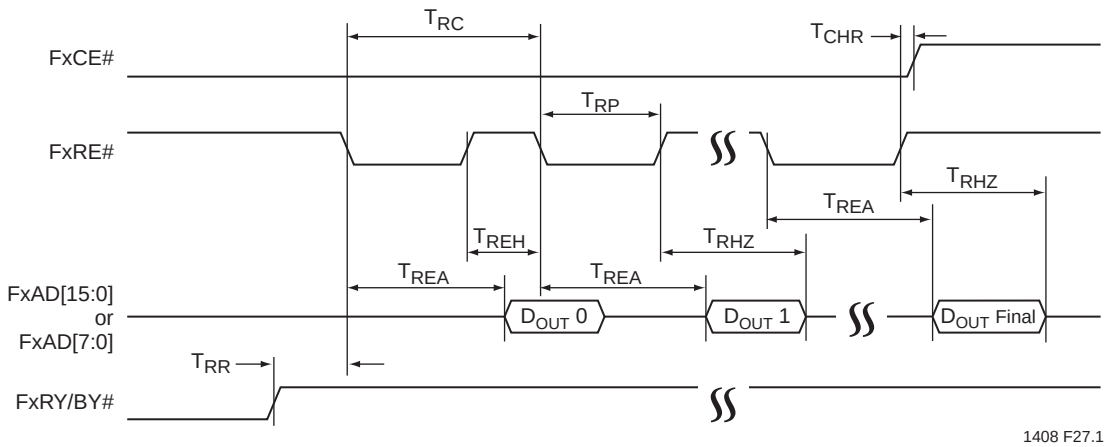
FIGURE 7: Media Data Loading Latch Cycle



Note: In signal names, x = either 0 or 1.
FxRY/BY# is the signal from the flash media's Ready/Busy pin.

FIGURE 8: Media Data Read Cycle in Normal Mode

Advance Information

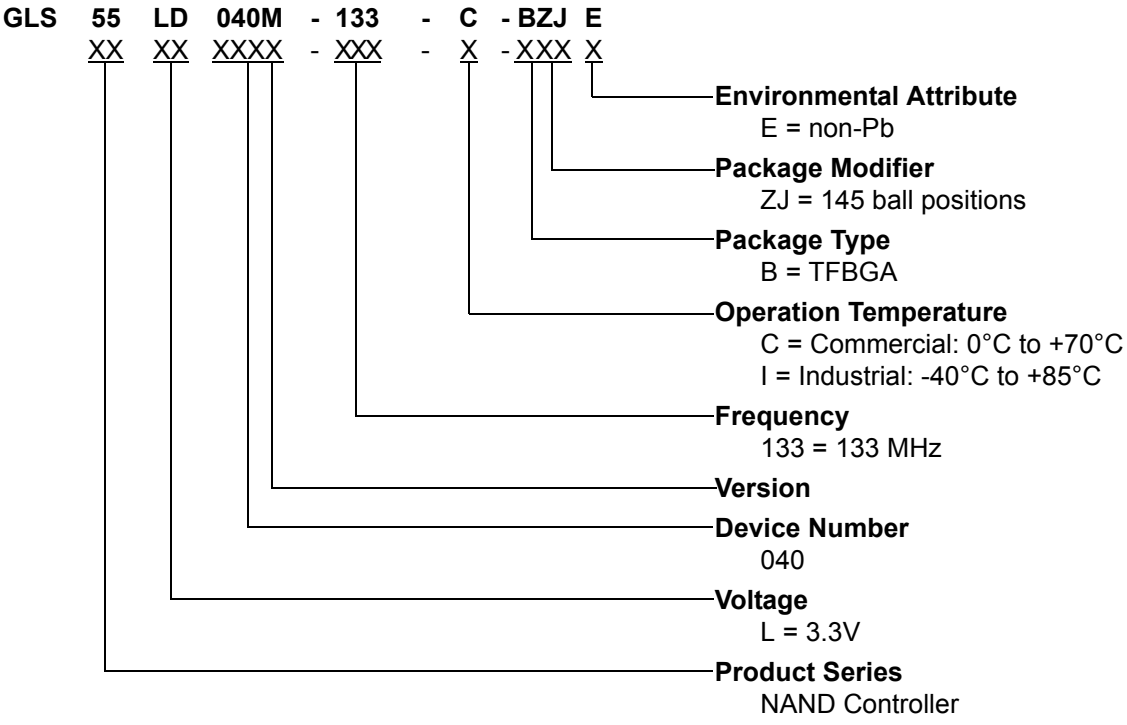


Note: In signal names, x = either 0 or 1.
FxRY/BY# is the signal from the flash media's Ready/Busy pin.

FIGURE 9: Media Data Read Cycle in Extended Data Out (EDO) Mode

Advance Information

PRODUCT ORDERING INFORMATION



Valid Combinations

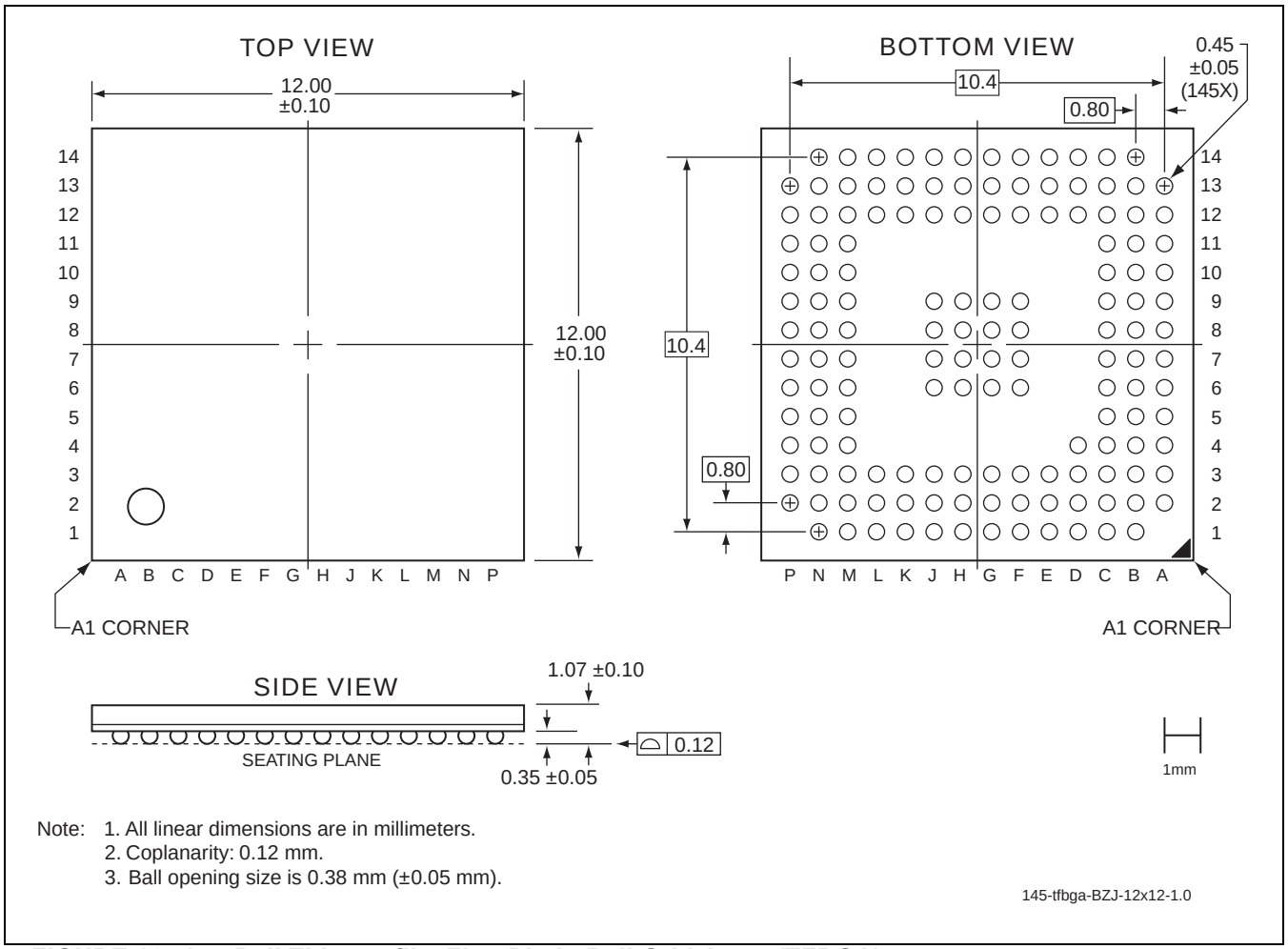
Valid combinations for GLS55LD040M

GLS55LD040M-133-I-BZJE GLS55LD040M-133-C-BZJE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Advance Information

PACKAGING DIAGRAM



Note: 1. All linear dimensions are in millimeters.
2. Coplanarity: 0.12 mm.
3. Ball opening size is 0.38 mm (±0.05 mm).

145-tfbga-BZJ-12x12-1.0

FIGURE 10: 145-Ball Thin-profile, Fine-Pitch, Ball Grid Array (TFBGA)
Greenliant Package Code: BZJ

Revision History

Number	Description	Date
00	• Initial Release Advance Information	Sep 2009
01	• Revised Features • Updated Table 2 on page 11 • Revised “Power-down Mode” on page 13. • Replaced “Software Interface” on page 15. • Updated Tables 3, 11, 14, 17 • Revised“Absolute Maximum Stress Ratings” on page 32.	Apr 2010
02	• Transferred from SST to Greenliant	May 2010

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