FEATURES:

- Organized as 256K x8 / 512K x8
- Single Voltage Read and Write Operations
  - 4.5-5.5V for GLS29SF020/040
  - 2.7-3.6V for GLS29VF020/040
- Superior Reliability
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- Low Power Consumption:
  - Active Current: 10 mA (typical)
  - Standby Current:
    - 30 µA (typical) for GLS29SF020/040
    - 1 µA (typical) for GLS29VF020/040
- Sector-Erase Capability
  - Uniform 128 Byte sectors
- Fast Read Access Time:
  - 55 ns for GLS29SF020/040
  - 70 ns for GLS29VF020/040
- Latched Address and Data
- Fast Erase and Byte-Program:
  - Sector-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time:
    - 4 seconds (typical) for GLS29SF/VF020
    - 8 seconds (typical) for GLS29SF/VF040
- Automatic Write Timing
  - Internal Vpp Generation
- End-of-Write Detection
  - Toggle Bit
  - Data# Polling
- TTL I/O Compatibility for GLS29SF020/040
- CMOS I/O Compatibility for GLS29VF020/040
- JEDEC Standard
  - Flash EEPROM Pinouts and command sets
- Packages Available
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
- All non-Pb (lead-free) devices are RoHS compliant

PRODUCT DESCRIPTION

The GLS29SF020/040 and GLS29VF020/040 are 256K x8 / 512K x8 CMOS Small-Sector Flash (SSF) manufactured with high-performance SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The GLS29SF020/040 devices write (Program or Erase) with a 4.5-5.5V power supply. The GLS29VF020/040 devices write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pin assignments for x8 memories.

Featuring high performance Byte-Program, the GLS29SF020/040 and GLS29VF020/040 devices provide a maximum Byte-Program time of 20 µsec. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of at least 10,000 cycles. Data retention is rated at greater than 100 years.

The GLS29SF020/040 and GLS29VF020/040 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. They also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.
Device Operation
Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read
The Read operation of the GLS29SF020/040 and GLS29VF020/040 devices are controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram in Figure 4 for further details.

Byte-Program Operation
The GLS29SF020/040 and GLS29VF020/040 devices are programmed on a byte-by-byte basis. Before programming, the sector where the byte exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation
The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The GLS29SF020/040 and GLS29VF020/040 offer Sector-Erase mode. The sector architecture is based on uniform sector size of 128 Bytes. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (20H) and sector address (SA) in the last bus cycle. The sector address is latched on the falling edge of the sixth WE# pulse, while the command (20H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. For timing waveforms, see Figure 9. Any commands issued during the Sector-Erase operation are ignored.

Chip-Erase Operation
The GLS29SF020/040 and GLS29VF020/040 devices provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1s” state. This is useful when the entire device must be quickly erased.

Write Operation Status Detection
The GLS29SF020/040 and GLS29VF020/040 devices provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ7) and Toggle Bit (DQ6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ7 or DQ6. In order to pre-
vent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

**Data# Polling (DQ7)**

When the GLS29SF020/040 and GLS29VF020/040 devices are in the internal Program operation, any attempt to read DQ7 will produce the complement of the true data. Once the Program operation is completed, DQ7 will produce true data. Note that even though DQ7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read DQ7 will produce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling timing diagram and Figure 17 for a flowchart.

**Toggle Bit (DQ6)**

During the internal Program or Erase operation, any consecutive attempts to read DQ6 will produce alternating ‘0’s and ‘1’s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 8 for Toggle Bit timing diagram and Figure 17 for a flowchart.

**Data Protection**

The GLS29SF020/040 and GLS29VF020/040 devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

**Hardware Data Protection**

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 2.5V for GLS29SF020/040. The Write operation is inhibited when $V_{DD}$ is less than 1.5V for GLS29VF020/040.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

**Software Data Protection (SDP)**

The GLS29SF020/040 and GLS29VF020/040 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of a six-byte load sequence. These devices are shipped with the Software Data Protection permanently enabled. The specific software command codes are shown in Table 4. During SDP command sequence, invalid commands will abort the device to read mode, within $T_{RC}$.

**Product Identification**

The Product Identification mode identifies the devices as GLS29SF020, GLS29SF040 and GLS29VF020, GLS29VF040 and manufacturer as Greenliant. This mode may be accessed by software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 4 for
software operation, Figure 11 for the Software ID Entry and Read timing diagram, and Figure 18 for the Software ID Entry command sequence flowchart.

### TABLE 1: Product Identification

<table>
<thead>
<tr>
<th>Product ID</th>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer’s ID</td>
<td>0000H</td>
<td>BFH</td>
</tr>
<tr>
<td>Device ID</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GLS29SF020</td>
<td>0001H</td>
<td>24H</td>
</tr>
<tr>
<td>GLS29VF020</td>
<td>0001H</td>
<td>25H</td>
</tr>
<tr>
<td>GLS29SF040</td>
<td>0001H</td>
<td>13H</td>
</tr>
<tr>
<td>GLS29VF040</td>
<td>0001H</td>
<td>14H</td>
</tr>
</tbody>
</table>

---

**Product Identification Mode Exit/Reset**

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read operation. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 12 for timing waveform, and Figure 18 for a flowchart.

---

**FIGURE 1: Functional Block Diagram**
FIGURE 2: Pin Assignments for 32-lead PLCC

FIGURE 3: Pin Assignments for 32-lead TSOP (8mm x 14mm)
TABLE 2: Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Name</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>A&lt;sub&gt;MS&lt;/sub&gt;-A&lt;sub&gt;0&lt;/sub&gt;</td>
<td>Address Inputs</td>
<td>To provide memory addresses. During Sector-Erase A&lt;sub&gt;MS&lt;/sub&gt;-A&lt;sub&gt;8&lt;/sub&gt; address lines will select the sector.</td>
</tr>
<tr>
<td>DQ7-DQ0</td>
<td>Data Input/output</td>
<td>To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.</td>
</tr>
<tr>
<td>CE#</td>
<td>Chip Enable</td>
<td>To activate the device when CE# is low.</td>
</tr>
<tr>
<td>OE#</td>
<td>Output Enable</td>
<td>To gate the data output buffers.</td>
</tr>
<tr>
<td>WE#</td>
<td>Write Enable</td>
<td>To control the Write operations.</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>Power Supply</td>
<td>To provide power supply voltage: 4.5-5.5V for GLS29SF020/040 2.7-3.6V for GLS29VF020/040</td>
</tr>
<tr>
<td>V&lt;sub&gt;SS&lt;/sub&gt;</td>
<td>Ground</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>No Connection</td>
<td>Pin not connected internally</td>
</tr>
</tbody>
</table>

1. A<sub>MS</sub> = Most significant address
   A<sub>MS</sub> = A<sub>17</sub> for GLS29SF/VF020 and A<sub>18</sub> for GLS29SF/VF040

TABLE 3: Operation Modes Selection

<table>
<thead>
<tr>
<th>Mode</th>
<th>CE#</th>
<th>OE#</th>
<th>WE#</th>
<th>DQ</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>DOUT</td>
<td>A&lt;sub&gt;IN&lt;/sub&gt;</td>
</tr>
<tr>
<td>Program</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>DIN</td>
<td>A&lt;sub&gt;IN&lt;/sub&gt;</td>
</tr>
<tr>
<td>Erase</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>X&lt;sup&gt;1&lt;/sup&gt;</td>
<td>Sector address, XXH for Chip-Erase</td>
</tr>
<tr>
<td>Standby</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>X</td>
</tr>
<tr>
<td>Write Inhibit</td>
<td>X</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>X</td>
<td>High Z/ DOUT</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>High Z/ DOUT</td>
<td>X</td>
</tr>
<tr>
<td>Product Identification</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>See Table 4</td>
<td></td>
</tr>
</tbody>
</table>

1. X can be V<sub>IL</sub> or V<sub>IH</sub>, but no other value.
TABLE 4: Software Command Sequence

<table>
<thead>
<tr>
<th>Command Sequence</th>
<th>1st Bus Write Cycle</th>
<th>2nd Bus Write Cycle</th>
<th>3rd Bus Write Cycle</th>
<th>4th Bus Write Cycle</th>
<th>5th Bus Write Cycle</th>
<th>6th Bus Write Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr(^1) Data</td>
<td>Addr(^1) Data</td>
<td>Addr(^1) Data</td>
<td>Addr(^1) Data</td>
<td>Addr(^1) Data</td>
<td>Addr(^1) Data</td>
</tr>
<tr>
<td>Byte-Program</td>
<td>555H AAH 2AAH 55H</td>
<td>555H A0H BA</td>
<td>Data</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sector-Erase</td>
<td>555H AAH 2AAH 55H</td>
<td>555H 80H AAH</td>
<td>555H AAH</td>
<td>2AAH 55H</td>
<td>555H 10H</td>
<td>SA(^3) 20H</td>
</tr>
<tr>
<td>Chip-Erase</td>
<td>555H AAH 2AAH 55H</td>
<td>555H 80H</td>
<td>555H AAH</td>
<td>2AAH 55H</td>
<td>555H 10H</td>
<td></td>
</tr>
<tr>
<td>Software ID Entry(^4,5)</td>
<td>555H AAH 2AAH 55H</td>
<td>555H 90H</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software ID Exit(^6)</td>
<td>XXH F0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Software ID Exit(^6)</td>
<td>555H AAH 2AAH 55H</td>
<td>555H F0H</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. Address format A\(_{14}\)-A\(_0\) (Hex).
   Addresses A\(_{15}\)-AMS can be V\(_{IL}\) or V\(_{IH}\), but no other value, for the Command sequence for GLS29SF/VF020/040.
   AMS = Most significant address
   AMS = A\(_{17}\) for GLS29SF/VF020 and A\(_{18}\) for GLS29SF/VF040.
2. BA = Program Byte address
3. SA\(_X\) for Sector-Erase; uses AMS-A\(_7\) address lines for GLS29SF/VF020/040
4. The device does not remain in Software Product ID mode if powered down.
5. With AMS-A\(_1\) = 0; Greenliant Manufacturer’s ID = BFH, is read with A\(_0\) = 0,
   GLS29SF020 Device ID = 24H, is read with A\(_0\) = 1
   GLS29VF020 Device ID = 25H, is read with A\(_0\) = 1
   GLS29SF040 Device ID = 13H, is read with A\(_0\) = 1
   GLS29VF040 Device ID = 14H, is read with A\(_0\) = 1
6. Both Software ID Exit operations are equivalent
Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

- Temperature Under Bias: -55°C to +125°C
- Storage Temperature: -65°C to +150°C
- D. C. Voltage on Any Pin to Ground Potential: -0.5V to VDD+0.5V
- Voltage on A9 Pin to Ground Potential: -5.0V to 13.2V
- Package Power Dissipation Capability (TA = 25°C): 1.0W
- Through Hole Lead Soldering Temperature (10 Seconds): 300°C
- Surface Mount Solder Reflow Temperature: 260°C for 10 seconds
- Output Short Circuit Current: 50 mA

Operating Range for GLS29SF020/040

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temp</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>4.5-5.5V</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>4.5-5.5V</td>
</tr>
</tbody>
</table>

Operating Range for GLS29VF020/040

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temp</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>2.7-3.6V</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>2.7-3.6V</td>
</tr>
</tbody>
</table>

AC Conditions of Test

- Input Rise/Fall Time: 5 ns
- Output Load: CL = 30 pF for 55 ns
- Output Load: CL = 100 pF for 70 ns
- See Figures 13, 14, and 15

TABLE 5: DC Operating Characteristics VDD = 4.5-5.5V for GLS29SF020/040

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idd</td>
<td>Power Supply Current</td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td>Read</td>
<td>25 mA</td>
<td>VDD=VDD Max</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>30 mA</td>
<td>CE#=OE#=VIL, WE#=VIH, all I/Os open</td>
</tr>
<tr>
<td>isb1</td>
<td>Standby VDD Current (TTL input)</td>
<td>3 mA</td>
<td>CE#=VIH, VDD=VDD Max</td>
</tr>
<tr>
<td>isb2</td>
<td>Standby VDD Current (CMOS input)</td>
<td>100 µA</td>
<td>CE#=VIH, VDD=VDD Max</td>
</tr>
<tr>
<td>l1</td>
<td>Input Leakage Current</td>
<td>1 µA</td>
<td>VIN=GND to VDD, VDD=VDD Max</td>
</tr>
<tr>
<td>l0</td>
<td>Output Leakage Current</td>
<td>10 µA</td>
<td>VOUT=GND to VDD, VDD=VDD Max</td>
</tr>
<tr>
<td>vil</td>
<td>Input Low Voltage</td>
<td>0.8 V</td>
<td>VDD=VDD Min</td>
</tr>
<tr>
<td>vih</td>
<td>Input High Voltage</td>
<td>VDD</td>
<td>VDD=VDD Max</td>
</tr>
<tr>
<td>vihc</td>
<td>Input High Voltage (CMOS)</td>
<td>VDD-0.3</td>
<td>VDD=VDD Max</td>
</tr>
<tr>
<td>vol</td>
<td>Output Low Voltage</td>
<td>0.4 V</td>
<td>VDD=VDD Min</td>
</tr>
<tr>
<td>voh</td>
<td>Output High Voltage</td>
<td>2.4 V</td>
<td>IOL=2.1 µA, VDD=VDD Min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IOH=400 µA, VDD=VDD Min</td>
</tr>
</tbody>
</table>
2 Mbit / 4 Mbit Small-Sector Flash
GLS29SF020 / GLS29SF040
GLS29VF020 / GLS29VF040
# TABLE 6: DC Operating Characteristics \( V_{DD} = 2.7\text{-}3.6\text{V} \) for GLS29VF020/040

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td>Power Supply Current</td>
<td></td>
<td>25 mA</td>
</tr>
<tr>
<td>I_D</td>
<td>Read</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td></td>
<td>30 mA</td>
</tr>
<tr>
<td>I_SB</td>
<td>Standby ( V_{DD} ) Current</td>
<td></td>
<td>30 µA</td>
</tr>
<tr>
<td>I_L</td>
<td>Input Leakage Current</td>
<td></td>
<td>1 µA</td>
</tr>
<tr>
<td>I_O</td>
<td>Output Leakage Current</td>
<td></td>
<td>10 µA</td>
</tr>
<tr>
<td>V_L</td>
<td>Input Low Voltage</td>
<td>0.8 V</td>
<td></td>
</tr>
<tr>
<td>V_H</td>
<td>Input High Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_HC</td>
<td>Input High Voltage (CMOS)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_O</td>
<td>Output Low Voltage</td>
<td>0.2 V</td>
<td></td>
</tr>
<tr>
<td>V_OH</td>
<td>Output High Voltage</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# TABLE 7: Recommended System Power-up Timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPU-READ(^1)</td>
<td>Power-up to Read Operation</td>
<td>100</td>
<td>µs</td>
</tr>
<tr>
<td>TPU-WRITE(^1)</td>
<td>Power-up to Program/Erase Operation</td>
<td>100</td>
<td>µs</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

# TABLE 8: Capacitance \( (T_A = 25^\circ C, f=1 \text{ Mhz}, \text{other pins open}) \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Condition</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{IO}(^1)</td>
<td>I/O Pin Capacitance</td>
<td>( V_{IO}=0) V</td>
<td>12 pF</td>
</tr>
<tr>
<td>C_{IN}(^1)</td>
<td>Input Capacitance</td>
<td>( V_{IN}=0) V</td>
<td>6 pF</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

# TABLE 9: Reliability Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum Specification</th>
<th>Units</th>
<th>Test Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>N_END(^1)</td>
<td>Endurance</td>
<td>10,000</td>
<td>Cycles</td>
<td>JEDEC Standard A117</td>
</tr>
<tr>
<td>T_DR(^1)</td>
<td>Data Retention</td>
<td>100</td>
<td>Years</td>
<td>JEDEC Standard A103</td>
</tr>
<tr>
<td>LUTH(^1)</td>
<td>Latch Up</td>
<td>100 + ( I_{DD} ) mA</td>
<td></td>
<td>JEDEC Standard 78</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
**AC CHARACTERISTICS**

**TABLE 10: Read Cycle Timing Parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>GLS29SF020/040-55</th>
<th>GLS29VF020/040-70</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>TRC</td>
<td>Read Cycle Time</td>
<td>55</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>TCE</td>
<td>Chip Enable Access Time</td>
<td>55</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>TAA</td>
<td>Address Access Time</td>
<td>55</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>TOE</td>
<td>Output Enable Access Time</td>
<td>30</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td>TCLZ¹</td>
<td>CE# Low to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TOLZ¹</td>
<td>OE# Low to Active Output</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TCHZ¹</td>
<td>CE# High to High-Z Output</td>
<td>20</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>TOHZ¹</td>
<td>OE# High to High-Z Output</td>
<td>20</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>TOH¹</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**TABLE 11: Program/Erase Cycle Timing Parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TB_P</td>
<td>Byte-Program Time</td>
<td></td>
<td>20</td>
<td>µs</td>
</tr>
<tr>
<td>TAS</td>
<td>Address Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TAH</td>
<td>Address Hold Time</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCS</td>
<td>WE# and CE# Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCH</td>
<td>WE# and CE# Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TOES</td>
<td>OE# High Setup Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TOEH</td>
<td>OE# High Hold Time</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCP</td>
<td>CE# Pulse Width</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TWP</td>
<td>WE# Pulse Width</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TWPH¹</td>
<td>WE# Pulse Width High</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TCPH¹</td>
<td>CE# Pulse Width High</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TDS</td>
<td>Data Setup Time</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TDH¹</td>
<td>Data Hold Time</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>TIDA¹</td>
<td>Software ID Access and Exit Time</td>
<td></td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>TSE</td>
<td>Sector-Erase</td>
<td></td>
<td>25</td>
<td>ms</td>
</tr>
<tr>
<td>TSCN</td>
<td>Chip-Erase</td>
<td></td>
<td>100</td>
<td>ms</td>
</tr>
</tbody>
</table>

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
FIGURE 4: Read Cycle Timing Diagram

FIGURE 5: WE# Controlled Program Cycle Timing Diagram

**Note:** \( A_{MS} \) = Most significant address
\( A_{MS} = A_{17} \) for GLS29SF/VF020 and \( A_{18} \) for GLS29SF/VF040
FIGURE 6: CE# Controlled Program Cycle Timing Diagram

Note: AMS = Most significant address
AMS = A17 for GLS29SF/VF020 and A18 for GLS29SF/VF040

FIGURE 7: Data# Polling Timing Diagram
**FIGURE 8: Toggle Bit Timing Diagram**

Note: $A_{MS} = \text{Most significant address}$  
$A_{MS} = A_{17}$ for GLS29SF/VF020 and $A_{18}$ for GLS29SF/VF040

**FIGURE 9: WE# Controlled Sector-Erase Timing Diagram**

Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 11)  
$A_{MS} = \text{Most significant address}$  
$A_{MS} = A_{17}$ for GLS29SF/VF020 and $A_{18}$ for GLS29SF/VF040  
$SA_{X} = \text{Sector Address.}$
2 Mbit / 4 Mbit Small-Sector Flash
GLS29SF020 / GLS29SF040
GLS29VF020 / GLS29VF040

FIGURE 10: WE# Controlled Chip-Erase Timing Diagram

SIX-BYTE CODE FOR CHIP-ERASE

ADDRESS $A_{MS}$

2 AA

55

55

55

55

T_{SCE}

CE#

OE#

T_{WP}

WE#

DQ_{7-0}

SW0 SW1 SW2 SW3 SW4 SW5

AA

55

80

AA

55

10

Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 11)

$A_{MS} = \text{Most significant address}$

$A_{MS} = A_{17}$ for GLS29SF/VF020 and $A_{18}$ for GLS29SF/VF040

FIGURE 11: Software ID Entry and Read

Three-Byte Sequence for Software ID Entry

ADDRESS $A_{14-0}$

2 AA

55

0000

0001

T_{IDA}

CE#

OE#

T_{WP}

WE#

DQ_{7-0}

SW0 SW1 SW2

AA

55

90

BF Device ID

T_{AA}

T_{WP}H

Note: Device ID = 24H for GLS29SF020, 13H for GLS29SF040

25H for GLS29VF020, 14H for GLS29VF040
FIGURE 12: Software ID Exit and Reset
AC test inputs are driven at V_{IHT} (3.0V) for a logic “1” and V_{ILT} (0V) for a logic “0”. Measurement reference points for inputs and outputs are V_{IT} (1.5 V_{DD}) and V_{OT} (1.5 V_{DD}). Input rise and fall times (10% → 90%) are <10 ns.

Note: V_{IT} - V_{INPUT Test}  
V_{OT} - V_{OUTPUT Test}  
V_{IHT} - V_{INPUT HIGH Test}  
V_{ILT} - V_{INPUT LOW Test}

FIGURE 13: AC Input/Output Reference Waveforms for GLS29SF020/040

AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic “1” and V_{ILT} (0.1 V_{DD}) for a logic “0”. Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% → 90%) are <5 ns.

Note: V_{IT} - V_{INPUT Test}  
V_{OT} - V_{OUTPUT Test}  
V_{IHT} - V_{INPUT HIGH Test}  
V_{ILT} - V_{INPUT LOW Test}

FIGURE 14: AC Input/Output Reference Waveforms for GLS29VF020/040
FIGURE 15: Test Load Examples
Start

Load data: AAH
Address: 555H

Load data: 55H
Address: 2AAH

Load data: A0H
Address: 555H

Load Byte
Address/Byte
Data

Wait for end of
Program (TBP,
Data# Polling
bit, or Toggle bit
operation)

Program
Completed

FIGURE 16: Byte-Program Algorithm
FIGURE 17: Wait Options
FIGURE 18: Software ID Command Flowcharts

Software ID Entry Command Sequence

- Load data: AAH
  - Address: 555H

- Load data: 55H
  - Address: 2AAH

- Load data: 90H
  - Address: 555H

- Wait TIDA

- Read Software ID

Software ID Exit & Reset Command Sequence

- Load data: AAH
  - Address: 555H

- Load data: 55H
  - Address: 2AAH

- Load data: F0H
  - Address: 555H

- Wait TIDA

- Load data: F0H
  - Address: XXH

- Return to normal operation

Wait TIDA

Return to normal operation
FIGURE 19: Erase Command Sequence

**Chip-Erase Command Sequence**

1. Load data: AAH
   Address: 555H

2. Load data: 55H
   Address: 2AAH

3. Load data: 80H
   Address: 555H

4. Load data: AAH
   Address: 555H

5. Load data: 55H
   Address: 2AAH

6. Load data: 10H
   Address: 555H

7. Wait TSCE

8. Chip erased to FFH

**Sector-Erase Command Sequence**

1. Load data: AAH
   Address: 555H

2. Load data: 55H
   Address: 2AAH

3. Load data: 80H
   Address: 555H

4. Load data: 55H
   Address: 2AAH

5. Load data: 20H
   Address: SAt

6. Wait TSE

7. Sector erased to FFH
### PRODUCT ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed</th>
<th>Suffix1</th>
<th>Suffix2</th>
</tr>
</thead>
<tbody>
<tr>
<td>GLS29xFxxx</td>
<td>XXX</td>
<td>XX</td>
<td>XXX</td>
</tr>
</tbody>
</table>

- **Environmental Attribute**
  - $E^1 = \text{non-Pb}$
- **Package Modifier**
  - $H = \text{32 leads}$
- **Package Type**
  - $N = \text{PLCC}$
  - $W = \text{TSOP (type 1, die up, 8mm x 14mm)}$
- **Temperature Range**
  - $C = \text{Commercial = } 0\degree\text{C to } +70\degree\text{C}$
  - $I = \text{Industrial = } -40\degree\text{C to } +85\degree\text{C}$
- **Minimum Endurance**
  - $4 = 10,000 \text{ cycles}$
- **Read Access Speed**
  - $55 = 55 \text{ ns}$
  - $70 = 70 \text{ ns}$
- **Device Density**
  - $040 = 4 \text{ Mbit}$
  - $020 = 2 \text{ Mbit}$
- **Function**
  - $F = \text{Chip- or Sector-Erase}$
  - $\text{Byte-Program}$
- **Voltage**
  - $S = 4.5-5.5\text{V}$
  - $V = 2.7-3.6\text{V}$

---

1. Environmental suffix “E” denotes non-Pb solder.
   Greenliant non-Pb solder devices are “RoHS Compliant”.
Valid combinations for GLS29SF020
GLS29SF020-55-4C-NHE  GLS29SF020-55-4C-WHE
GLS29SF020-55-4I-NHE  GLS29SF020-55-4I-WHE

Valid combinations for GLS29VF020
GLS29VF020-70-4C-NHE  GLS29VF020-70-4C-WHE
GLS29VF020-70-4I-NHE  GLS29VF020-70-4I-WHE

Valid combinations for GLS29SF040
GLS29SF040-55-4C-NH   GLS29SF040-55-4C-WH
GLS29SF040-55-4C-NHE  GLS29SF040-55-4C-WHE
GLS29SF040-55-4I-NH   GLS29SF040-55-4I-WH
GLS29SF040-55-4I-NHE  GLS29SF040-55-4I-WHE

Valid combinations for GLS29VF040
GLS29VF040-70-4C-NH   GLS29VF040-70-4C-WH
GLS29VF040-70-4C-NHE  GLS29VF040-70-4C-WHE
GLS29VF040-70-4I-NH   GLS29VF040-70-4I-WH
GLS29VF040-70-4I-NHE  GLS29VF040-70-4I-WHE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.
2 Mbit / 4 Mbit Small-Sector Flash
GLS29SF020 / GLS29SF040
GLS29VF020 / GLS29VF040

PACKAGING DIAGRAMS

FIGURE 20: 32-lead Plastic Lead Chip Carrier (PLCC)
Greenliant Package Code: NH

Note:
1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

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SSF is a trademark and SuperFlash is a registered trademark of Silicon Storage Technology, Inc., a wholly owned subsidiary of Microchip Technology Inc.
Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

FIGURE 21: 32-lead Thin Small Outline Package (TSOP) 8mm x 14mm
Greenliant Package Code: WH
## TABLE 12: Revision History

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>05</td>
<td>• 2002 Data Book</td>
<td>May 2002</td>
</tr>
<tr>
<td>06</td>
<td>• Removed 512 Kbit, 1 Mbit, and 2 Mbit parts</td>
<td>Mar 2003</td>
</tr>
<tr>
<td></td>
<td>• Commercial temperature and 70 ns parts removed</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• PH package is no longer offered</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Part number changes - see page 24 for additional information</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Changes to Tables 5 and 6 on page 8 and page 10:</td>
<td></td>
</tr>
<tr>
<td></td>
<td>– Clarified Test Conditions for Power Supply Current and Read parameters</td>
<td></td>
</tr>
<tr>
<td></td>
<td>– Clarified $I_{DD}$ Write to be Program and Erase</td>
<td></td>
</tr>
<tr>
<td></td>
<td>– Corrected $I_{DD}$ Program and Erase from 20 mA to 30 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>– Corrected $I_{DD}$ Read from 20 mA to 25 mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Clarified measurement reference points $V_{IT}$ and $V_{OT}$ to be 1.5V instead of 1.5V$_{DD}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Corrected the $V_{OL}$ test condition $I_{OL}$ to be 2.1 mA instead of 2.1 µA in Table 5 on page 8</td>
<td></td>
</tr>
<tr>
<td>07</td>
<td>• Corrected the Test Conditions for the Read Parameter in Table 5 on page 8</td>
<td>Apr 2003</td>
</tr>
<tr>
<td>08</td>
<td>• Added Commercial temperatures for all packages (See page 24 for details)</td>
<td>Aug 2003</td>
</tr>
<tr>
<td>09</td>
<td>• 2004 Data Book</td>
<td>Dec 2003</td>
</tr>
<tr>
<td></td>
<td>• Changed status to “Data Sheet”</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>• Added 70 ns technical data and MPNs for SST29VF040 only</td>
<td>Feb 2004</td>
</tr>
<tr>
<td>11</td>
<td>• Added RoHS compliance information on page 1 and in the “Product Ordering Information” on page 23</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Reinstated 512 Kbit, 1 Mbit, and 2 Mbit devices and MPNs (excluding the PDIP package)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Removed 55 ns technical data and MPNs for SST29VF040</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Added non-Pb MPNs for all devices</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Clarified the solder temperature profile under “Absolute Maximum Stress Ratings” on page 8</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>• Removed all entries related to SST29SF/VF512 and SST29SF/VF010</td>
<td>Nov 2005</td>
</tr>
<tr>
<td></td>
<td>• Removed leaded parts for 020 products.</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>• Changed $I_{DD}$ Read from 20mA to 25mA, and Changed $I_{DD}$ Write from 20mA to 30mA in Table 5 on page 8 and Table 6 on page 10</td>
<td>Oct 2006</td>
</tr>
<tr>
<td>14</td>
<td>• Changed $I_{SB}$ from 15 to 30 µA in Table 6 on page 10.</td>
<td>Oct 2008</td>
</tr>
<tr>
<td>15</td>
<td>• Transferred from SST to Greenliant</td>
<td>May 2010</td>
</tr>
</tbody>
</table>